Week 2:FDM Applied to Solve Laplace Equation for Various Capacitor Configurations

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Abstract

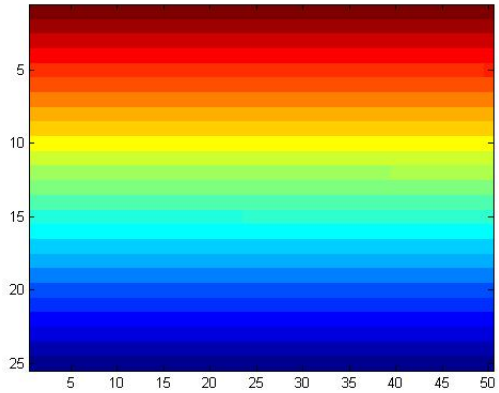
Finite Difference Method (FDM) has been used to solve the capacitor problem in various configurations. These can be used to further model the parasitic capacitances that occur in integrated circuits between the interconnects and the substrate.

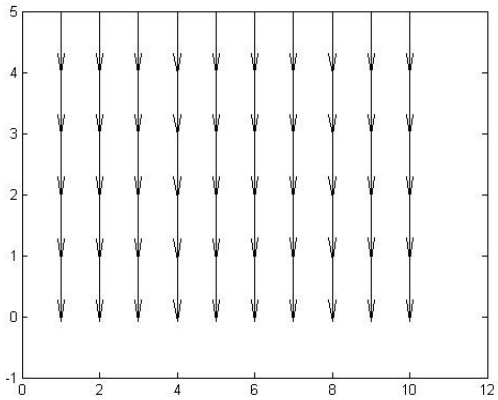
1 Introduction

FDM approximates the second derivative at a point as the average of the four surrounding points. At the boundary, the V can be updated using either the Dirichlet or the Neumann boundary condition. For conductors, one can use the dirichlet conditions, and for boundaries far away from the capacitor system, Neumann boundary condition, (gradient being zero) can be applied.

2 Simple capacitor cross section segment

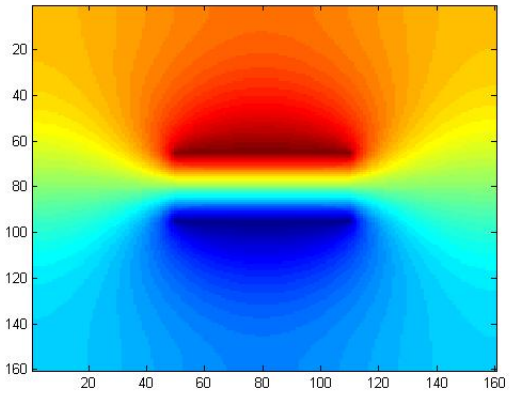
In this case, a close up of the cross section of the capacitor has been considered and Neumann conditions (set to 0) have been applied at the edges. As a result, no fringing in the field can be observed. Dirichlet conditions of +10V and 0V have been applied on the top and bottom plate of the capacitor, and laplace equation has been solved.

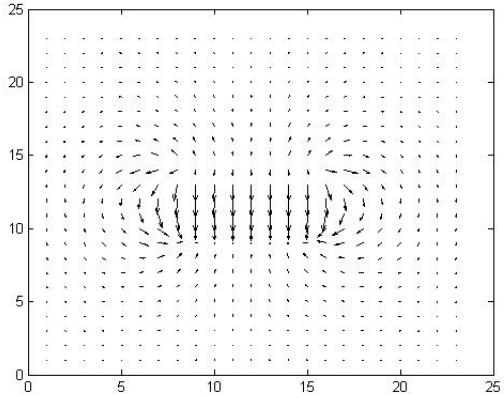




3 Parallel Plate Capacitor

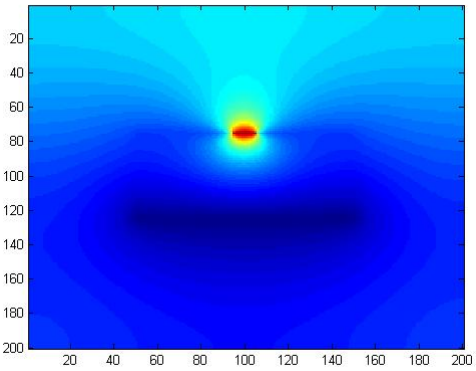
Fringing can be observed in this configuration as we have considered several times the capacitor plates' length to be the boundary. The results (Equipotential lines) can be observed as follows:

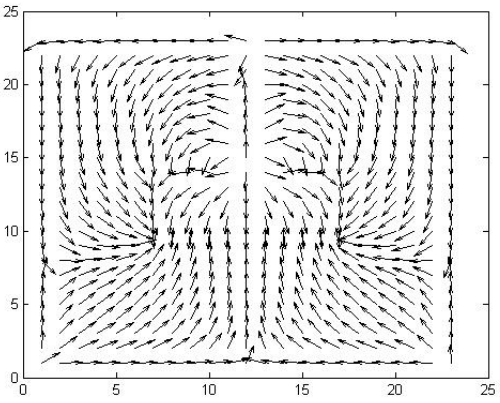




4 Capacitor with one plate larger

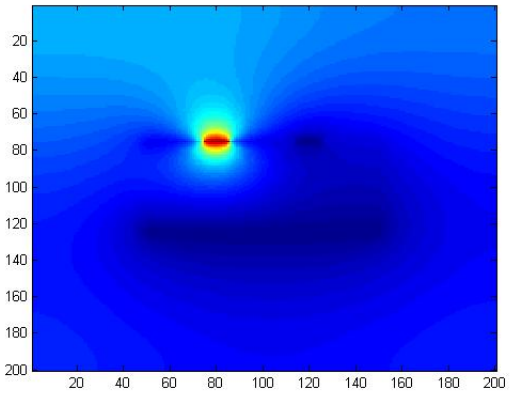
The upper plate is 10 times as smaller as the lower plate. as a result, most of the higher voltage is only very near to the upper plate. One can observe the field lines pointing along the dielectric's width. The field has been normallized as the actual values are too small to be visualize. Hence the field inthe middle can't be seen very clearly.

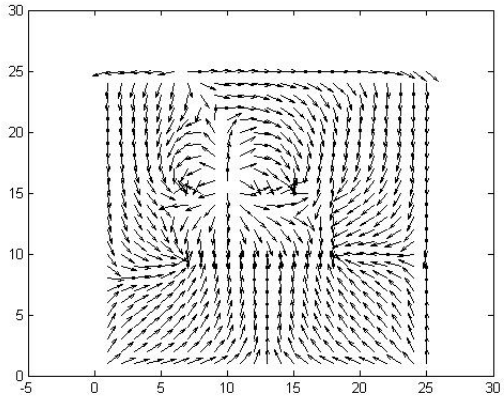




5 Two separate plates with ground at the bottom

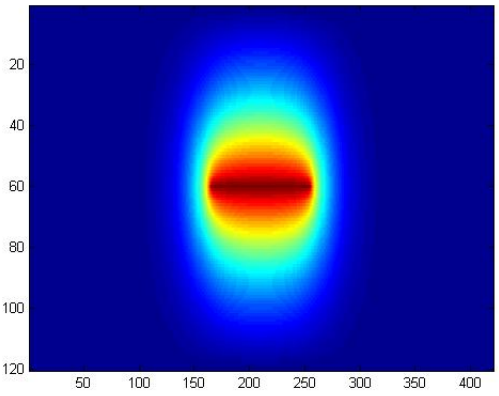
One 10V plate is kept on the top left of the dielectric and a ground plate to the right. Some field lines can be seen to go between the interconnects.

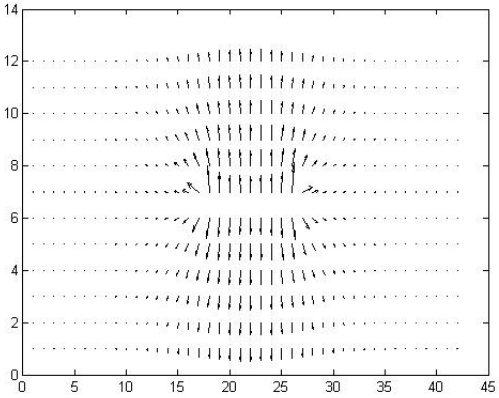




6 Microstrip Capacitance

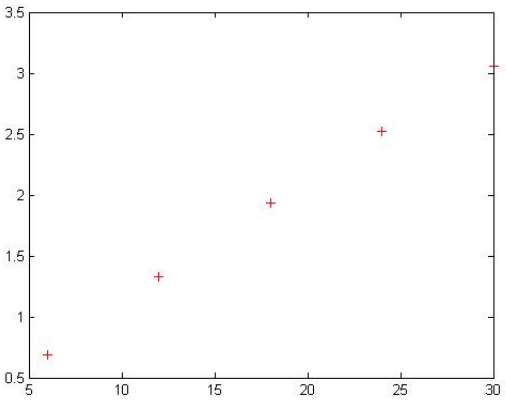
The field structure is given as follows:



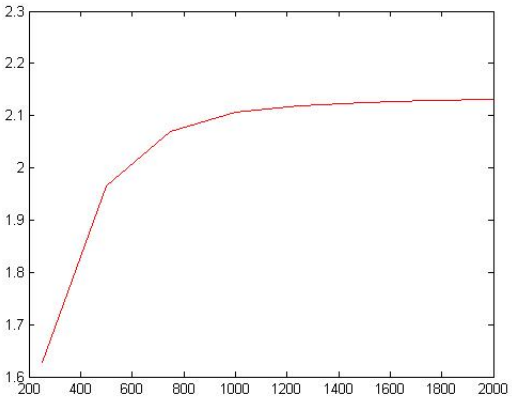


7 Observation

The microstrip has a epsilon_real = C/Cair ratio of 5.300 for w = 1.5. For 2000 as maximum number of iterations, the grid unit length N vs Z0 (normallized) plot is as shown(almost linear):



Also, As we increase the oteration count, we get closer and converge towards a value for Z0. The I vs Z0 plot is as follows:



8 Result and Discussion

The electrostatic field configuration for various capacitor configuration has been obtained, and the general trend in field lines can be verified.