CSE 490/590 Computer Architecture Spring 2023 Homework 3

1. Assume the presence of the following memories in a MIPS system:

   L1 cache
   L2 cache
   Main Memory
   Hard drive

Show the memory hierarchy and order them in terms of

   a. Speed
   b. Memory capacity (Size)
   c. Cost per byte

2.
   a. If a direct mapped cache has a hit rate of 95%, a hit time of 4 ns, and a miss penalty of 100 ns, what is the AMAT?
   b. If replacing the cache with a 2-way set associative increases the hit rate to 97%, but increases the hit time to 5 ns, what is the new AMAT?
   c. If an L2 cache is added with a hit time of 20 ns and a hit rate of 50%, what is the new AMAT?

3. Suppose that in 1000 memory references there are 40 misses in the first-level cache and 20 misses in the second-level cache.
   a. What are the local and global miss rates for each level of cache?

   Assume the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of the L2 cache is 10 clock cycles, the hit time of the L1 cache is 1 clock cycle, and there are 1.5 memory references per instruction.

   b. What is the average memory access time?

4.
   a. What is write back cache? Discuss both the advantages and disadvantages of using the write-back policy.
   b. What is write through cache? Discuss both the advantages and disadvantages of using the write-through policy.

5. Here is a series of address references given as word addresses: 2, 3, 11, 16, 21, 13, 64, 48, 19, 11, 3, 22, 4, 27, 6 and 11. Consider a word-addressable cache.

   Assuming a Direct-mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss.

   a. For each of these references, identify the binary address, the tag, and the index.
   b. What is the hit rate?

6. A processor with Instruction cache miss rate of 2% and Data cache miss rate of 4% and costs 10 cycles to access either of the caches. 40% of the instructions to be executed are Load and Store Instruction. The CPI with ideal cache (no misses) is 2.

a. Compute the actual CPI
b. Consider the datapath was improved so that the CPI can be reduced from 2 to 1.5 (all the other specs remain the same). Compute the actual CPI and compare it with (a)

7. Consider a direct-mapped cache of 128 blocks and each block can hold 16 words. The total memory capacity is 8 GByte with 8Byte word sizes. It is a word addressable memory.

   a. What is the address format?
   b. If we change the cache to a 4-way set associative cache, what is the new address format?

8. a) Consider a main memory size of 4 Bytes. Each block in the cache can hold only 1 word (here 1 word = 1 Byte). Find the miss rate for the address references 0 4 0 4 0 4 0 4 in a direct mapped cache.

   b) Consider a main memory size of 4 Bytes. Consider a 2 way set associative cache which are initially empty. Each block in the cache can hold only 1 word (here 1 word = 1 Byte). Find the miss rate for the same address references (0 4 0 4 0 4 0 4).

   c) Compare (a) and (b) and list the advantages of associative cache.