Hardware Implementation of an Invariant Observer

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This dissertation is submitted for the degree of

Bachelor of Science

2014

Declaration

I hereby declare that except where specific reference is made to the work of others, the contents of this thesis are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other University. This thesis is the result of my own work and includes nothing which is the outcome of work done in collaboration, except where specifically indicated in the text.

Marko Stanisic
2014

Abstract

The Invariant Observer is a Runtime Verification Unit monitoring a signal ϕ from a System under Test in real time and determining whether the signal was in an active state and had been active up to τ clock cycles before. If this is the case then signal ϕ is observed as being invariant in the past within the time interval $[0,\tau]$.

In their paper „Runtime Verification of Embedded Real Time Systems“, Reinbacher et al. [4] presented a hardware implementation of an Invariant Observer. In this thesis a different hardware implementation is shown, that allows for parallel execution of several instances, leading to significant performance improvements if the time required for determining whether ϕ holds, is not neglectable.

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Chapter 1

Introduction

1.1 Overview of the Bachelor Thesis

In embedded real time systems it is necessary to make efforts to verify a system design. A system design can be formalized by a mathematical specification within a properly chosen dynamic system model. One approach to system design verification is a deduction, which shows that the design implies the requirements.

In critical Real Time Systems (RTS) timing constraints have to be considered in the requirement engineering. Such Real Time Systems are modelled by states changing over time. Time constraints can be formulated as constraints on the duration of critical states. A real time logic should be able to specify that real time constraints. Generally it seems that two main classes of real time logic are present, explicit or implicit temporal logic.[3]

Explicit temporal logic makes use of explicit expressions of time variables. The time variable can be the representation of a time interval or a variable in temporal logic. Implicit temporal logic (for example MTL - Metric Temporal Logic) is using temporal operators that constrain the extent of a state. It is based on interval temporal logic and the duration concept. Implicit temporal logic can be very useful to express before/after relations between concurrent actions. For further details [3] can be a good source of information. In runtime verification a monitor evaluates executions of a **System under Test (SUT)** [4]. The evaluation is formalised from a formal specification described in temporal logic.

For ultra critical systems it is important to meet four major requirements:

1. Functionality: cannot change target's behaviour
2. Certifiability: must avoid re-certification
3. Timing:must not interfere with the target's timing
4. Swap:must not exhaust size, weight and power tolerance

A **Runtime Verification Unit (RVU)** is a verification monitor that meets these four major requirements. As part of this requirements, the RVU must be separated from SUT. In fact it is a synthesized hardware that monitors the execution of a SUT.
The topic of my thesis "Hardware Implementation of an Invariant Observer" can also be considered as a RVU, it evaluates the execution of a SUT and checks it for invariance conditions. My observer is an alternative implementation of the invariant observer INVARIANT-SYMBOL published in [4], that bypasses the problem of resource limitation and makes use of the significant advantages of a highly parallel **Field Programmable Gate Array(FPGA)** hardware implementation. The most important difference is that my observer is not bounded to a specific τ, but the observers in [4] are bounded.This feature will be explained in the next section.

In the publication "**Real-Time Runtime Verification on Chip**" [4] the concept of a RVU and the principles of that Verification Framework are described in greater detail.

A survey about the functionality of the invariant observer is given in the following sections.

1.2 The Invariant Observer

This section is a survey about the invariant observer and how it works. More details about the observer algorithm are presented in the next chapter.
The Invariant Observer acts like the temporal (invariant previously) operator $\boxdot_\tau \phi$ of the Metric Temporal Logic (MTL) and is certainly restricted to the past (ptMTL). Such a temporal operator takes an input ϕ, the calculation of a propositional formula, and evaluates if ϕ holds for the past τ execution times, including the current execution time in a discrete time setting. For example the logical consequence $e^n \models \boxdot_3 \phi$ expresses that the operator $\boxdot_3 \phi$ is true at current time n iff (if and only if) the evaluation of ϕ is true now and was also true the last $\tau = 3$ execution times. In fact the $\boxdot_\tau \phi$ is a specialization of the $\boxdot_{[0,\tau]} \phi$ ptMTL operator which restricts the range of the invariance qualification.
Figure 1.1 and Figure 1.2 show an example for such a temporal operator.

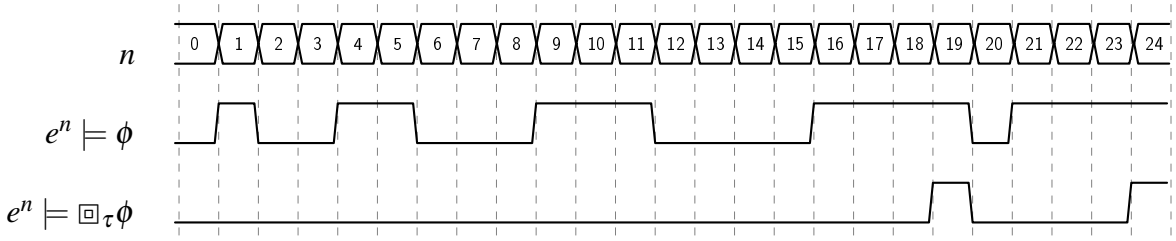

Fig. 1.1 Example for Invariant Operator $\boxdot_\tau \phi$ with τ=3

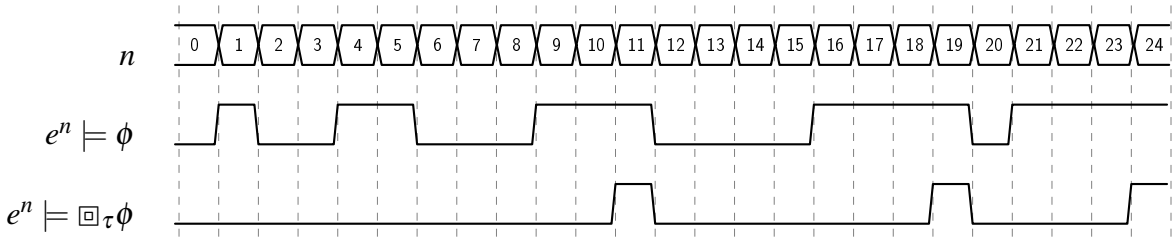

Fig. 1.2 Example for Invariant Operator $\boxdot_\tau \phi$ with τ=2

My approach of the invariant observer is based on some certain requirements. The following subsections will discuss these requirements.

1.2.1 Arbitrary calculation time of logical propositions

To introduce the first requirement we begin with the discussion of the problem that the calculation of a propositional formula ϕ could take several clock cycles (execution times). This means that an observer has to wait until the calculation of the proposition is finished. In [4] the observer needs to guarantee that it finishes evaluation of atomic propositions within a tight time bound. In our case, if we start calculation of a propositional formula ϕ at every clock cycle and the calculation itself needs y clock cycles, than we need at least y observer stages to cover finished calculations at every clock cycle. These observer stages are part of the whole observer. After y clock cycles, at every following clock cycle, a calculation of ϕ will be available. At least one observer stage will be ready, too, to evaluate a calculation ϕ at any time. In other words, we are implementing temporal pipeline stages that represent components of the invariant operator and these components together are evaluating the invariance qualification of the proposition ϕ. We don't have one observer, in fact the observer is composed from several observer stages. As a matter of fact, this solution only requires the calculation time of a proposition ϕ to be bounded by some previously known time y.

Propositional formulas can be composed from several other complex propositional subformulas or atomic propositions. In some cases a subformula is waiting for the resolution of an another subformula. In [4] this balance is achieved by the restriction of the atomic proposition class in sense of the abstract domain of logahedron.

1.2.2 Pipelined Observer Stages

Consider every finished calculation of a propositional formula ϕ as a signal value of the signal W(ϕ), every value in that signal is timely ordered just in the order it was calculated. Obviously, every represented execution time of W(ϕ) is the same as the execution time of the Observer. This means, at every execution time (clock cycle) an observer stage is evaluating a signal W(ϕ) at that time. In our case, signal W(ϕ) is apparently shifted by y clock cycles to the right. This view is encouraged by the fact, that at the beginning of the monitoring, the observer stages have to wait, until the first valid value of the signal W(ϕ) is available for evaluation of any observer stage which is duly put at disposal. The following observer stage evaluates, at execution time $n = y+1$, the second valid value of W(ϕ), and so on and so forth. It should be considered, that the evaluation of a signal value from W(ϕ) relates to a propositional formula ϕ, which was relevant y clock cycles before. But it should also be mentioned that the signal values between execution time $n = 0$ and $n = y-1$ are evaluated

as well, but obviously with a negative result, because no calculation can be started before any input is available.

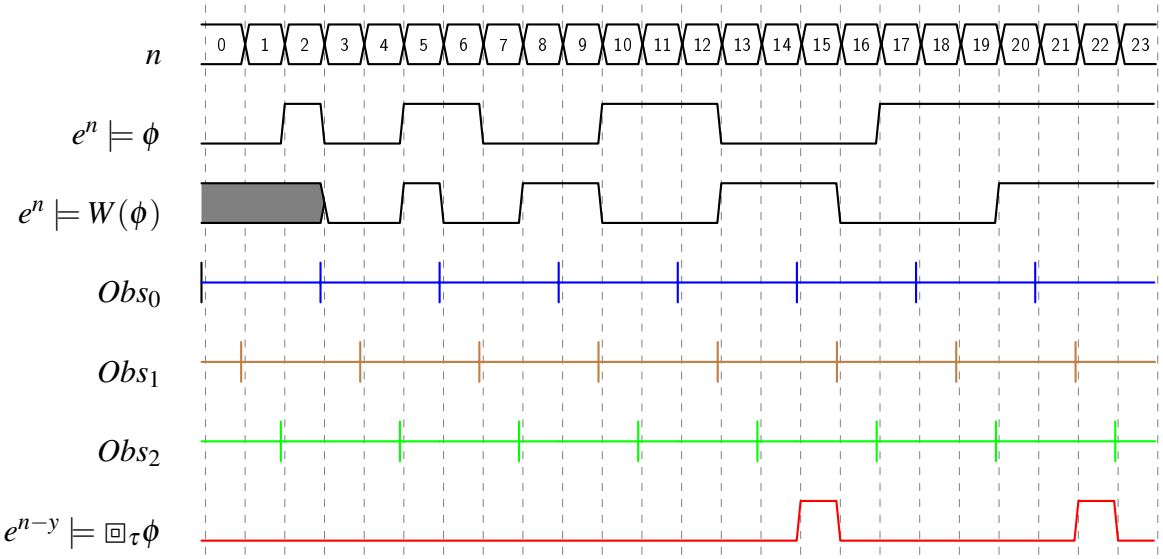

Fig. 1.3 Example for m=3 observer stages monitoring a signal W(ϕ), τ=2

The example in Figure 1.3 shows that the calculation of the first value from W(ϕ) needs y execution times. So no value is defined in the cycles before. If we take the view only from the proposition ϕ as a signal, then we calculate at every execution time n, from the latest inputs and subformulas at that time, exactly the proposition ϕ at that moment. But this holds under the assumption that the result of such a calculation is available immediately. The signal W(ϕ) shows us, what happens if calculations of proposition ϕ need some time, here we assume y=3 clock cycles. As mentioned, W(ϕ) is like signal ϕ shifted to the right. In Figure 1.3 we also see at which execution time the observer stages evaluate the signal W(ϕ). But this is only a preview about these observer stages. The algorithm about their real behaviour will be explained in the next chapter. The most important thing here is that these observers are working delayed. Every new observer stage starts its work after the observer stage before. This is important, because every clock cycle must be covered as long as the calculation of W(ϕ) takes. The last signal shows us the invariance qualification $e^{n-m} \models \boxdot_\tau \phi$ for τ=2, which holds at execution time $n = 15$ and $n = 22$, but either for one cycle only.

The invariance qualification will be resolved if we connect every observer stage in a binary “and” operation. In Figure 1.3 the result is simply calculated with:

$$\boxdot_2 \phi = Obs_0 \text{ and } Obs_1 \text{ and } Obs_2$$

Summarized, every observer stage is included in a binary "and" operation and all these observer stages together are computing at every execution time n , if the logical consequence $e^{n-m} \models \boxdot_{\tau}\phi$ holds. If we consider all these observer stages together as one temporal (invariance before) operator, than this operator checks at every execution time n, the invariance qualification of the proposition ϕ, m clock cycles before. Regarding Figure 1.3, it is true now if the proposition ϕ, m clock cycles before, was invariant with τ=2 .

1.2.3 System Settings of the Invariant Observer Stages

This was a brief introduction about the specific behaviour of the invariant observer as a whole. We will next detail on the parameter settings. It starts with the question of how many observer stages do we actually need ? We already know that at least y are necessary. If we have to define a number of observer stages with variable ”m” then the following condition must be hold: $m \geq y$. Depending on how long the calculation of a proposition ϕ needs, a minimum of y observer stages are necessary, but upwards can be chosen arbitrarily. This shows us also the possibility to apply the Observer with his observer stages on different evaluations of system inputs despite the time they need and it works in real time. If we use only one observer stage (means immediate evaluation of ϕ), then it works as a native invariant operator.

The next interesting aspect, and maybe the most powerful argument of this design way, is the invariance parameter τ. The number of observer stages ”m” stays in no relation to the invariance parameter τ. Following conditions are possible: $m \geq \tau$ or $m < \tau$. As long as the observer is configured to cover the computation time of W(ϕ), it can be used for every arbitrary choice of τ. In [4] this setting is fixed. My implementation of an invariant observer is able to change that parameter during run-time, but this feature is not specified in the requirements, and should be treated as such.

The next chapter shows the algorithm of the observer stages and how every observer stage works. Also a representation of the software implementation will be explained in great detail.

Chapter 2

Software Implementation and Algorithm

2.1 Algorithm of the Invariant Observer Stages

The following algorithm shows the proper behaviour of an observer stage.

Algorithm 1 Pseudo Code of an Observer Stage

Require: Precondition: $m \geq y$

```
1:  Initialize: count = 0
2:  if (clock mod m) = 0 then
3:      if W(φ) = 0 then
4:          /*evaluates finished calculation of φ after m clock cycles*/
5:          count = 0
6:      else
7:          /*do nothing*/
8:      end if
9:  end if
10: /*Following code executes every clock cycle*/
11: if count = τ + 1 then
12:     output = 1
13: else
14:     output = 0
15: end if
16: count = min(count + 1, τ + 1)
17: return output
```

As shown in Algorithm 1 the algorithm is split in two main parts. From the start of the observer stage, and periodically every m clock cycles, the upper part checks the status of the current signal value W(ϕ). If W(ϕ) has an active state (e.g. W(ϕ)=1), the counter keeps his

old value, otherwise it will be set to zero. It is important that one observer stage recognizes, that the invariance qualification was not satisfied at this time. When the conjunction of all observer stages is computed, at any arbitrary execution time n, and at least one stage does not have an active output, then the result is false. This means, that at the execution time n, the invariance qualification is not fulfilled. The bottom part is executed at every clock cycle and increments the counter value up to the maximum value of the invariance qualification's range. If the counter reaches the maximum value, the respective observer stage activates its output to an active state. In fact, the counter represents the invariance qualification of length 'τ'. The term '$\tau+1$' indicates that the present value must also be involved in the invariance qualification. The counter value will be initialized with zero at the beginning of the algorithm. Hypothetically, if the counter is initalized with '$\tau+1$' the ouptut is activated immediately, because of the bottom algorithm. But this is a contradiction to the assumption that W(ϕ)=0 for all execution times n before zero.

It should be mentioned that this current design does not implement or handle the calculations of the truth value of propositions ϕ, which is indicated with W(ϕ). On the other hand, the observers from [4] are responsible for taking the necessary inputs, calculate the atomic propositions (with ATCheckers) and immediately evaluate the ptMTL-operator qualifications. These steps have to be done in a tight time bound. In our case, W(ϕ) must be updated from another entity in such a way, that at every clock cycle an observer stage must have a consistent value for evaluation. The following subsection is an overview about the implementation of the Algorithm 1 in VHDL.

2.2 VHDL Implementation of the Algorithm

In Appendix A.2, there is an implementation in VHDL which follows the meaning of Algorithm 1. We will discuss the different process entities and the relations with Algorithm 1. Finally, we get an overview about the improvements which are significant for a faster design. This VHDL design of an observer stage has got the following inputs and outputs:

(a) inputs:

- **invariance_tau** is a signal variable which gets the value for τ
- **enable_in** signal activates the observer stage
- **signal_phi** is the signal state of W(ϕ)

(b) output:

- **enable_out** is a signal whose state is set to active after the activation of the current observer stage, but delayed for exact one clock cycle.
- **output signal** is simply the output state of the observer stage.

The Observer Stage is split in a synchronous and an asynchronous design, in terms of a Moore State Machine. The process labelled “sync” (at line 83 of the VDHL-Code A.2)represents the synchronous part of that design where the register states are changed at every clock cycle. The synchronous process is only executed if the combined signal **enable_logic** has been activated, indicating a specific behaviour of the observer stages. (VDHL-Code A.2, line 22) The observer stages are linked to each other through cascade connections. The first stage activates the next observer stage through the signal **enable_out** after being activated through **enable_input**. If the signal **enable_input** of an observer stage is being activated,in a clock cycle, then the signal **enable_out** will be activated in the clock cycle afterwards.

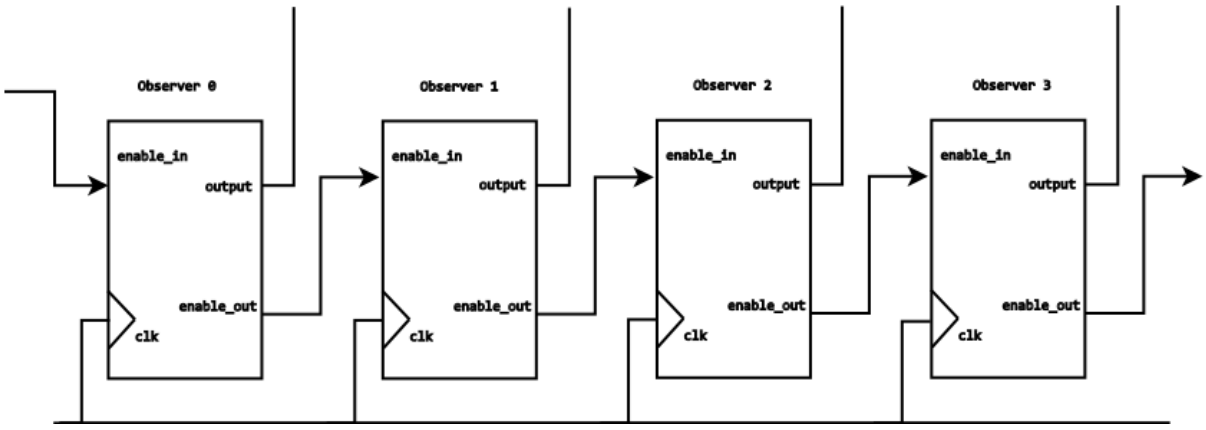

Fig. 2.1 Example for m=4 Invariant Observer Stages concatenated in cascade.

This ensures, that these observers are starting delayed, each 1 clock cycle after its predecessor.
Signal **inc_tau**(VDHL-Code A.2, line 21) increments the input signal **invariance_tau**, which represents $\tau + 1$ at every execution time. The asynchronous part works immediately after every change of the system state. (VDHL-Code A.2, line 25 and line 51) In the following descriptions of the asynchronous parts, only temporary signals are changed, but

these signals transfer their values inside the synchronous part at every clock cycle, except **inc_tau** and **enable_logic**. Every of these signals are indicated with "_next" at the end of their names, but in the following descriptions only their register counterparts will be mentioned.

The process entity **comb_cycle**(VDHL-Code A.2, line 25) is the description of an internal clock counter which only counts up and down between values 0 and m. The signal **cycle** is significant for checking the condition "(clock mod m) = 0" from Algorithm 1.

The process entity **comb_logic** implements the main part of the algorithm. Signal **count_p** will be incremented in each clock cycle until it reaches $\tau + 1$. The counter should be initialised to zero (as indicated in the algorithm), but is incremented immediately at every clock cycle. (VDHL-Code A.2, line 55) Or in other words, if **count_p** is reset to zero in a clock cycle, it will be incremented immediately in the "same" clock cycle. To demonstrate this fact we have an additional signal **count**, initialised with 1. But this signal is only for reasoning and will be reduced by the syntheses tool. The synchronous design is cumbersome in a way, which is due to the way of how the states change. If the counter is supposed to be incremented after evaluating some conditions, this does not imply an immediate change of the counter. To overcome this handicap the counter **count_p** is initialised to 2(VDHL-Code A.2, line 56) which means, that at every clock cycle we check if the counter count_p will reach a maximum at the next clock cycle. This enables us to change things on time. According to the Algorithm 1 at line 5, **count_p** will only be reset if signal $W(\phi)$ has been evaluated as being not active in **comb_cycle**. (VDHL-Code A.2, line 56)

The first if-branch at line 53 of the VDHL-Code A.2 checks two cases. At first it will be checked if the clock passed m cycles or not and second if the signal **enable_logic** is supposed to be active. The first question is in term of Algorithm 1, line 2. The second question concerns the signal **enable_logic**. This signal combines **enable_in** and **reset** in one signal. If signal **enable_logic** is active, means that the observer stage is active and no reset condition happens. The else-branch of the first if-branch at line 67 of the VDHL-Code A.2 checks the condition in terms of Algorithm 1, line 11. The content of the if-branch (line 53) and the else-branch (67) are nearly the same, but there are two exceptions. Inside the if-branch, beginning at line 54, the status of signal W(ϕ) will be checked, according to Algorithm 1, line 3. And inside the else-branch at line 75, if m cycles are no yet passed and signal **count_p** is already at the maximum, then signals **count_p**, **count** and **output** keep their old values. The

other parts of **comb_cycle** are straightforward, if you compare it with the algorithm. In case the counter **count_p** reaches the maximum, the **output** of the observer stage is activated.

The current design has been made optimizing for throughput. Besides from design decisions like using count_p instead of count, this led to the following general design rules:

It is very important that no Latches are built by the syntheses tool, so every if-branch must contain the same changes on the same signals. A further point is to reduce the number of if-branches to a minimum. If-branches inside of an If branch extends signal paths and reduce the maximum clock design of the whole design. In the next chapter we get an overview of the hardware realisation of the current design, which shows us a more visual view on that.

Chapter 3

Hardware Implementation

The following sections show an overview about the hardware implementation of the Invariant Observer Design. It starts with a description about the hardware platform on which the observer runs and some details about the synthesis tools. At the end of this chapter, there comes a design view about the synthesized hardware and a discussion about the design steps.

3.1 Hardware Platform for a Prototype

The Invariant Observer is synthesized on a Field Programmable Gate Array(FPGA), on this platform it is possible to get an insight about the runtime behaviour and to see the observer in action. The FPGA board, that was used for the simulations, is a **DE2-115** modell from ALTERA[1]. That board is ideal to illustrate fundamental concepts and advanced designs, and it gives a possibility to meet necessary real-time requirements. The DE2-115 is equipped with a **Cyclone IV EP4CE115F29** FPGA Chip and it is powerful enough to emulate a CPU(ex. Nios from Altera). In [4] this FPGA board was used for performance studies, besides other FPGA's, so it was logical to use a similar environment. The **DE2-115** has an on-board oscillator of 50 Mhz and in combination with a Phase Locked Loop(PLL) it is possible to increase the operating frequency for advanced tests. In the following section it will be shown, how enhanced frequencies can change the design on the Register Transfer level(RTL) and why bad design decisions can influence the maximal speed of a design. In Appendix D there is a schema illustration about the components of the **DE2-115** FPGA board.

3.2 Synthesis and Design

This section gives an overview about the synthesis tool and details about the Register Transfer Level design view. An interesting part in this section is to see how the synthesis tool creates hardware structures based on the code of the Observer VHDL implementation.
For synthesis and compilation of the observer VHDL code, the **Altera Quartus II Version 12.1 Build 177 Full Version** was used.

3.2.1 Design View of the Register Transfer Level

In Quartus II, after compilation of the design and after creation of the netlists, you can use a tool named **RTL Viewer**, which shows how the components of the design will be created on a Hardware Platform. It is an abstract view on the **Register Transfer Level**. This tool can be very handy if someone want to see how the hardware should look like. Based on the illustration of the hardware, some decisions can be reconsidered in terms of the performance.
Figure 3.1 is the hardware schematic view of a single observer stage (m=1), which is modelled as a single observer with input frequency of 50Mhz. In which way, this test cases was modelled, will be discussed in the next chapter. The next Figure 3.2 shows exact the same design case like Figure 3.1 but with the difference that the operating frequency is 150Mhz. In Figure 3.2, it is illustrated how the syntheses tool reorientates the hardware design, to meet the requirements of that clock speed. The worst case path determines the maximum frequency, which is allowed for that design. A more detailed description about the timing model is in the next subsection.

3.2.2 Timing Model of the Design

One important thing that have to be considered is that the signal path from the beginning of the observer entity to the end should be as short as possible, this concludes to some important design facts. The maximum frequency of the whole system is limited by the longest path of the design, which means that the performance of a system is expressed by the maximum frequency at which it may be operated. So it should be logical for every entity in the netlist, to keep the signal path as short as possible. The performance maximum can be computed by the Quartus Tool named **TimeQuest Timing Analyzer**, which gives estimations about the maximum frequency of the design. The longest signal path of a design is indicated by the **worst case path** in the tool.

The first version of the observer stage had a low performance level, a illustration of this version is shown in the Appendix C.2. The TimeQuest Timing Analyzer consider some uncertainties for the performance estimations. From [2] it is known how the Quartus Tool creates timing models. These are created in the TimeQuest Timing Analyzer after building the netlist, as part of the compilation process of a design. A FPGA has to operate in a continuum of conditions. These conditions include the die junction temperature which can vary among specific ranges, for example commercial parts have a range of 0°C to 85°C and industrials a bigger range. A further condition is the voltage supply level with regard to critical voltages for maintaining FPGA performance(Vcc and the various I/O supplies).
The timing analyzer shows estimations for three cases

1. Slow 1200mv 85°C model
2. Slow 1200mv 0°C model
3. Fast 1200mv 0°C model

These are operating-condition corners which are usually end point combinations of the ranges in temperature, voltage and manufacturing processes. Each operating-condition is used to model the timing delays under specific end points of temperature, voltage, and manufacturing process conditions. The first case with “Slow 1200mv 85°C model” seems natural and was more considered for test cases, because it shows frequencies under long term operating conditions. A lot of tests about estimations of the maximum frequency of different design cases have been exercised(shown in the next chapter), and only the estimations from “Slow 1200mv 85°C model” were significant for further discussions. In the next chapter there is a summary of these tests.

3.2.3 Design Decisions based on Register Transfer level

At the first time, where the VHDL Code of the observer stage was behavioural correct, some performance and optimization decisions had to be reconsidered. The most important thing is to separate synchronous and asynchronous design. So, it was necessary to split the first version of a completely synchronous design, where every action is only triggered after every clock cycle. A more parallel approach was necessary where only state changes are done synchronously, but other actions should be triggered immediately after any change of the state. And a asynchronous system part can be separated in several independent asynchronous components, which achieves more system parallelism and a better performance. As already mentioned in chapter 2, this system design is similar to a Moore State Machine,

where the logic is separated in a transition logic, an output logic and a state memory. And only the state memory should be changed on every clock cycle. The design approach of the invariant observer is similar, but with the difference that the output logic and transition logic components are merged together. The hardware schemas from the Register Transfer Level illustrations were beneficial, because they showed how the components where created with its VHDL background. For example If-statements should be created in a way, that allow no Latches. This means that every else-branch should contain the same components like the if-branch. Following that rule, mutexes will be created which are shown here in the example of Figure 3.1. Every mutex has two inputs(according to if, else), which are selected depending on the third input(MUX21). At the beginning of the entity there are several adders and these are representations for the different addition operations which has to be done according to the behaviour of the observer. **Add2** emulates "$cycle\_next = cycle + 1$", **Add1** emulates "$cycle\_next = cycle - 1$" and **Add3** emulates "$count\_p = count\_p + 1$" according to the sourcecode of the Observer Stages in Appendix A.2. In Figure 3.1, the MUX 21 Mutex at the beginning, indicated by **cycle_next[15..0]**, is the if-branch, according to the sourcecode in Appendix A.2, which decides if "$cycle = 0$" or not. The **MUX21[cycle_next[31..16]]** below stands for the branch "if $cycle = observernumber$". **MUX21[cycle_next[15..0]]** decrements cycle_next in normal case, but increments it only once if the value of cycle_next reaches the bottom limit. **MUX21[cycle_next[31..16]]** works the opposite way. As you can see, the tool enhanced cycle_next up to 48bit to reserve memory for intermediate results. In the middle of the hardware scheme, there are two another **MUX21[cycle_next[15..0]]**, the first(left to right) decides between "$cycle\_next = cycle + 1$" or "$cycle\_next = cycle - 1$" and the second between the result from first Mutex before and the reset value. **MUX21[cycle_next[47..32]]** decides between keeping the old value "$cycle\_next = cycle$" or taking over the value from **MUX21[cycle_next[31..16]]**. The overview regarding count_p is similar, but a deeper insight about that Quartus translation behaviour would exceed that subsection. As you can see in the hardware schema, there are 5 registers(cycle, count_p, direction, output, enable_out) and these representates the state of the Invariant Observer and they may only change their values after every clock_cycle. The dimensions of the registers are conform to the dimensions of the input conditions. For example if inc_tau has a value with only 5 bits, then count_p is accordingly large-dimensioned to 6 Bit. This is only a cut-out, about how the Quartus II translates VHDL Code. A lot of other hardware representations are shown in Appendix C, actually they have the same components but another orientations. The next subsection shows something about problems during the progress of that development.

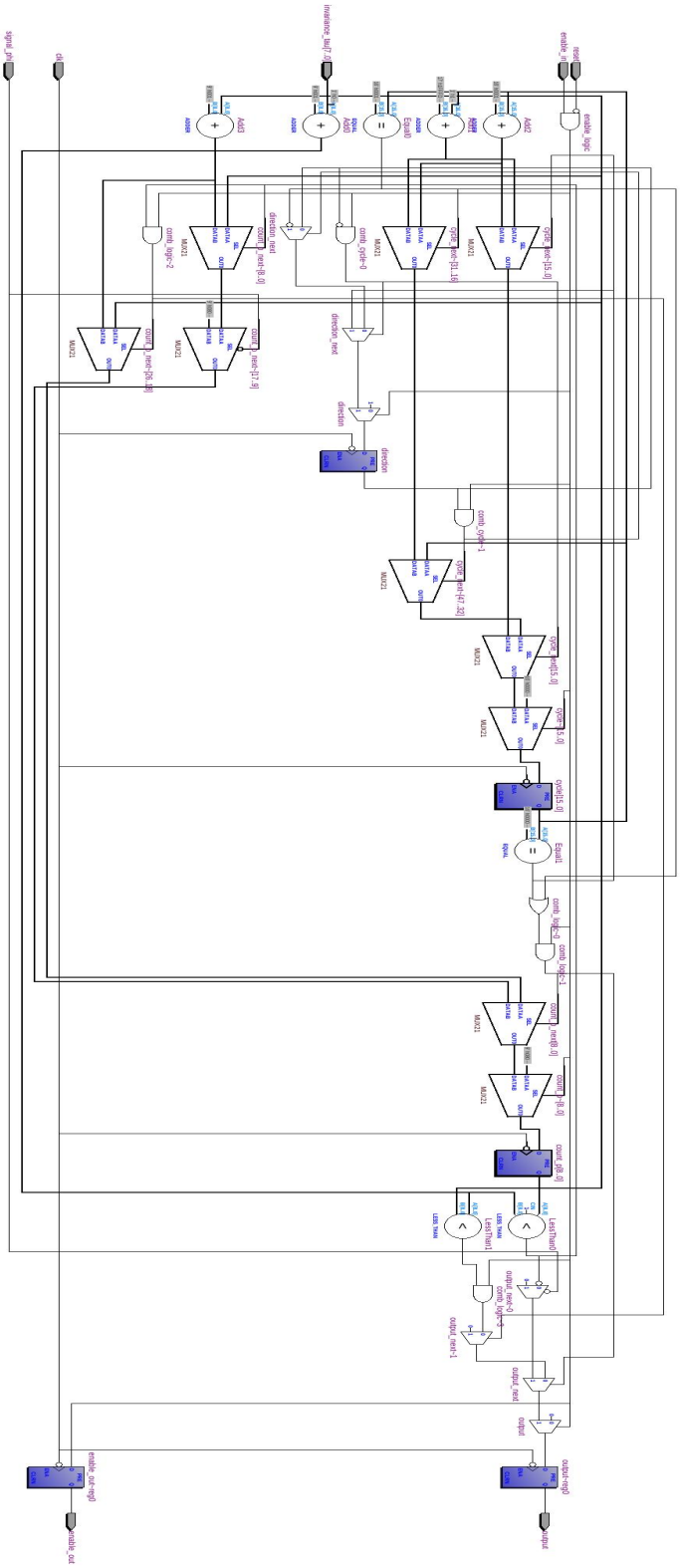

Fig. 3.1 Shows a RTL View of a single observer stage with input clock of 50Mhz

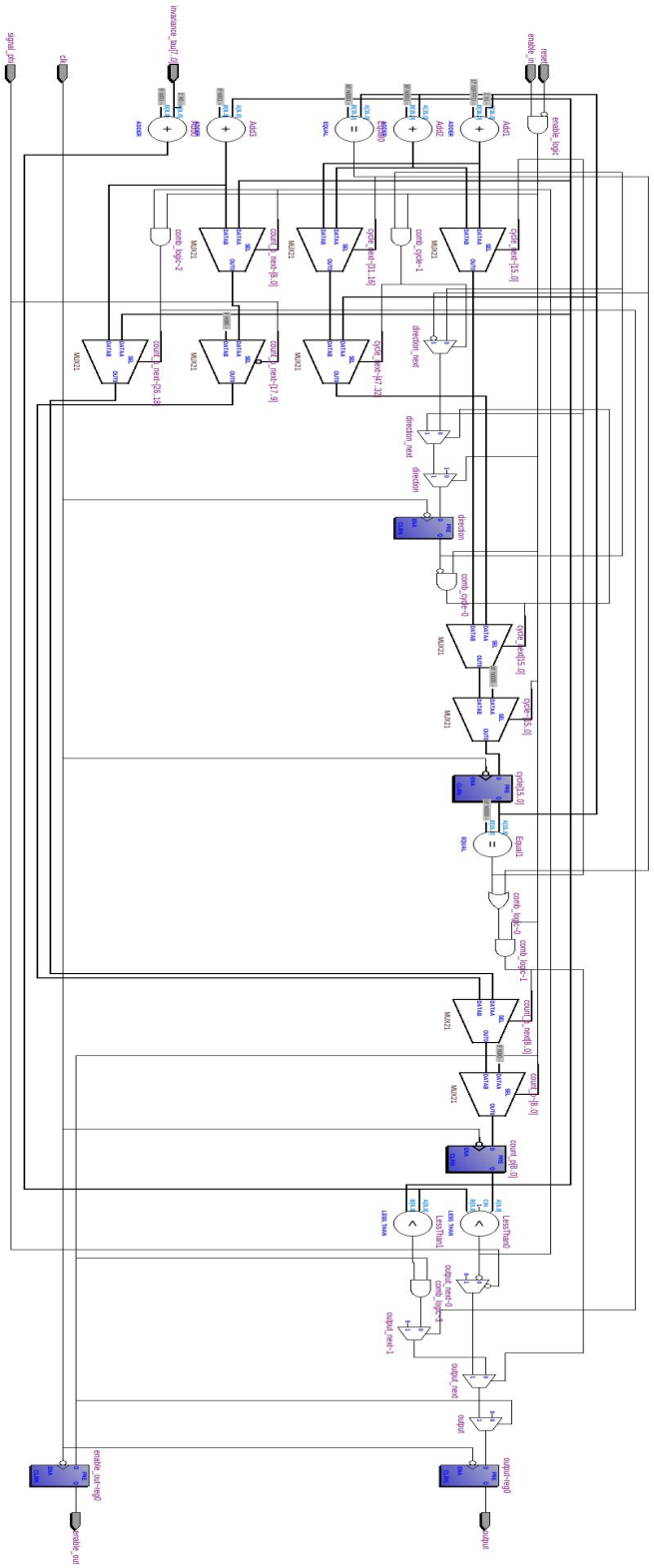

Fig. 3.2 Shows a RTL View of a single observer stage with input clock of 150Mhz

3.3 Design problems in the development

This subsection is only a kind of a protocoll about problems during the development.

1. The starting condition of the Algorithm 1 was uncertain, the question was, should variable count be initialised with 0 or with $(\tau+1)$. If count=$(\tau+1)$ then the output is immediately switched on, which correspond to an invariance qualification. From the specification of an observer in [4], it is known from the proof of Theorem 1(in [4]) that $\forall i : (i \in [max(0, n-\tau), n] \rightarrow e^i \models \phi)$ which follows that at the beginning of an execution if $n-\tau$ exceeds th bottom border, but the signal ϕ is true, the invariance qualification is fulfilled by that specification. This condition only holds if signal ϕ is known at that time, in our case the status of signal ϕ is always(if $m \geq 1$) taken from the past. So it is not known which status the signal ϕ has before execution time e^0. Hence, the Algorithm 1 was initialised in a manner, that no decisions can be made about invariance qualifications.

2. The Invariance Observer was tested with a self-made signalgenerator which imitates input ϕ. As a result, two clock domains were created, although the clock signals came from the same PLL(Phase Locked Loop). If the observers clock is an "even" multiple of the second clock frequency(signalgenerator), there was no problem, but if the clock frequencies are choosed in a different way, then it comes to clock drifts.

3. The file (*.sdc file)for timings has to be adjusted every time, if there are changes in one of the clock domains. The PLL output timings have to be analyzed separately by the TimeQuest Timing Analyzer. If this does not happen, false estimations are created for "Slow 1200mv 85°C model" maximum frequencies and worst case paths.

4. The first download of the compiled design to the FPGA was no succesfull, because the Quartus Tool was not correctly adjusted to that plattfom. Following points had to be changed:

   - The correct architecture must be set
   - the voltage level must be set for all inputs and outputs

5. It should be always considered what is the active state of an input component or output component, for example input KEY is low active and it was used to reset the FPGA board.

Chapter 4

Experiments and Testing

This Chapter is a detailed description about the simulations and experiments carried out on the Invariant Observer. The first section introduces a survey about the environment of the experiments and their semantic property. After the first section there comes a short overview about the simulations with ModelSim. In the final section there is a detailed description about the test cases and experiments, even something about the performance studies which where mentioned in subsection 3.2.3 of Chapter 3 before.

4.1 Reasoning and Environment of the Experiments

This section should be considered as an answer for the following questions “Which results do we gain from these experiments?” and “How are the experiments done?”.

4.1.1 Reasoning and Meaning

The Invariant Observer will interact in an environment where at least soft real-time, but rather hard real-time conditions will be considered. Therefore, the correct behaviour has to be shown with regard to the algorithm and the resulting VHDL Implementations. A good start to show a correct behaviour are simulations, but it should be mentioned that no clear assertions can be made about correct timings of the underlying Design. This question will be examined in section “Experiments”. How the simulations and experiments were executed, and which insights they produced, will be discussed in the next subsection. After the simulations, to present a first proof about the correct principle of the Invariant Observer, the VHDL Design had to be synthesized on a Hardware. A FPGA Board was the best solution,

besides other possibilities like ASIC's or a Microcontroller. An ASIC (Application-specific integrated circuit) is the most performant solution, but that solution is hard-wired and any change of the design is very expensive. But it could be considered as the final product implementation. A Microcontroller would never reach the performance of a FPGA Board and FPGA's are more cost effective and nearly performant like hard-wired solutions. Any change of the design can be easily downloaded on a FPGA Board, so it seems logical to use a FPGA as the prototyping platform. One important part of the experiments was to show the timing boundaries of the Observer Design. (e.g. the maximum performance on a FPGA board like the DE2-115, which was used for the experiments). But other FPGA's with stronger capabilities could reach better performance goals. In [4] for example, several FPGA models were used to reach a more expressive experiment. Another part of the experiments was to show the ability of handling any propositional formula ϕ, which is a temporal description of ongoing operations from an observed system. The evaluation of ϕ takes time, maybe several clock cycles, until the final computation W(ϕ) is finished. That circumstance was not exactly tested, but a different approach was introduced to emulate that behaviour. A more expressive experiment should be executed if this work will be continued.

The next subsection will explain the detailed investigations of the Invariant Observer through the experiments.

4.1.2 Build-up of Experiments

At the beginning some facts about the Invariant Observer will be repeated, to give a better understanding about the tests that were made. The Invariant Observer consist of several Observer Stages. To cover every clock cycle e^n, where a finished computation of a proposition $W(\phi)$ is evaluated, we need at least as many Observer Stages ($m \geq y$), as the computation (y clock cycles) needs. As a reminder, the Observer Stages are not responsible for the computation of the propositions (in contrast to [4]), but for the final evaluation of the status of the computation. So it seems logical to create a signal W(ϕ) which gives, at every clock cycle, a pseudo computation of a proposition ϕ. With that approach, it was easy to show the correct behaviour of the Invariant Observer. For example we have m=3 Observer (means theoretically that the computation of ϕ needs less than 3 clock cycles), and we want to show the invariance of signal W(ϕ), actually the finished computation $W(\phi)$ at every clock cycle, with $\tau = 10$. That 3 Observer Stages show whether the signal $W(\phi)$ was invariant 11 clock cycles, the current clock cycle included. The experiments have been exercised with a plain implementation of a signal $W(\phi)$ and with a more complex implementation of $W(\phi)$, which

gives a stronger argument of the correct behaviour. More about that in the sections “Experiments” and “Simulations”. These two versions of a simulated input signal for the Observer stages are justified with the fact, that the Quartus synthesis tool could create distinct implementations of the Observer Design, because it must match the correct timing behaviours in both cases. As a result, the experiments are separated in two parts, as already mentioned in the subsection 4.1.1 before, but this will be discussed in the section “Experiments”. The next section gives us an insight about the simulations.

4.2 Simulations

To simulate the VHDL Design of the Observer Stages the simulation tool **ModelSim (Version 10.1d)** from **MentorGraphics** was used. A testbench, created for simulations in Modelsim, gives a good overview about the intended behaviour of the implemented algorithm and it is useful for debugging and error detection. At the beginning, only one Observer Stage was simulated, because it demonstrates the simplest case. After error corrections and successful simulations of one Observer Stage, further simulations were proceeded with more Observer Stages.
In Figure 4.1 there is illustrated a simulation with m=5 Observer, where every Observer Stage monitors the yellow coloured input signal W(ϕ) for Invariance $\tau = 3$. The most left column shows the names of the illustrated signals. For every Observer (OBS1 to OBS5), signals cycle, $count_p$ and their corresponding outputs (add1 to add5) are shown to overlook their behaviour on the yellow coloured input signal *phi_s* (=W(ϕ)). Signals cycle and $count_p$ are already described in 2.2 and 3.2.3, so there is nothing additional. Signals add1 to add5 (grey coloured) are the outputs of the different Observer Stages, which are linked together in a binary add operation. The result of that operation is illustrated as the red coloured signal $output_s$ which shows the final result of the Invariance Observer.
Signal *phi_s* is generated by a complex signalgenerator to get a nearly universal test signal. The green coloured signal at the top indicates the system clock which drives the signalgenerator and all the Observer Stages at the same time. But the signalgenerator is driven on the rising edge, the Oberver Stages are driven on the falling edge. This fact is important to understand one further explanations of the simulation. The most important thing that is shown in that illustration is that the Observer Stages activate together the final *output_s* exactly $tau + 1$ (with $\tau = 3$) clock cycles after signal phi_s still holds his active state. This case is indicated between these two big vertical lines. It shows that the Invariance Observer monitored an Invariance Situation of signal *phi_s*, according to the behaviour described in

Chapter 2. That Invariance Situation continues three clock cycles until signal phi_s goes into a non active state and therefore output_s.
As mentioned before, signal phi_s changes his state on a rising edge, whereas an Observer Stage checks the state of signal phi_s on a falling edge. This also explains the delayed reaction of the Observer Stages on changes of the input signal as you can see in Figure 4.1. But this handicap could be enhanced by driving the Observers clock a multiple faster. The output of the signalgenerator phi_s is designed in a way to increase the invariance of his active state continuously, so it was reasonable to see how the final red coloured output behaves in comparison with phi_s. To make it clear, signal phi_s which is created by the signalgenerator only delivers a pseudo input for the Observer Stages which can be understood like as, at every clock cycle, a computation of ϕ is finished and the result of that computation W(ϕ) is illustrated as true (active state) or false (low state). But this also means, also for further simulations and experiments, that the number of Observer Stages in Figure 2.1 has no intended meaning. There could be less or more than five Observer Stages, the simulation would behave the same.
Finally, it should be discussed how the Observer Stages are initialised. The fourth signal from the top enable_s activates the first Observer Stage which is located at the beginning of an Observer Cascade Chain. This principle was already shown in Figure 2.1. After one clock cycle the following Observer Stage will be activated by signal en_1 from the Stage before, and after one clock cycle again signal en_2 activates the next Observer Stage and so on. In Figure 4.1 this behaviour is illustrated at the beginning by signal enable_s, signals en_1 till en_4 and the last output in the cascade by signal next_obs.
A further illustration from another simulation is shown in Appendix B with m=10 Observer.
A lot of simulations with different configurations were made, with different numbers of Observer Stages and different Invariance Qualifications. Automated Testing was necessary to have a stronger error check in case of changes in the design. Assertions as part of the VHDL language were inserted in to the Code to have a possibility to check if the behaviour of the Observer Stages is still the same. Modelsim gives also the possibility of scripting, which is very helpful when a lot of simulation parameters have to be handled.
The following final section introduces the experiments with a FPGA Board.

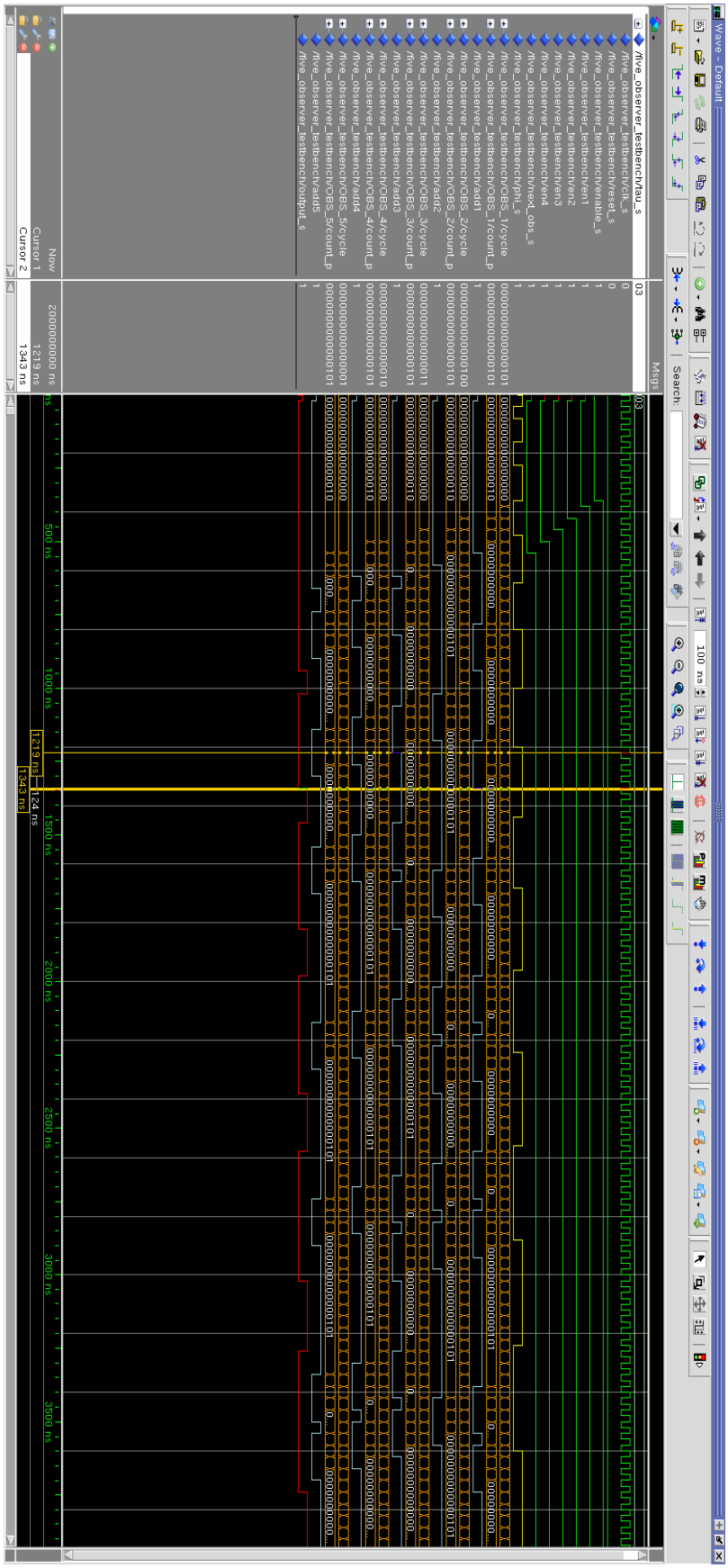

Fig. 4.1 Illustration of a Simulation with m=5 Observer and Invariance $\tau = 3$

4.3 Experiments

This section treats the experiments done for the Invariance Observer Design. The main part of the experiments were dedicated for testing the behaviour of the Invariant Observer. Other experiments were justified by the reason to figure out the maximum performance of the Observer Design. It is decent to present only the edge cases of the experiments, which have reasonable arguments, but that much is clear that a lot of more test cases where exercised. For the first, it was important that the correct behaviour of the Invariant Observer was tested and demonstrated on the FPGA Board. The correct behaviour of the Invariant Observer Design, synthesized on a DE2-115 FPGA board, will be shown by the following pictures made with the logic analyzer (Agilent 16803A). The logic analyzer was used to monitor the output pins **GPIO(0)** to **GPIO(34)** from the FPGA Board. An example of a TOP VHDL file which embeeds the Invariant Observer Design inside a Test Environment is shown in Appendix A.2. A lot of TOP files with different configurations where created, but this one example (A.3 and A.4) should only show how the experiments work. The output of every Observer Stage is connected to a GPIO output pin, and every of these GPIO pins can be measured and displayed on the logic analyzer. The pictures shown for up to 5 Observers (Figure 4.3 and Figure 4.2) show only the ouputs from **GPIO(0)** to **GPIO(14)** in the left side of every these pictures. For 10 Observers, the examples in Figure 4.4 and Figure 4.4 illustrate the output pins from **GPIO(0)** to **GPIO(31)**. For example the first signal **GPIO(0)** is always the **reset_s** signal similar to the arrangement in Figure 4.1. The names of the signals in the following picture are also the same like in the simulation, so it should be clear what the signals in the appropriate line means.

4.3.1 Testing the Behaviour

The experiments in this subsection are realized with a signalgenerator which was build individually to simulate a continuously increasing invariance signal. This is only the case, because we want to see the correct behaviour of the Observer Stages indicated by **add0** to **addn** and **final_output**. The signalgenerator and the observer stages are driven with the same input clock of 50Mhz, only for demonstrations. An indicated f_{max} means the maximum frequency estimation from the Quartus Tool for the whole design according to the Slow 1200mv 85°C model, which was described in subsection 3.2.2. But that will be more considered in the next subsection regarding the performance, whereas this section has no significant arguments regarding the performance of the Observer Stages, because f_{max} also depends on the included signalgenerator. The pictures in that subsection are very similar to

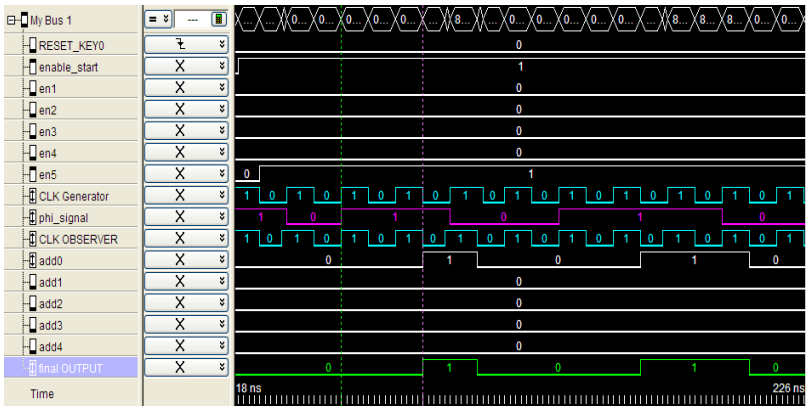

Fig. 4.2 Illustration from the Logic,only one Observer Stage with m=1,$\tau = 1$

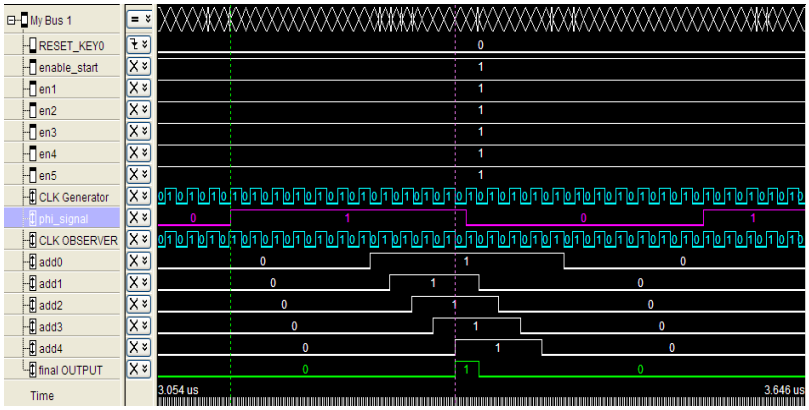

Fig. 4.3 Illustration from the Logic analyzer which shows the m=5,$\tau = 10$

the explanations in Section 4.2 regarding simulations, so only some few informations will be added. Every picture contains two clock signals, one for the signalgenerator and one for the Observer Stages, this was introduced only for the possibility that the frequency of **CLK_OBSERVER** is a multiple of **CLK_Generator**, but that idea was declined because of some irregular behaviours which will be discussed in the Summary of Chapter 5. In principle **CLK_Generator** and **CLK_OBSERVER** should be the same.

The simplest case is what the first picture Figure 4.2 shows, is one Observer $m = 1$ and $\tau = 1$. Likewise in the simulation explained the vertical lines indicates the start of an active signal phi_s and the start of it's Invariance Condition.

- $\tau = 1$ *with* $f_{max} = 91,41$ *Mhz* (shown in Figure 4.2)
- $\tau = 10$ *with* $f_{max} = 87,61$ *Mhz*

Figure 4.3 shows 5 Observer (m=5) with observing an Invariance of 10 clock cycles

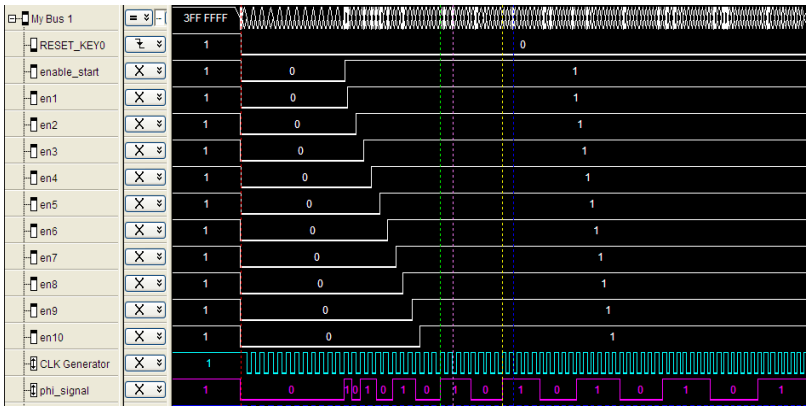

Fig. 4.4 Illustration from the Logic analyzer which shows the m=10,$\tau = 1$

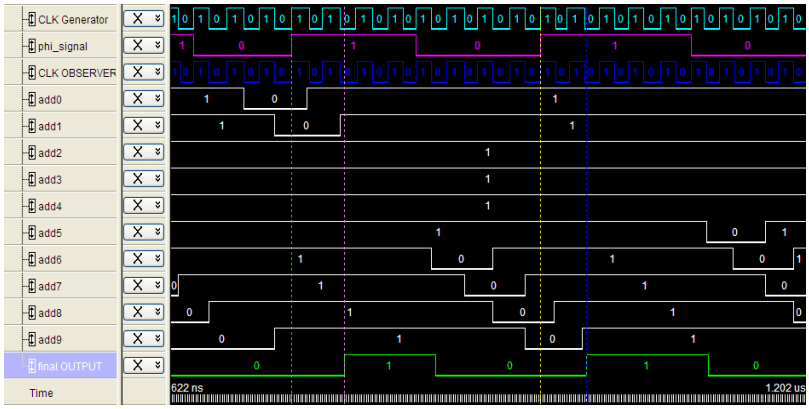

Fig. 4.5 Illustration from the Logic analyzer which shows the m=10,$\tau = 1$

Signal **final_OUTPUT** is the binary conjunction from **add0** to **add4**. The vertical lines indicate the beginning of the observation by the Observer Stages (phi_s in active state) and the Invariance Condition $\tau = 10$ fullfilled at the right vertical line. If every falling edge of signal **CLK_OBSERVER** is counted between both vertical lines, it should be equal to $\tau + 1 = 11$. Same principle should hold for further pictures.

Figure 4.4 and Figure 4.5 show the same experiment (illustration from logic analyzer separated in two pictures) with 10 Observer (m=10) which are observing Invariance of $\tau = 1$ on signal phi_s. Figure 4.5 illustrates the same behaviour like the pictures before.
Figure 4.5 also shows how the Observer Stages are activated, one by one. Signal **enable_start** shows the start of that start-up sequence, which illustrates the behaviour according to the Algorithm 1 that every Observer Stage turns on the next following Observer Stage after one clock cycle as illustrated by Figure 2.1.

The next subsection shows a chain of experiments which could be argued as “What is the maximum possible clock frequency that can drive the Observer Stages?”

4.3.2 Maximum Performance

This subsection discusses the maximum possible performance of the Observer Stage Design under involvement of the limitation by the DE2-115 FPGA Board. The following testchain comprise the Invariant Observer Design and a plain Signalgenerator, which only changes the signalvalue of his output at every clock cycle. For this experiment it was important that the Quartus II tool take his focus on the Observer circuit, and estimations of the Slow 1200mv 85°C model depends only on the Observer Design. Another modification is that the Phase-Locked Loop (PLL) is used actively, which means that the clock frequency of the Observer Design will be increased in several steps, depending on the experiment case. At every increase of the input clock frequency, the timing model file (*.sdc) must be updated with the Time Quest Analyzer tool. Then depending on the current clock, the number of Observer Stages will be increased, to see the maximum performance for that configuration. The maximum range of Invariance $\tau = 255$ is always used, but some experiment cases may have additional tests with another Invariance τ where the differences in the performance can be seen. Similar to the previous subsection, f_{max} means the maximum frequency according to the Slow 1200mv 85°C model as a result of the Quartus Timing Model estimation.

Legend:
(LE is the number of Logic Elements used on the FPGA Board from available 114480LE)

(1) Inputfrequency for all Observer Stages: **50Mhz** with plain Signalgenerator

a) 1 Observer , $\tau = 255$ and $f_{max} = 86,4Mhz$

b) 10 Observer, $\tau = 255$ and $f_{max} = 101,83Mhz$

c) 100 Observer, $\tau = 10$ and $f_{max} = 83,81Mhz$ (6718 LE$\sim$6%)
$\tau = 255$ and $f_{max} = 79,88Mhz$

d) 300 Observer, $\tau = 255$ and $f_{max} = 74,01Mhz$

e) 1000 Observer, $\tau = 255$ and $f_{max} = 66,00Mhz$ (72514 LE$\sim$63%)

(2) Inputfrequency for all Observer Stages: **100Mhz** with plain Signalgenerator

a) 1 Observer , $\tau = 255$ and $f_{max} = 96,82Mhz$

b) 10 Observer, $\tau = 255$ and $f_{max} = 134,99Mhz$

c) 100 Observer, $\tau = 255$ and $f_{max} = 116,44Mhz$

d) 1000 Observer, $\tau = 1$ and $f_{max} = 106,09Mhz$
$\tau = 255$ and $f_{max} = 95,27Mhz$ (72755 LE$\sim$64%)

(3) Inputfrequency for all Observer Stages: **200Mhz** with plain Signalgenerator

a) 1 Observer , $\tau = 255$ and $f_{max} = 90,82Mhz$

b) 10 Observer, $\tau = 255$ and $f_{max} = 139,30Mhz$ (possible **MAXIMUM**)

c) 100 Observer, $\tau = 255$ and $f_{max} = 114,57Mhz$

d) 1000 Observer, $\tau = 255$ and $f_{max} = 103,46Mhz$

In the experiment from (3) case b) the synthesis with the maximum possible performance of the Invariant Observer Design was created by the Quartus Tool. In Appendix C.2 there is an illustration of the RTL View of that design case. As high the performed input clock is, as well must Quartus sythesize the design to meet the requirements for that frequency. This results to the fact that the worst case path time must stay inside the time needed for a clock cycle. In all three experiments from (1) to (3) it can be seen that it is not always possible to meet these requirements for an input clock. Especially, in the experiments with 200MHZ input clock there is no single case that meets that requirement.

One interesting thing that can be seen in all three experiments (1),(2),(3) is that for case b) with 10 Observers, the Quartus tool reach always the maximum performance out of these cases. 1000 Observer occupy nearly 64% of the capacity of the Logic Elements that a FPGA Board possesses, so that means that the upper bound of possible Observers are close to 1500. This is the maximum limit of Observers that can be synthesized on the DE2-115 board. Other boards with higher capacity are obviously capable to contain more Observers. (e.g. DE4 model series with Stratix IV FPGA cores with up to 820K LE) Finally, the differences between different values of τ are not significant as we can see in 1c), 2d), hence the variance keeps inside 10Mhz.

Chapter 5

Summary

It was introduced an alternative version of an Invariant Observer from [4] which circumvents specific design restrictions from [4]. For example, propositions ϕ are not restricted by the logahedron class of atomic proposition like in [4], so there is not a tight time bound to fulfil. With the possibility of a massively parallel constuction of the Observer Stages as parts of a complete Invariant Observer which allows evaluating a proposition ϕ at every clock cycle, it could result to a big performance step. The Observer Stages are in way more flexible than in [4], besides the possibility to change the Invariant τ during runtime. But these agile advantages should be tested in a more detailed experiment and under real-time conditions. Another point to mention is, that the experiments considered only the case that the Observer Stages are running in the same time domain like the system that evaluates the proposition ϕ to W(ϕ). For example three clock cycles which passes for W(ϕ) are also the same three clock cycles for the Observer Stages. It came out, that a better resolution could be performed if the frequency that drives the Observer Stages is multiple higher than the frequency of the system that evaluates W(ϕ). For example if the evaluation system for W(ϕ) is driven with 10Khz and the Observer Stages with 20Khz and an Invariance of $\tau = 2$ on W(ϕ) should be monitored, then the Observer Stages must observe an invariance of $\tau = 4$ to meet the same time domain. That aspect should be considered in further real-time experiments. In [4] these two systems are acting together. The Invariant Observer should be considered as a temporal operator which follows the specifications of ptMTL $\boxdot_{[y,y+\tau]}$ but with the restriction that it can not perform the observation of the invariance inside intervall [0,y]. That means, that the computation time for a proposition ϕ can not be less than y (maybe the only disadvantage). The design approach of the Invariant Observer shows maybe possibilities to implement other temporal operators from the Metric Temporal Logic like the “Exists-Operator within Intervals”, that could be also an attempt for further studies.

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Appendix A

Source Implementation in VHDL

A.1 Observer Stage

A.2 TOP File

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  use IEEE.NUMERIC_STD.ALL;
4
5
6  entity observer is
7  generic (
8    observernumber:unsigned(15 downto 0):=x"0001"  -- how many observer are instan
   tiated
9        );
10 port (
11
12   clk          :in   std_logic;
13   reset        :in   std_logic;
14   enable_in    :in   std_logic;
15   invariance_tau  :in   std_logic_vector(7 downto 0);
16   signal_phi      :in   std_logic;
17   output    :out  std_logic;
18   enable_out      :out  std_logic
19   );
20
21 end entity;
22
```

Fig. A.1 Code of Observer Entity Design

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  use IEEE.NUMERIC_STD.ALL;
4
5
6
7  architecture Behavioural of observer is
8
9  signal inc_tau                  : unsigned(8 downto 0):= "000000000";
10 signal count,count_next         : unsigned(15 downto 0):= x"0001";
11 signal count_p,count_p_next     : unsigned(15 downto 0):= x"0002";
12 signal cycle,cycle_next         : unsigned(15 downto 0) := x"0000";
13 signal direction,direction_next : std_logic := '1';
14
15
16 signal enable_logic             : std_logic := '0';
17 signal output_next              : std_logic := '0';
18 begin --BEGIN ARCHITECTURE
19
20 -- parallel logic
21 inc_tau <= unsigned(invariance_tau) + to_unsigned(1,9) ;
22 enable_logic <= enable_in and not reset;
23
24 -- changes cycle up from 0 to observernumber and down back to 0
25 comb_cycle: process(cycle,direction,enable_logic)
26 begin --changes cycle_next, direction, changeDirection
27   if(direction = '0' and enable_logic = '1') then
28     if(cycle = 0)then
29       direction_next <= '1';
30       cycle_next <= cycle + 1;
31     else
32       direction_next <= '0';
33       cycle_next <= cycle - 1;
34     end if;
35   elsif(direction = '1' and enable_logic = '1') then
36     if(cycle = observernumber)then
37       direction_next <= '0';
38       cycle_next <= cycle - 1;
39     else
40       direction_next <= '1';
41       cycle_next <= cycle + 1;
42     end if;
43   else
44     direction_next <= direction;
45     cycle_next <= cycle;
46   end if;
47 end process comb_cycle;
48
49
50 -- main logic of the observer
51 comb_logic: process(inc_tau,count,count_p,cycle,signal_phi,enable_logic)
52 begin
53   if ( (cycle = observernumber  or cycle = 0) and enable_logic = '1') then -- m
   cycles passed
54     if(signal_phi = '0') then   -- w(phi) = 0
55         count_next  <= x"0001";
56         count_p_next <= x"0002";
57         output_next <= '0';
58     elsif(count_p <= inc_tau) then
59       count_next  <= count  + 1; --every clock cycle
60       count_p_next <= count_p + 1 ;
61         output_next      <= '0';
62     else
63       count_next   <= count;
64       count_p_next <= count_p;
65       output_next      <= '1';
66     end if;
67   elsif(count_p <= inc_tau and enable_logic = '1') then
68     count_next  <= count + 1; --every clock cycle
69     count_p_next <= count_p + 1 ;
70       output_next      <= '0';
71   elsif(count_p > inc_tau and enable_logic = '1') then
72     count_next  <= count;
73     count_p_next <= count_p;
74     output_next  <= '1';
75   else
76     count_next   <= count;
77     count_p_next <= count_p;
78     output_next  <= '0';
79   end if;
80 end process comb_logic;
81
82 --the synchronisation logic
83 sync: process(clk,enable_logic)
84   begin
85     if(clk'event and clk = '0')then
86       if(enable_logic = '1') then
87         cycle          <= cycle_next;
88         direction      <= direction_next;
89         count          <= count_next;
90         count_p        <= count_p_next;
91         output         <= output_next;
92         enable_out     <= '1';
93       else
94         cycle          <= x"0000";
95         direction      <='1';
96         count   <= x"0001";
97         count_p <= x"0002";
98           output      <= '0';
99           enable_out <='0';
100      end if;
101    end if;
102  end process sync;
103 end architecture;--END ARCHITECTURE
```

Fig. A.2 Code of the Behavioural Design of an Invariant Observer

```
LIBRARY ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use IEEE.std_logic_misc.all;

entity top_10Obs is

port (
  ClOCK_50          :in    std_logic;
  KEY               :in    std_logic_vector(3 downto 0) ;
  GPIO              :out   std_logic_vector(34 downto 0) );

end entity;

-------------------- ARCHITECTURE ----------------------------------
--------------------------------------------------------------------
architecture rtl of top_10Obs is

constant  tau_range  :integer := 20;

component Altplc is
  PORT(
    areset      : IN STD_LOGIC  := '0';
    inclk0      : IN STD_LOGIC  := '0';
    c0          : OUT STD_LOGIC ;  -- 50Mhz
    c1          : OUT STD_LOGIC ;  -- 50Mhz
    c2          : OUT STD_LOGIC ;  -- 100 Mhz
    c3          : OUT STD_LOGIC    -- 100 Mhz
  );
end component;


component signalgenerator is
  port(
    clk     :in  std_logic   := 'X';
    reset   :in  std_logic   := 'X';
    output  :out std_logic   -- export
  );
end component signalgenerator;


component observer
    generic (
      observernumber :unsigned(15 downto 0):=x"0001"  -- how many observer are
  instantiated
      );
    PORT (
      clk           :in     std_logic       := 'X';
      reset         :in     std_logic       := 'X';
      enable_in     :in     std_logic;
      invariance_tau :in    std_logic_vector(7 downto 0);
      signal_phi    :in     std_logic;
      output        :out    std_logic;
      enable_out    :out    std_logic
      );
end component;

-------------------------------------------------------------------------
-- <BEGIN_0>
FOR OBS_0 : observer
 use entity work.observer(Behavioural);
FOR OBS_1 : observer
 use entity work.observer(Behavioural);
FOR OBS_2 : observer
 use entity work.observer(Behavioural);
FOR OBS_3 : observer
 use entity work.observer(Behavioural);
FOR OBS_4 : observer
 use entity work.observer(Behavioural);
FOR OBS_5 : observer
 use entity work.observer(Behavioural);
FOR OBS_6 : observer
 use entity work.observer(Behavioural);
FOR OBS_7 : observer
 use entity work.observer(Behavioural);
FOR OBS_8 : observer
 use entity work.observer(Behavioural);
FOR OBS_9 : observer
 use entity work.observer(Behavioural);

-- <END_0>

-------------------------------------------------------------------------
-- <BEGIN_1>
signal add: std_logic_vector(9 downto 0):=(others=>'0');
signal clk_s              : std_logic       :='0';
signal clk_g              : std_logic       :='0';
signal reset_s            : std_logic       :='0';
signal enable_s           : std_logic       :='0';
signal phi_s              : std_logic       :='0';
signal next_obs_s  : std_logic       :='0';
signal en1                :std_logic:='0';
signal en2                :std_logic:='0';
signal en3                :std_logic:='0';
signal en4                :std_logic:='0';
signal en5                :std_logic:='0';
signal en6                :std_logic:='0';
signal en7                :std_logic:='0';
signal en8                :std_logic:='0';
signal en9                :std_logic:='0';

-- <END_1>
-------------------------------------------------------------------------
signal output_s           : std_logic       :='0';
signal tau_s              : std_logic_vector(7 downto 0) := (others => '0');


-------------------------------------------------------------------------
---- BEGIN OF ARCHITECTURE ----------------------------------------------
-------------------------------------------------------------------------
---
begin

signalgenerator_top : component signalgenerator
  port map (
    output => phi_s,
    reset => reset_s,
    clk => clk_g
    );

PLL: component AltPLc
PORT MAP (areset => reset_s,inclk0 => CLOCK_50 ,c1 => clk_g,c0 =>clk_s) ;

-------------------------------------------------------------------------
-- <BEGIN_2>
OBS_0: observer GENERIC MAP(observernumber => x"000A")
  PORT MAP ( output=>add(0),clk=>clk_s,reset =>reset_s, enable_in =>enable_s,invariance_tau => tau_s,
signal_phi=> phi_s,enable_out=>en1) ;
OBS_1: observer GENERIC MAP(observernumber => x"000A")
  PORT MAP ( output=>add(1),clk=>clk_s,reset =>reset_s, enable_in =>en1,invariance_tau => tau_s,signa
l_phi=> phi_s,enable_out=>en2);
OBS_2: observer GENERIC MAP(observernumber => x"000A")
  PORT MAP ( output=>add(2),clk=>clk_s,reset =>reset_s, enable_in =>en2,invariance_tau => tau_s,signa
l_phi=> phi_s,enable_out=>en3);
OBS_3: observer GENERIC MAP(observernumber => x"000A")
  PORT MAP ( output=>add(3),clk=>clk_s,reset =>reset_s, enable_in =>en3,invariance_tau => tau_s,signa
```

Fig. A.3 Example Code of a TOP file for experiments

```
l_phi=> phi_s,enable_out=>en4) ;
OBS_4: observer GENERIC MAP(observernumber => x"000A")
   PORT MAP ( output=>add(4),clk=>clk_s,reset =>reset_s, enable_in =>en4,invariance_tau => tau_s,signa
l_phi=> phi_s,enable_out=>en5) ;
OBS_5: observer GENERIC MAP(observernumber => x"000A")
   PORT MAP ( output=>add(5),clk=>clk_s,reset =>reset_s, enable_in =>en5,invariance_tau => tau_s,signa
l_phi=> phi_s,enable_out=>en6) ;
OBS_6: observer GENERIC MAP(observernumber => x"000A")
   PORT MAP ( output=>add(6),clk=>clk_s,reset =>reset_s, enable_in =>en6,invariance_tau => tau_s,signa
l_phi=> phi_s,enable_out=>en7) ;
OBS_7: observer GENERIC MAP(observernumber => x"000A")
   PORT MAP ( output=>add(7),clk=>clk_s,reset =>reset_s, enable_in =>en7,invariance_tau => tau_s,signa
l_phi=> phi_s,enable_out=>en8) ;
OBS_8: observer GENERIC MAP(observernumber => x"000A")
   PORT MAP ( output=>add(8),clk=>clk_s,reset =>reset_s, enable_in =>en8,invariance_tau => tau_s,signa
l_phi=> phi_s,enable_out=>en9) ;
OBS_9: observer GENERIC MAP(observernumber => x"000A")
   PORT MAP ( output=>add(9),clk=>clk_s,reset =>reset_s, enable_in =>en9,invariance_tau => tau_s,signa
l_phi=> phi_s,enable_out=> next_obs_s) ;

--- <END_2>
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
---<BEGIN_3>
ouput_s <= and_reduce(add);
---<END_3>
-------------------------------------------------------------------------------

-------------------------------FPGA OUTPUTS-----------------------------------
-------------

reset_s <= not KEY(0);

GPIO(0) <= reset_s;
GPIO(1) <= enable_s;
GPIO(2) <= en1;
GPIO(3) <= en2;
GPIO(4) <= en3;
GPIO(5) <= en4;
GPIO(6) <= en5;
GPIO(7) <= en6;
GPIO(8) <= en7;
GPIO(9) <= en8;
GPIO(10) <= en9;
GPIO(11) <= next_obs_s;
GPIO(12) <= clk_g;
GPIO(13) <= phi_s;
GPIO(14)<= clk_s;

GPIO(15) <= add(0);
GPIO(16) <= add(1);
GPIO(17) <= add(2);
GPIO(18) <= add(3);
GPIO(19) <= add(4);
GPIO(20) <= add(5);
GPIO(21) <= add(6);
GPIO(22) <= add(7);
GPIO(23) <= add(8);
GPIO(24) <= add(9);
GPIO(25)<= ouput_s;

tau_s       <= std_logic_vector(to_unsigned(tau_range,8));
-------------------------------SYNCHRONIZED-----------------------------------
-------------
sync:process(clk_s)
```

```
begin
if(clk_s'event and clk_s='1') then
   if reset_s ='0' then
      enable_s <= '1';
   else
      enable_s <= '0';
   end if;
end if;
end process;

end architecture;
```

Fig. A.4 Example Code of a TOP file for experiments

Appendix B

Modelsim Simulations

B.1 Simulations with 10 Observer

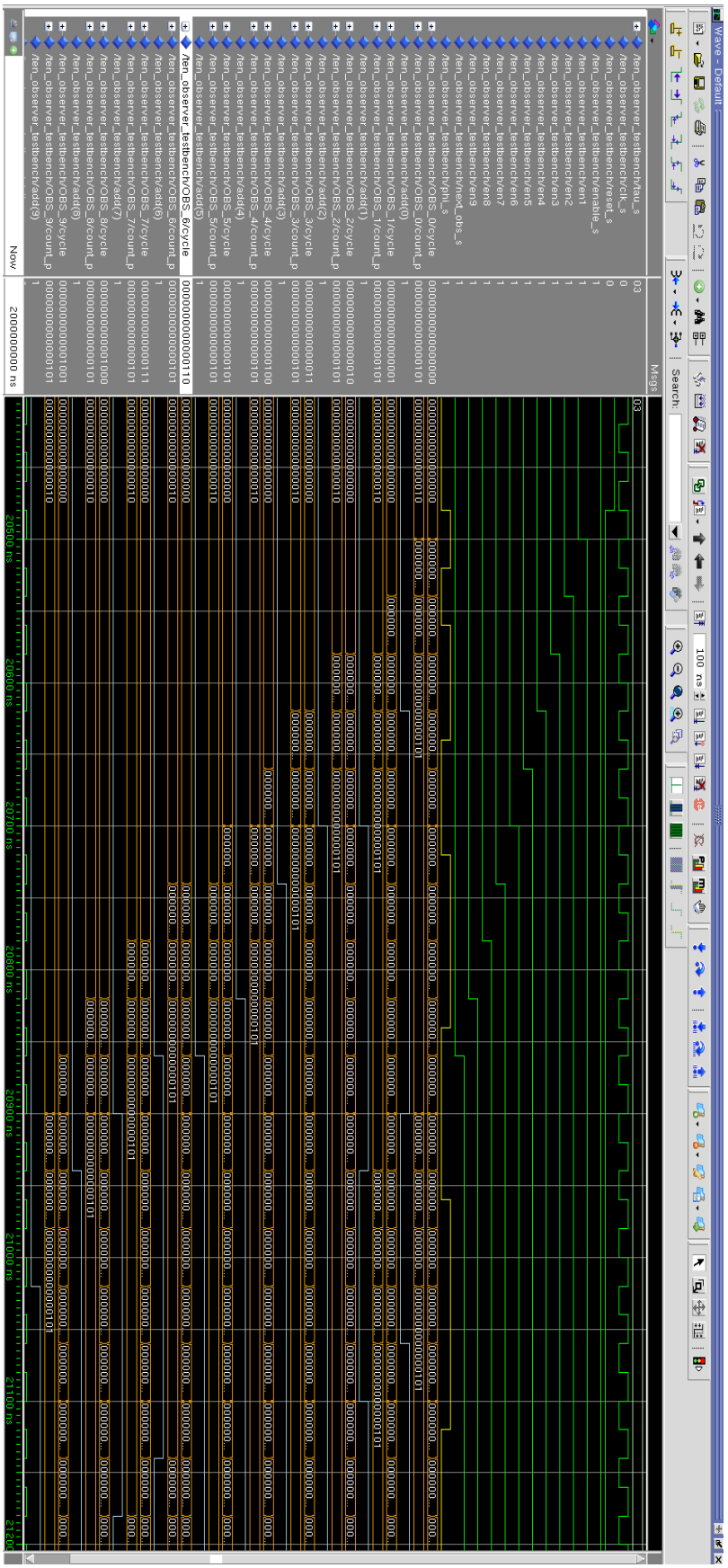


Fig. B.1 m=10 Observer and $\tau = 3$ with view about cascade activation of the observer

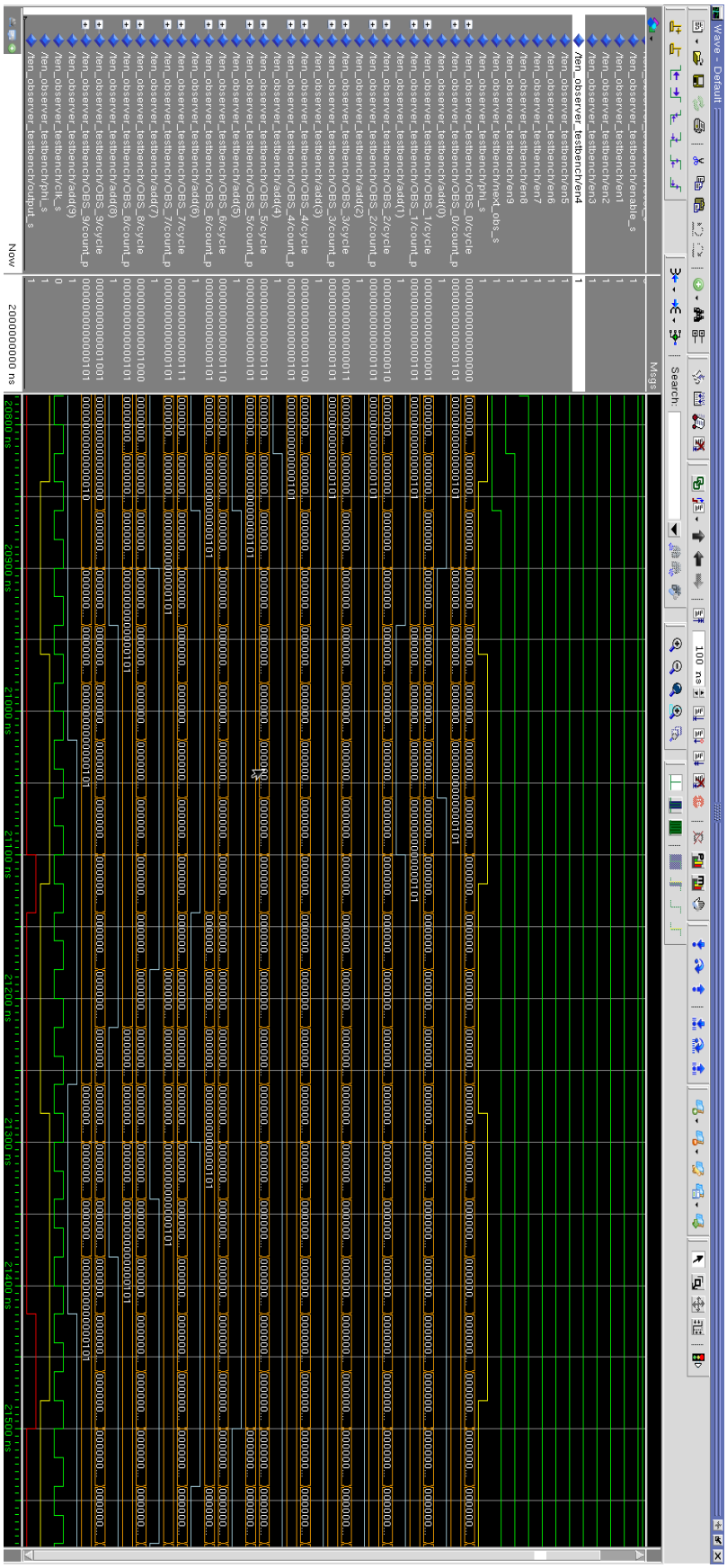


Fig. B.2 m=10 Observer and $\tau = 3$ with view about the output of the Observer Stages and final red-colored output

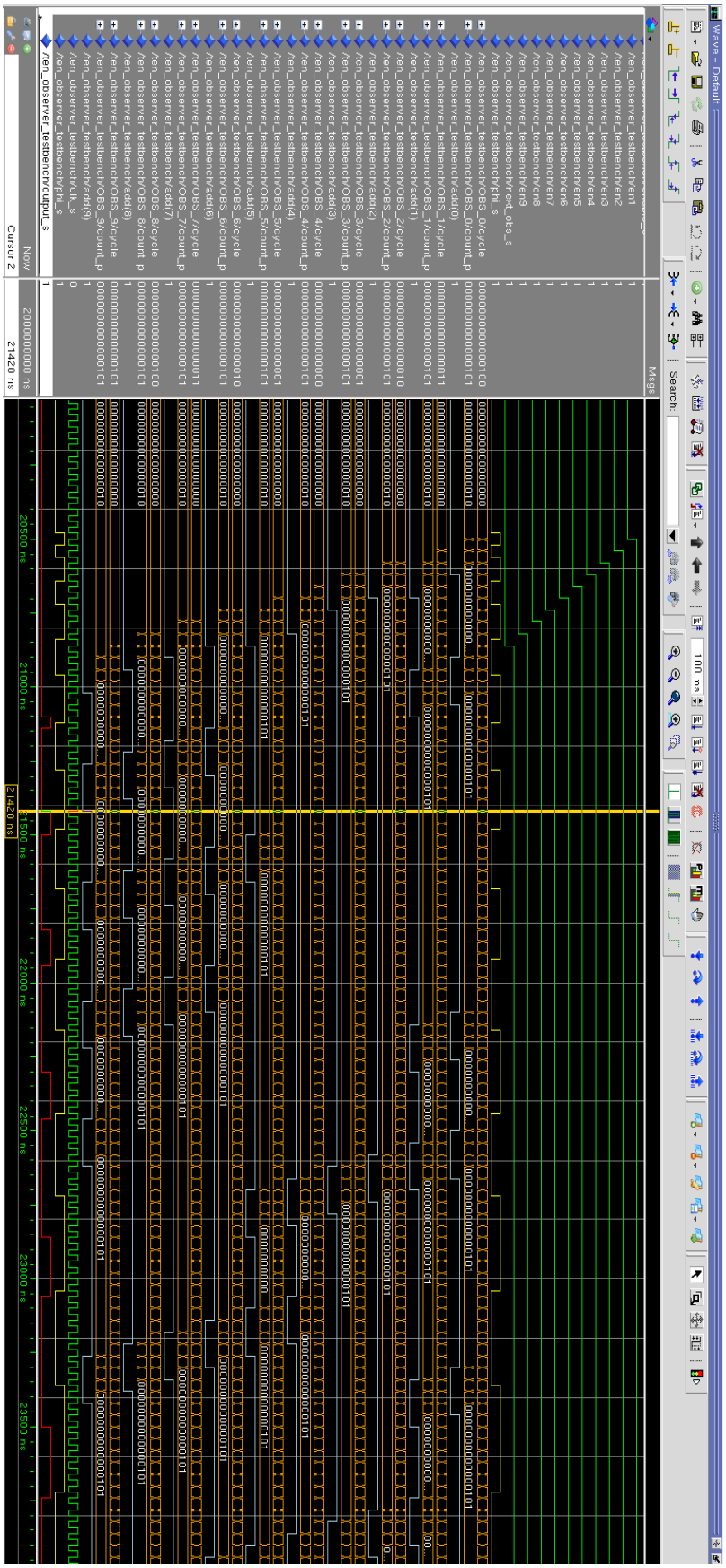


Fig. B.3 m=10 Observer and $\tau = 3$ with an overall view

Appendix C

Register Transfer Level Design View

C.1 Design of the First Version

C.2 Design of the most performant Version

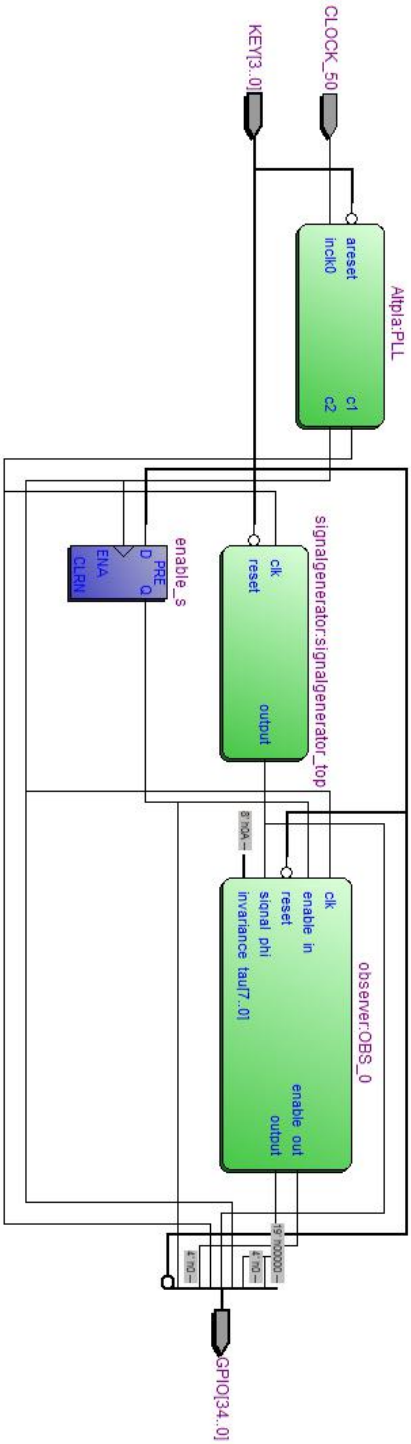


Fig. C.1 Illustration of the TOP Design of the first correct version,but without improvements

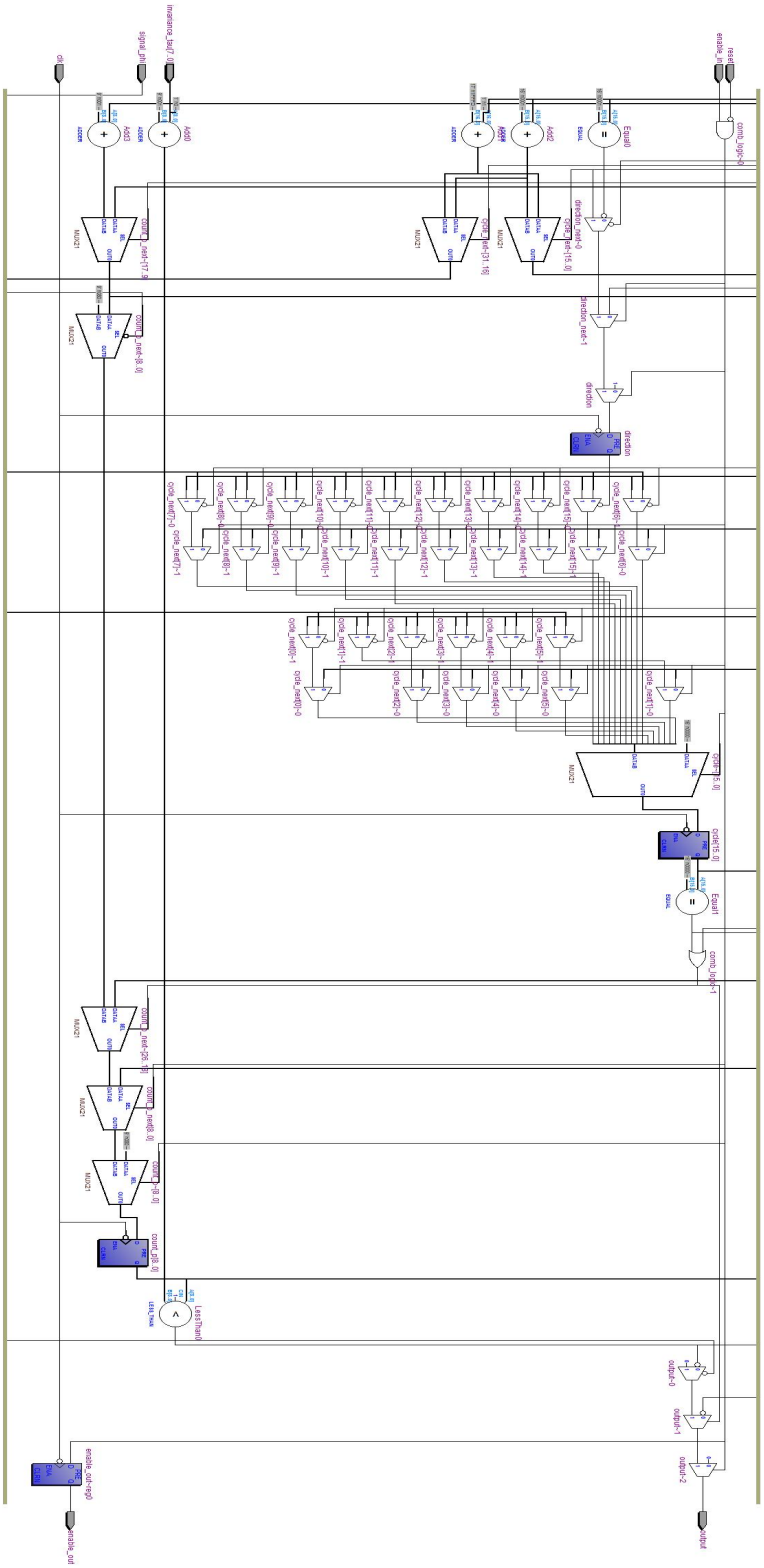


Fig. C.2 Illustration of the Observer Design of the first correct version,but without improvements

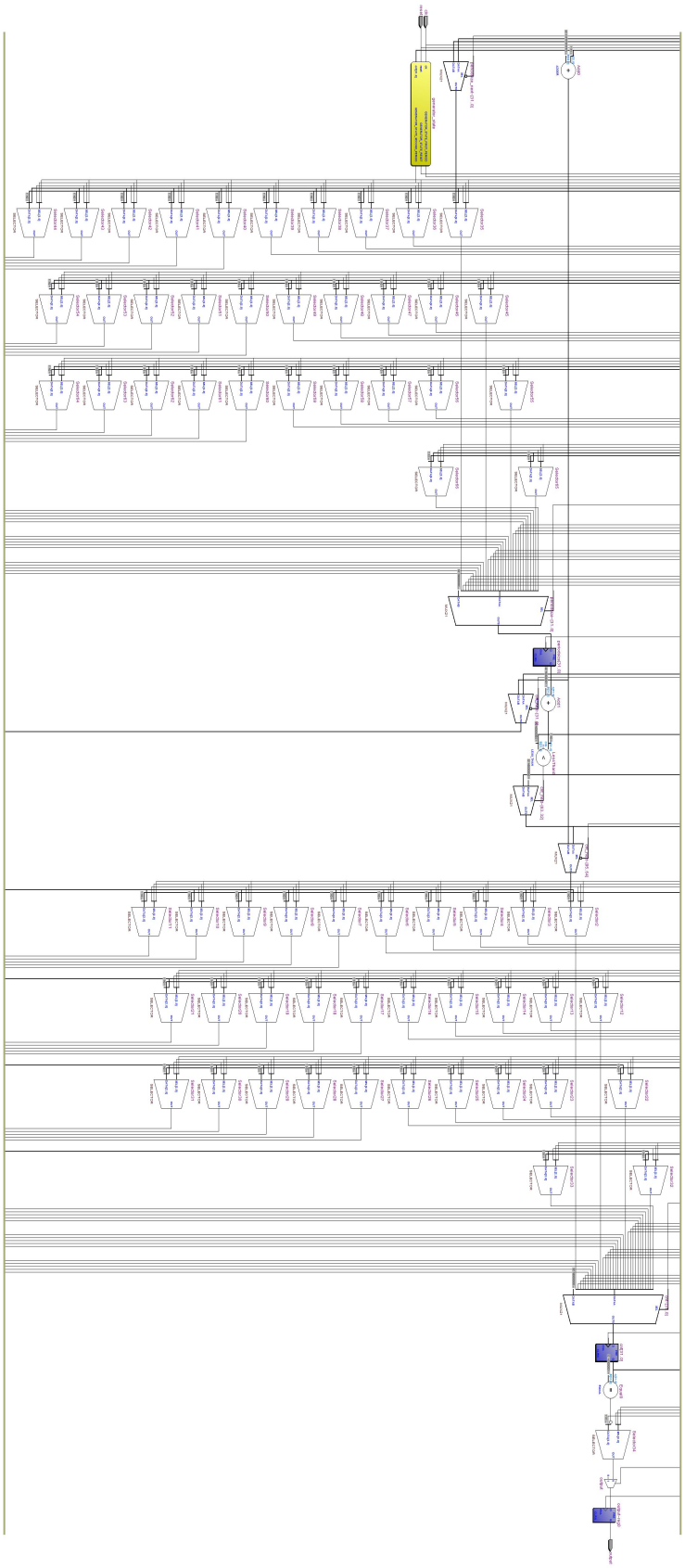


Fig. C.3 Illustration of the Signalgenerator of the first correct version,but without improvements

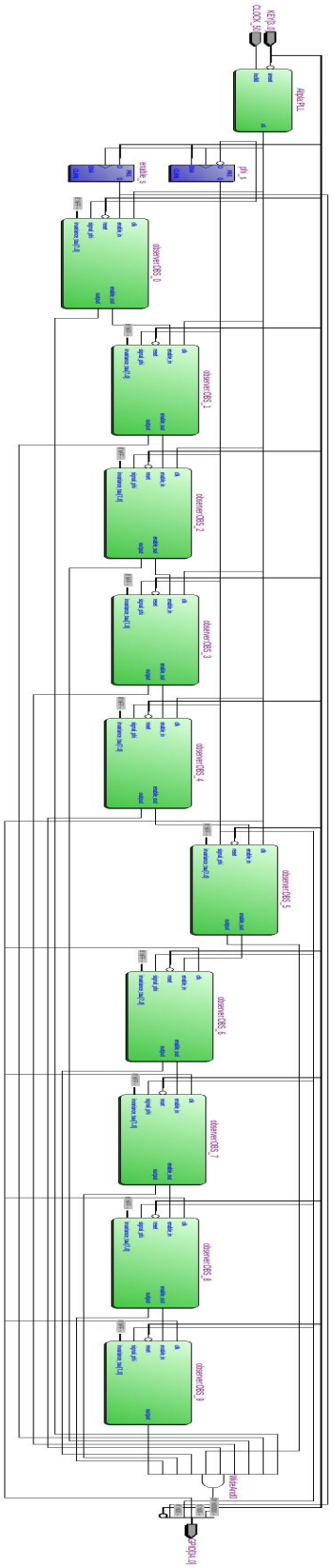


Fig. C.4 Illustration of the TOP Design with the the best performance

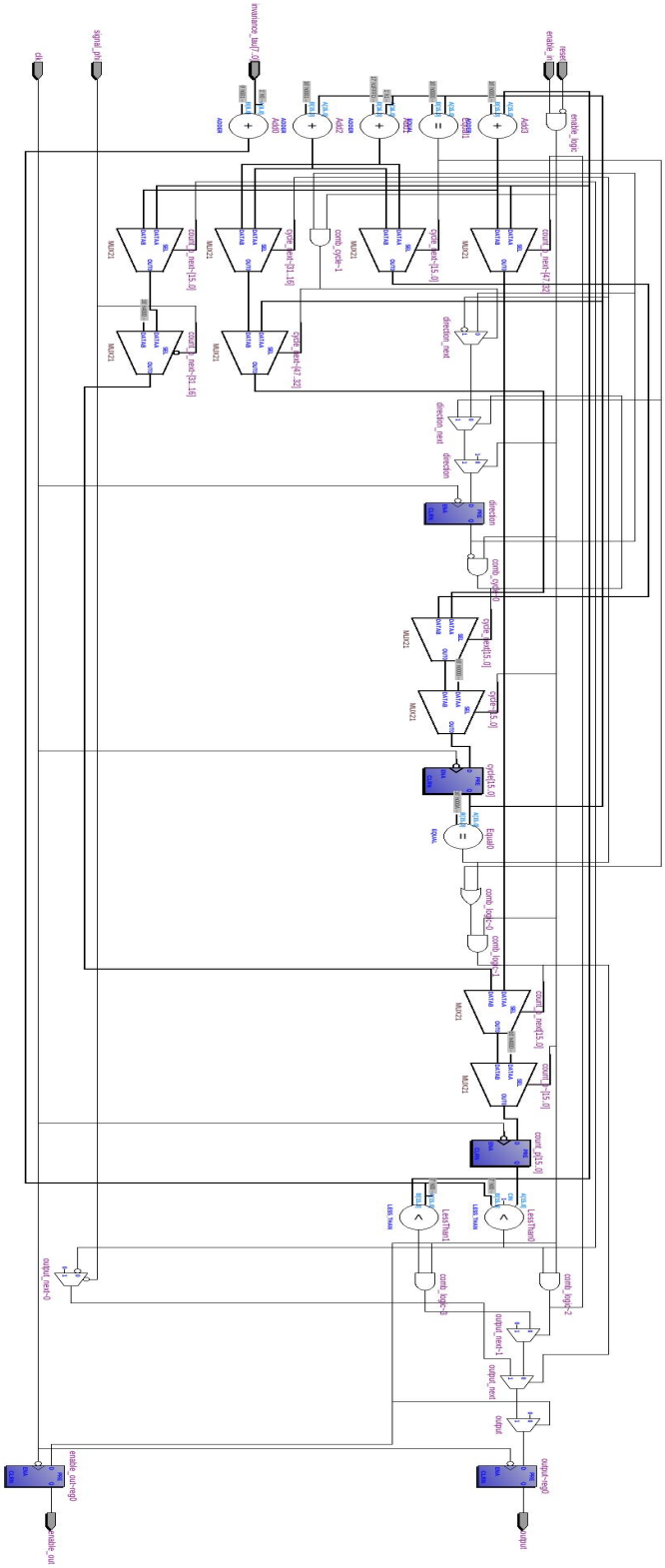


Fig. C.5 Illustration of the Observer 0 from 9

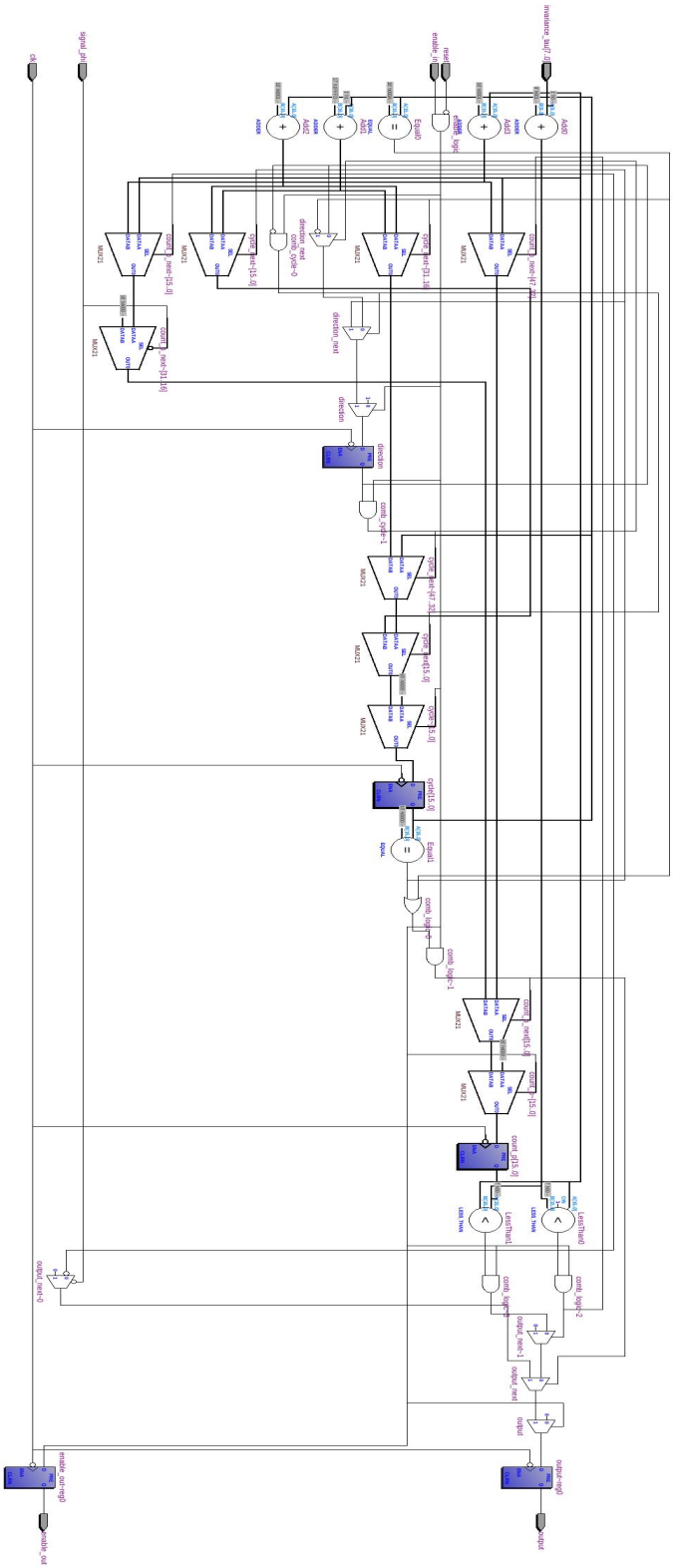


Fig. C.6 Illustration of the Observer 0 from 9

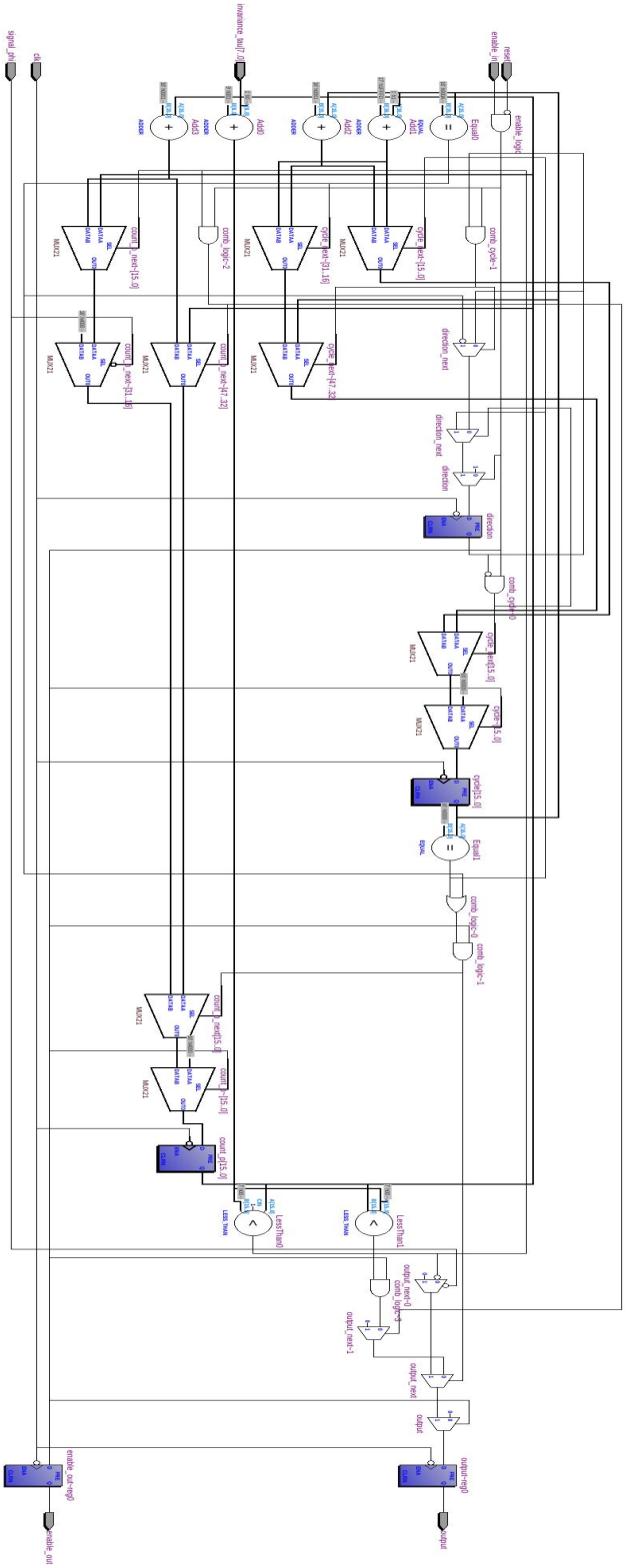
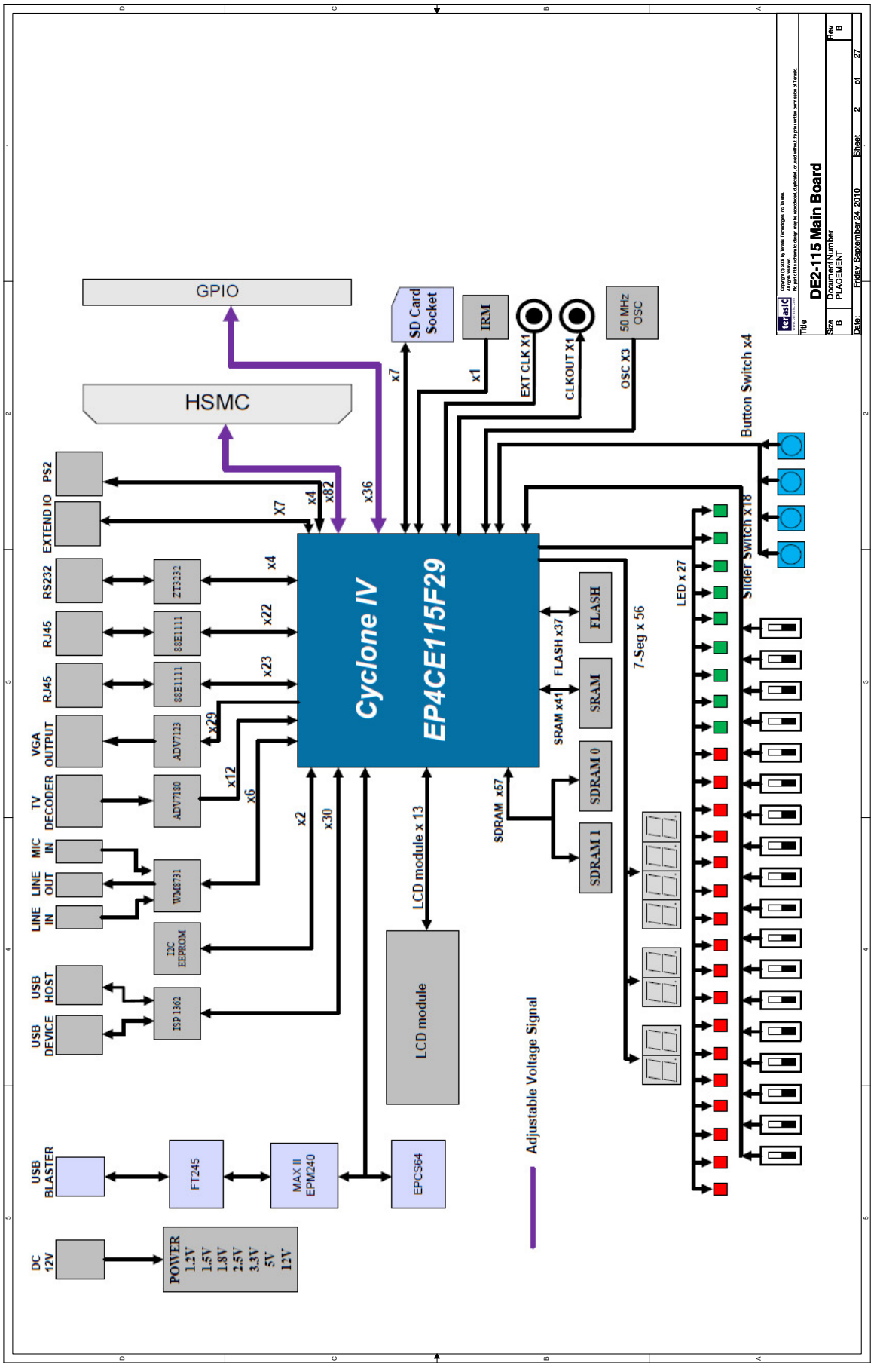


Fig. C.7 Illustration of the Observer 5 from 9

Appendix D

Datasheets and Descriptions


GPIO
HSMC
SD Card Socket
IRM
EXT CLK X1
CLKOUT X1
50 MHz OSC
OSC X3
Button Switch x4
Slider Switch x18
LED x27
7-Seg x56
FLASH
FLASH x37
SRAM
SRAM x41
SDRAM 0
SDRAM 1
SDRAM x57
Cyclone IV
EP4CE115F29
LCD module x 13
LCD module
Adjustable Voltage Signal
PS2
EXTEND IO
RS232
RJ45
RJ45
VGA OUTPUT
TV DECODER
MIC IN
LINE OUT
LINE IN
USB HOST
USB DEVICE
ZT3232
88E1111
88E1111
ADV7123
ADV7180
WM8731
I2C EEPROM
ISP 1362
USB BLASTER
FT245
MAX II EPM240
EPCS64
DC 12V
POWER
1.2V
1.5V
1.8V
2.5V
3.3V
5V
12V
x7
x1
x36
x82
x4
X7
x4
x22
x23
x29
x12
x6
x2
x30
Title
DE2-115 Main Board
Size
B
Document Number
PLACEMENT
Rev
B
Date:
Friday, September 24, 2010
Sheet
2
of
27