PRS/KS/24/2212

Faculty of Science & Technology

Fourth Semester B.E. (Information Technology) (C.B.S.) Examination

COMPUTER ARCHITECTURE AND ORGANIZATION

Paper–4

Time : Three Hours] [Maximum Marks : 80

INSTRUCTIONS TO CANDIDATES

(1) All questions carry marks as indicated.
(2) Solve Question **1 OR** Question No. **2**.
(3) Solve Question **3 OR** Question No. **4**.
(4) Solve Question **5 OR** Question No. **6**.
(5) Solve Question **7 OR** Question No. **8**.
(6) Solve Question **9 OR** Question No. **10**.
(7) Solve Question **11 OR** Question No. **12**.
(8) Assume suitable data wherever necessary.
(9) Illustrate your answers wherever necessary with the help of neat sketches.

1. (a) Explain the various addressing modes with examples. 7
   (b) Explain 3-address, 2-address, 1-address and zero address instruction formats. Why there is a need of small length instructions ? 6

OR

2. (a) Differentiate between the following : 8
   (i) Multiprocessor and Multicomputer.
   (ii) Big endian assignment and little endian assignment.
   (b) What are different functional units of basic computer system ? 5
3. (a) Write and explain control sequences for Add (R3), R1. 7
   (b) Describe execution of complete instruction using three bus architecture. 6

OR

4. (a) Explain the instruction formats of M 68000 machine. 7
   (b) Explain single bus organization of a data path of a processor with block diagram. 6
5. (a) Discuss horizontal and vertical microinstruction formats indicating their advantages and disadvantages. 7
   (b) Why grouping of control signal is necessary ? Explain in brief. 3
   (c) List out the applications of microprogramming. 4

OR

6.	(a)	Explain Hardwired Control Unit.	7
	(b)	Write a control signal generation for ADD R0, R1 where result is stored in R0. What is the importance of control signal in a CPU to execute an instruction ?	7
7.	(a)	Explain IEEE single and double precision format with suitable example.	7
	(b)	Represent 1/32 and –1/16 in IEEE 754 Single & Double precision format.	7
		OR	
8.	(a)	Perform the 11/3 Integer division using :	8
		(i) Restoring Division Method	
		(ii) Non-Restoring Division Method.	
	(b)	Using Booth's multiplication algorithm solve the following :	6
		(i) – × 7 5	
		(ii) – × – 11 13	
9.	(a)	Define virtual memory. Explain virtual to physical address translation in virtual memory.	7
	(b)	Explain memory interleaving with diagram.	6
		OR	
10.	(a)	Explain various mapping techniques in cache memory.	7
	(b)	Write advantages of Dynamic RAM cell over Static RAM cell.	6
11.	(a)	Define interrupts. Explain in detail different types of interrupts.	7
	(b)	What are tightly and loosely coupled systems ? Explain.	6
		OR	
12.	(a)	Explain working of DMA in detail.	7
	(b)	Write short notes on (any **two**) :	6
		(i) Pipelining	
		(ii) RISC and CISC processor	
		(iii) Array processor.	

PRS/KS/24/2637

Faculty of Science & Technology

Fourth Semester B.Tech. (Information Technology) (C.B.C.S.) Examination

COMPUTER ARCHITECTURE AND ORGANIZATION

Time : Three Hours] [Maximum Marks : 70

INSTRUCTIONS TO CANDIDATES

(1) All questions carry marks as indicated.
(2) Solve Question No. **1 OR** Question No. **2**.
(3) Solve Question No. **3 OR** Question No. **4**.
(4) Solve Question No. **5 OR** Question No. **6**.
(5) Solve Question No. **7 OR** Question No. **8**.
(6) Solve Question No. **9 OR** Question No. **10**.
(7) Assume suitable data wherever necessary.
(8) Diagrams and chemical equations should be given wherever necessary.

1. (A) What is addressing mode ? Explain different addressing mode with example. 7
   (B) Explain Stack and Subrouting with proper example. 7

OR

2. (A) Differentiate between the big–endian assignment and little–endian assignment. 4
   (B) Explain Instruction execution and straight line sequencing. 4
   (C) Explain subroutine linkage and parameter passing methods with suitable example. 6
3. (A) Explain with diagram single and three bus CPU structure. 10
   (B) Explain sequencing of control signals. 4

OR

4. (A) Write down the control steps for execution of following instruction. ADD LOC, R1 (where LOC is memory location). 7
   (B) Explain control sequence for Add (r1), r2 using single Bus organisation. 7
5. (A) Explain grouping of control signals with a suitable example. 7
   (B) Discuss horizontal and vertical microinstruction formats indicating their advantages and disadvantages. 7

OR

6. (A) Why control signals are needed in a CPU to execute an instruction ? Write control signal generation for ADD R0, R1 where result is stored in R0. 8
   (B) Explain in brief :
   Bit Slices
   Emulation. 6
7. (A) Explain how arithmetic operations are performed in floating point numbers. 5
   (B) What is Booth's multiplication ? Provide solution of -13×11 using Booth's method. 5
   (C) Explain IEEE single precision format with suitable example. 4

OR

Model Questions

8. (A) Multiply the following pair of signed 2's complement number using Booths multiplication and bit pair recording technique. 8
A = 010111, B =110110 where
A is multiplicand and B is multiplier.
(B) Solve : 6
(i) 1010 DIV 0101
(ii) 8/3 Integer division
by using Restoring Division and Non-Restoring Division Method.

9. (A) Explain in detail : 8
(i) Semiconductor RAM Memories
(ii) Mapping Techniques.
(B) Define virtual memory. Explain address translation in virtual memory. 6

OR

10. (A) Explain the need of cache memory. 5
(B) Desing 8K X8 bit RAM system using a 1K X4 bits RAM IC's and appropriate decoders. 5
(C) Explain memory interleaving with diagram. 4

B.Tech. (Information Technology) Fourth Semester (C.B.C.S.)

Computer Architecture & Organization

P. Pages : 2 **PSM/KW/23/2637**

Time : Three Hours Max. Marks : 70

Notes : 1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Due credit will be given to neatness and adequate dimensions.
8. Assume suitable data whenever necessary.
9. Illustrate your answers whenever necessary with the help of neat sketches.

1.	a)	What is addressing mode? Explain different addressing mode with example.	**7**
	b)	What are the different functional unit of Basic computer system?	**7**
		OR	
2.	a)	Explain 3-address, 2-address, 1-address & zero address instruction formats with example.	**7**
	b)	Explain instruction execution and straight line sequencing.	**7**
3.	a)	Write down the control steps for execution of following instruction. ADD LOC, R1 (where LOC is memory location)	**7**
	b)	Explain with proper diagram single bus & three bus structure.	**7**
		OR	
4.	a)	Explain the instruction formats of M68000 machine.	**7**
	b)	Describe execution of complete instruction using three bus architecture.	**7**
5.	a)	Differentiate between Hardwired & microprogrammed control unit.	**7**
	b)	Differentiate between horizontal & vertical microinstruction.	**7**
		OR	
6.	a)	Explain Hardwired control unit.	**7**
	b)	Explain microprogrammed control unit in detail.	**7**
7.	a)	Using Booth's multiplication algorithm solve the following.	**8**

i) -7×5 ii) -11×13

	b)	Represent 1/32 and -1/16 in IEEE 754 single precision format.	**6**
		OR	
8.		Perform the 8/3 Integer division using-	**14**
		i) Restoring division method	
		ii) Non-restoring division method	
9.	a)	Design a 8K×8 bits RAM system using a 1K×4 bits RAM IC's & appropriate decoders.	**7**
	b)	Define virtual memory? Explain virtual to physical address translation in virtual memory.	**7**
		OR	
10.	a)	Consider a direct mapped cache with 64 blocks, 64 block size of 16 bytes. To what block number does byte address 1200 maps.	**7**
	b)	Discuss the advantages of dynamic RAM over static RAM cell.	**7**

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B.Tech. Fourth Semester (Information Technology) (C.B.C.S.) Summer 2023

Computer Architecture & Organization

P. Pages : 2 **MSP/KS/23/2597**

Time : Three Hours Max. Marks : 70

Notes : 1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Due credit will be given to neatness and adequate dimensions.

1. a) State and explain various Addressing modes with example. **10**

b) Differentiate between multiprocessor and multi computers. **4**

OR

2. a) Explain Basic operational between the processor and memory. **7**

b) Describe memory location and addresses in terms of Byte Addressability, Big Endian and Little Endian Assignment and word Alignment. **7**

3. a) Illustrate with block diagram single and two bus organisation of datapath of a processor. **8**

b) Explain with one address, two address and three address instruction the following equations **6**

$Z=(A+B-C)*(C-D+E)/(A*B-C)$

OR

4. a) Describe the execution of complete instruction using three bus architecture. **7**

b) Write control steps for execution of complete instruction ADD(R3), R1. **7**

5. a) Discuss various microinstruction format supported by microprogrammed control unit. **6**

b) Write short notes on: **8**
i) Emulation ii) Bit Slices
iii) Macro Processor iv) Microprogramming

OR

6. a) Discuss microprogram control unit for microinstruction with diagram. **7**

b) Write a short note on generation of next address field in microprogram with diagram. **7**

Model Questions

7.	a)	Write a note on Floating point arithmetic operations.	**6**
	b)	Demonstrate the following multiplication using booth's algorithm for signed multiplication 11×-6.	**8**
		OR	
8.	a)	Perform a division $96 \div 06$ using non-restoring method.	**8**
	b)	Write a note on carry look ahead address or fast adders.	**6**
9.	a)	Write a note on Direct memory Access.	**6**
	b)	Explain Virtual Memory. Also write how virtual address is translated to physical address.	**8**
		OR	
10.	a)	List and explain the various mapping techniques used in cache memory.	**10**
	b)	Differentiate between Semiconductor RAM and ROM memories.	**4**

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B.Tech. (Information Technology) Fourth Semester (C.B.C.S.) Winter 2022

Computer Architecture & Organization

P. Pages : 2 **SPM/KW/22/2597**

Time : Three Hours Max. Marks : 70

Notes : 1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Assume suitable data whenever necessary.

1. a) What are different functional units of basic computer system? **7**

b) Discuss in brief about addressing mode. Also explain different addressing modes with example. **7**

OR

2. a) Explain Instruction execution and straight line sequencing. **8**

b) Differentiate between multiprocessor & multi computers. **6**

3. a) Explain the instruction formats of M 68000 machine. **8**

b) Explain the role of stack in subroutine (all implementation) with example. **6**

OR

4. a) Discuss about sequencing of control signals. **7**

b) What considerations we need to take for High Level Language? **7**

5. a) Give the microcontrolled control signals for the following instructions: **8**
i) ADD R_1 (single operand) ii) ADD R_1, R_2 (single operand)
iii) ADD R_1, R_2, R_3 iv) MOV R_2, R_1

b) What is Emulation? Explain in brief. **6**

OR

6. a) Perform the 8/3 Integer division using **7**
i) Restoring Division Method.
ii) Non-Restoring Division Method.

b) Solve 1010 DIV 0101 using non restoring division algorithm. **7**

Model Questions

7.	a)	Differentiate between: i) RAM and ROM ii) RISC and CISC	**7**
	b)	Explain about static RAM and Dynamic RAM.	**7**
		OR	
8.	a)	Define virtual memory? Explain virtual to physical address translation in virtual memory.	**6**
	b)	What are different types of memory mapping techniques? Explain.	**8**
9.	a)	Explain loosely coupled and tightly coupled system with example.	**7**
	b)	Define interrupts. Explain in detail different types of interrupts.	**7**
		OR	
10.		Write short notes on **any three.** i) Pipelining. ii) Array processor. iii) Memory Mapped I/O. iv) Memory Interleaving.	**14**

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