

Operation (NOR based SR latch)		Description
S	R	Q_{next}
0	0	Q_{prev}
0	1	Hold (no change)
1	0	Set \rightarrow stores '1'
1	1	Reset \rightarrow stores '0'
		invalid
		Not allowed (both high)

b) D latch (Data latch)

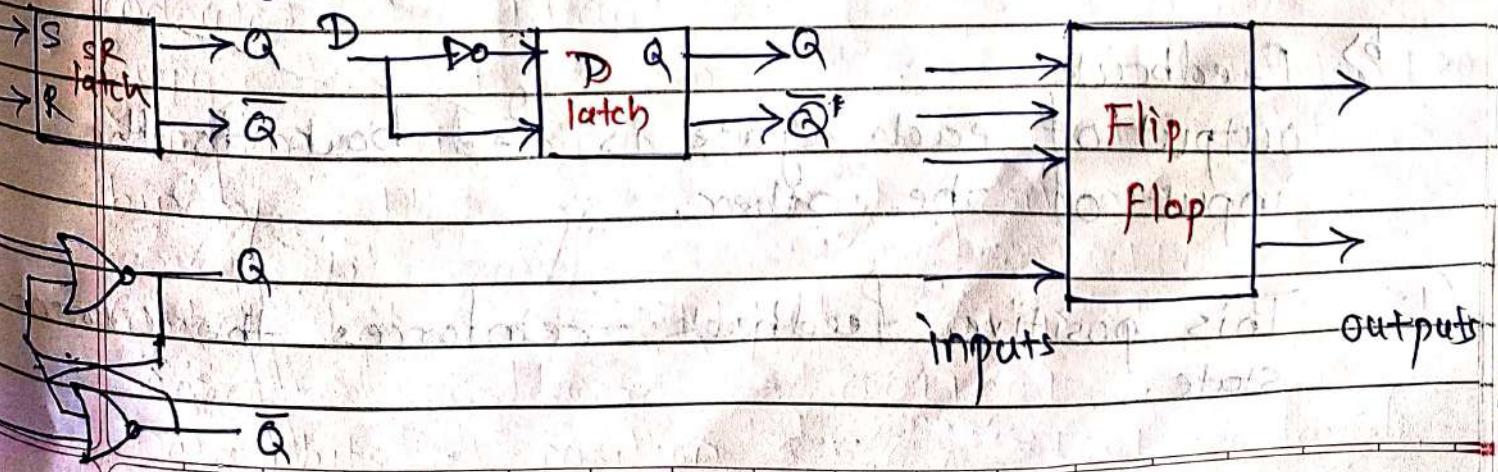
- Modified version of SR latch to avoid invalid state.
- Has D (Data) and Enable (E) inputs.
- Stores the value of D when Enable = 1
- Holds the value when Enable = 0.

Equation

$$Q_{\text{next}} = D \quad \text{when } \text{Enable} = 1$$

c) Flip-Flop (Edge triggered)

- If we want storage synchronized with a clock, we use D Flip-Flop.
- Stores 1 bit value on a clock edge (rising / falling)



Applications:

- Basic storage unit in digital electronics.
- Building block for.
 - Registers
 - RAM cells
 - Counters and FSMs

Circuit Properties of Bistable latch:

A bistable latch is a circuit with two stable states. (hence bi-stable)

It can store one bit of information (0/1).

Built using two cross coupled gates

Forms the basis of memory elements like Flip-flops and registers.

Circuit properties:

a) Bistability

The latch can reset in $Q=1, \bar{Q}=0$ or $Q=0, \bar{Q}=1$. It allows latch to store a bit.

b) Feedback

Output of each gate is fed back to the input of the other.

This positive feedback reinforces the current state.

- c) Memory (State Retention)
because of feedback, the latch remembers its state even when inputs are inactive.
- Only changes states when a valid input (set or reset) is applied.

d) Control inputs -

SR latch \rightarrow inputs are Set(S) and Reset(R)

D latch \rightarrow Data(D) and Enable(E)

The inputs determine when the latch changes states.

e) Complementary output

always provide Q and \bar{Q}

f) Metastability risk under invalid inputs.

(if both inputs are activated simultaneously ($S=R=1$ in nor latch) the circuit may enter a condition where outputs are unpredictable)

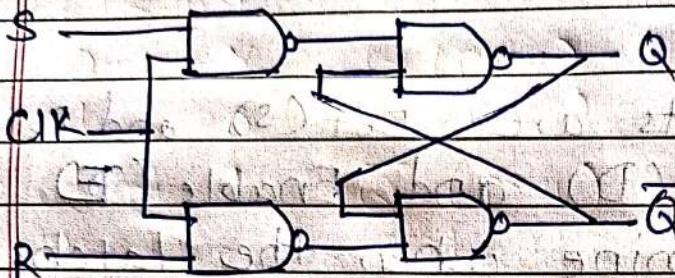
g) Asynchronous operation

Simple bistable latches are level sensitive and work without a clock.

- they change state immediately when input changes

Clocked SR-Flip-Flop

Synchronous SR-FF or gated SR latch is a sequential logic circuit with Set (S) & Reset (R) inputs that changes its output (Q) only when a clock pulse is applied.



S R Q \bar{Q}

0 0 0 0

0 0 1 0

0 1 0 0

0 1 0 0

1 0 1 0

1 0 0 1

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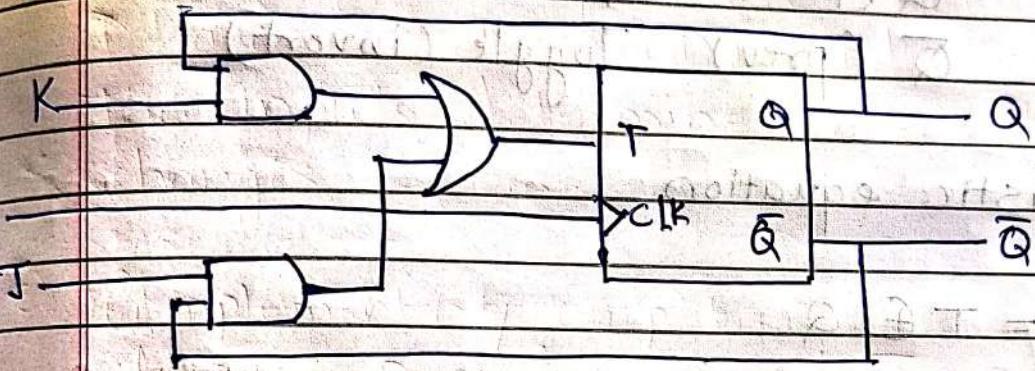
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J-K-T Flip Flop

- An improvement over the SR Flip-Flop
- solves the invalid state problem ($S=R=1$)
- inputs J, K, clock (CLK)

inputs \rightarrow J (set); K (reset), CLK (clock)
 Outputs \rightarrow Q, & \bar{Q}



Truth Table

CLK	J	K	Q(next)	operation
0	X	X	Q(prev)	No change
1	0	0	Q(prev)	Hold
1	0	1	0	Reset
1	1	0	1	Set
			\bar{Q} (prev)	Toggle

When $J=K=1$ output toggles.

Characteristic equation

$$Q(\text{next}) = J\bar{Q} + \bar{K}Q$$

T Flip-Flop \rightarrow

T-Flip Flop

(T - Toggle)

It changes the output on each clock edge and gives an output that is half the frequency of the signal to the input.

CIR : T Q(next) operation

0	X	Q(prev)	No change
---	---	---------	-----------

1	0	Q(prev)	Hold
---	---	---------	------

1	1	\bar{Q} (prev)	Toggle (invert)
---	---	------------------	-----------------

Characteristic equation

$$Q(\text{next}) = T \oplus Q$$

Applications

1) JK FF

Counters (synchronous / asynchronous)

Shift registers

Universal building block

2) T-FF

Counters (binary, ripple, synchronous)

Frequency division (each FF divides Freq. by 2)

D-type Flip-Flop.

Data / Delay Flip-Flop

most commonly used Flip Flop

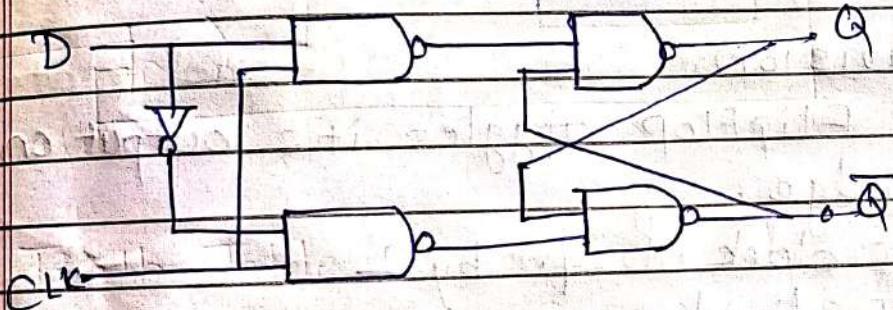
It has only one data input (D) & clock input (CLK)

stores value of D at triggering edge of clock

Eliminates the invalid condition



$$Q(n+1) = D(n)$$



Truth table

D	clk	\bar{Q}
0	1 (Rising edge)	0
1	1 (Falling edge)	1

When clock signal is low, FF holds its current state and ignores input D.

When clock signal is high, the flip-flop samples and stores D input.

If $D=0$ then Q will be 0.

If $D=1$ then Q will be 1.

\bar{Q} is complement of output Q



Applications of Flip-Flop

1) Data storage & Registers.

A single flip-flop stores 1 bit of information. Multiple flip-flops combined form register to store multiple bits.

Used in microprocessor, digital system, memory buffers.

2) Counters

Flip Flops are building blocks of counters.

Used in clocks, timers, event counters etc.

3) Frequency division.

A T or JK flip-flop toggles its output on each clock edge.

This divides clock freq. by 2.

Cascading FF divides by 4, 8, 16 etc.

Used in digital watches, communication systems.

4) Shift register.

Connecting FF in series makes a shift register used for

Serial to parallel conversion

Parallel to serial

Temporary storage.

5) State machines.

Used in CPU, vending machines, traffic light controllers.

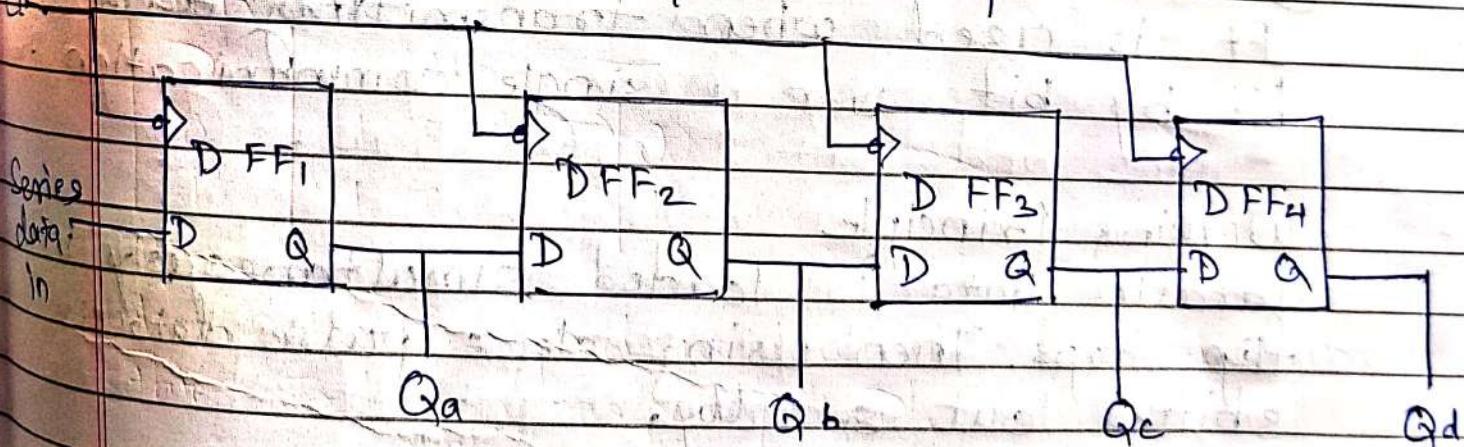
6) Used in debouncing circuits to remove false triggers.

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- 7) FF synchronize data transfer between different clock domains in digital systems.
 - 8) SRAM (Static RAM) built from flip-flop.
FF form basic storage cells of cache memory.
 - 9) Pulse detection
 - 10) Counters in digital electronics lab.

Series to Parallel Converter

It is a digital circuit that converts serial input data into parallel output data.

Series data arrives one bit at a time on single line, and the converter outputs all bits simultaneously on multiple lines.



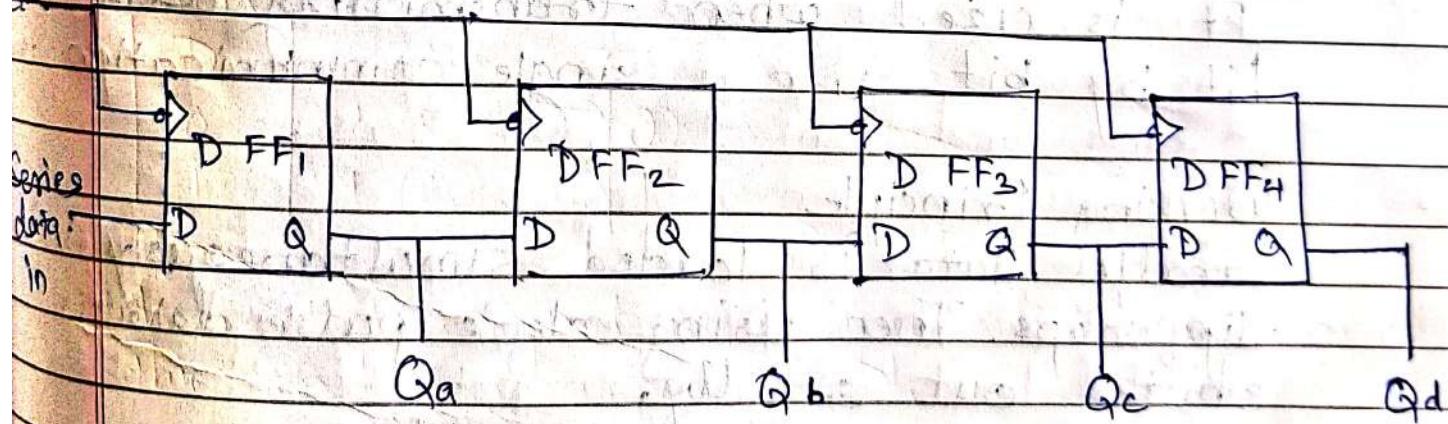
- The circuit uses flip-flop to store incoming bits
- each FF stores one bit.
- Clock signal synchronizes the data transfer from the serial input to the flip-flop.
- Number of flip-flops = number of bits to store.
- Once the full data word has been received, the parallel o/p.

- 7) FF synchronize data transfer between different clock domains in digital systems.
- 8) SRAM (Static RAM) built from flip-flop.
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- each FF stores one bit.
- clock signal synchronizes the data transfer from the serial input to the flip-flop.
- Number of flip-flops = number of bits to store.
- Once the full data word has been received the converter moves to ~ 10 ns monolithically on parallel o/p.

Operation table (4 bit S/P converter)		Serial input	Q ₃	Q ₂	Q ₁	Q ₀
Clock pulse						
1	1	1	0	0	0	1
2	1	0	0	0	1	0
3	1	1	0	1	0	1
4	1	1	1	0	1	1

After 4 clock pulses, all 4 bits are available in parallel.

Parallel to serial Converter

(P/S) converter converts parallel data into serial data.

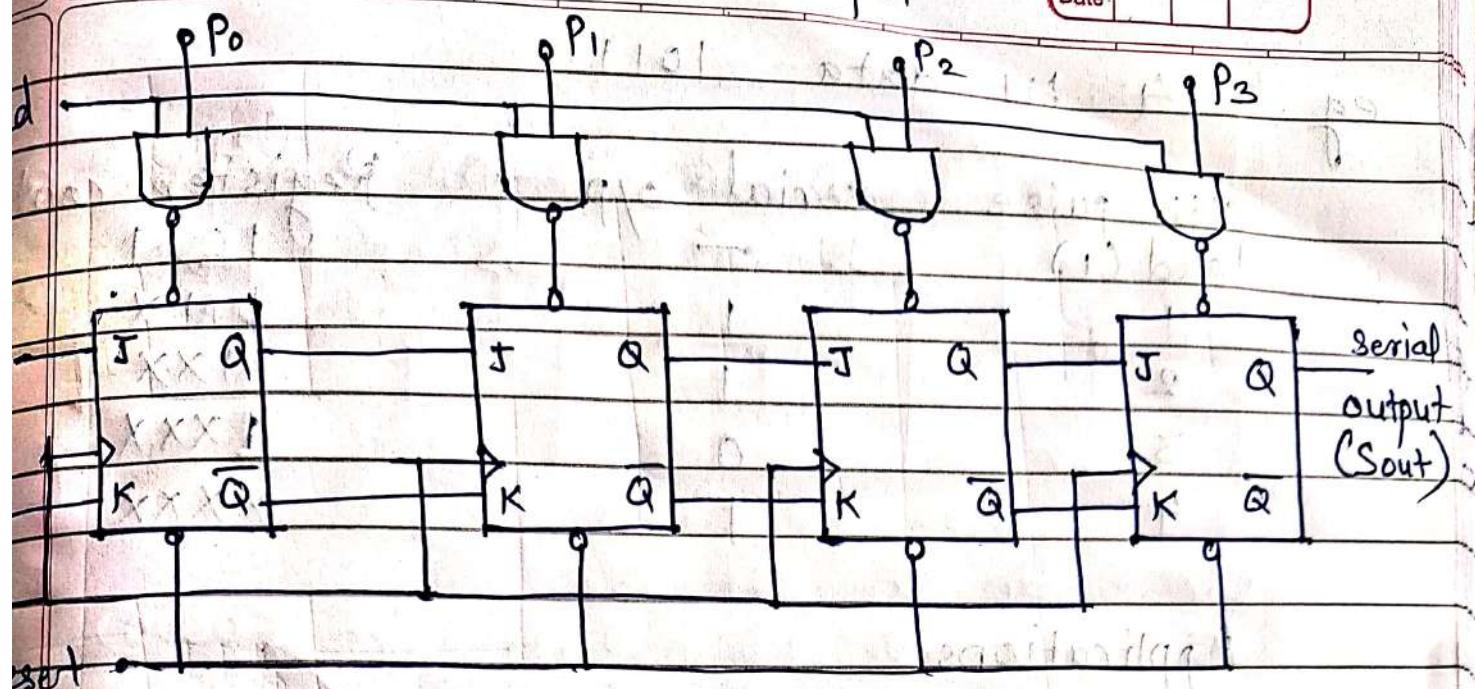
This is opposite of the Serial to parallel converter.

It is used when transmitting data bit by bit over a single communication line.

Working Principle

Parallel data is loaded simultaneously into flip flops. Then using clock pulse data is shifted out serially.

Implemented using a shift register - specifically a parallel in serial-out register



Each flip flop stores one bit, when the load signal is active, all 4 bits are loaded in parallel.

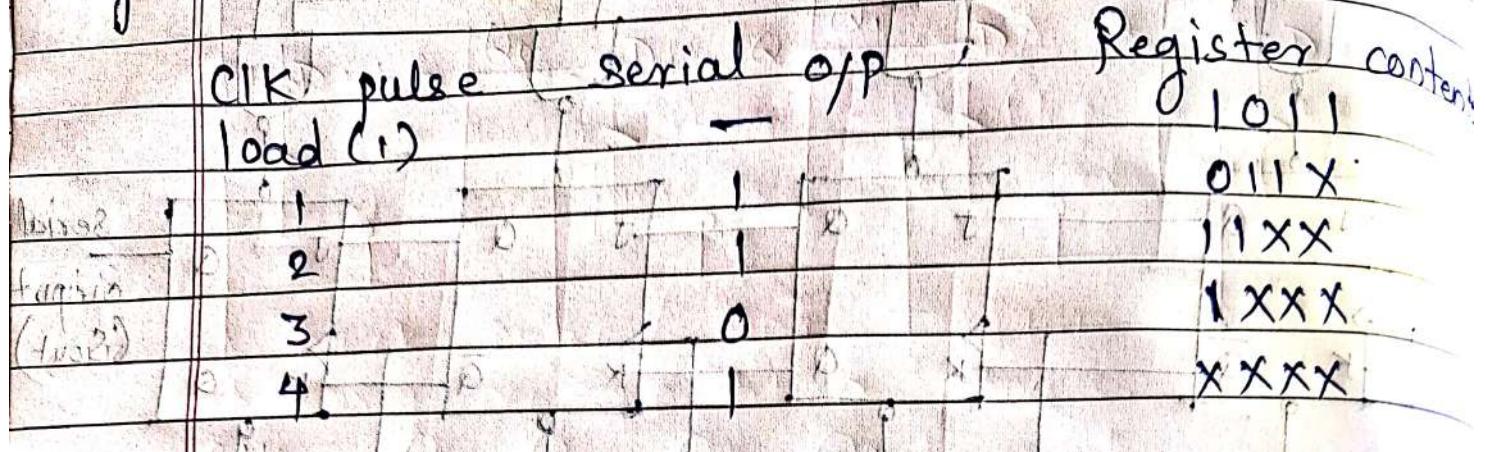
Then for each clock pulse, bit shift right outputting one bit at a time from 1st flip flop.

Mode of control

Control	operation	Description
Load 1	Parallel load	Loads D ₃ -D ₀ into FF

Load 0 : Shift mode shift data right, output bits serially on each clock pulse.

eg. 994 bit data 1011



Applications

- 1) Data transmission
 - 2) Microprocessor & Microcontroller
 - 3) Digital Communication system.

Ring Counter

A ring counter is a special type of shift register used in digital electronics. Commonly employed for sequencing, operating, timing and control applications.

Shift register is made up of flip-flops connected in loop, the output of last flip flop is fed back to the input of the first.

- For n bit ring counter,
 - n flip-flops (usually D or JK type)
 - n possible states (only one flip-flop is High at a time)
 - The output of last FF loops back to first.

Working principle

Initially one flip flop is set to 1 and all others to 0.

e.g. for 4 bit ring counter.

Q_3	Q_2	Q_1	Q_0
0	0	0	1

On each clock pulse, the '1' shifts one position to the left (or right, depending on design)

After 1st pulse \rightarrow 0 0 1 0

After 2nd pulse \rightarrow 0 1 0 0

After 3rd pulse \rightarrow 1 0 0 0

After 4th pulse \rightarrow 0 0 0 1

The sequence repeats continuously, hence the name is 'ring counter'.

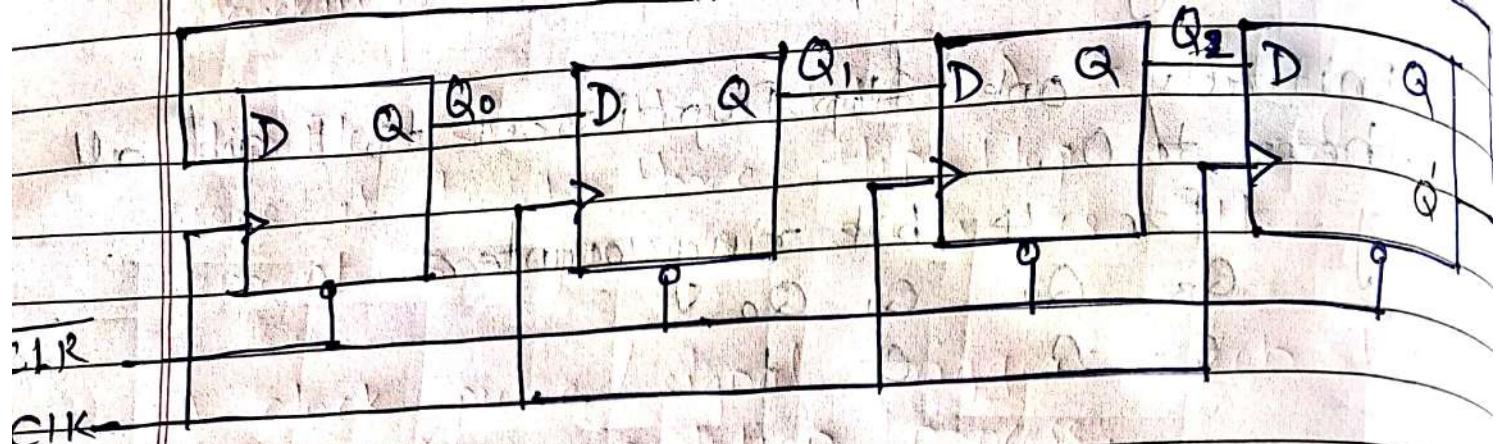
There are two types of ring counters

1) Straight ring counter

2) Twisted ring counter

Applications

- 1) Sequence generation
- 2) Digital timers
- 3) LED chasers and display lights.
- 4) Stepper motor control.



	Q ₀	Q ₁	Q ₂	Q ₃
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	0	1
5	0	1	0	1
6	0	0	1	1
7	0	0	0	1

Sequence states highlighted in circles:

- Row 0: 0000
- Row 2: 0001
- Row 4: 0011
- Row 6: 0111
- Row 7: 1111

Sequence generator

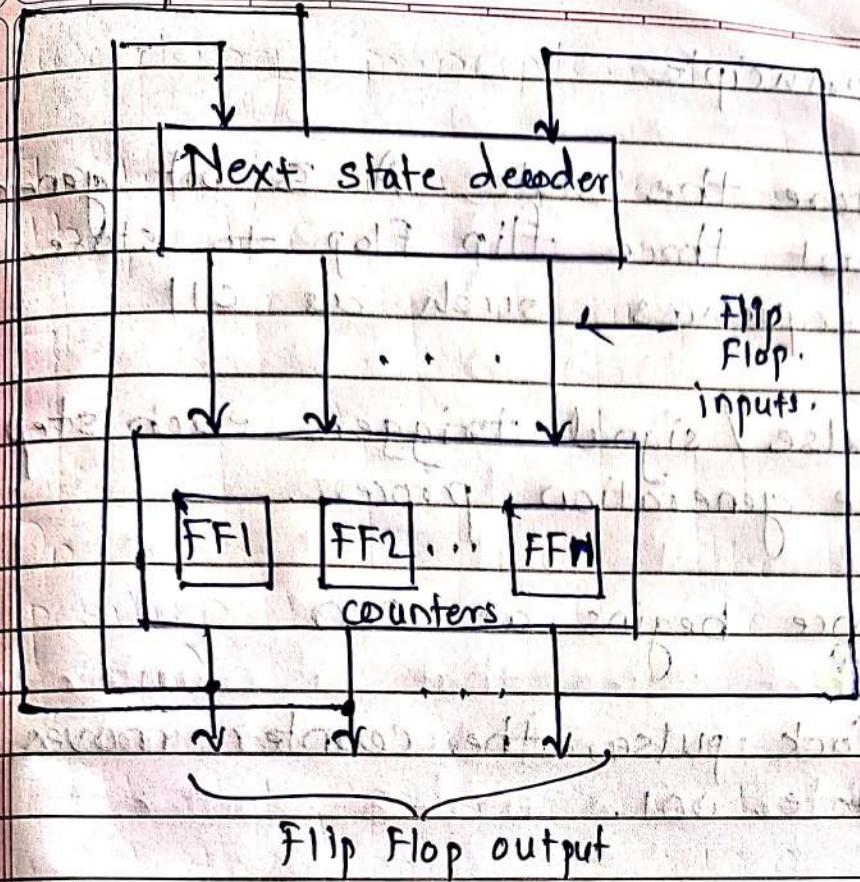
A sequence generator is a circuit designed to produce a specific sequence of digital output signals in a predetermined order.

These sequences are often binary and are used to control the timing, operation, or logic flow of digital systems.

They typically consist of flip-flops, logic gates or sometimes shift registers.

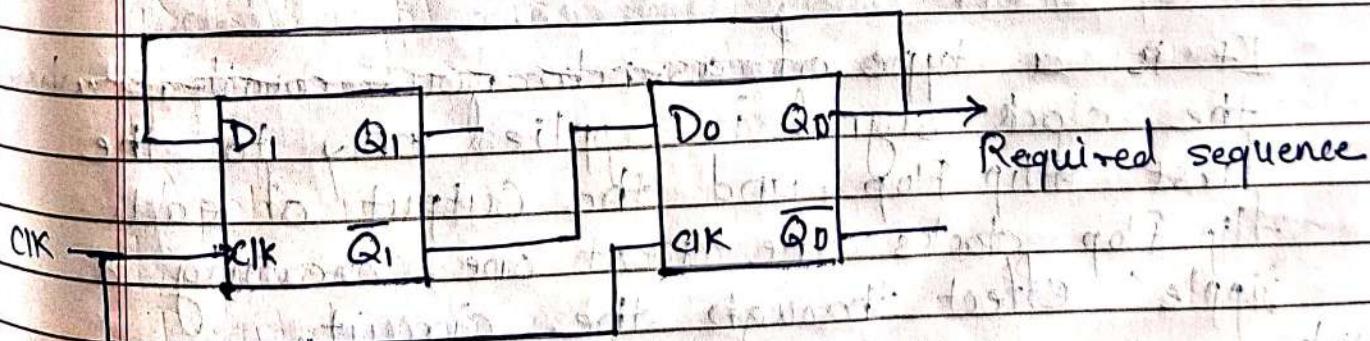
Counter outputs are used as inputs to the

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$$Q_1 \rightarrow Q_0 \text{ (Initial) } Q_0 + D_1 \rightarrow D_0$$

0	0	0	0	1	1	0	0
0	1	1	1	0	1	0	0
1	1	1	0	0	0	0	0
1	0	0	0	0	0	0	0



Boolean expⁿ for D_0 & D_1 can be designed as,

$$\begin{aligned} D_0 &= \overline{Q_1} \overline{Q_0} + \overline{Q_1} Q_0 \\ &= \overline{Q_1} (\overline{Q_0} + Q_0) \\ &= \overline{Q_1} \end{aligned}$$

$$\begin{aligned} D_1 &= \overline{Q_1} Q_0 + Q_1 Q_0 \\ &= Q_0 (\overline{Q_1} + Q_1) \\ &= Q_0 \end{aligned}$$

Working principle

Flip-Flop store the state. A 3 bit generator uses at least three flip flop to store current 3 sequences such as 011.

A clock pulse / signal triggers each step of the sequence generation process.

The sequence begins at 000.

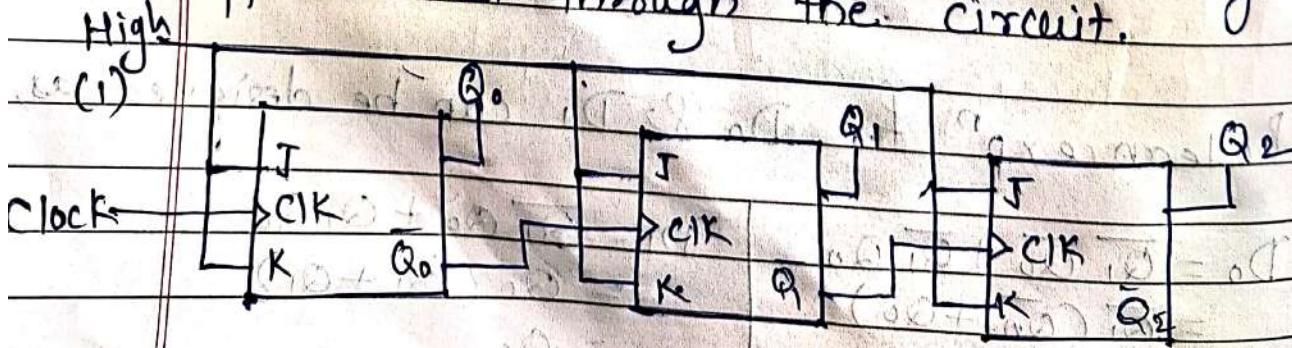
After a clock pulse, the counter moves to the next state, 001.

After the next clock pulse, it moves to 010 and so on. Counter up until it reaches 111.

After 111, the sequence returns to 000 to repeat the cycle.

Ripple Counter

It is a type of asynchronous counter where the clock signal is applied only to the first flip flop, and the output of each flip flop clocks the "next" one, creating a 'ripple' effect through the circuit.



dia: 3 bit ripple counter with JK Flip Flop

A R. counter is a cascaded arrangement of flip flops where the output of one flip-flop drives the clock input of the following F.F.

A n bit ripple counter can count up to 2^n states.

It is known as ripple counter because of the way the clock pulse ripples its way through the flip-flops.

A counter may be an up counter that counts upward or can be a down counter counts downwards or can do both.

When counting up, for the n bit counter the count sequence goes from 000, 001, 010, ..., 110, 111, 000, 001, ... etc.

When counting down the count sequence goes in the manner 111, 110, ..., 010, 001, 000, 111, 110, ... etc.

In the circuit shown in figure, Q₀ (LSB) will toggle for every clock pulse because JK ff. works in toggle mode when both J and K are applied High i/p.

The following counter will toggle when the previous one changes from 1 to 0.

Truth table →

	Q ₂	Q ₁	Q ₀	Counting
0	0	0	0	0, 1, 2, 3, 4, 5, 6, 7
1	0	1	0	8, 9, 10, 11, 12, 13, 14, 15
2	1	0	0	16, 17, 18, 19, 20, 21, 22, 23
3	1	0	1	24, 25, 26, 27, 28, 29, 30, 31
4	1	1	0	32, 33, 34, 35, 36, 37, 38, 39
5	1	1	1	40, 41, 42, 43, 44, 45, 46, 47
6	0	1	1	56, 57, 58, 59, 60, 61, 62, 63
7	1	1	1	64, 65, 66, 67, 68, 69, 70, 71

The number of states that a counter is known as its mod (modulo) number.
 ∴ 3 bit counter is a mod-8 counter.

Advantages

- Can be easily designed by T₁ / D FF.
- Can be used in low speed circuits & divide by N-counters.

Disadvantages

- Extra FF are needed to do desynchronization.
- Propagation delay is large.
- Counting errors may occur due to propagation.

Synchronous counters.

It is a digital counter where all flip-flops are triggered by a single common clock pulse causing them to change state simultaneously.

This eliminates the ripple effect and propagation delays found in asynchronous counters, making it faster and more reliable for high speed applications.

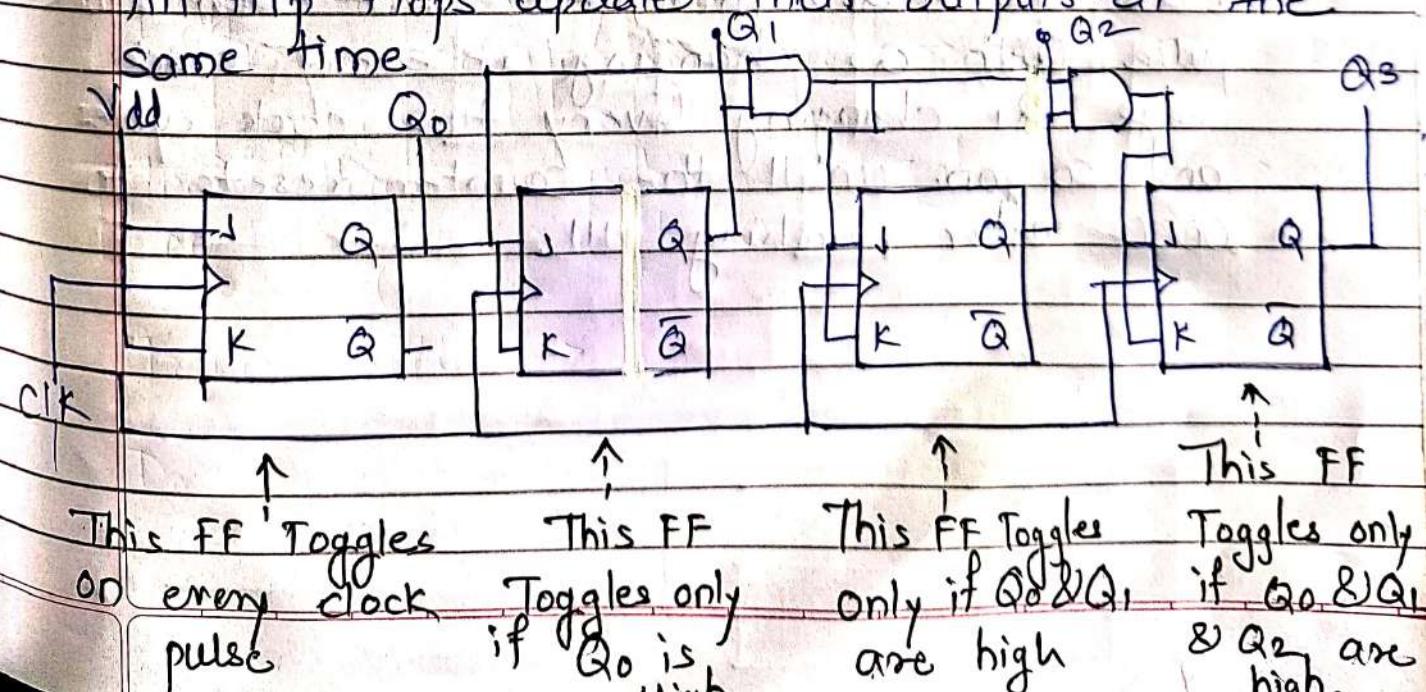
They are used for counting events in a synchronized and reliable manner.

Working

- A single clock signal is fed to all flip flops in the counter.

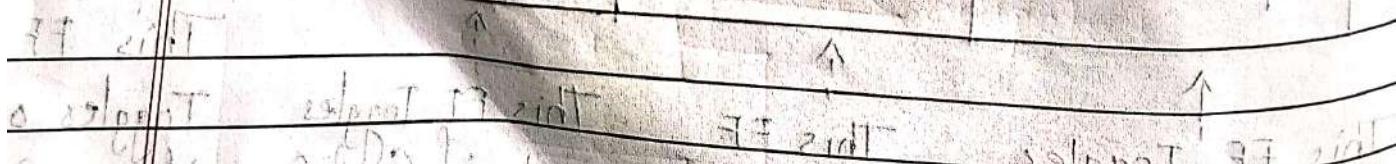
At each clock pulse, the logic gates determine the next state of each flip-flop based on its current state.

All flip flops update their outputs at the same time.



Count	Q_3	Q_2	Q_1	Q_0	Output
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	0	0
3	0	1	1	0	1
4	0	1	1	1	1
5	0	1	0	0	0
6	0	1	0	1	1
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	1	0	1
14	1	1	1	0	0
15	1	1	0	0	0
0	0	0	0	0	0

A 4-bit synchronous up counter \Leftrightarrow has truth table that shows its 16 states, from 0000 to 1111, where output bits (Q_3, Q_2, Q_1, Q_0) increment with each clock pulse, Q_3 with Q_0 changing at every clock edge, Q_1 changing every two clock cycles, and so on until the counter resets to 0000 after reaching 1111.



Counter design using flip-flop

- To design a counter using flip flops, first determine the number of flip-flops needed based on the desired count ($N \leq 2^n$).
 - Then create a state diagram and state table to define the sequence, followed by flip flop excitation table to determine the required inputs for each flip-flop.
 - Finally we k-map to simplify Boolean expression for the flip-flop inputs and draw the logic circuit diagrams based on these expressions.
- * A counter is a device which stores the number of times a particular event or process has occurred, often in relation to a clock signal. Counters are used in digital electronics for counting purpose.

e.g. 2 bit synchronous counter using JK FF.

Practical - Design 2-bit counter with sequence 00, 01, 10, 11, 00 etc.

Two JK flip flops are needed.

i.e. FF1 & FF2 (for Q₁ & Q₀)

Boolean expression

For J₀ - The required i/p is always 1, regardless of the current state.

For K₀ - The required input is always 1 regardless of the current state.

For J_1 : $J_1 = Q_0$ (applies to all states)

For K_1 : $K_1 = Q_0$

State table

Current state Next state Required JK inputs

Q₁, Q₀

Q₁, Q₀

J₁, K₁

00

J₁ = 0, K₁ = 0

J₀ = 1, K₀ = 0

01

J₁ = 1, K₁ = 0

J₀ = 0, K₀ = 1

10

J₁ = 0, K₁ = 1

J₀ = 1, K₀ = 0

High

J₁ = 1, K₁ = 1

J₀ = 0, K₀ = 1

	FF ₀	FF ₁
Q ₁	J ₀	Q ₀
Q ₀	K ₀	J ₁
CIR		

A Special Counter IC's

In digital electronics, counter are sequential circuits used to count pulses and events.

Types of special Counter IC's

1) Binary counters

IC 7493, IC 74LS393

- These count in binary (0, 1, 2, 3...)
- IC 7493 is a 4-bit binary counter.
- Consist of a series of JK FF arranged to count from 0 to 15.

2) Decade counters

IC 7490, IC 4017

- Count from 0 to 9 (10^1 states)
- IC 7490 (BCD Decade counter) produces a binary coded decimal o/p.

IC 4017 (Johnson decade counter) is commonly used in light chasers and sequence generators. It gives 10 decoded o/p, one high at a time.

3) Up / Down counters

IC 74190, IC 74191

- Can count upward or downward based on control i/p.

IC 74191 → synchronous 4 bit UP/DOWN Counter.

4) Programmable counters

IC 8253, IC 8254

These can be preset to start counting from a specific number.

- used for timing and event counting.

5) Ring Johnson counters

J-K counters (TTL 4017) are used in sequence generators.

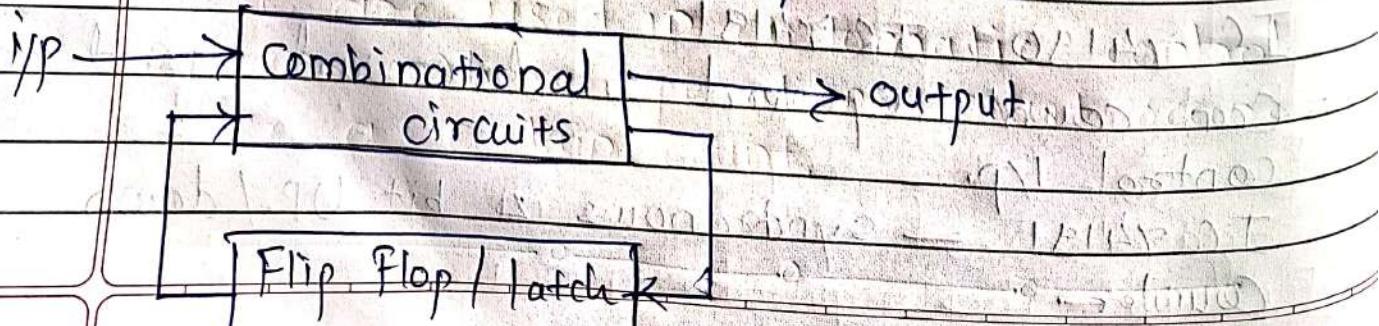
Asynchronous sequential counters

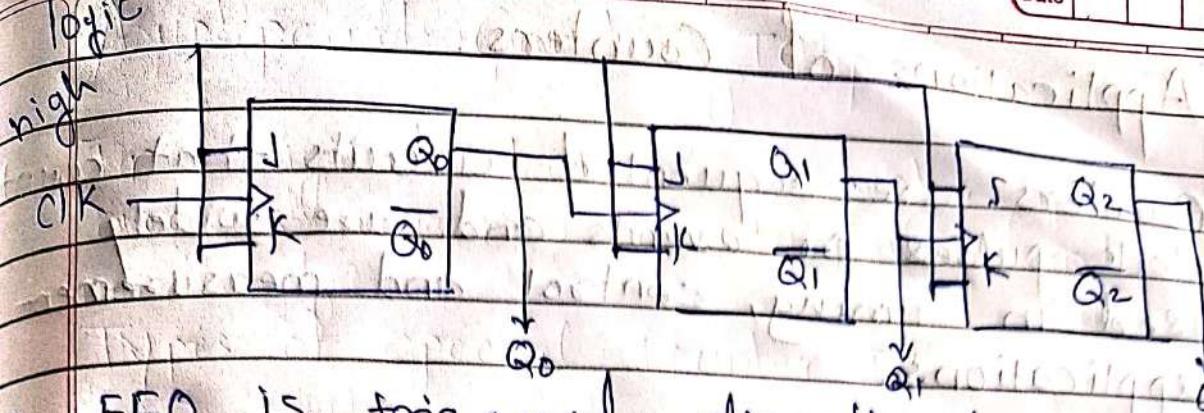
These are general types of logic circuit in which output changes occur immediately when inputs change without waiting for clock signal.

It depends on propagation delay of logic gates rather than clock pulse.

The change of internal state occurs when there is a change in the input variable.

Their memory elements are either un-coded flip-flops or time delay elements.





- FFO is triggered directly by external clock.
 - FFI is triggered by Q0 (O/p of FFO)
 - FF2 is triggered by Q1 (O/p of FFI)
 - The binary counting sequence progresses from 000 to 111.

Truth table

Clock pulse don't Q₂ Q₁, Q₀ Decimal

Widow's orphans often go on the road.

Digitized by srujanika@gmail.com

D. 4 | 0 0 1 w 4
S | 0 1 5

6. Final distribution 0. 2016 6
7. Standardized distribution of Leontine 7

Each flip flop is triggered by the previous one, not by the same clock.

Applications of Counters

Counters are sequential circuits that count clock pulses or events and are widely used in timing, control and measurement applications.

- Counters are often used for frequency division.
- Counters are backbone of digital clock, stopwatches and timers. They count clock pulses generated by crystal oscillator to display seconds, minutes and hours.
- Counters can count external events or objects such as no. of cars entering a parking lot.
- Counter measures frequency by counting the number of pulses received in a fixed time interval.
- Counters are used in digital voltmeter and Analog to digital converter.
- Used in sequence generators and state machines.
- These are used in automatic control systems where operations must occur after a certain count.

Sequential Circuits and Systems

Sequential circuits are digital circuits where output depends on both present input and past history.

- Memory elements → like latches, flip-flops

There are two types of sequential circuits.

Synchronous Asynchronous

- | | |
|-------------------------------------|---|
| - Use clock signal | - Do not use clock signal |
| state changes occur at clock edges. | state changes immediately when input changes. |
| - e.g. counters, shift registers | - Faster but prone to race conditions |

1 bit Memory

A 1 bit memory stores a single binary value 0 or 1.

It is simplest form of memory unit.

Used as a building block for larger memories (Registers, RAM etc.)

- A 1 bit memory cell is typically built using

- a) SR latch (Set-Reset latch)
- Made up of two cross-coupled NOR or NAND gates.

- It has two inputs - Set (S) & Reset (R)
- It has one output Q (and often its complement \bar{Q})