```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
////////
// Company:
// Engineer:
//
// Create Date: 11.04.2025 16:04:35
// Design Name:
// Module Name: Vend_TB
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
////////


module Vend_TB();
reg clk,rst;
reg  [4:0] Item;
reg  EN;
reg pay;
wire [5:0]  Vend;
wire  done;

VendingMachine VD_1(clk,rst,Item,EN,pay,Vend,done);

always begin
    clk = 1; #30;  // High for 30ns
    clk = 0; #30;  // Low for 30ns
end

initial begin

     // Enable the neuron
    rst = 1;  // Apply reset
    #30;
    rst = 0;  // Release reset
    pay=0;

    EN=0;

    Item=5'd6;
    #100;
    #100;

     EN=1;
     #100;
    Item=5'd2;
```

```
    #100;
    #40;

    #200

     pay=1;



   #100;

    pay=0;
    #100;
     EN=0;

     #70;

    Item=5'd6;
//    #70
//     EN=0;
    #100;
     EN=1;
     #100;
    Item=5'd3;
     #200

     pay=1;

        #100;

    pay=0;









end









endmodule
```