USB PD Multi-Fast Charging Protocol Receiver Chip CH224

Manual
Version 1: 2.1

https://wch.cn

1.

Overview

The CH224Q/CH224A is a USB PD fast charging protocol receiver chip supporting USB PD3.2, with maximum power support up to PD3.2 EPR 140W. It supports single-resistor configuration, I/O level configuration, and I2C configuration. The I2C interface enables reading of protocol handshake status and current PD stage rated current. The chip integrates a high-voltage LDO, features low static power consumption, high integration, and minimal peripheral requirements. It incorporates output voltage detection and overvoltage protection, making it suitable for expanding high-power input in various electronic devices such as wireless chargers, small appliances, and lithium-battery power tools.

The CH224K/CH224D/CH221K are USB PD fast charging receiver chips supporting USB PD 3.0, with a maximum power rating of 100W. They support both single-resistor and I/O level configurations.

2. Features

- Supports input voltages from 4V to 30V
- Supports PD3.2 EPR, AVS, PPS, S P R protocols and BC1.2 boost fast charging protocols
- Supports eMarker simulation and automatic VCONN detection
- Supports multiple methods for dynamic adjustment of requested voltage
- Supports 400kHz I^2C communication
- Integrated high-voltage LDO with low static power consumption
- High integration on a single chip, minimal peripherals, low cost
- Built-in overvoltage protection (OVP) module

3. Pin Configuration

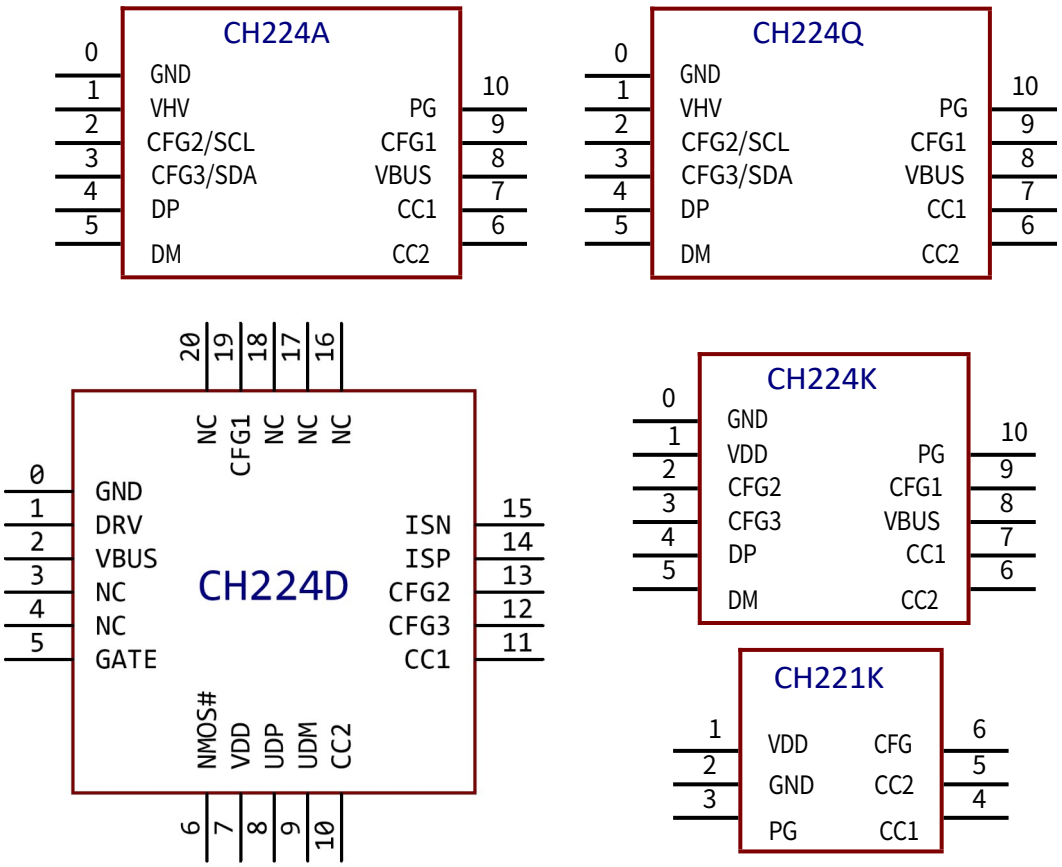


Table 3-1 Package Specifications

Package Type	Plastic Body Dimensions	Pin Pitch		Package Description	Ordering Code
DFN10	2*2mm	0.4mm	15.7 mil	Dual-sided leadless 10-pin	CH224Q
ESSOP10	3.9mm	1.00mm	39.4 mil	Narrow-pitch 10-pin surface mount with base plate	CH224A
ESSOP10	3.9mm	1.00mm	39.4 mil	Narrow-pitch 10-pin surface mount with base plate	CH224K
QFN20	3*3mm	0.40mm	15.7 mil	No leads on four sides, 20 pins	CH224D
SOT23-6	1.6mm	0.95mm	37mil	Small 6-pin surface mount	CH221K

Note: *1.* Pin #1 refers to the bottom plate for *ESSOP10*, *DFN10*, QFN20 packages.

2. For new projects, we recommend using *the* compact and *versatile* CH224Q *and CH224A* which are designed for *PCB* compatibility with *CH224K*.

4. Pin Definitions

Table 4-1 CH224Q, CH224A Pin Definitions

Pin Number		Pin Name	Pin Type[1]	Function Description
CH224Q	CH224A			
0	0	GND	P	Common ground terminal, heat sink base plate.
1	1	VHV	P	Operating power supply input, external 1uF capacitor to ground (note voltage rating)
4	4	DP	I/O	USB bus.
5	5	DM		
7	7	CC1	I/O	Type-C CC signal line.
6	6	CC2		
9	9	CFG1	I	Power Mode Configuration Input Pin 1.
2	2	CFG2/SCL	I,PU	Power mode configuration input pin 2 or I2C clock input pin.
3	3	CFG3/SDA	I/O,PU	Power tap configuration input pin 3 or I2C data bidirectional pin.
8	8	VBUS	I	Voltage detection input, must be shorted to VHV.
10	10	PG	OD	Default Power Good indicator, active low, customizable function.

Table 4-2 CH224K Pin Definitions

Pin Number	Pin Name	Pin Type[1]	Function Description
CH224K			
0	GND	P	Common ground terminal, heat sink base plate.
1	VDD	P	Operating power supply input, externally connected 1uF capacitor to ground, series resistor to VBUS.
4	DP	I/O	USB bus.
5	DM		
7	CC1	I/O	Type-C CC signal cable.
6	CC2		
9	CFG1	I	Power Mode Configuration Input Pin.
2	CFG2	I	
3	CFG3	I	
8	VBUS	I	Voltage detection input; requires a series resistor to the external VBUS input.
10	PG	OD	Default Power Good indicator, active low, customizable function.

Table 4-3 CH224D Pin Definitions

Pin Number	Pin Name	Pin Type[1]	Function Description
CH224D			
0	GND	P	Common ground terminal, heat sink base plate.
2	VBUS	P	Operating power supply input. It is recommended to connect an external 0.1uF or 1uF capacitor to ground.
7	VDD	P	Internal regulator output terminal. Connect an external 1uF capacitor to ground.
8	DP	I/O	USB bus.
9	DM		
11	CC1	I/O	Type-C CC signal cable.
10	CC2		
19	CFG1	I	Power Level Configuration Input Pin.
13	CFG2	I	
12	CFG3	I	
1	DRV	O	Low-drive output for driving configuration resistors.
14	ISP	I	Differential input for detecting operating current and custom functions.
15	ISN		

5	GATE	O,HV	NMOS, custom function.
6	NMOS#	I	Drives NMOS enable, active low; should be shorted to GND.

Table 4-4 CH221K Pin Definitions

Pin Number CH221K	Pin Name	Pin Type(1)	Function Description
1	VDD	P	Operating power supply input. Connect an external 1uF capacitor to ground and a resistor in series to VBUS.
2	GND	P	Common ground terminal.
4	CC1	I/O	Type-C CC signal line.
5	CC2		
3	PG	I,OD	Default Power Good indicator, active low, customizable function.
6	CFG	OD	Power mode configuration input pin.

Note *1*: Pin type abbreviations explained: *I* = Signal *I n p u t* = ; *O*= ; *P* = : Power supply or ground; *OD* = : Open-drain output; *HV*= : High-voltage pin; *PD* = : Built-in pull-down resistor; *PU* = : Built-in pull-up resistor.

5. Functional Description

5.1 Overview

The CH224Q/CH224A is a protocol-aware power receiver chip supporting PD3.2 EPR, AVS, PPS, S P R protocol handshakes, BC1.2, and other boost fast-charging protocols. It handles voltage requests within the 5–30V range and dynamically configures voltage levels via single-resistor configuration, I/O level configuration, or I2C configuration. The CH224Q features a smaller form factor, making it suitable for applications requiring higher integration density.

The CH224A is pin-compatible with the CH224K. In most cases, it can be replaced by swapping peripheral components without modifying the PCB. Refer to Chapter 7 for details.

5.2 CH224Q/CH224A Voltage Range Configuration ( )

5.2.1 Single Resistor Configuration

Suitable for applications where different requested voltages are achieved by modifying resistor values on the same PCB.

CFG1 is connected to GND via a resistor, with different resistor values corresponding to different voltage request levels. When using the single-resistor configuration, the CFG2 and CFG3 pins can be left floating. The resistor-to-request-voltage mapping is as follows:

Table 5-1 Resistance and Request Voltage Reference Guide

Resistor Value Configuration	Request Voltage
6.8K Ω	9V
24K Ω	12V
56K Ω	15V
120K Ω	20V
210K Ω	28V

5.2.2 I/O Level Configuration

Applicable for scenarios where the MCU dynamically adjusts the request voltage or the PCB traces are fixed at a specific request voltage.

Table 5-2 I/O Level and Request Voltage Reference Guide

CFG1	CFG2	CFG3	Request Voltage
0	0	0	9V
0	0	1	12V
0	1	1	20V
0	1	0	28V
1	X	X	5V

"X" in the table indicates not applicable.

"0" in the table indicates a low level; externally, it should be shorted to GND.

"1" in the table indicates a high level. CFG2 and CFG3 have built-in pull-up resistors and support 3.3V or 5V level inputs. They can be driven using push-pull or open-drain outputs. To set CFG1 to a high level, depending on the application scenario, there are three methods:

(1) Pull up to the VHV pin via a 100K Ω resistor (when no control of CH224 is required)

(2) Connect a 2KΩ resistor in series to the MCU's GPIO and output a high level using push-pull mode (when controlling CH224 with 5V levels)

(3) Directly connect to the MCU's GPIO and output a high level using push-pull mode (when controlling CH224 with a 3.3V level)

5.2.3 I2C Configuration

When configured as a single resistor, the chip automatically enables I2C configuration functionality. At this point, voltage requests can be controlled or relevant information read via I2C communication.

The seven-bit I2C address for the CH224Q/CH224A is 0x22 or 0x23 (excluding the read/write bit).

Table 5-3 Chip Function Register Table

Address	Name	Function
0x09	I2C Status Register	Retrieve current protocol status
0x0A	Voltage Control Register	Switch Request Voltage
0x50	Current Data Register	Retrieve Maximum Available Current for Current Gear
0x51	AVS Voltage Configuration Register (High 8 Bits)	Configure upper 8 bits of AVS request voltage
0x52	AVS Voltage Configuration Register (Lower 8 Bits)	Configure the lower 8 bits of the AVS request voltage
0x53	PPS Voltage Configuration Register	Configure PPS request voltage

0x09: I2C Status Register

Bit	7	6	5	4	3	2	1	0
Name	Retain	Retain	Retain	EPR Activation	PD Activation	QC3 Activation	QC 2 Activation	BC Activation
Default	0	0	0	0	0	0	0	0
Read/Write	Read-only							

information

T0, 1, 2, 3, 4 are set to 1, it indicates successful handshake for the corresponding protocol. 0x0A: Voltage Control Register

Bit	7	6	5	4	3	2	1	0
Name	Request Voltage Value, Reference Details							
Default	0x00							
Read/Write	Write Only							

Voltage Detailed

0: 5V 1: 9V 2: 12V 3: 15V 4: 20V 5: 28V

6: PPS Mode 7: AVS Mode

Explanation: 0x50: Current

Bit	7	6	5	4	3	2	1	0
Name	Maximum Current Reference Value (Unit: 50mA)							
Default Value	0xXX							
Read/Write	Read-only							

Indicates the maximum current value available at the current PD power level. This register is only active when negotiating the PD protocol. 0x51, 0x52: AVS Voltage Configuration Register High 8 Bits, AVS Voltage Configuration Register Low 8 Bits

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Enable	AVS Request Voltage Value (Unit: 100mV)														
Default	0x0000															
Read/Write	Write Only															

Voltage Configuration Register Bits 0–7 represent the lower 8 bits of the requested voltage, bits 8–14 represent the upper 7 bits, and the most significant bit is the enable bit.

During configuration, first write the lower 8 bits, then write the upper 7 bits and enable bit (set to 1) together. When requesting AVS for the first time, configure the voltage first, then set the voltage control register to AVS mode. Subsequent voltage adjustments can be made directly by modifying the AVS voltage configuration register.

0x53: PPS Voltage Configuration Register

Bit	7	6	5	4	3	2	1	0
Name	PPS Set Voltage (Unit: 100mV)							
Default	0x00							
Read/Write	Write Only							

t requesting PPS, configure the voltage first, then set the voltage control register to PPS mode. Subsequent voltage adjustments can be made directly by modifying the PPS voltage configuration register.

configuration register.

0x60~0x8F: PD

Default Value	0x00
Read/Write	Read-only

adapter's power supply capacity is less than 100W, reading this area provides complete power SRCCAP data. When the chip is in E P R mode (28V), reading this area provides complete EPR_SRCCAP data.

5.3 Simulated eMarker Functionality

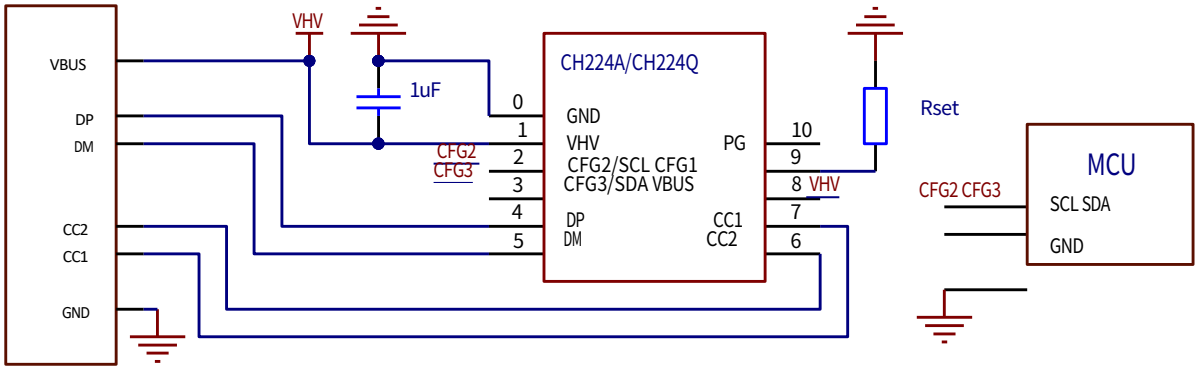
To utilize the simulated eMarker functionality, requests for outputs exceeding 20V or 60W require the use of a Type-C male connector with a 1KΩ resistor connected between the CC2 pin and GND (contact our technical support for

6. Reference Schematic

6.1 CH224Q/CH224A Reference Schematic

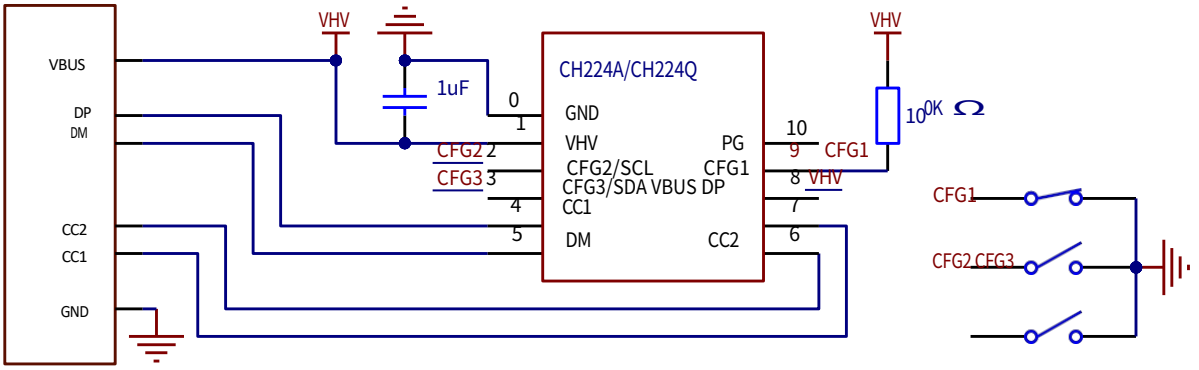
6.1.1 Single-Resistor Configuration and I2C Configuration Reference Schematic (Rset resistance values correspond to requested voltage as per Table 5-1)

Single-resistor configuration is achieved by connecting a specific value configuration resistor to GND via the CFG1 pin. In this case, CFG2 and CFG3 can be used for I2C configuration. If I2C configuration is not used, CFG2 and CFG3 can be left floating.

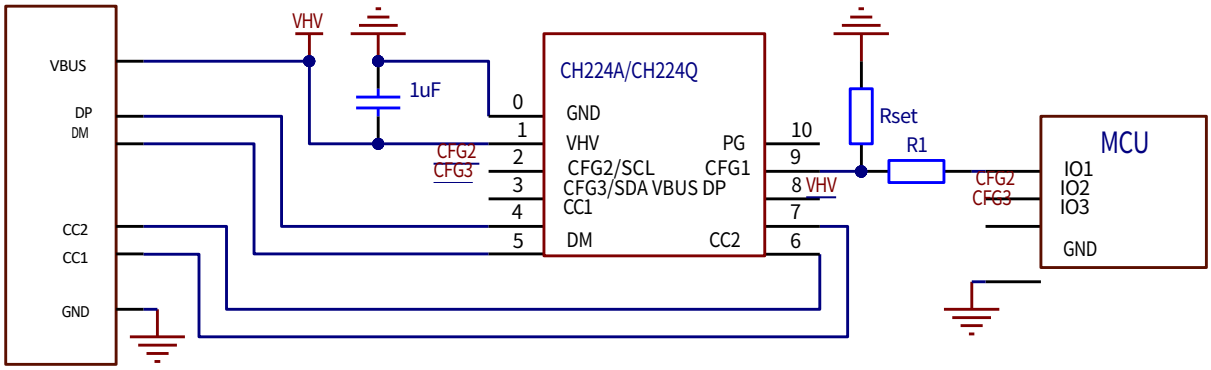


6.1.2 I/O Level Configuration Reference Schematic (I/O Level Corresponding to Request Voltage Reference Table 5-2)

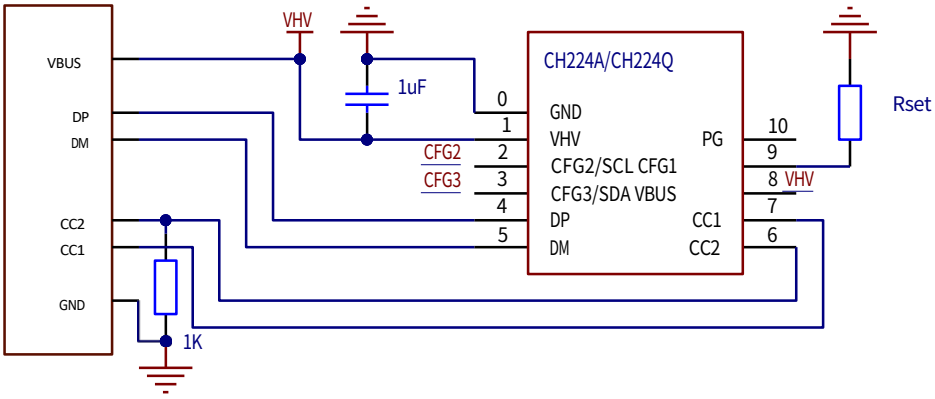
When the electrical system does not need to interact with or control the CH224, CFG1 can be pulled high level by connecting a 100K Ω resistor in series to the VHV pin (see the figure below for I/O level configuration 20V)



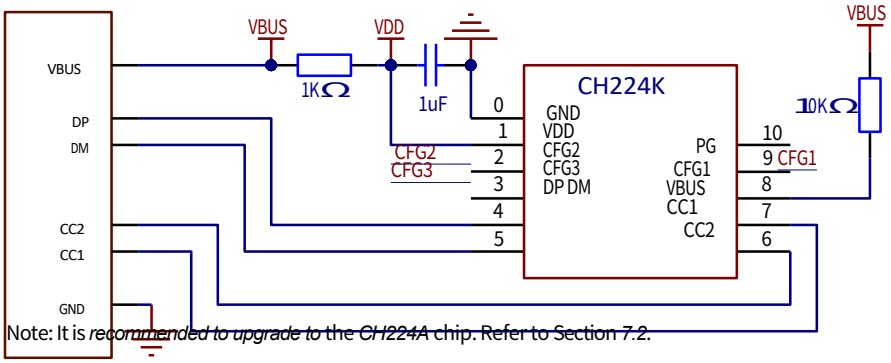
When the power system provides 3.3V or 5V power and requires control of CH224, CFG1 can be connected to the GPIO of the system's MCU (as shown below) If the system's high level is 3.3V, R1 should be 0 Ω; if the system's high level is 5V, R1 should be 2K Ω.



6.1.3 Using the Type-C Male Port eMarker Simulation Function



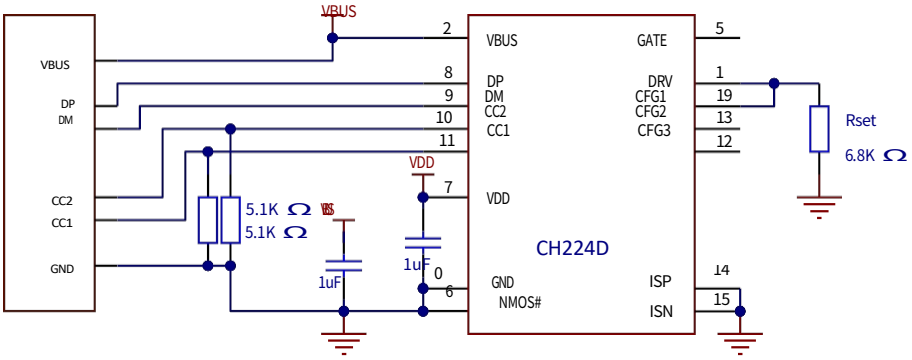
6.2 CH224K Reference Schematic (I/O Level Configuration 20V shown)



CFG1	CFG2	CFG3	Request Voltage
1	X	X	5V
0	0	0	9V
0	0	1	12V
0	1	1	15V
0	1	0	20V

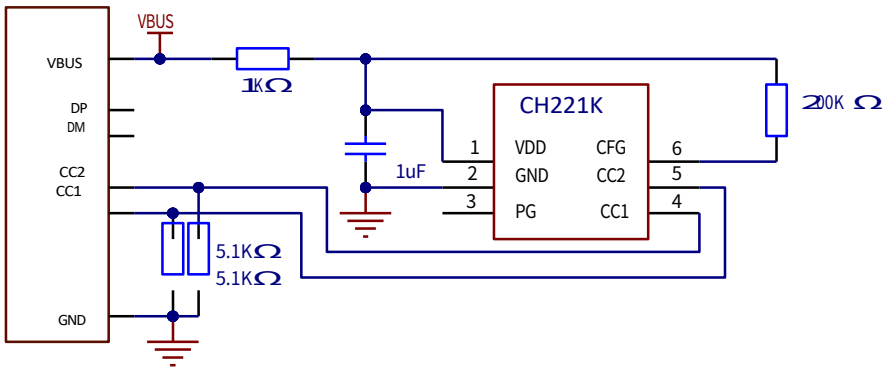
Note: It is *recommended to upgrade to* the *CH224A* chip. Refer to Section 7.2.

6.3 CH224D Reference Schematic (showing single resistor configuration for 9V)



Rset Resistance Value	Request voltage
6.8K Ω	9V
24K Ω	12V
56K Ω	15V
NC	20V

6.4 CH221K Reference Schematic (Single Resistor Configuration 20V Shown)



Rset Resistance	Request voltage
10KΩ	5V
20KΩ	9V
47KΩ	12V
100KΩ	15V
200KΩ	20V

7. CH224A Replacement Guide for CH224K

The CH224A is pin-compatible with the CH224K. In most cases, replacement can be achieved by swapping peripheral components without modifying the PCB. Below are the differences between the chips and common replacement examples.

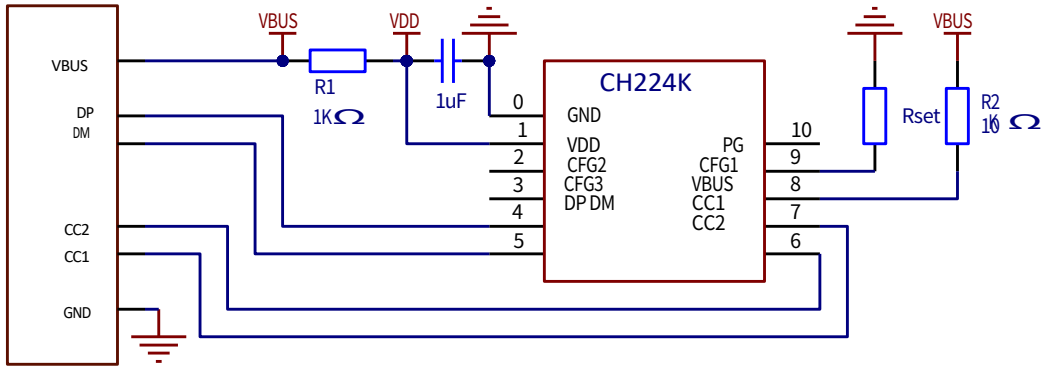
7.1 Differences Between CH224A and CH224K

- Pin 1 of CH224A is VHV (32V), while Pin 1 of CH224K is VDD (3.6V).
- CH224A's CFG2 and CFG3 pins include internal pull-up resistors, while CH224K's CFG2 and CFG3 pins do not have internal pull-up resistors.
- The CFG1 voltage rating for CH224A is 3.8V, while that for CH224K is 8V.
- The VBUS voltage rating for CH224A is 32V, while that for CH224K is 13.5V

7.2 Common Replacement Examples

7.2.1 Original CH224K uses single-resistor configuration mode (Rset resistor reserved, CFG2 and CFG3 pins left floating or shorted to GND)

Figure 7-1 Original CH224K Single Resistor Configuration Schematic

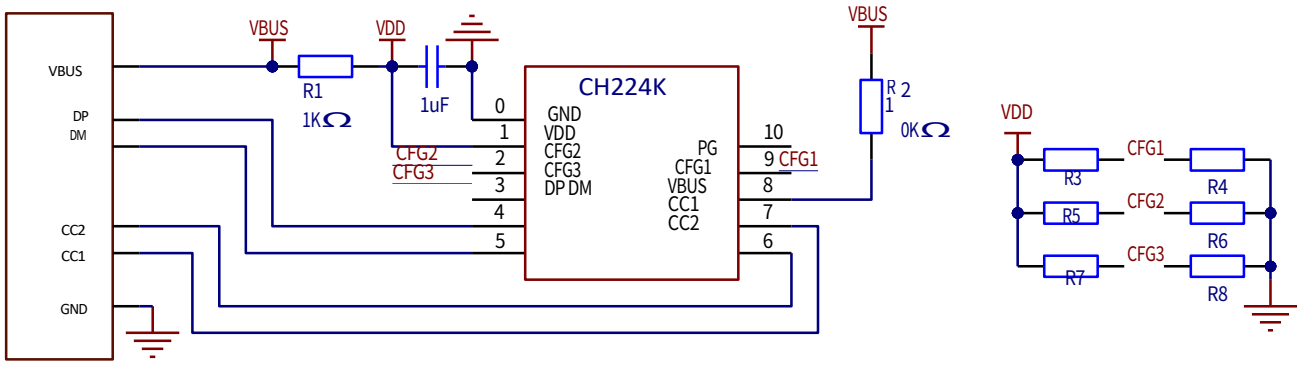


The following modifications are required:

1. Shorten R1 or replace it with a 0Ω resistor;
2. Shorten R2 or replace it with a 0Ω resistor;
3. Change Rset to the configuration resistor for CH224A.

7.2.2 The original CH224K uses an I/O level configuration mode (CFG1, CFG2, CFG3 reserved configuration pads or resistors)

Figure 7-2 Original CH224 I/O Level Configuration Schematic



Note: *In the diagram above, R3/R4, R5/R6,* and *R7/R8 (*) are reserved resistors or pads.

The following modifications are required:

1. Shorten R1 or replace it with a 0Ω resistor;
2. Short R2 or replace it with a 0Ω resistor;

3. Replace the original R3 with a 100K Ω resistor; do not solder R5 or R7 (CH224A's CFG2 and CFG3 have internal pull-up resistors)
4. Short R4, R6, and R8 based on the I/O level configuration mode selected for the CH224A.

7.3 Additional Notes

- The resistor values or corresponding I/O level voltages used for single-resistor configuration and I/O level configuration differ between CH224A and CH224K.

8. Parameters

8.1 Absolute Maximum Ratings

8.1.1 CH224Q/A Absolute Maximum Ratings (Critical or exceeding absolute maximum ratings may cause chip malfunction or damage)

Name	Parameter Description	Minimum Value	Maximum	Unit
TA	Operating Ambient Temperature	-40	105	℃
TS	Storage Ambient Temperature	-55	125	℃
VHV	Operating power supply voltage	-0.5	32.0	V
VIOHV	Voltage on pins supporting high voltage (PG, VBUS)	-0.5	32.0	V
VIOCC	Voltage on CC1 and CC2 pins	-0.5	32.0	V
VIOUX	Voltage on DP, DM, CFG1 pins	-0.5	3.8	V
VIOFT	Voltage on CFG2 and CFG3 pins	-0.5	6.5	V
PD	Maximum power dissipation for the entire chip (VHV voltage × current)		300	mW

8.1.2 CH221K Absolute Maximum Ratings (Critical or exceeding absolute maximum ratings may cause abnormal operation or damage to the

Name	Parameter Description	Minimum	Maximum value	Unit
TA	Operating Ambient Temperature	-40	105	℃
TS	Storage ambient temperature	-55	125	℃
VDD	Operating supply voltage (VDD pin connected to power supply, GND pin connected to ground)	-0.5	5.8	V
VODHV	Voltage on the high-voltage open-drain output pin PG	-0.5	13.5	V
VIOCC	Voltage at CC1 and CC2 pins	-0.5	8	V
VIOUX	Voltage on the C F G pin	-0.5	VDD+0.5	V
PD	Maximum power consumption of the entire chip (VDD voltage × current)		250	mW

8.1.3 CH224K Absolute Maximum Ratings (Critical or exceeding absolute maximum ratings may cause abnormal operation or damage to the

Name	Parameter Description	Minimum	Maximum	Unit
TA	Operating ambient temperature	-40	90	℃
TS	Storage ambient temperature	-55	125	℃
VDD	Operating supply voltage (VDD pin connected to power supply, GND pin connected to ground)	3.0	3.6	V
VODHV	Voltage on the VBUS pin	-0.5	13.5	V
VIOCC	Voltage on CC1, CC2, and C F G 1 pins	-0.5	8	V
VIOUX	Voltage on DP, DM, CFG2, CFG3, and	-0.5	VDD+0.5	V
PD	Maximum power consumption of the entire chip (VDD voltage × current)		400	mW

8.1.4 CH224D Absolute Maximum Ratings (Critical or exceeding absolute maximum ratings may cause abnormal operation or damage to the

Name	Parameter Description	Minimum	Maximum	Unit
TA	Operating Ambient Temperature	-40	100	℃
TS	Storage Ambient Temperature	-55	125	℃
VDD	Operating supply voltage (VDD pin connected to power supply, GND pin connected to ground)	-0.5	6	V
VODHV	Voltage on the VBUS pin	-0.5	24	V
VIOCC	Voltage on CC1 and CC2 pins	-0.5	20	V
VIOUX	Voltage on DP, DM, CFG1, CFG2, CFG3, DRV, NMOS#, ISP, ISN pins Voltage on pin	-0.5	VDD+0.5	V
VIOHX	Voltage on the GATE pin	-0.5	VIOHV+6.5	V
PD	Maximum power consumption of the entire chip (VDD voltage × current)		300	mW

8.2 Electrical Parameters

8.2.1 CH224Q/A Electrical Parameters (Test Conditions: TA = 25℃)

Name	Parameter Description	Minimum Value	Typical Value	Maximum	Unit
VHV	High-voltage power supply voltage VHV	3.3	5.0	30	V
ICC	Operating Power Supply Current		1.8	12	mA
VILI2C	I2C Low Level Effective Voltage	0		0.8	V
VIHI2C	I2C High Level Active Voltage	1.5		3.3	V
RPUFB	Pull-up resistor for CFG2 and CFG3 pins	7	10	15	KΩ
VVHVX	VHV Power Supply Overvoltage Reset OVR Protection Voltage	32	33	34	V
VR	Power-on reset voltage threshold	2.2	2.4	2.65	V

8.2.2 CH221K Electrical Parameters (Test Conditions: TA = 25℃)

Name	Parameter Description	Minimum Value	Typical Value	Maximum	Unit
VLDOK	Internal Power Supply Regulator VDD Parallel Voltage Regulation	3.0	3.3	3.6	V
ILDO	Internal Power Supply Regulator VDD Parallel Absorption Current Capacity	0		30	mA
VR	Power-on reset voltage threshold	2.2	2.4	2.6	V

8.2.3 CH224K Electrical Parameters (Test Conditions: TA = 25℃)

Name	Parameter Description	Minimum	Typical Value	Maximum	Unit
VLDOK	Internal Power Supply Regulator VDD Parallel Voltage Regulation	3.24	3.3	3.36	V
ILDO	Internal Power Supply Regulator VDD Parallel Absorption Current Capacity	0		30	mA
TOTA	Reference threshold temperature for over-temperature protection module OTA	90	105	120	°C
VR	Power-on reset voltage threshold	2.2	2.4	2.6	V

8.2.4 CH224D Electrical Parameters (Test Conditions: TA = 25℃)

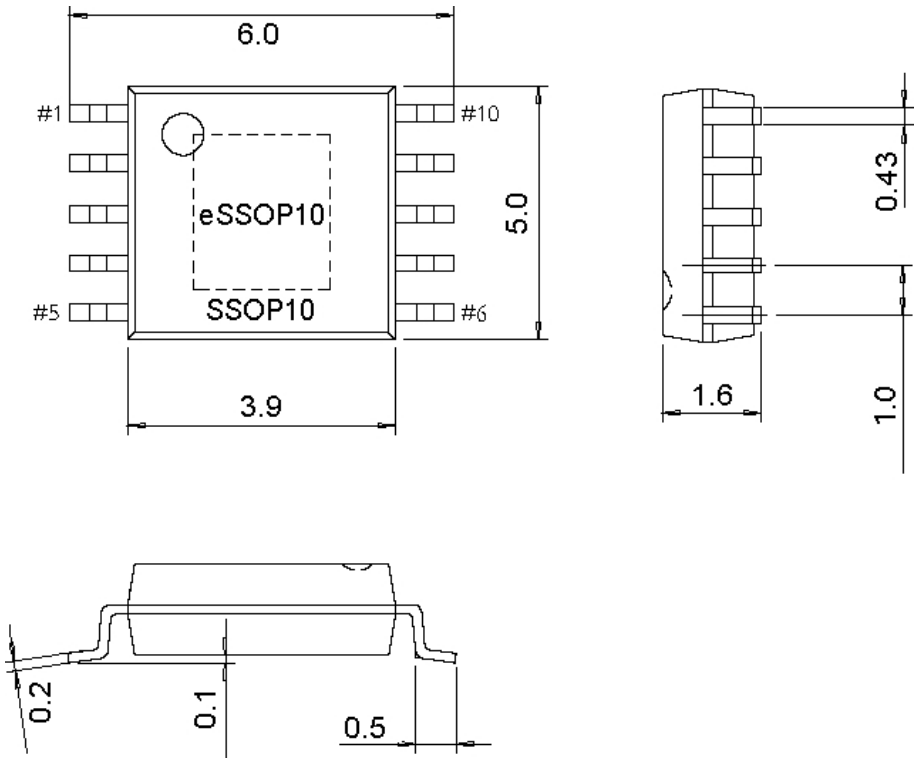
Name	Parameter Description	Minimum	Typical Value	Maximum	Unit
VLDOK	Internal Power Supply Regulator VDD Output Voltage	4.6	4.7	4.8	V
ILDO	Internal Power Supply Regulator VDD External Load Capacity			10	mA
VR	Power-on reset voltage threshold	2.2	2.4	2.6	V

9. Package Information

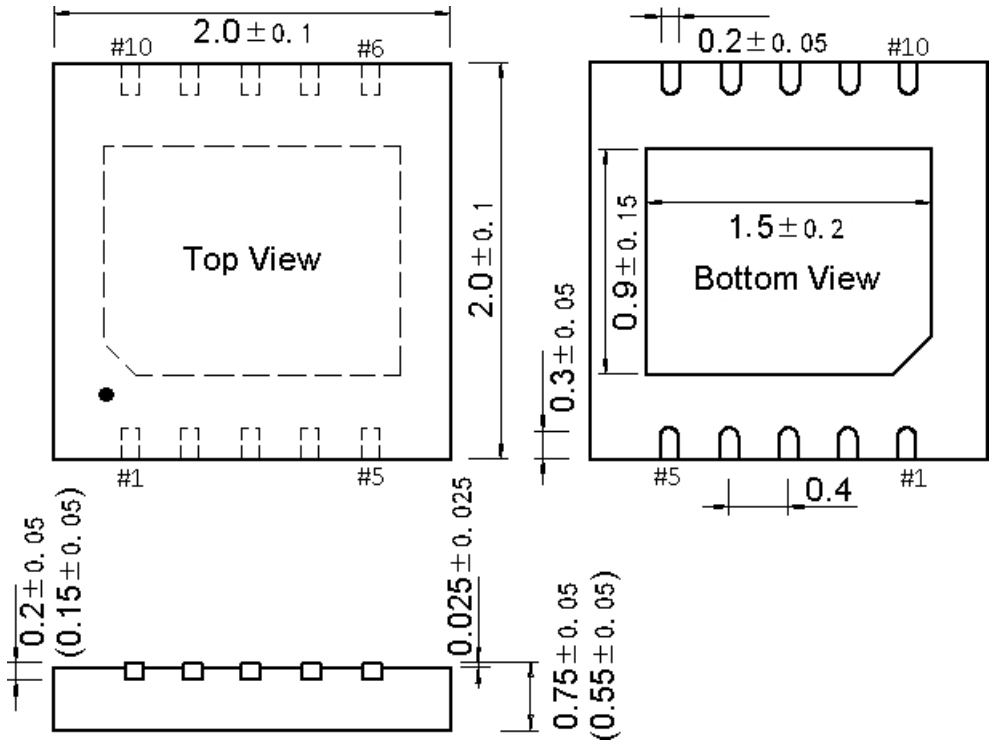
Note: Dimensions are specified in millimeters ( )

Pin center spacing is nominal with no tolerance; all other dimensional tolerances are no greater than ±0.2 mm.

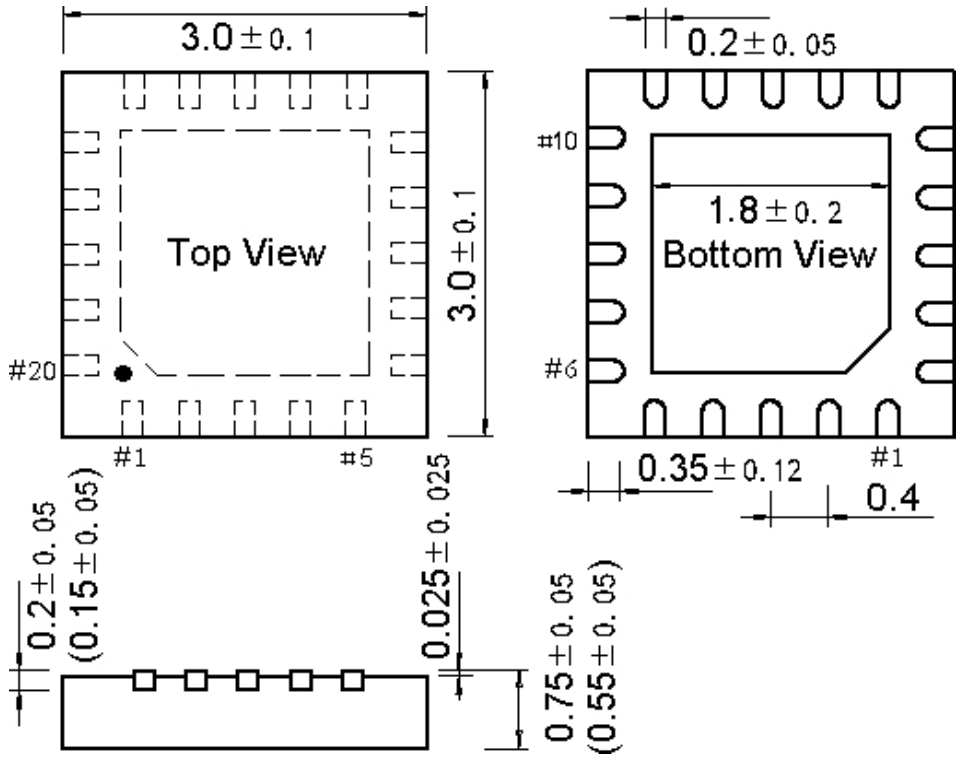
9.1 ESSOP10



9.2 DFN10



9.3 QFN20



9.4 SOT23-6