Matrix Semiconductor, Inc.

OTP MATRIX® 3-D MEMORY - 32PIN TSOP

16MB, 32MB, 64MB

DATA SHEET

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1.0 REVISION HISTORY

REVISION	HISTORY	REV. DATE	REMARK
1.0	Production Release	7/30/04	Prior Rev. history may be accessed through archived files.
1.1	Updated Release	5/11/05	Removed 48TSOP, Updated Part Numbers, Removed Bad Page Specification
1.11	Updated Release	6/24/05	Inserted Matrix trademarks; corrected numbering & spacing; omitted 48TSOP reference from 8.0.

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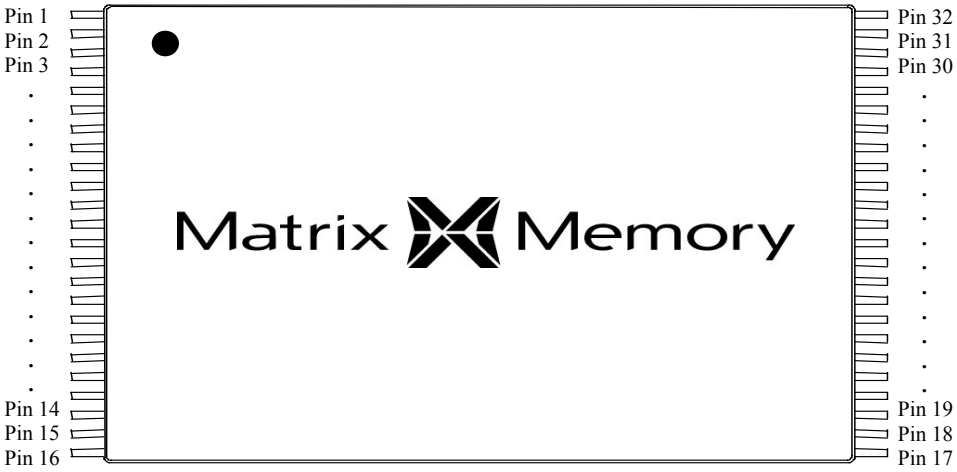
2.1 PIN PLACEMENT



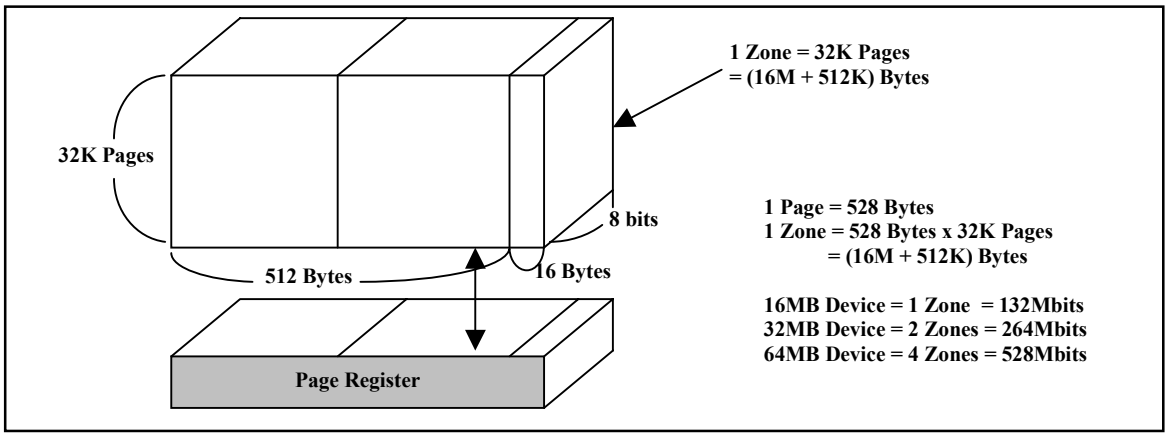
2.2 MATRIX® 3-D MEMORY (3DM) PIN MAP

PIN		PIN		PIN		PIN	
1	NC	9	GND	17	NC	25	GND
2	NC	10	NC	18	NC	26	V_{DD}
3	R/B#	11	NC	19	NC	27	IO_5
4	NC	12	CLE	20	IO_1	28	IO_6
5	RE#	13	ALE	21	IO_2	29	IO_7
6	CE#	14	WE#	22	IO_3	30	IO_8
7	NC	15	WP#	23	IO_4	31	ID3DM
8	V_{DD}	16	NC	24	NC	32	NC

2.3 DETAILED PIN DESCRIPTION

PIN NAME	PIN FUNCTION	DETAILED PIN DESCRIPTION
IO_1 - IO_8	Data Input/Outputs	Handles the input and output of addresses, commands, and data.
CE#	Chip Enable	Acts as the device selection signal. When set to 'H' in the read state, the standby mode is assumed. In the Busy state during the execution of write operations (R/B# = L), both 'H' and 'L' are accepted. (Standby will not be assumed when 'H')
CLE	Command Latch Enable	Enables commands to be sent to the internal command register of the device. Setting the level to 'H' when the WE# signal falls and rises causes the data on the I/O terminals to be written into the command register
ALE	Address Latch Enable	Controls whether data is sent to the internal address register or the internal data register in the device. By setting the level to 'H' when the WE# signal falls and rises, the data present at the I/O terminals is written into the address register as address data. By setting the level to 'L' when the WE# signal falls and rises, the data present at the I/O terminals is written into the data register as input data
RE#	Read Enable	Enables the output of data serially from the I/O terminals. From the time RE# falls, valid output data will be present at the I/O terminals after tREA, and the internal column address counter advances (+1)
WE#	Write Enable	Used to write data present at the I/O terminals into the device
WP#	Write Protect	Prohibits writing. At 'L', the operation of the internal high voltage generating circuit is reset. Normally, the system is operated with this signal 'H', but if the power supply signals are irregular (ON/OFF, etc.), this signal should be 'L' in order to protect stored data from unexpected operations. In the event that the Vdd voltage is outside the range in which correct operation is assured, it is recommended that the level be set to 'L'
R/B#	Ready/Busy Output	Serves as open drain output that indicates the internal operating conditions of the device. During write and read operations, Busy (R/B# L) is output. Ready is automatically output when the operation is finished
ID3DM	Identify 3DM	Disables the Identify 3DM Protocol when tied to V_{DD}. See the "Identify 3DM Protocol" section of this datasheet for more details.
GND	Ground Input	Ground
V_{DD}	Power Supply	Power Supply Voltage

3.0 ARRAY ORGANIZATION



4.0 OPERATING COMMAND REQUIREMENTS

Command, address and data are all written through I/O's by bringing WE# to low while CE# is low. Data is latched on the rising edge of WE#. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle. The 64Mbyte physical space requires 26 addresses, thereby requiring four cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Write need the same four address cycles following the required command input. Device operations are selected by writing specific commands into the command register. The following table defines the specific commands of the Matrix® 3DM chip.

COMMAND	OP CYCLE	VALID DURING BUSY
Serial Data Input	80 h	N
Read1	00 h	N
Read2	01 h	N
Read3	50 h	N
Reset	FF h	Y
Page Write	10 h	N
Status Read	70 h	Y
ID Read	90 h	N
* ID3DM	90 h	N

**Three consecutive IDREAD cycles to release the part from write protect mode.*

5.0 PROGRAMMING REQUIREMENTS

5.1 PROGRAMMING DATA REQUIREMENTS

ITEM	SIZE	REMARKS
Minimum word size*	64 bits	Data must be octbyte aligned

**Partial pages must be programmed by padding the new input data with data previously in memory to form one complete page*

5.2 PAGE REWRITE SPECIFICATION

SYMBOL	PARAMETER	MIN	MAX
Now	Maximum number of programming commands allowed for each page	-	64

6.0 OPERATION MODES AND COMMAND TABLES

6.1 OPERATING MODES

MODE	CLE	ALE	CE#	WE#	RE#	WP#
Command Input	H	L	L		H	X
Address Input	L	H	L		H	X
Data Input	L	L	L		H	X
Data Output	L	L	L	H		X
While writing	X	X	X	X	X	H
Write Protect	X	X	X	X	X	L

H: V_{IH} L: V_{IL} X = V_{IH} or V_{IL}

6.2 READ MODES

COMMAND	1ST CYCLE	POINTER
Read1	00 h	0 to 255
Read2	01 h	256 to 511
Read3	50 h	512 to 527

6.3 VALID READ OPERATING MODES

MODE	CLE	ALE	CE#	WE#	RE#	$D_1 - D_8$	STATUS
Read Mode	L	L	L	H	L	D_{OUT}	Active
Output Deselect	L	L	L	H	H	Z	Active
Standby	L	L	H	H	X	Z	Standby

6.4 DEVICE CODES

MEMORY SIZE	DEVICE CODE
16MB	73h
32MB	75h
64 MB	76h

6.5 STATUS REGISTER OUTPUTS

PIN	STATUS	"0"	"1"
IO_1	Pass or Fail (only valid if IO_6 = "1")	Pass	Write Failure: Failed repair during Write
IO_2	Reserved	Default	--
IO_3	Reserved	Default	--
IO_4	Reserved	Default	--
IO_5	Reserved	Default	--
IO_6	Reserved	Default	--
IO_7	Ready or Busy	Busy	Ready
IO_8	Write Protect	Protected	Not Protected *

* *Before ID3DM is issued, this location will indicate protected, after ID3DM protocol or if ID3DM pin is pulled high, it will reflect the status of the WP# pin.*

6.6 PERFORMANCE SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYPICAL	MAX
t_{PROG}	Write time	-	400 us*	8 ms**
t_R	Data transfer time	-	200 us	460 us
$t_{RSTread}$	Device reset time (read cycle)	-	2 us	10 us
$t_{RSTwrite}$	Device reset time (write cycle)	-	2 us	10 us

**t_{PROG} typ is defined as 50% 0 data pattern in programming factory at nominal conditions.*

***t_{PROG} max may occur during rare redundancy self-repair operation.*

6.7 AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	MIN	MAX	SYMBOL	PARAMETER	MIN	MAX
t_{CYCLE}	Cycle time	50 ns	--	t_{CEH}	CE# high hold time (last serial read)	100 ns	--
t_{CLS}	CLE setup to WE#	0 ns	--	t_{READ}	RE# access time (ID read)	--	35 ns
t_{CLH}	CLE hold to WE#	10 ns	--	t_{RHZ}	RE# high to output high impedance	--	30 ns
t_{CS}	CE# setup to WE#	0 ns	--	t_{REH}	RE# high hold time	15 ns	--
t_{CH}	CE# hold to WE#	10 ns	--	t_{IR}	Ouput high impedance to RE# low	0 ns	--
t_{WP}	WE# pulse width	25 ns	--	t_{RSTO}	RE# access time (status read)	--	35 ns
t_{ALS}	ALE setup to WE#	0 ns	--	t_{CSTO}	CE# access time (status read)	--	45 ns
t_{ALH}	ALE hold WE#	10 ns	--	t_{WHR}	WE# high to RE# low	30 ns	--
t_{DS}	Data setup to WE#	20 ns	--	t_{WHC}	WE# high to CE# low	30 ns	--
t_{DH}	Data hold to WE#	10 ns	--	t_{AR1}	ALE lot to RE# low (Add. Reg. & ID read)	100 ns	--
t_{WC}	Write cycle time	50 ns	--	t_{CR}	CE# lot to RE# low (Data Reg. & ID read)	100 ns	--
t_{WH}	WE# high hold time	15 ns	--	t_{WB}	WE# high to busy	--	100 ns
t_{RP}	Read pulse width	35 ns	--	t_{AR2}	ALE low to RE# low (read cycle)	50 ns	--
t_{RC}	Read cycle time	50 ns	--	t_{RB}	Last RE# high to busy (sequential read)	--	200 ns
t_{REA}	RE# access time (serial data)	--	35 ns	t_{CRY}	CE# high to ready: $R = (V_{DDmax} - V_{OLmax}) / (I_{OL}+I_L)$	--	2 us
T_{WW}	WP# high to WE# low	100 ns	--	t_{CHZ}	CE# high to output high impedance	--	20 ns
T_{RR}	Ready to RE# low	20 ns	--				

6.8 OPERATING ENVIRONMENT

6.8.1 DC REQUIREMENTS

SYMBOL	PARAMETER	MIN	MAX
V_{DD}	Supply voltage	2.7 V	3.6 V
V_{IH}	Input high voltage	2.2 V	V_{DD} + 0.3 V
V_{IL}	Input low voltage	-0.3 V	0.6 V
V_{OH}	Ouput high voltage (I_{OH} = -400uA)	2.4 V	-
V_{OL}	Output low voltage (I_{OL} = 2.1mA)	-	0.4 V
I_{CC1} *	Read current (typ)	20 mA	
I_{CC2}	Read current (max)	30 mA	
I_{CC3} *	Write current (typ)	40 mA	
I_{CC4}	Write current (max)	80 mA	
I_{CCS}	Standby current	100 uA	
I_{LI}	Input Leakage	±10 uA	
I_{LO}	Ouput Leakage	±10 uA	

** Typical values measured at room temperature and 3.3V.*

6.8.2 ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	MIN	MAX
V_{DD}	Supply Voltage		4.6 V
V_{IH}	Input high voltage	--	V_{DD}+0.3 ≤ 4.6V
V_{IL}	Input low voltage	-0.3 V	--

6.8.3 CAPACITANCE

SYMBOL	PARAMETER	MIN	MAX
C_L	Capacitance due to input or output pin	10 pF	15 pF

6.8.4 STORAGE CONDITION

SYMBOL	PARAMETER	MIN	MAX
Tstore	Storage Temperature Requirements	-25 °C	150 °C
Lshelf*	Shelf Lifetime	>10 Years	

**Shelf lifetime is specified with an average temperature of 25°C ± 10°C*

6.8.5 LIFETIME AND DATA RETENTION

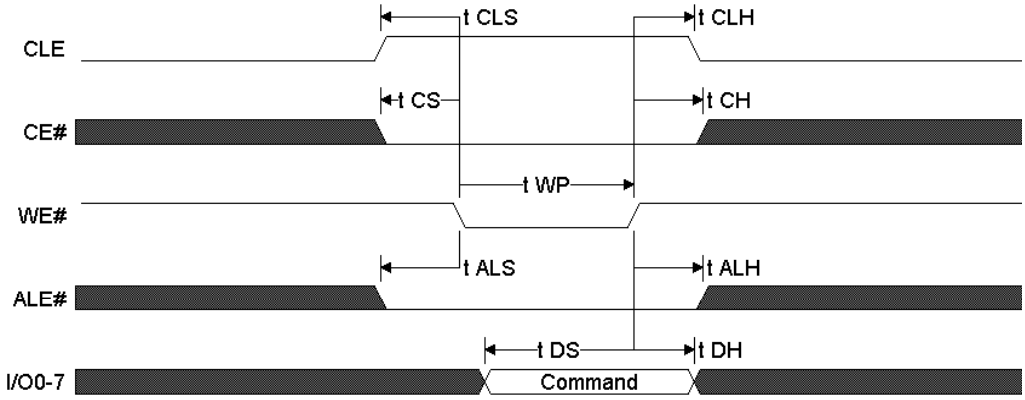
SYMBOL	PARAMETER	MIN	MAX
Ldr	Data Retention Lifetime	10 Years	-

6.8.6 OPERATING TEMPERATURE

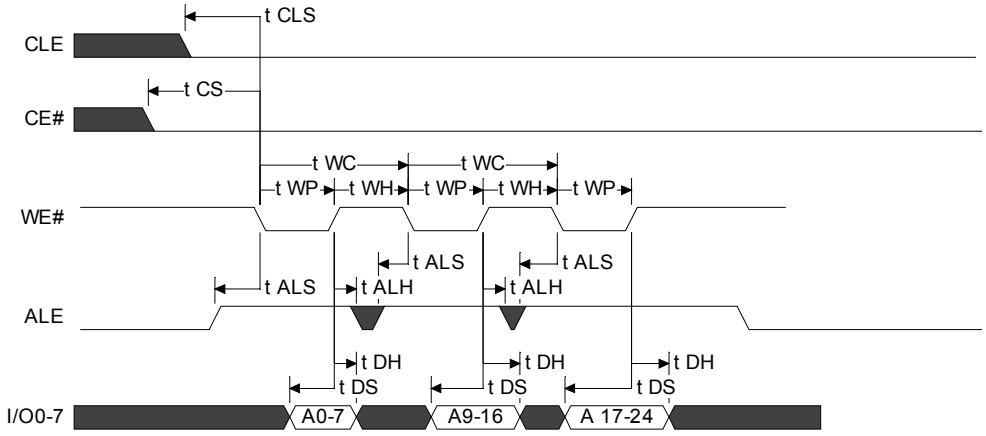
SYMBOL	PARAMETER	MIN	MAX
Toper	Operational Temperature Requirements	0 °C	70 °C

7.0 TIMING SPECIFICATION

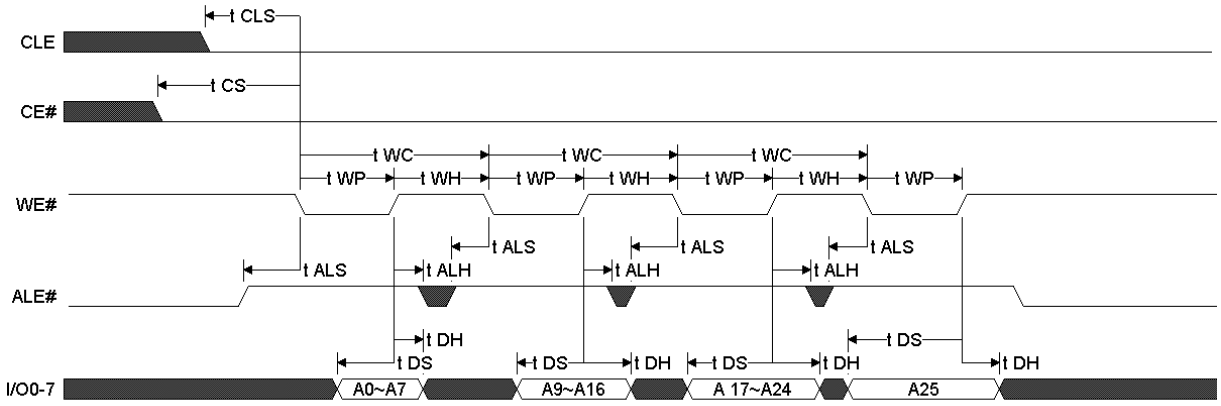
7.1 COMMAND LATCH CYCLE



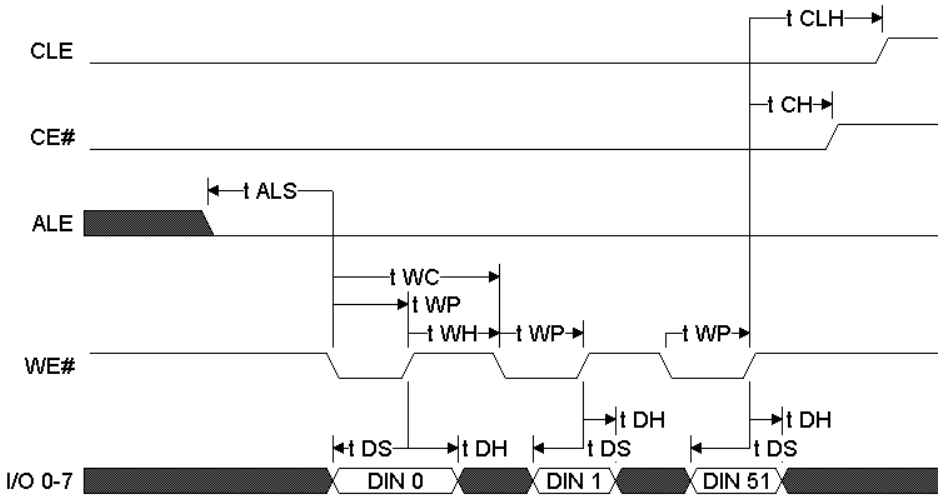
7.2 ADDRESS LATCH CYCLE
(Address Cycle for 128Mb and 256Mb)



(Address Cycle for 512Mb)

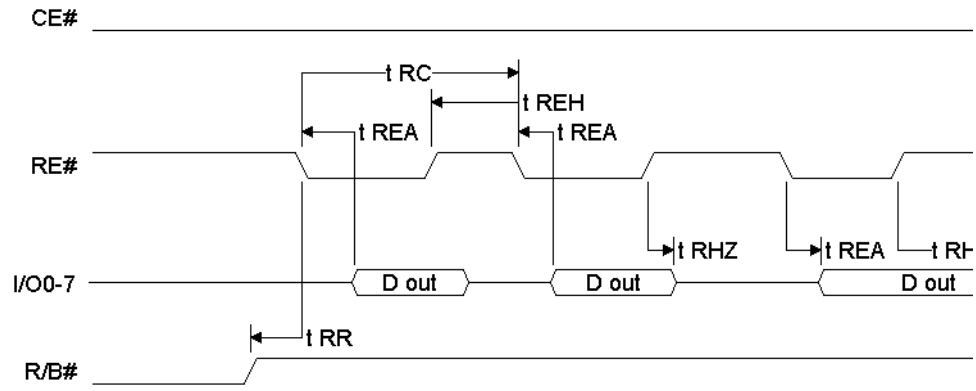


7.3 INPUT DATA LATCH CYCLE

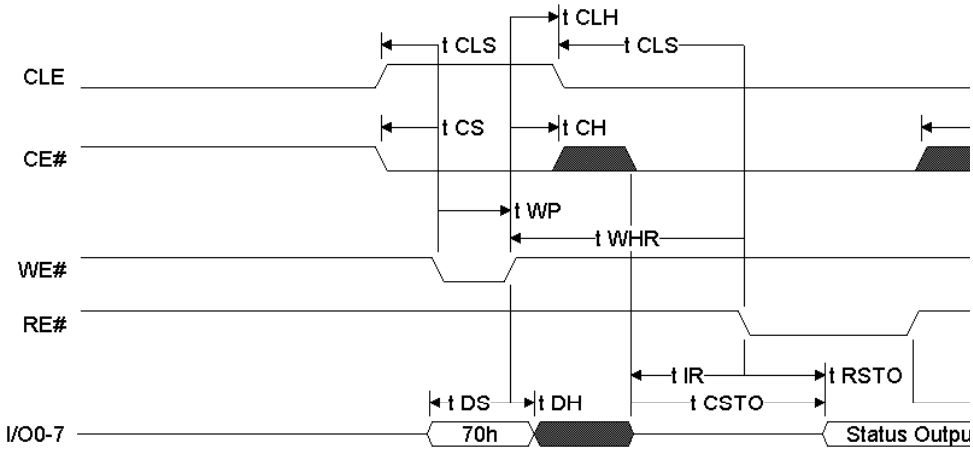


7.4 SEQUENTIAL OUT CYCLE AFTER READ

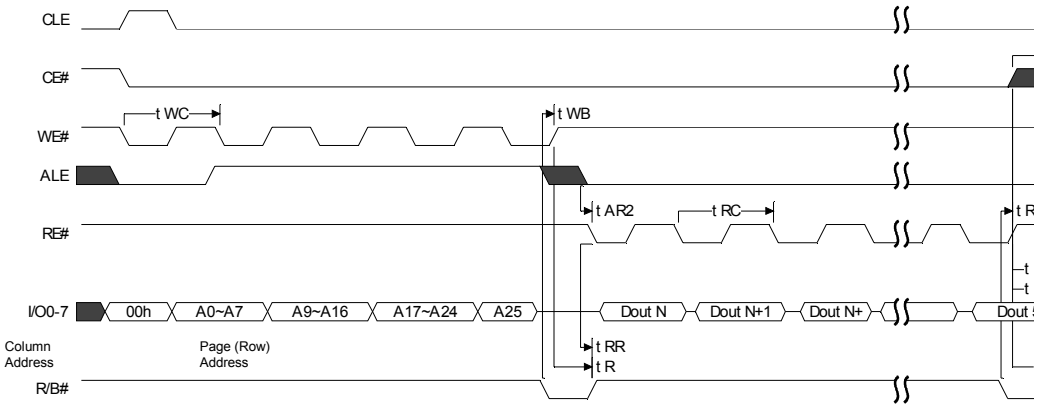
(CLE = L, WE# = H, ALE = H)



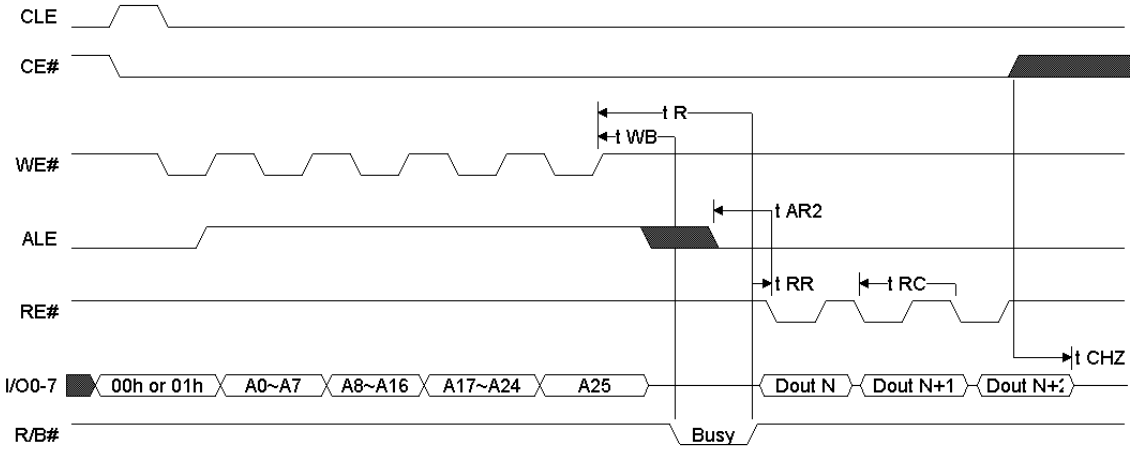
7.5 STATUS READ CYCLE



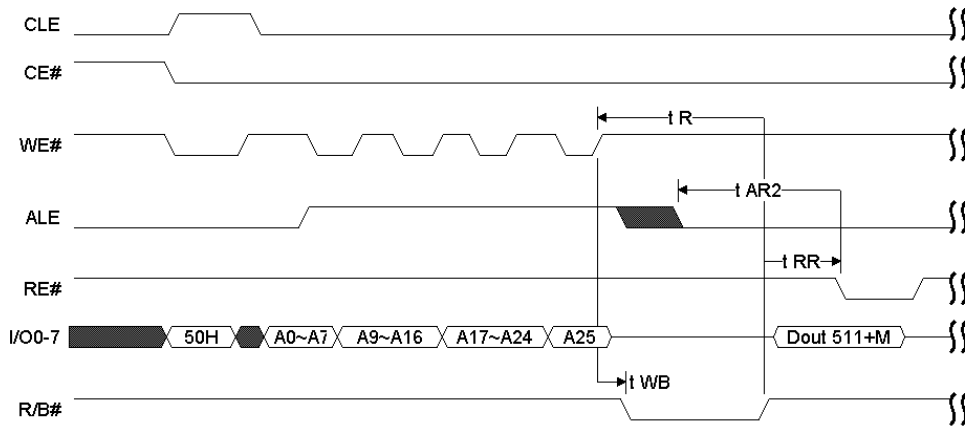
7.6 READ1 AND READ2 OPERATIONS (READ ONE PAGE)



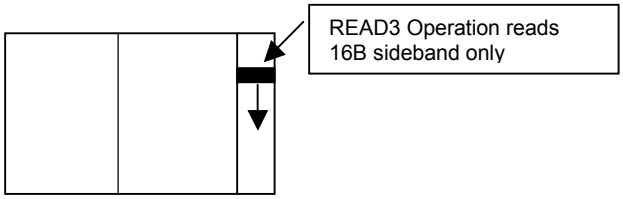
7.7 READ1 AND READ2 OPERATIONS (INTERCEPTED BY CE#)



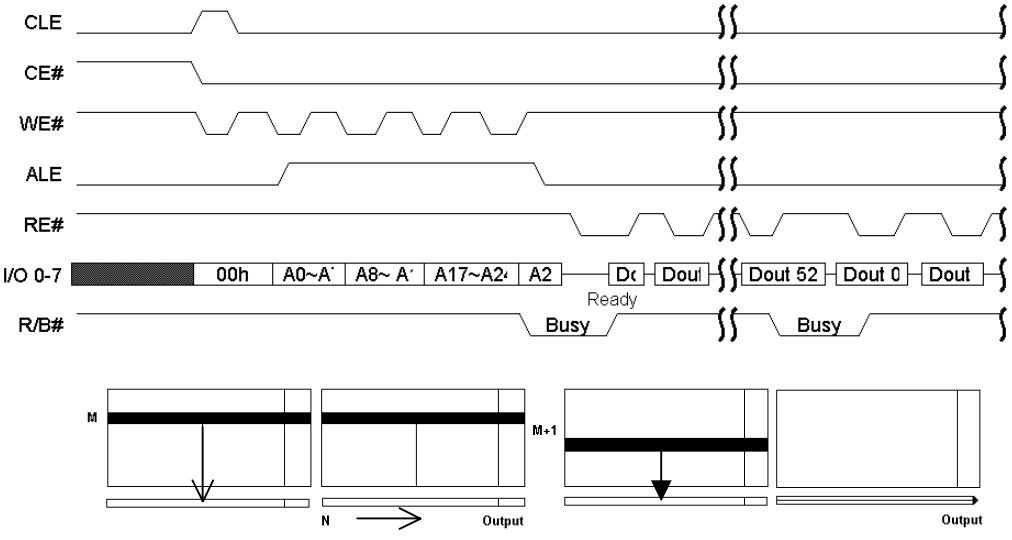
7.8 READ3 OPERATION (READ ONE PAGE)



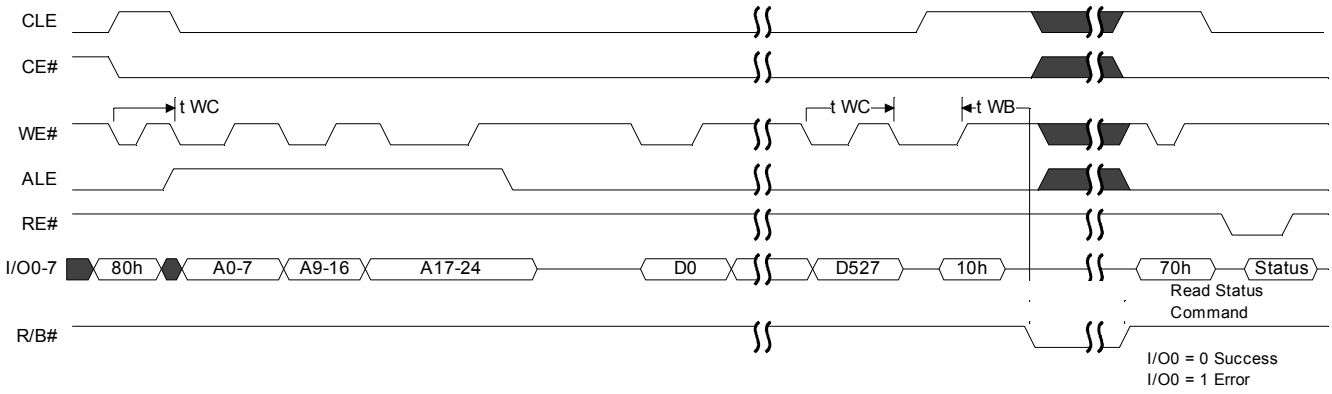
M Address
A0~A3: Valid Address
A4~A7: Don't Care



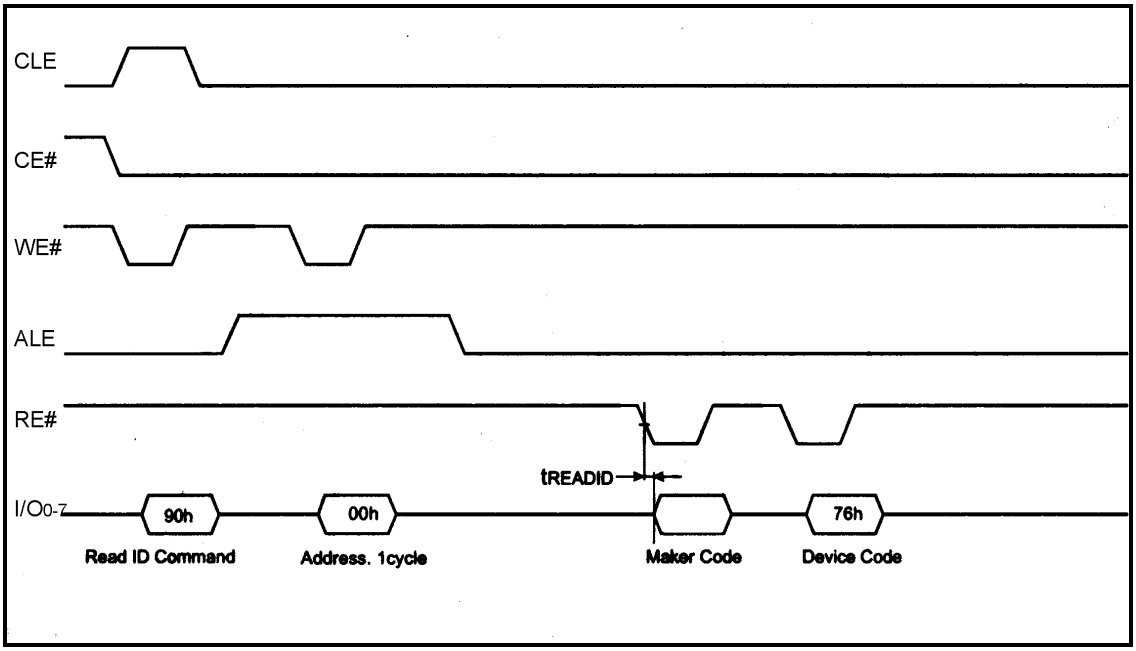
7.9 SEQUENTIAL ROW READ OPERATION (WITHIN A BLOCK)



7.10 PAGE WRITE OPERATION



7.11 MANUFACTURE & DEVICE ID READ OPERATION



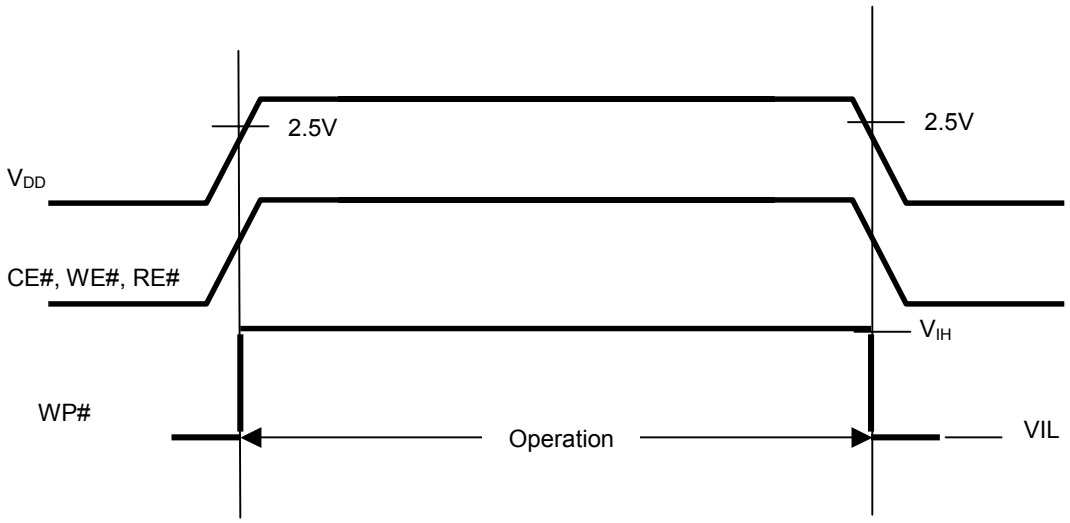
8.0 IDENTITY 3DM PROTOCOL

The "Identify 3DM" protocol is used to prevent unintentional overwriting of data on Matrix's memory devices from hosts which are not enabled for Matrix media. A host may identify its ability to use Matrix® 3DM during a data session using this protocol or it may bypass the protocol in hardware.

PROTOCOL: After an initial power-on, the Matrix® 3DM module is set to a "read only" state. In this state, write operations are not permitted. In order to allow write operations, an ID3DM command must be performed by sending three consecutive IDREAD commands to the device. This sequence tells the memory that the host device is enabled to use Matrix® 3DM. Once this command is executed the card is "unlocked," and write operations are permitted.

HARDWARE BYPASS: Alternatively, the "Identify 3DM" protocol may be bypassed in hardware by setting Pin 31 (TSOP32) to V_{DD}. This allows all supported commands to be issued immediately, bypassing the protocol above.

9.0 POWER ON REQUIREMENTS



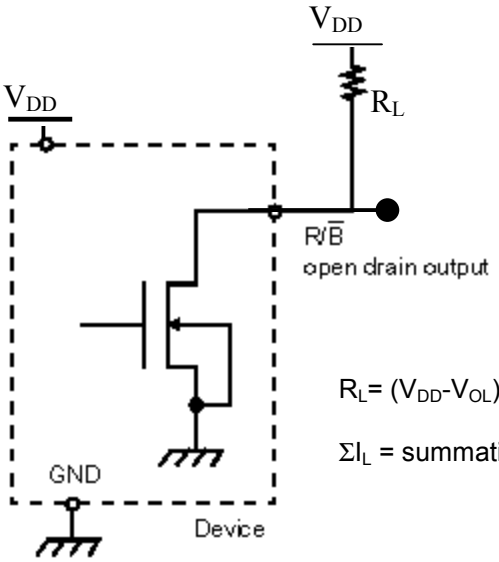
To ensure proper startup a RESET command should be entered after V_{DD} has been established.

10.0 READ/BUSY# LOAD REQUIREMENTS

The Ready/Busy# signal requires a pull-up resistor for this open-drain output.
For the resistance (R_L) refer to the following equation:

$$R_L = \frac{V_{DD}\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \Sigma\ I_L}$$

$\Sigma\ I_L$ is the sum of the input current of all devices connected to the Ready/Busy# pin.

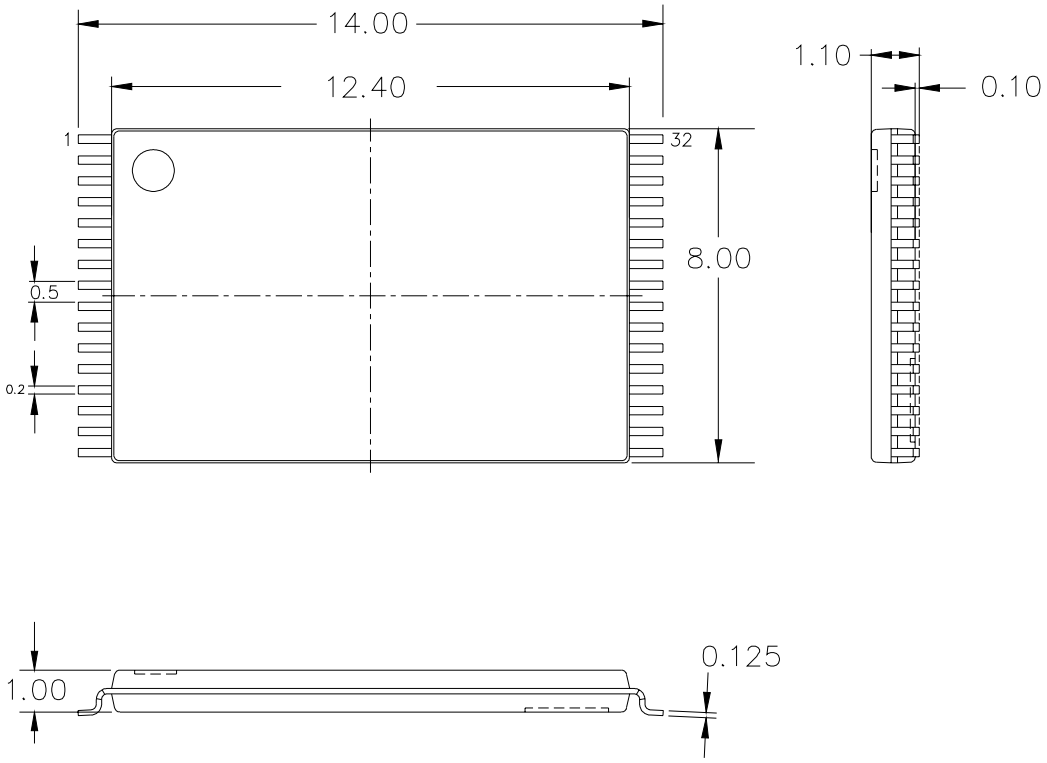


$R_L = (V_{DD}-V_{OL})/(I_{OL}+\Sigma I_L)$

ΣI_L = summation of all input currents tied to the R/B# pin

11.0 PACKAGE DIMENSIONS

11.1 32-PIN TSOP



Notes:

- *All dimensions listed are nominal values listed in mm.*
- *Limited volume 48-pin TSOP available for samples only.*
- *Alternative packages may be available upon request.*

12.0 PART NUMBER INFORMATION

Memory Capacity	Package Description	Ordering Part Number	Operational Part Number (On TSOP)
16MB	32-pin TSOP	3DM-16TS-T004	11252-XX-XX
16MB	32-pin TSOP Pb-Free	3DM-16TS-T008	11277-XX-XX
32MB	32-pin TSOP Pb-Free	3DM-32TS-T006	11278-XX-XX
64MB	32-pin TSOP Pb-Free	3DM-64TS-T005	11219-XX-XX