Faculty of Engineering and Computer Science
Expectations of Originality

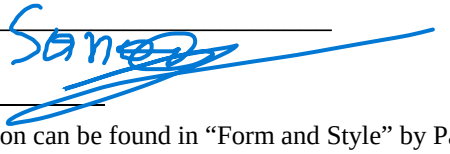
This form sets out the requirements for originality for work submitted by students in the Faculty of Engineering and Computer Science. Submissions such as assignments, lab reports, project reports, computer programs and take-home exams must conform to the requirements stated on this form and to the Academic Code of Conduct. The course outline may stipulate additional requirements for the course.

1. Your submissions must be your own original work. Group submissions must be the original work of the students in the group.
2. Direct quotations must not exceed 5% of the content of a report, must be enclosed in quotation marks, and must be attributed to the source by a numerical reference citation[1]. Note that engineering reports rarely contain direct quotations.
3. Material paraphrased or taken from a source must be attributed to the source by a numerical reference citation.
4. Text that is inserted from a web site must be enclosed in quotation marks and attributed to the web site by numerical reference citation.
5. Drawings, diagrams, photos, maps or other visual material taken from a source must be attributed to that source by a numerical reference citation.
6. No part of any assignment, lab report or project report submitted for this course can be submitted for any other course.
7. In preparing your submissions, the work of other past or present students cannot be consulted, used, copied, paraphrased or relied upon in any manner whatsoever.
8. Your submissions must consist entirely of your own or your group's ideas, observations, calculations, information and conclusions, except for statements attributed to sources by numerical citation.
9. Your submissions cannot be edited or revised by any other student.
10. For lab reports, the data must be obtained from your own or your lab group's experimental work.
11. For software, the code must be composed by you or by the group submitting the work, except for code that is attributed to its sources by numerical reference.

You must write one of the following statements on each piece of work that you submit:
For individual work: **"I certify that this submission is my original work and meets the Faculty's Expectations of Originality",** with your signature, I.D. #, and the date.
For group work: **"We certify that this submission is the original work of members of the group and meets the Faculty's Expectations of Originality",** with the signatures and I.D. #s of all the team members and the date.

A signed copy of this form must be submitted to the instructor at the beginning of the semester in each course.

I certify that I have read the requirements set out on this form, and that I am aware of these requirements. I certify that all the work I will submit for this course will comply with these requirements and with additional requirements stated in the course outline.

Course Number: COEN313 winter 2024 Instructor: Otmane Ait Mohamed
Name: BERTIN MIHIGO SANO I.D. # 40157663
Signature:  Date: April 6th 2024

[1] Rules for reference citation can be found in "Form and Style" by Patrich MacDonagh and Jack Bordan, fourth edition, May, 2000, available at http://www.encs.concordia.ca/scs/Forms/Form&Style.pdf.
Approved by the ENCS Faculty Council February 10, 2012

Digital Design Project: Room Occupation Monitor

GitHub repo: https://github.com/sanobertin/RoomMonitor

Introduction

This smart system tracks occupation in a room by monitoring the number of entries and exists in a room. It makes use of sensors that tracks a change light intensity at the door when someone enters and alerts the signal to the system for tracking purposes. When the room reaches a maximum occupancy of 255 individuals, it alerts by activating a signal that would trigger for example an alarm, sound, or notification. Further the system also provides a numeric output showing number of people that are currently occupying the room.

Below is a conceptual diagram of the design of out digital system.

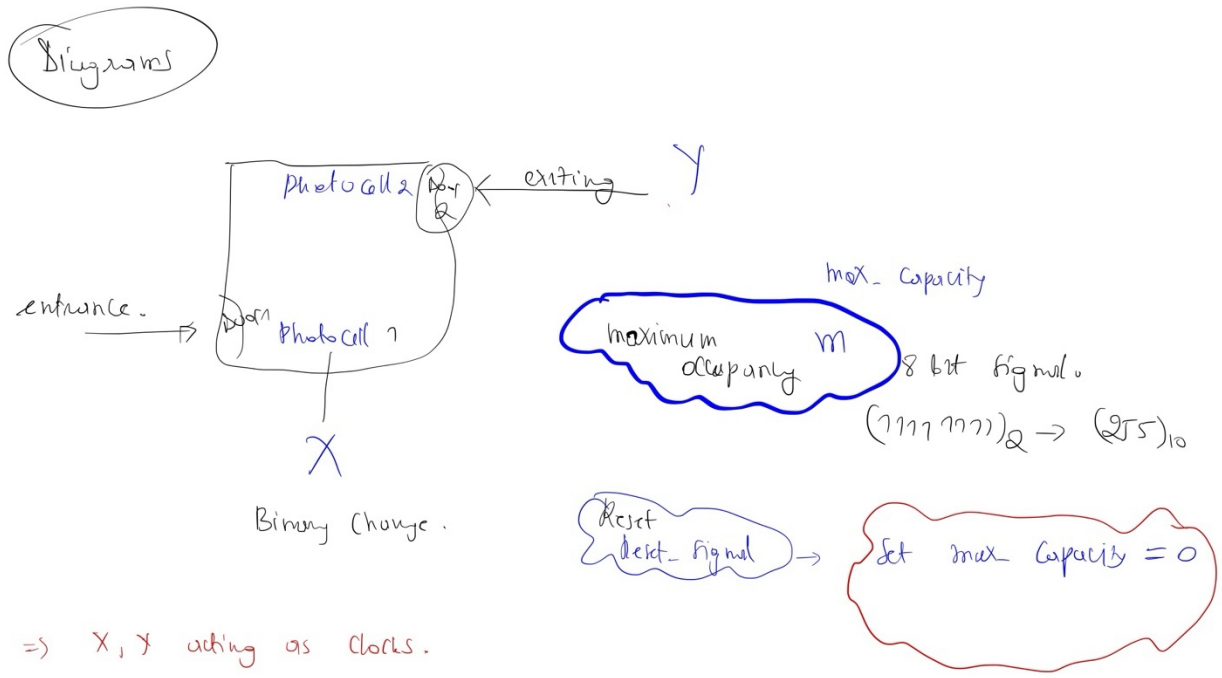


Figure 1: Design Requirements

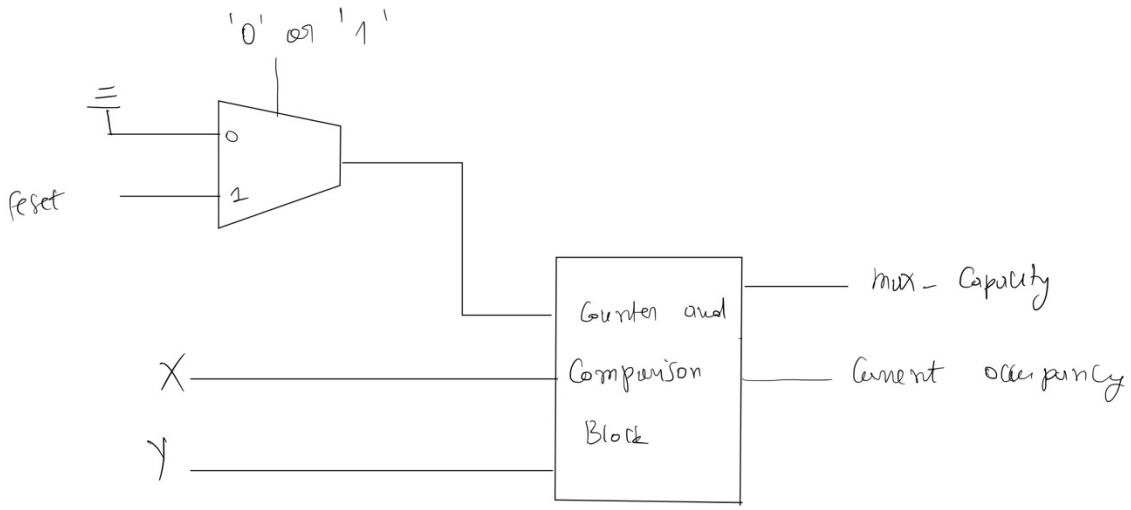


Figure 2: Gate & Block level design of the system.

Design Process

Note: Implementation was not done on the actual Artix A7 FPGA board. As such Design constraints will be omitted in the overall design.

VHDL code:

```
-- ID: 40157663
-- Name: Bertin Mihigo Sano
-- Project is due for submission on April 5th, 2024
library IEEE;
library work;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.numeric_std.all;

entity room_occupancy is
    Port ( X : in  STD_LOGIC; --  input from the photocell. detects entrance
           Y : in  STD_LOGIC; --  input from the photocell. detects exiting
           reset : in  STD_LOGIC; -- sets max occupancy to 0
           current_occupancy : out unsigned(7 downto 0);
           max_capacity: out  STD_LOGIC -- output to the LED. indicates if the room is full or not aka '1' if full, '0' if not
           );
end room_occupancy;

architecture rtl of room_occupancy is
    constant max_occupancy : unsigned(7 downto 0) := (others => '1'); -- note that 11111111 is 255 in decimal
    signal temp: unsigned(7 downto 0):= (others => '0');
    begin
    process(X, Y, reset)
    begin
        if reset = '1' then
            temp <= (others => '0');
            max_capacity <= '0';
            -- current_occupancy <= temp;
        end if;
        if temp = max_occupancy then
            max_capacity <= '1';
            -- current_occupancy <= temp;
        end if;
        if temp >0 and rising_edge(Y) then
        if  reset = '1' then temp <= (others => '0'); else temp <= temp - 1; end if;
            -- current_occupancy <= temp;
        end if;
        if(temp < max_occupancy) and rising_edge(X) then
        if  reset = '1' then temp <= (others => '0'); else temp <=  temp + 1; end if;
                -- current_occupancy <= temp;
        end if;
    end process;
    current_occupancy <= temp;
end rtl;

-- end of my code
```

Simulation:

In the simulation below the behavior the circuit is tested in runtime. It is composed of 2 parts. In the first we ignore the reset to showcase the behaviour when it reaches **max_occupancy = 1**. In the second part we make use of the reset at some time interval (2000 ms in the case shown below) to highlight the reset function in the circuit,

Figure 3: Initial simulation state.

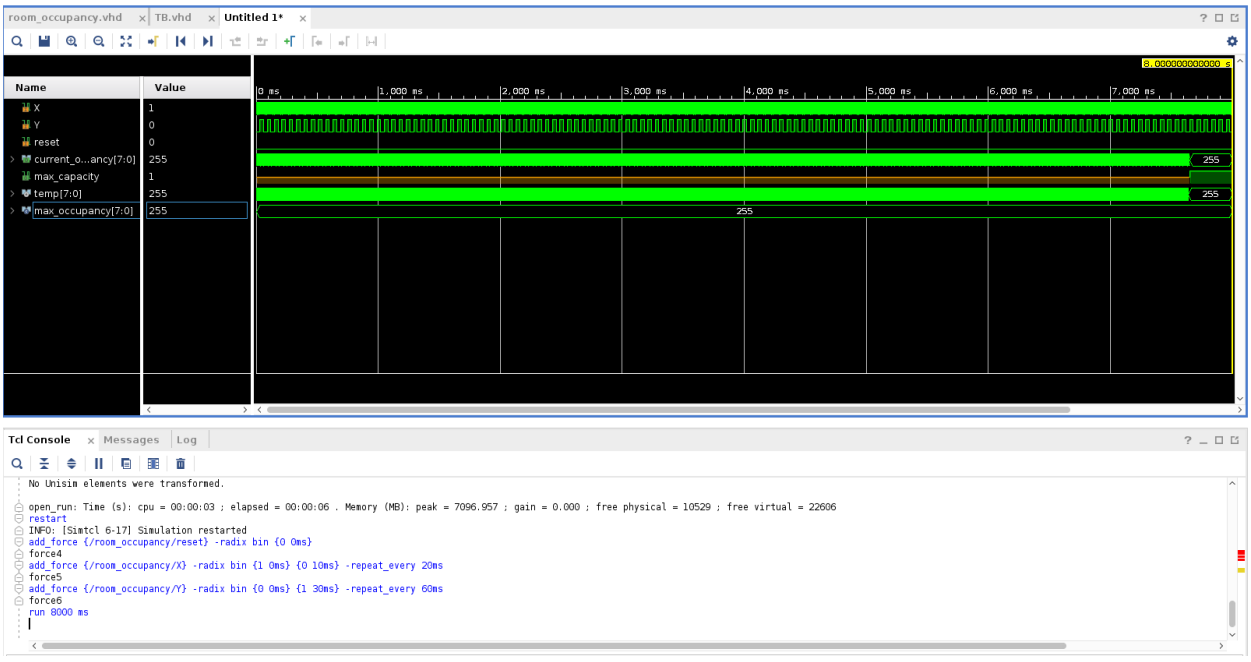


Figure 4: after 8000 ms run

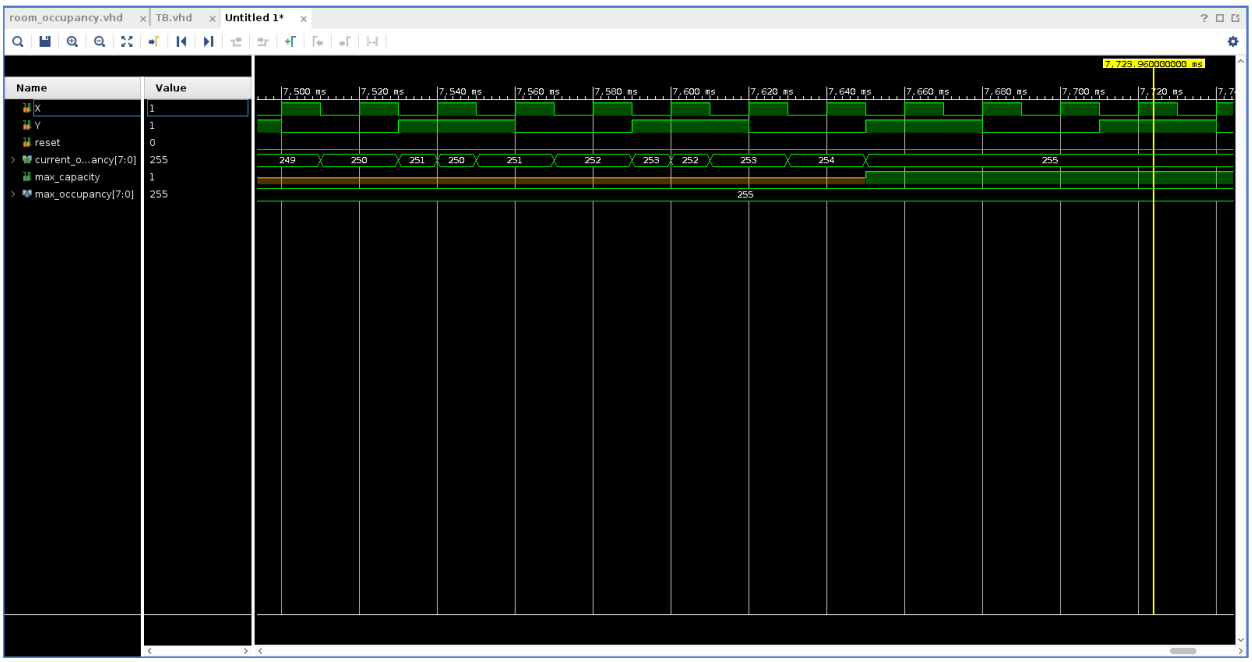


Figure 5: After maximum capacity is reached.

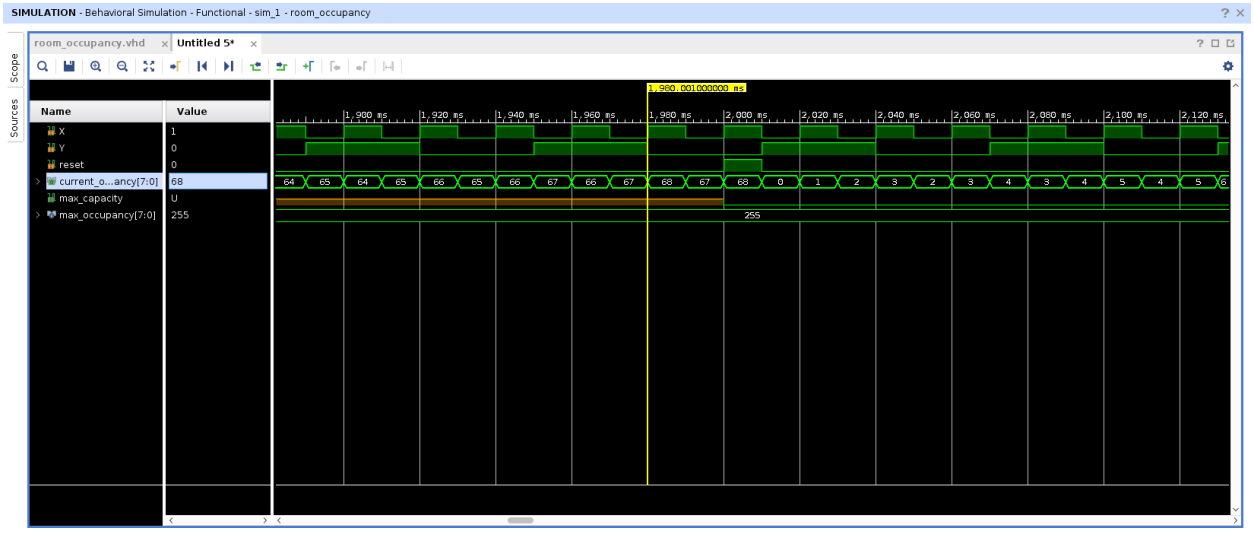


Figure 6: At the reset trigger at 2000 ms

Note: due to higher max_occupancy limit of decimal 255, a long simulation is needed to reach this threshold, and Y signal period is intentional longer than X signal so that overtime max_occupation keeps increasing.

Testbench

The code below is a sample snapshot of the testbench written for auto testing our system in VHDL for functionality. The i signal is

```vhdl
-- ID: 40157663
-- Name: Bertin Mihigo Sano
-- Project is due for submission on April 5th, 2024
-- This is a testbench for room_occupancy.vhd
library IEEE;
library work;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.numeric_std.all;

entity tb is
end tb;

architecture testbench of tb is

signal X_tb, Y_tb, reset_tb, max_capacity_tb: std_logic := '0' ;
constant max_occupancy_tb : unsigned(7 downto 0) := (others => '1');
signal current_occupancy_tb : unsigned(7 downto 0):= (others => '0');
signal i: integer:=0;


begin
    room_occupancy_tb: entity work.room_occupancy(rtl) port map (
    X => X_tb,
    Y => Y_tb,
    reset => reset_tb,
    max_capacity => max_capacity_tb,
    current_occupancy => current_occupancy_tb);

    process
        begin
        report("start simulation here:");
        --wait until reset_tb = '0';
        X_tb <= not X_tb after 10 ms;
        Y_tb <= not Y_tb after 30 ms;
        reset_tb <= not reset_tb after 100ms;
        i <= i+1 after 10 ms;


        assert  (i<=500) report "I ended simulation after 300ms" severity ERROR;
        wait for 10 ms;
    end process;
end testbench;

-- end of my code
```

RTL Analysis and Synthesis

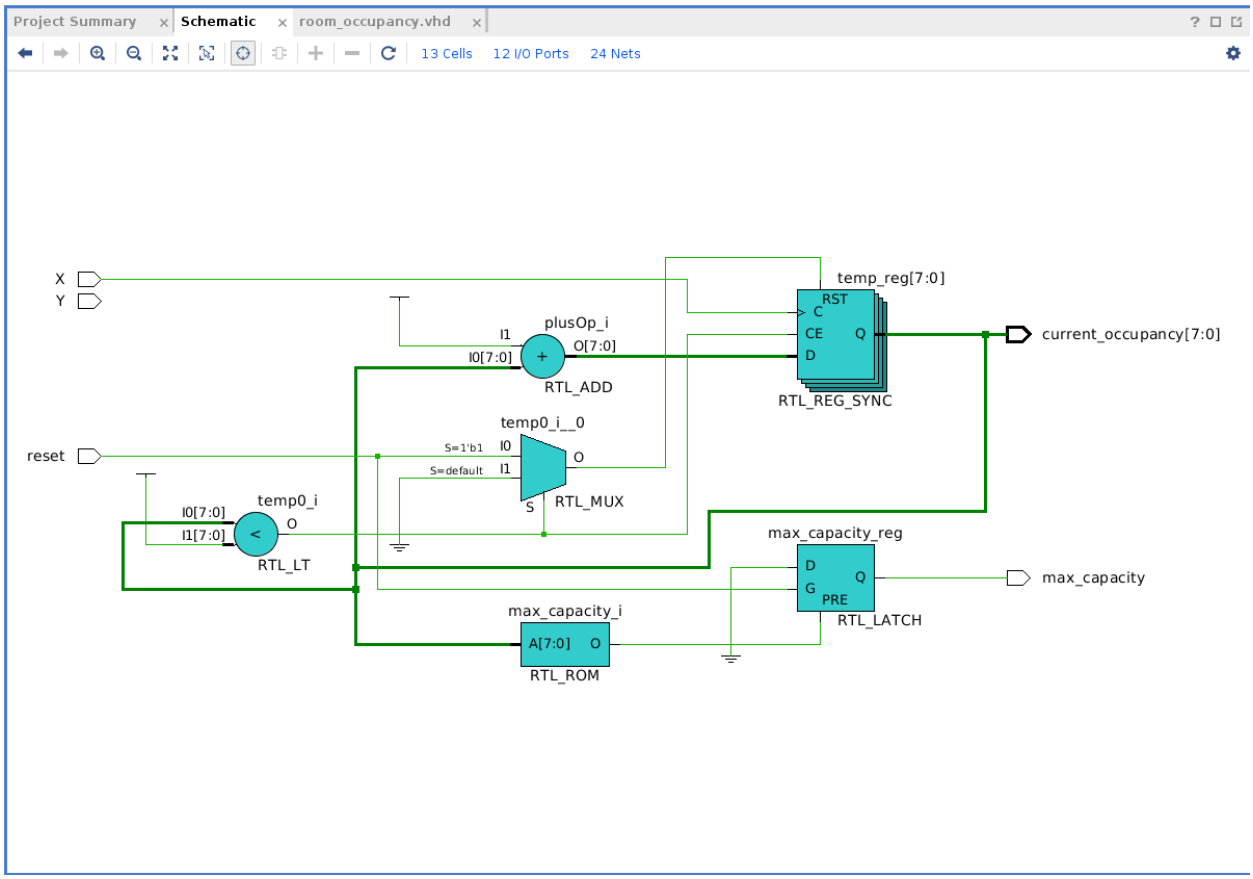
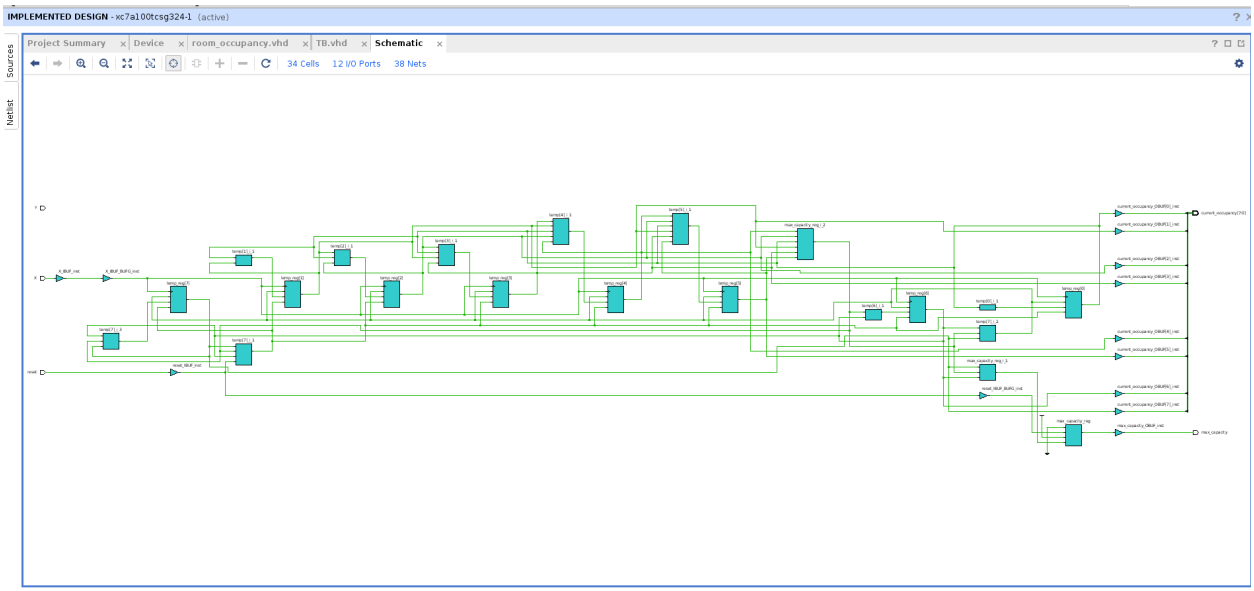


Figure 7: Schematic view of the digital system.

Implementation



Conclusion & Results

In the design of this digital system, the simulation proved the working expectation of the circuit at some critical points of this circuit. Major challenges of the design included defining two processes that can modify the current_occupancy(our counter in circuit). Another challenge is the nesting of clocked signals which violates VHDL rules of design. Furthermore, the point of mention is by looking the schematic diagram, Y is not connected directly to the circuit, and this can lead to the unintended behavior of the system in real world. Nevertheless, comprehensive VHDL design knowledge and more control on the production of this schematic by Vivado could have overcame this challenge.

References & Tools used.

[1]. Xilinx Vivado v2018

[2]. Vivado Simulator

[3]. Linux OS

[4]. Tcl scripts for simulations

[5]. 'VHDLwhiz – The Best Resource for VHDL Engineers'. VHDLwhiz, 12 Dec. 2023, https://vhdlwhiz.com/.

[6]. 'COEN 313 Lecture notes & other course related resources', Winter 2024, Otmane Ait Mohamed