COEN313 Digital Design Project **Winter 2024**

You have been assigned the exciting task of designing a sophisticated digital system capable of accurately tracking and monitoring the occupancy of a room. Within this system, the primary entrance door is equipped with a highly responsive photocell, which, upon the obstruction of light, induces a change in a binary signal denoted as **X**. Similarly, individuals exiting the room pass through a second door featuring a photocell, triggering a binary signal **Y** when the light is interrupted.
The system has a "programmable" maximum occupancy threshold, adjustable through a signal **m**. Assume **m** is an 8-bit signal. When the room's occupancy reaches this defined maximum, the system must promptly respond by asserting a **max_capacity** signal. This acts as a clear indication that the room has reached its full capacity, thereby preventing further admissions until space becomes available again.
Upon the activation of a **reset** signal, the system is designed to revert to its initial state allowing for the accurate tracking of occupancy to commence anew.

1. Provide a conceptual diagram for the digital system. Clearly identify the different blocks such as multiplexers, flip-flops, incrementor, etc. and their interconnect.
2. Model your circuit using VHDL.
3. Provide a relevant testbench. Make sure to cover enough scenarios to verify your design.
4. Provide simulation and synthesis results for a Xilinx Nexys A7 FPGA development board (note: no actual FPGA implementation is required). Include the Vivado log file in the report.
5. Based on the results, comment on the quality of the design in term of speed and FPGA resource utilization.

Evaluation and grading criteria

The project will be evaluated based on:

- Delivery on time.
- High level description of the specification to be realized.
- Design methodology.
- Quality of the VHDL code.
- Simulation and synthesis results.
- Report and Documentation.

Grade Range	Criteria
90 – 100	Outstanding, **surpassed** objectives, perfectly organized report
85 – 89	Excellent, met **all** objectives
80 – 84	Excellent, met **most** of objectives
70 – 79	Good quality, met **some** of objectives
60 – 69	Did not meet a **majority** of objectives
0 - 59	Reserved for **poor results** or student that did not put in much effort.

Report

Use the Concordia Form and Style to prepare your report:
https://www.concordia.ca/content/dam/ginacody/docs/Form-Style.pdf

Project reports and VHDL code due date is **23:59 Friday April 05, 2024**, through Moodle. A submission link will be available.

Each student fill-in and sign the Confirmation of Originality form, which covers the originality for all submitted work content (report, software), by ticking the respective boxes. Carefully read page 2 of the Confirmation of Originality form. Submission of this form is **MANDATORY** (check Agenda for the submission deadline). **Failure to submit it will result in a grade of zero for the WHOLE Project**.

Project Code Guidelines

Students are required to submit their VHDL code in a **compressed file** (zip, rar, etc.) of a clean directory with a **README** document clearly describing the files in the directory and the process for executing the code. The README file shall be in **TXT format** and included in the zipped file.

IMPORTANT NOTICE: STUDENTS MUST SUBMIT AN ORIGINAL WORK THAT IS NOT COPIED NOR PLAGIARIZED. Students submitting unoriginal content of Project Report, Project Code (regardless of the formatting) will be reported with an Incident Report to the Department. Such incident would result in offense to Article 18 as stated in the Academic Code of Conduct, which can result in an EXPEL FROM CONCORDIA UNIVERSITY.