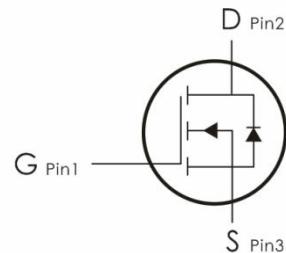
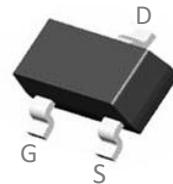


Description:

This N-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge. It can be used in a wide variety of applications.



Features:

- 1) $V_{DS}=30V, I_D=5A, R_{DS(on)}<30m\Omega @ V_{GS}=10V$
- 2) Low gate charge.
- 3) Green device available.
- 4) Advanced high cell density trench technology for ultra $R_{DS(on)}$.
- 5) Excellent package for good heat dissipation.

Absolute Maximum Ratings: ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Continuous Drain Current- $T_A=25^\circ C^1$	5	A
	Continuous Drain Current- $T_A=70^\circ C^1$	3.6	
I_{DM}	Pulse Drain Current Tested ²	16	A
P_D	Power Dissipation- $T_A=25^\circ C^3$	1	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

Thermal Characteristics:

Symbol	Parameter	Max	Units
$R_{\Theta JA}$	Thermal Resistance,Junction to Ambient ¹	125	$^\circ C/W$
$R_{\Theta JC}$	Thermal Resistance Junction-Case ¹	80	$^\circ C/W$

Package Marking and Ordering Information:

Part NO.	Marking	Package
DO3400D	A09T:	SOT-23

Electrical Characteristics: ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_D=250 \mu\text{A}$	30	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=24\text{V}, T_j=25^\circ\text{C}$	---	---	1	μA
		$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=24\text{V}, T_j=55^\circ\text{C}$	---	---	5	μA
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 12\text{V}, V_{\text{DS}}=0\text{A}$	---	---	± 100	nA
On Characteristics						
$V_{\text{GS(th)}}$	GATE-Source Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}, I_D=250 \mu\text{A}$	0.5	0.7	1.2	V
$R_{\text{DS(ON)}}$	Drain-Source On Resistance ²	$V_{\text{GS}}=10\text{V}, I_D=4\text{A}$	---	25	30	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_D=3\text{A}$	---	28	40	
		$V_{\text{GS}}=2.5\text{V}, I_D=2\text{A}$	---	35	47	
G_{FS}	Forward Transconductance	$V_{\text{DS}}=5\text{V}, I_D=3\text{A}$	---	19	---	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{\text{DS}}=15\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	---	660	920	pF
C_{oss}	Output Capacitance		---	50	70	
C_{rss}	Reverse Transfer Capacitance		---	42	60	
Switching Characteristics						
$t_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}}=15\text{V}, I_D=3\text{A}, V_{\text{GS}}=4.5\text{V}, R_G=3.3 \Omega$	---	3.2	6.4	ns
t_r	Rise Time		---	41.8	75	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time		---	21.2	42	ns
t_f	Fall Time		---	6.4	12.8	ns
Q_g	Total Gate Charge		---	8.34	11.7	nC
Q_{gs}	Gate-Source Charge	$V_{\text{GS}}=4.5\text{V}, V_{\text{DS}}=15\text{V}, I_D=3\text{A}$	---	1.26	1.8	nC
Q_{gd}	Gate-Drain "Miller" Charge		---	1.88	2.6	nC

R_G	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	1.5	3	Ω
Drain-Source Diode Characteristics						
V_{SD}	Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ C$	---	---	1.2	V
I_S	Source drain current ^{1,4}	$V_G=V_D=0V, \text{Force Current}$	---	---	5	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	16	A
T_{rr}	Reverse Recovery Time	$I_F=3A, dI/dt=100A/\mu s, T_J=25^\circ C$	---	6.8	---	ns
Q_{rr}	Reverse Recovery Charge		---	2.3	---	nC

Notes:

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics: ($T_c=25^\circ C$ unless otherwise noted)

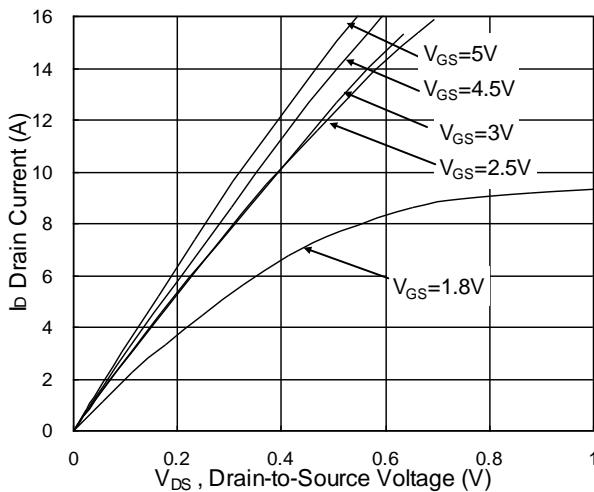


Fig.1 Typical Output Characteristics

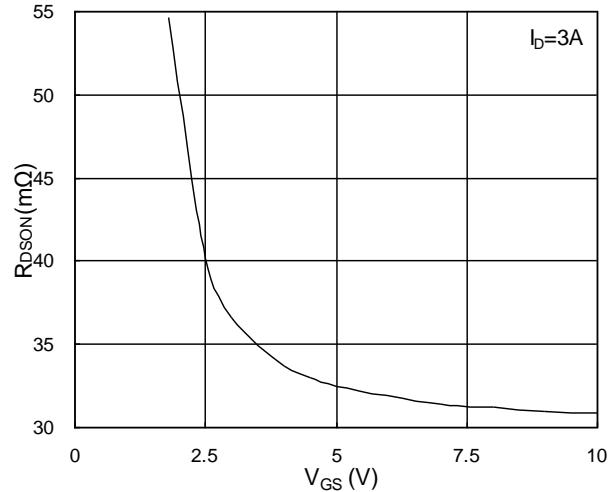


Fig.2 On-Resistance vs G-S Voltage

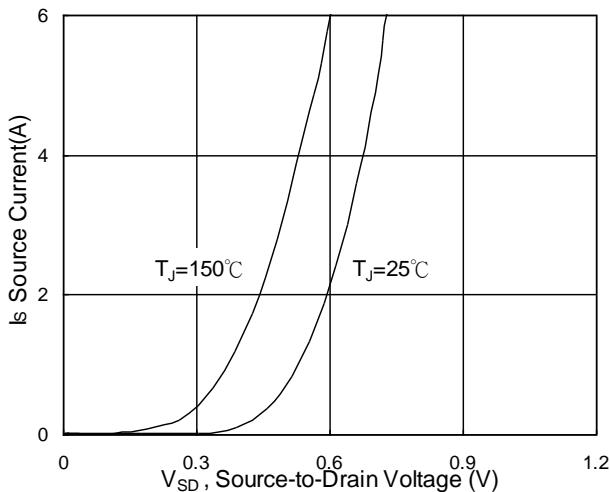


Fig.3 Source Drain Forward Characteristics

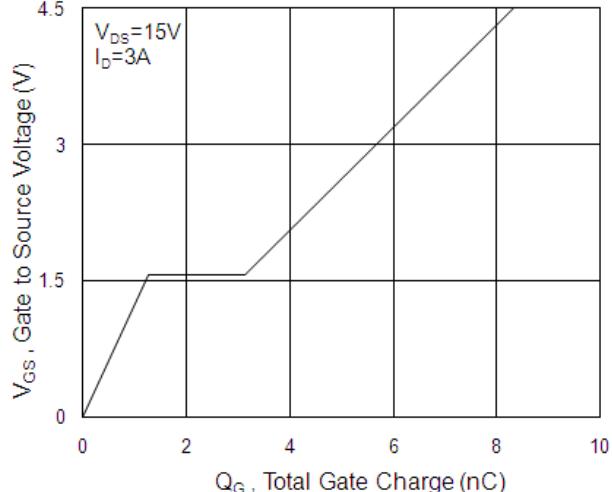


Fig.4 Gate-Charge Characteristics

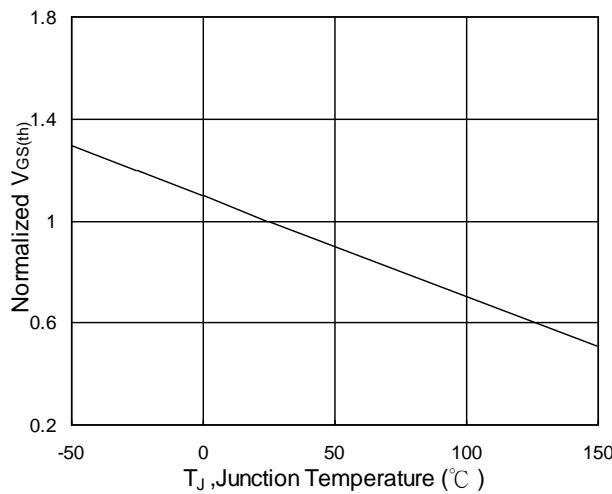


Fig.5 Normalized $V_{GS(th)}$ vs T_J

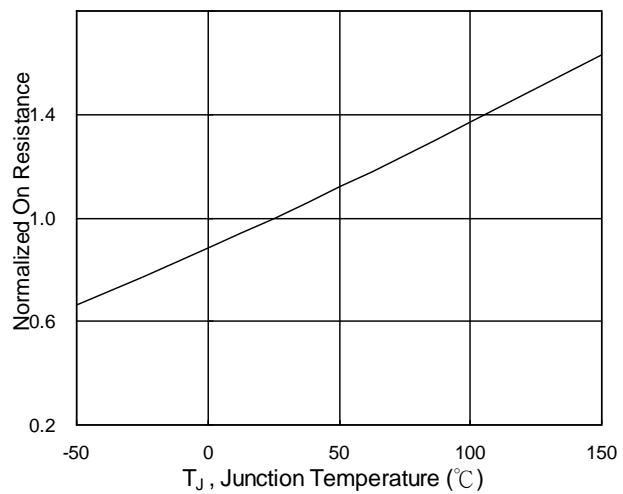


Fig.6 Normalized $R_{DS(on)}$ vs T_J

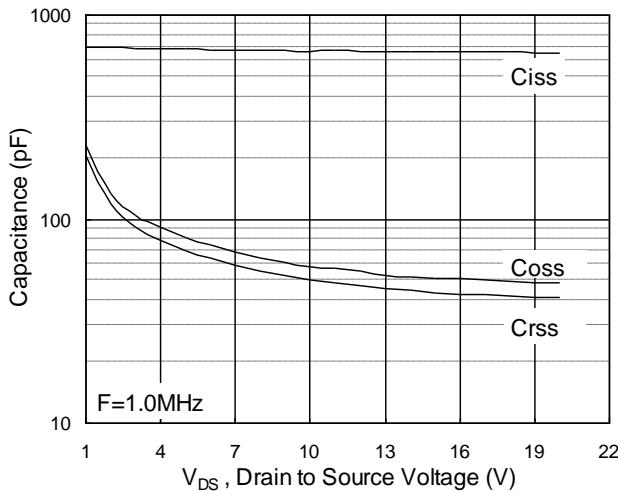


Fig.7 Capacitance

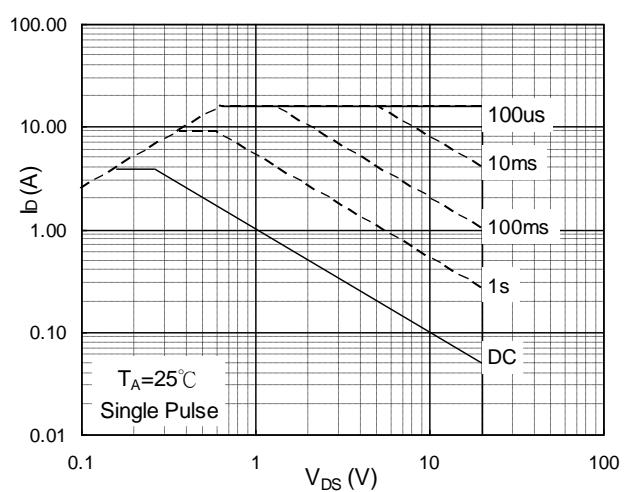


Fig.8 Safe Operating Area

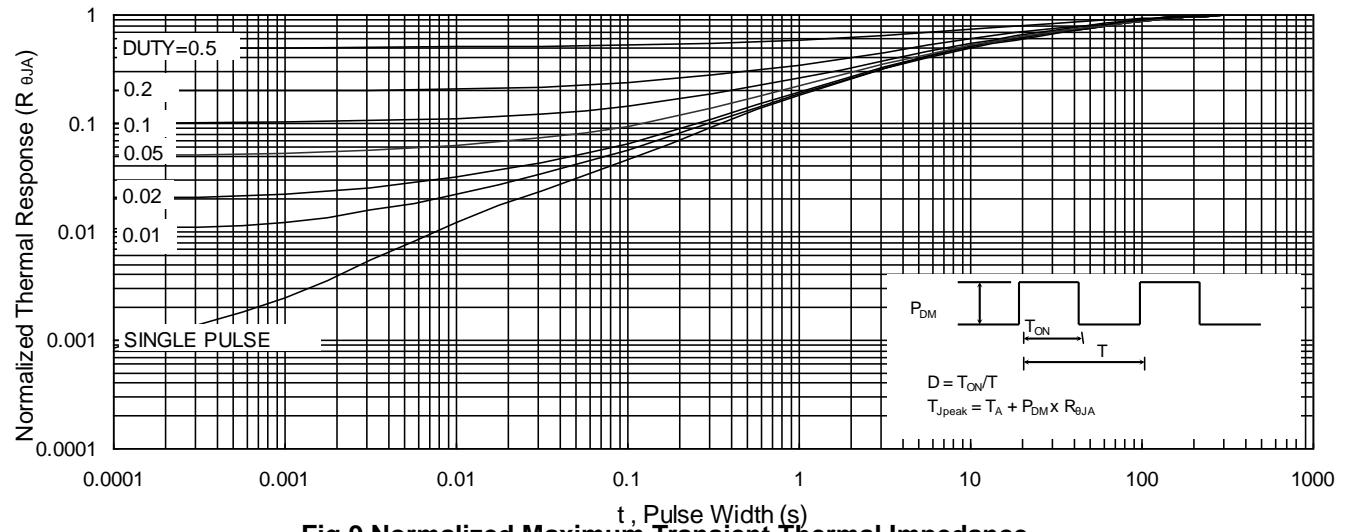


Fig.9 Normalized Maximum Transient Thermal Impedance

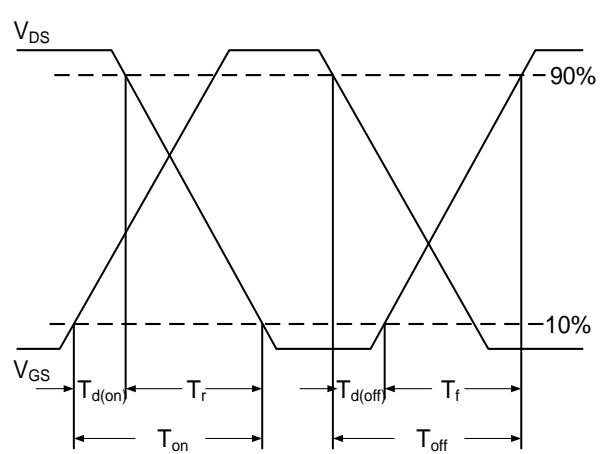


Fig.10 Switching Time Waveform

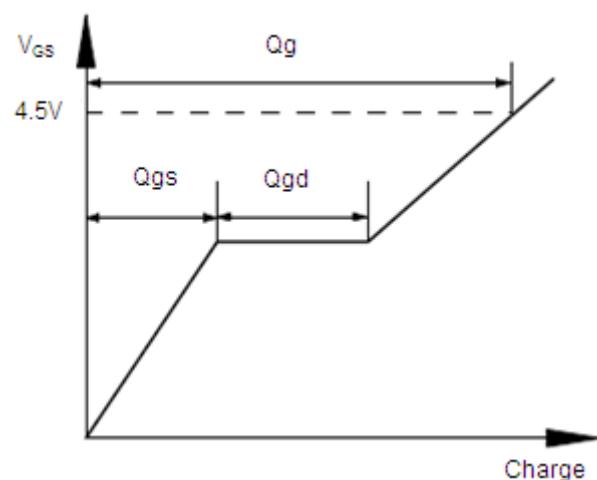


Fig.11 Gate Charge Waveform