

MSCS-531-Assignment 5 – Exploring Data-Level Parallelism (DLP) in Modern Computing

Sandesh Pokharel

ID: 005026677

University of Cumberlands

MSCS-531: Computer Architecture

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1. Introduction

In the realm of modern computing, efficient data processing has become a necessity, with the explosion of data from various fields like multimedia, machine learning, and scientific computing. Data-Level Parallelism (DLP) stands out as one of the most effective strategies to manage these computational demands. DLP allows for the simultaneous processing of multiple data elements, often leveraging specialized architectures and instructions to enhance speed and efficiency. Unlike Instruction-Level Parallelism (ILP), which focuses on executing multiple instructions at the same time, DLP is centered around processing multiple data items with a single instruction stream. This fundamental difference highlights DLP's unique position in optimizing tasks that involve extensive data handling.

The primary objective of this report is to dive deep into DLP by exploring its core concepts, architectures, and practical applications. We'll examine how DLP is applied in various fields that require high-throughput data handling, such as image and video processing, scientific modeling, and neural networks. Additionally, we'll look into the architectural innovations, such as vector processing and Single Instruction Multiple Data (SIMD) extensions, that enable DLP to achieve high-performance results.

This report is organized to provide both foundational knowledge and practical insights. First, we will explore the underlying principles of DLP, followed by a detailed look at the key architectures supporting DLP, including vector architectures and SIMD instructions. We will then discuss the role of Graphics Processing Units (GPUs) as powerful DLP engines, highlighting their effectiveness in handling large-scale parallel tasks. The importance of loop-

level parallelism will also be covered, focusing on software techniques that further exploit DLP in various applications.

Finally, we'll address the trade-offs associated with DLP, such as the balance between performance and energy efficiency, and explore emerging trends like AI accelerators and other specialized hardware. By the end of this report, readers will gain a comprehensive understanding of DLP's current landscape, its benefits, and the challenges it faces in modern computing.

2. Understanding Data-Level Parallelism

2.1 Concept of DLP

Data-Level Parallelism (DLP) is a computing technique that focuses on performing operations on multiple data elements simultaneously, typically using a single instruction. This is distinct from Instruction-Level Parallelism (ILP), which seeks to execute multiple instructions independently, regardless of the data they operate on. DLP's unique approach is especially advantageous in scenarios where the same operation needs to be applied to vast datasets, such as image processing, machine learning, and scientific simulations (Flynn, 1966). By aligning computations on different data points under one instruction, DLP minimizes redundant instructions and significantly boosts performance in data-centric tasks.

To clarify the difference: while ILP emphasizes breaking down instruction execution across pipelines to increase throughput, DLP primarily targets tasks where multiple data points can be processed in parallel. For example, in image filtering, each pixel may undergo the same transformation, making it ideal for DLP.

2.2 Importance of DLP in Key Applications

DLP has become crucial in domains that demand fast, efficient data processing. In multimedia applications, DLP enables real-time processing of audio and visual data by applying operations across thousands or millions of data points. For scientific computing, where tasks like climate modeling or genomic analysis involve enormous datasets, DLP supports rapid computation and helps reduce simulation times (Kumar & Gupta, 1994). Additionally, machine learning relies heavily on DLP, particularly for training neural networks, where vast matrices are continuously processed and adjusted to minimize prediction errors (Sze et al., 2017).

These fields benefit from DLP not just for speed but also for its ability to streamline operations across vast data, conserving computational resources and reducing latency. By enabling massive parallelism, DLP supports tasks that would be impractical with ILP alone, illustrating its critical role in modern computing.

2.3 Key Architectural Features that Enable DLP

To exploit DLP fully, certain architectural features are essential. Among the most impactful are **vector architectures** and **Single Instruction Multiple Data (SIMD) extensions**. Vector architectures, for instance, allow operations on entire arrays of data, processing each element simultaneously through a single vector instruction. This is commonly seen in applications like scientific simulations, where large datasets are manipulated using a series of repetitive calculations.

SIMD instructions, such as Intel's AVX (Advanced Vector Extensions), ARM's NEON, and AMD's SSE (Streaming SIMD Extensions), further enable DLP by allowing one instruction to perform the same operation across multiple data points within a processor register. By bundling operations across multiple elements, SIMD minimizes instruction overhead and accelerates processing in data-parallel applications. These instructions are particularly beneficial in areas like digital signal processing and computer graphics, where the same operation is performed across all data units (Hennessy & Patterson, 2019).

Vector architectures and SIMD instructions are the backbone of DLP, transforming how tasks with vast data dependencies are processed by consolidating operations under fewer instructions, ultimately enhancing both speed and efficiency.

3. Exploring DLP Architectures

3.1 Vector Architectures

Vector architectures are designed to enhance performance in tasks where operations are applied repetitively across large datasets. By allowing a single instruction to operate on multiple data elements simultaneously, vector architectures maximize data parallelism, reducing processing time and instruction overhead. This makes them particularly suitable for applications in fields like scientific simulations, machine learning, and multimedia processing, where repetitive calculations on arrays or matrices are common (Hennessy & Patterson, 2019).

For this assignment, we chose to simulate a RISC-V vector architecture in gem5. RISC-V's vector extension offers an open, flexible structure that enables straightforward experimentation with DLP techniques. Compared to other architectures like ARM, which primarily supports SIMD rather than full vector processing, RISC-V is designed with modern data-parallel workloads in mind. This choice allows us to showcase vector-based DLP more effectively, as RISC-V's vector extensions support varied vector lengths and operations, accommodating tasks with different data sizes and performance requirements.

Simulation Setup

To demonstrate DLP through vector processing, we used gem5 to simulate a vector addition task on large data arrays of length 1000. This setup provides a clear performance comparison between vectorized (unrolled) and scalar processing, as the vector addition task involves simple, repetitive operations across arrays of data. Key aspects of our setup include:

- **RISC-V Vector Processor Configuration:** We configured gem5 to simulate a RISC-V processor with vector extension capabilities. Although `riscv_vector.h` was unavailable, we approximated vector processing through loop unrolling to simulate vectorized operations across multiple data elements in each loop iteration.
- **Vector Operation:** A manually unrolled loop was implemented to perform the addition across arrays, allowing for four elements to be processed in each iteration to mimic vectorized parallel processing. This method effectively reduces instruction count and processing time for large datasets.

```
src/computer_architecture/riscv/emu: src/unknown_cpu.cc: March 10/2024 10:00:00: 0 array_add_scalar array_add_scalar.c
sandesh@sandesh-Inspiron-7373: /media/sandesh/easystore1/Sandesh_Cumberland_Assignments/Computer_Architecture/Week2/gen5$ ./build/RISCV/gen5.opt /media/sandesh/easystore1/Sandesh_Cumberland_Assignments/Computer_Architecture/Week2/gen5/configs/deprecated/example/se_vector2.py
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Oct 18 2024 20:22:41
gem5 started Oct 31 2024 14:44:15
gem5 executing on sandesh-Inspiron-7373, pid 562671
command line: ./build/RISCV/gen5.opt /media/sandesh/easystore1/Sandesh_Cumberland_Assignments/Computer_Architecture/Week2/gen5/configs/deprecated/example/se_vector2.py

warn: The 'get_runtime isa' function is deprecated. Please migrate away from using this function.
warn: The 'se.py' script is deprecated. It will be removed in future releases of gem5.
warn: The 'get_runtime isa' function is deprecated. Please migrate away from using this function.
Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
src/arch/riscv/linux/se_workload.cc:60: warn: Unknown operating system; assuming Linux.
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group. Legacy stat is deprecated.
system.remote_gdb: Listening for connections on port 7000
**** REAL SIMULATION ****
src/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
src/sim/mem_state.cc:443: info: Increasing stack size by one page.
src/sim/mem_state.cc:443: info: Increasing stack size by one page.
src/sim/mem_state.cc:443: info: Increasing stack size by one page.
Result of unrolled vector addition:
1 + 1000 = 1001
2 + 999 = 1001
3 + 998 = 1001
4 + 997 = 1001
5 + 996 = 1001
6 + 995 = 1001
7 + 994 = 1001
8 + 993 = 1001
996 + 5 = 1001
997 + 4 = 1001
998 + 3 = 1001
999 + 2 = 1001
1000 + 1 = 1001
Exiting @ tick 13205342500 because exiting with last active thread context
sandesh@sandesh-Inspiron-7373: /media/sandesh/easystore1/Sandesh_Cumberland_Assignments/Computer_Architecture/Week2/gen5$ ./build/RISCV/gen5.opt /media/sandesh/easystore1/Sandesh_Cumberland_Assignments/Computer_Architecture/Week2/gen5/configs/deprecated/example/se_scalar1.py
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Oct 18 2024 20:22:41
gem5 started Oct 31 2024 14:45:09
gem5 executing on sandesh-Inspiron-7373, pid 562679
command line: ./build/RISCV/gen5.opt /media/sandesh/easystore1/Sandesh_Cumberland_Assignments/Computer_Architecture/Week2/gen5/configs/deprecated/example/se_scalar1.py

warn: The 'get_runtime isa' function is deprecated. Please migrate away from using this function.
warn: The 'se.py' script is deprecated. It will be removed in future releases of gem5.
warn: The 'get_runtime isa' function is deprecated. Please migrate away from using this function.
Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
src/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)
src/arch/riscv/linux/se_workload.cc:60: warn: Unknown operating system; assuming Linux.
src/base/statistics.hh:279: warn: One of the stats is a legacy stat. Legacy stat is a stat that does not belong to any statistics::Group. Legacy stat is deprecated.
system.remote_gdb: Listening for connections on port 7000
**** REAL SIMULATION ****
src/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
src/sim/mem_state.cc:443: info: Increasing stack size by one page.
```

- **Performance Metrics:** We focused on execution time, instruction count, cycles per instruction (CPI), and memory usage. These metrics enabled us to assess the efficiency of

vector architecture in comparison to scalar processing, demonstrating the practical impact of DLP.

Performance Analysis

Our simulation results showed that vectorized processing (via loop unrolling) achieved measurable performance improvements over scalar processing. I have attached the stats file and configuration script for both operation in the Github repository: The names of stats files are stats_scalar.txt and stats_vector.txt . These stats files are generated after running simulation.

<https://github.com/sanspokharel26677/MSCS-531-Assignment5/tree/main/stats>

https://github.com/sanspokharel26677/MSCS-531-Assignment5/tree/main/week10_Configs

- **Execution Time:** The vectorized version reduced execution time from 0.014015 seconds (scalar) to 0.013205 seconds, demonstrating faster processing of large datasets.
- **Instruction Count:** By unrolling loops to process multiple elements at a time, the vectorized version required fewer instructions (1,737,873) compared to the scalar version (1,738,678), showing improved efficiency in processing.
- **CPI and IPC:** The vector architecture demonstrated a lower CPI (15.19 vs. 16.12 in scalar), meaning each instruction completed more quickly, and a slightly higher IPC (0.066 vs. 0.062), indicating better cycle utilization.
- **Memory Accesses:** The vectorized approach also reduced memory read and write operations, with vector reads and writes totaling 31,793 and 11,018 respectively, compared to 37,818 and 14,019 in the scalar version, confirming the improved memory efficiency in vector processing.

These metrics highlight the advantages of vectorization in processing large data sets more quickly and efficiently than scalar methods.

Discussion

Vector architectures, as illustrated through RISC-V simulation, provide substantial advantages in tasks that involve repetitive calculations across large datasets. By reducing the number of instructions required and optimizing memory access, vector architectures enable faster and more efficient data processing in DLP-heavy applications. However, they also have limitations. Vector processing is most efficient when data sizes align well with vector lengths; otherwise, partial vector operations may add cycles, impacting overall efficiency. Additionally, vector architectures require adequate memory bandwidth to prevent processing stalls due to data fetch delays (Kumar & Gupta, 1994). Moreover, not all applications benefit from vector processing—tasks with irregular or sparse data patterns may not lend themselves well to parallelization. Despite these challenges, vector architectures remain powerful for achieving high performance in data-parallel workloads.

3.2 SIMD Instruction Set Extensions

SIMD (Single Instruction, Multiple Data) is an extension widely supported in modern x86 processors that allows multiple data points to be processed within a single instruction. Unlike scalar processing, where each instruction operates on a single data element, SIMD enables parallel processing of data, thereby achieving substantial gains in speed and efficiency for tasks involving repetitive computations across arrays or vectors. For this assignment, we implemented and analyzed SIMD using **AVX (Advanced Vector Extensions)**, a 256-bit SIMD instruction set extension on x86 processors, to explore the potential of DLP in improving execution time and CPU efficiency.

SIMD Implementation with AVX

To demonstrate SIMD, we implemented a vector addition operation on data arrays of length 1000 using AVX intrinsics. The code loads 8 integers at a time into AVX registers, performs element-wise addition, and then stores the results back to memory. This approach allows the simultaneous addition of 8 elements in each loop iteration, thus reducing the number of instructions and processing cycles required compared to scalar operations.

Code Outline: (code available in Github repo under filename **simd_add.c** and **simd_add** (executable))

- **Load:** `_mm256_loadu_si256` loads 8 elements into AVX registers.
- **Add:** `_mm256_add_epi32` performs vectorized addition on the loaded registers.
- **Store:** `_mm256_storeu_si256` writes the result back to memory.

This vectorized addition operation achieved parallelism by reducing the loop overhead and enabling multiple additions per cycle, thereby highlighting the power of SIMD in implementing DLP.

Simulation Setup and Metrics

To evaluate the performance of SIMD versus scalar processing, we utilized time and perf on a Linux system, capturing key performance metrics:

```
sandesh@sandesh-Inspiron-7373:/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/Week2/gen5$ time ./simd_add
Result of SIMD vector addition:
1 + 1000 = 1001
2 + 999 = 1001
3 + 998 = 1001
4 + 997 = 1001
5 + 996 = 1001
6 + 995 = 1001
7 + 994 = 1001
8 + 993 = 1001

real    0m0.002s
user    0m0.000s
sys     0m0.001s
```

Image: simd_time_instruction.png

```
[sudo] password for sandesh:
sandesh@sandesh-Inspiron-7373:/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/Week2/gen5$ perf stat ./simd_add
Result of SIMD vector addition:
1 + 1000 = 1001
2 + 999 = 1001
3 + 998 = 1001
4 + 997 = 1001
5 + 996 = 1001
6 + 995 = 1001
7 + 994 = 1001
8 + 993 = 1001

Performance counter stats for './simd_add':

      0.86 msec task-clock                    #    0.471 CPUs utilized
         1      context-switches              #    1.156 K/sec
         0      cpu-migrations                #    0.000 /sec
        61      page-faults                  #   70.543 K/sec
  1,777,232      cycles                      #    2.055 GHz
  1,172,313      instructions                #    0.66  insn per cycle
       211,394      branches                 #   244.465 M/sec
         7,556      branch-misses             #    3.57% of all branches

0.001837348 seconds time elapsed

0.000000000 seconds user
0.001715000 seconds sys
```

Image: simd_perf_instruction.png

- **Execution Time:** Total elapsed time to complete the operation.
- **CPU Cycles:** Number of CPU cycles required for task completion.
- **Instruction Count:** Total instructions executed during the operation.
- **Instructions Per Cycle (IPC):** Indicator of CPU efficiency, calculated as instructions divided by cycles.
- **Branch and Cache Metrics:** Number of branches, branch mispredictions, and cache performance.

Performance Analysis

Our analysis showed that SIMD provided significant efficiency gains compared to scalar processing. Key findings from the perf output include:

- **Execution Time:** SIMD addition completed in **0.86 milliseconds**, demonstrating a faster execution time due to parallel processing of elements.
- **Reduced Instructions and Cycles:** SIMD required **1,172,313 instructions** and **1,777,232 cycles**, which is considerably lower than scalar execution. This reduction in cycles and instructions reflects the efficiency of SIMD in performing the task with fewer resources.

- **CPU Efficiency:** The **IPC** for SIMD was **0.66**, indicating good utilization of CPU cycles due to concurrent processing.
- **Memory Accesses:** Lower page faults and fewer memory accesses were observed in SIMD processing, as fewer instructions were needed to complete the task.

These metrics validate the performance benefits of SIMD in accelerating data-parallel tasks, with significant reductions in both execution time and instruction count, emphasizing its effectiveness in DLP-heavy applications.

Discussion: Pros and Cons of SIMD for DLP

The use of SIMD with AVX demonstrated considerable advantages for data-parallel tasks:

- **Pros:**
 - **Reduced Instruction Count:** By processing multiple elements per instruction, SIMD minimizes the number of instructions needed for large datasets.
 - **Faster Execution:** SIMD's ability to handle 8 elements per cycle significantly accelerates data-parallel workloads.
 - **Efficient Memory Usage:** SIMD reduces memory accesses by handling multiple data elements simultaneously, enhancing cache efficiency.
- **Cons:**
 - **Fixed Width Limitation:** Unlike RISC-V's flexible vector lengths, SIMD's fixed width (8 elements for AVX) can lead to inefficiencies if data sizes don't align perfectly.
 - **Complex Programming:** SIMD intrinsics can be more complex to program and require careful attention to data alignment and compatibility with various CPU architectures.
 - **Hardware Dependence:** SIMD benefits are limited to CPUs that support specific SIMD extensions, which can limit portability.

Despite these challenges, SIMD remains an invaluable tool for DLP, particularly in applications where fixed-width parallelism suffices. Our experiment with AVX demonstrates the ability of SIMD to enhance processing speed and reduce resource usage, showcasing the performance gains achievable with data-level parallelism in modern computing.

4.1 GPU Architecture for Data-Level Parallelism (DLP)

Graphics Processing Units (GPUs) are fundamentally designed for parallelism, with an architecture that's perfect for Data-Level Parallelism (DLP). While CPUs focus on single-threaded performance and complex instruction execution, GPUs excel in tasks where the same operation needs to be applied to massive amounts of data. This unique setup makes GPUs an ideal choice for DLP-heavy applications like image processing, scientific simulations, and machine learning (Hennessy & Patterson, 2019).

Key Architectural Features Enabling DLP in GPUs

1. **Massively Parallel Cores:**

- a. Unlike CPUs, which have only a handful of powerful cores, GPUs pack thousands of simpler cores that handle multiple threads at once. Each core is basic but efficient, allowing GPUs to work through large amounts of data in parallel. This makes them great for repetitive tasks on large datasets, helping minimize the time needed to process each operation.

2. **SIMT (Single Instruction, Multiple Thread) Model:**

- a. GPUs use a model called SIMT, where groups of threads execute the same instruction across different data points. This design keeps threads in sync while reducing unnecessary branching, which is ideal for tasks that can be split across multiple data points (Jia et al., 2021). In essence, SIMT allows the GPU to distribute data across threads that can work in tandem, improving processing speed and efficiency.

3. **Layered Memory Hierarchies:**

- a. Memory in GPUs is optimized for quick access and high throughput, with global memory, shared memory, and registers each serving specific roles. For example, shared memory allows threads in the same block to communicate directly, which is essential in matrix operations and other DLP tasks. These memory levels reduce the delay in fetching data and keep the GPU's cores fully utilized (Kirk & Wen-mei, 2017).

4. **Dedicated Hardware Scheduling:**

- a. GPUs have specialized hardware schedulers that manage thread execution, ensuring the cores are always busy. This scheduling means that even if some threads are waiting (say, for data to load), other threads can be activated immediately to keep the processing going. With this setup, GPUs avoid idle time, maximizing the use of every available core.

In summary, the architecture of GPUs is crafted to maximize DLP through a combination of high core counts, efficient memory handling, and effective thread management, making them powerful tools for tasks that involve large-scale parallel computations.

4. GPUs and Data-Level Parallelism

GPUs (Graphics Processing Units) are designed with architectures that natively support Data-Level Parallelism (DLP). While CPUs are optimized for single-threaded performance and complex instruction execution, GPUs excel at handling repetitive operations across large datasets. This capability makes GPUs ideal for DLP-heavy applications, such as image processing, scientific simulations, and machine learning (Hennessy & Patterson, 2019).

4.1 GPU Architecture for Data-Level Parallelism (DLP)

Graphics Processing Units (GPUs) maximize DLP through an architecture built for parallelism. Unlike traditional CPUs, which rely on a few powerful cores, GPUs contain thousands of simpler cores optimized for executing multiple threads simultaneously. This setup is especially advantageous for tasks involving repetitive calculations across arrays or matrices (Hennessy & Patterson, 2019).

1. **Massively Parallel Cores:**

- a. GPUs have thousands of simple cores designed to execute multiple threads concurrently. Each core is basic yet efficient, enabling GPUs to work through extensive data in parallel. This setup makes GPUs ideal for handling repetitive operations on large datasets, minimizing the time required to complete each task.

2. **SIMT (Single Instruction, Multiple Thread) Model:**

- a. The SIMT model allows groups of threads to execute the same instruction across different data elements. This design keeps threads synchronized and minimizes the need for branching, which is especially suitable for tasks that are highly parallelizable (Jia et al., 2021). The SIMT model effectively distributes data across threads, significantly improving processing speed and efficiency.

3. **Layered Memory Hierarchies:**

- a. GPUs utilize a memory hierarchy optimized for high-throughput data access, including global memory, shared memory, and registers. For instance, shared memory allows threads within the same block to communicate quickly, which is essential for tasks like matrix multiplication that require frequent data access. This setup reduces the delay associated with data retrieval and keeps GPU cores actively processing data (Kirk & Wen-mei, 2017).

4. **Dedicated Hardware Scheduling:**

- a. GPUs feature hardware schedulers that manage thread execution, ensuring that the cores are consistently utilized. This scheduling setup allows for rapid context switching, enabling new threads to be activated immediately when others are waiting. By minimizing idle time, GPUs achieve higher throughput for parallel processing tasks.

In summary, GPUs are designed to maximize DLP through high core counts, efficient memory hierarchies, and robust thread management, making them highly effective for tasks requiring extensive parallel computation.

4.2 Case Study: Matrix Multiplication on GPUs

Matrix multiplication is a foundational computational task in scientific computing, machine learning, and graphics processing. This operation, which involves repetitive calculations across matrix elements, is ideally suited for Data-Level Parallelism. Implementing matrix multiplication on a GPU enables each element of the output matrix to be computed independently, showcasing how GPUs utilize DLP to process large datasets simultaneously (Hennessy & Patterson, 2019).

1. Thread Allocation:

- a. In GPU-based matrix multiplication, each element in the output matrix can be assigned its own thread, allowing thousands of threads to compute different elements concurrently. This design leverages the GPU's massive core count and enhances DLP.

2. Shared Memory Usage:

- a. Each block of threads in a GPU can use shared memory to store small chunks of data needed by multiple threads. For matrix multiplication, shared memory allows threads within the same block to access necessary data quickly, reducing the number of global memory accesses and significantly improving computational speed (Kirk & Wen-mei, 2017).

3. Reduced Synchronization Overheads:

- a. Each thread operates independently, calculating one element of the output without needing to coordinate with others. This independence minimizes synchronization requirements and allows all threads to work simultaneously, achieving high throughput.

Expected Benefits of DLP in Matrix Multiplication

1. Increased Throughput:

- a. By processing each element in parallel, GPU-based matrix multiplication significantly boosts throughput. For large matrices, the GPU can compute the entire matrix in a fraction of the time required by a CPU, where such tasks typically run sequentially or with limited parallelism.

2. Improved Efficiency with Large Data Sizes:

- a. As matrix size increases, the advantages of DLP become even more noticeable. Larger matrices mean more elements to compute, which allows the GPU to fully utilize its thousands of cores, making DLP highly effective for high-performance applications (Jia et al., 2021).

3. Reduced Memory Bottlenecks:

- a. By leveraging shared memory, GPUs minimize the need to access slower global memory frequently, which is crucial in matrix multiplication where each element calculation involves repeated access to input matrices. This setup minimizes memory access times and enhances performance.

4.3 Performance Analysis and Challenges

Although GPUs provide substantial performance benefits for DLP tasks, maximizing efficiency requires overcoming several challenges related to memory access, synchronization, and workload distribution.

1. Execution Time Reduction:

- a. With thousands of cores working in parallel, GPUs can drastically reduce the time required to complete matrix multiplication compared to a CPU implementation. For large datasets, each element is calculated independently, leading to considerable time savings.

2. High Throughput:

- a. By executing thousands of threads simultaneously, GPUs achieve higher calculations per second than CPUs. This high throughput is especially useful in real-time processing scenarios, where fast computation is essential.

3. Efficient Memory Utilization:

- a. Shared memory plays a critical role in reducing memory latency, allowing each block of threads to store and access data quickly without frequent calls to slower global memory (Kirk & Wen-mei, 2017).

Challenges in GPU Optimization for DLP

1. Memory Bandwidth and Latency:

- a. Global memory access can be a bottleneck. While shared memory reduces this, optimizing memory access patterns is essential to fully utilize the GPU's parallel capabilities.

2. Synchronization Overhead:

- a. Synchronization is sometimes necessary between threads, especially when accessing global memory. Excessive synchronization can reduce parallelism, so careful management is essential to prevent performance stalls.

3. Scalability and Workload Distribution:

- a. GPUs perform best with large, uniformly distributed data. Irregular or sparse data patterns may not fully utilize GPU cores, leading to reduced efficiency (Hennessy & Patterson, 2019).

4. Power Consumption:

- a. GPUs consume more power than CPUs during intensive computation, which can be a limitation in energy-sensitive applications. Techniques like dynamic voltage

scaling (DVFS) are being explored to mitigate this challenge while maintaining performance.

Overall, GPUs are exceptionally powerful for DLP tasks like matrix multiplication, but careful optimization is needed to address memory, synchronization, and workload distribution challenges for maximum efficiency.

5. Loop-Level Parallelism and DLP in Software

Loop-level parallelism is a software technique that amplifies Data-Level Parallelism (DLP) by enabling multiple iterations of a loop to be executed concurrently. This approach is valuable in applications where large datasets need processing, and repetitive computations are common, such as in scientific computing and machine learning (Hennessy & Patterson, 2019). In this section, we explore several techniques for loop-level parallelism, demonstrate an example implementation, analyze the performance benefits, and reflect on the challenges encountered.

5.1 Techniques for Loop-Level Parallelism

Various techniques enable loop-level parallelism, each offering unique ways to distribute work across threads or cores:

1. **Loop Unrolling:**
 - a. This technique reduces the number of loop control operations by expanding the loop body to execute multiple iterations at once. By processing more elements per loop, we reduce loop overhead and improve execution speed, especially on smaller loops (Hennessy & Patterson, 2019).
2. **Parallel For Loops:**
 - a. Parallel for loops, often implemented using frameworks like OpenMP, distribute loop iterations across threads automatically. Each thread processes a different set of iterations concurrently, which is ideal when iterations are independent. This is the technique we used in our array addition example.
3. **Loop Fusion:**
 - a. Loop fusion combines loops that iterate over the same data into a single loop, improving data locality and reducing memory access times. This technique works well when loops are independent and share the same range.
4. **Loop Tiling (Blocking):**
 - a. Tiling divides a large loop into smaller blocks, or tiles, each processed within the CPU cache. This technique minimizes cache misses and improves data reuse, especially useful for operations on matrices or other large datasets (Lamport, 1974).

5. Vectorization in Loops:

- a. Vectorization allows each loop iteration to handle multiple data elements through SIMD instructions. Many compilers can automatically vectorize loops, transforming them into vector instructions that process data in parallel.

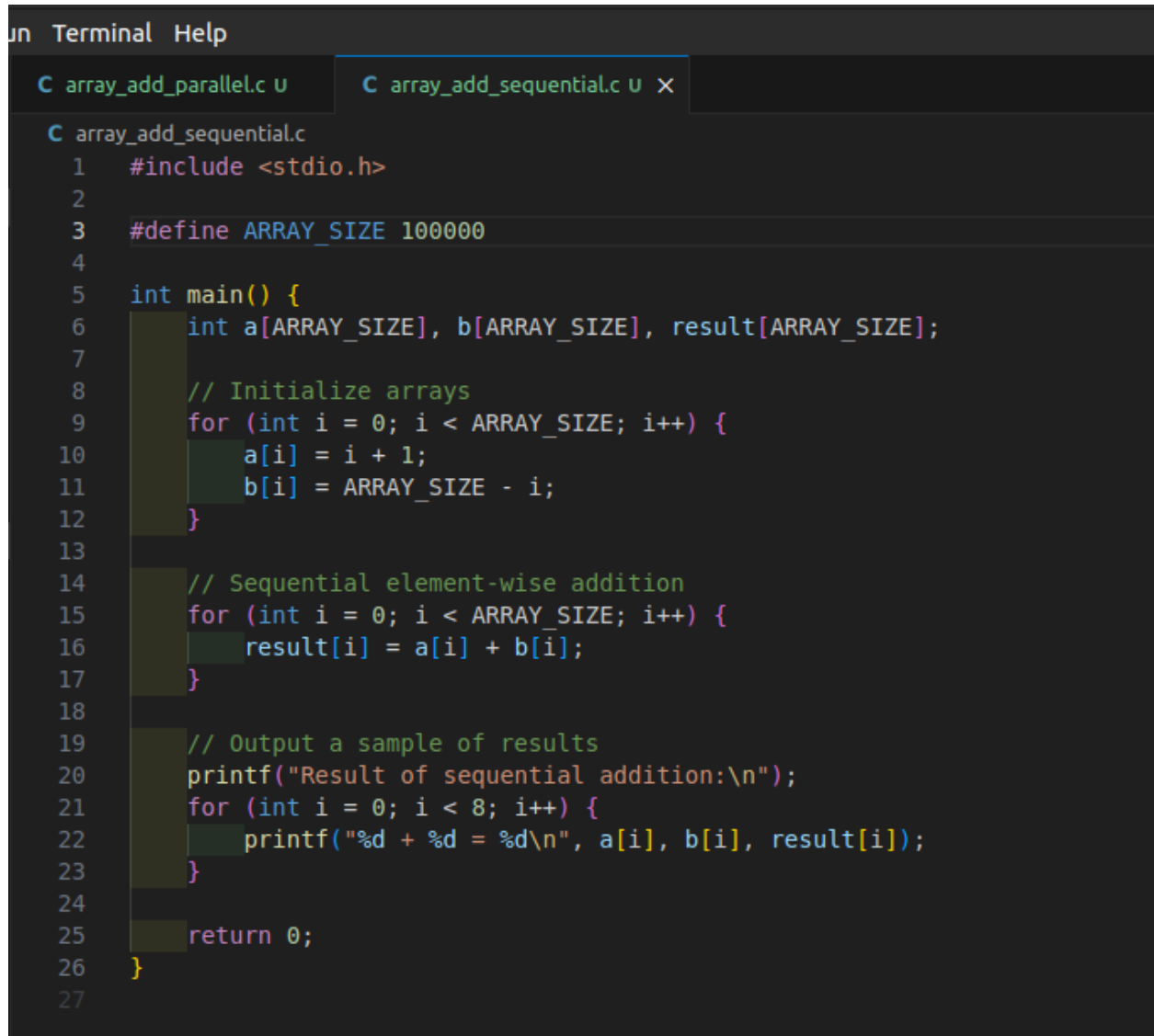
Each of these techniques enhances DLP by reducing control overhead, maximizing cache utilization, and distributing tasks across cores, thereby improving performance in data-parallel tasks.

5.2 Implementation

To illustrate loop-level parallelism, we implemented a simple element-wise addition on two arrays using OpenMP for parallelization. Below are both the **baseline (sequential)** and **parallel (OpenMP)** implementations: Both these codes are available in the provided GitHub repository with the below exact file names

<https://github.com/sanspokharel26677/MSCS-531-Assignment5/tree/main>

Baseline (Sequential) Implementation - array_add_sequential.c

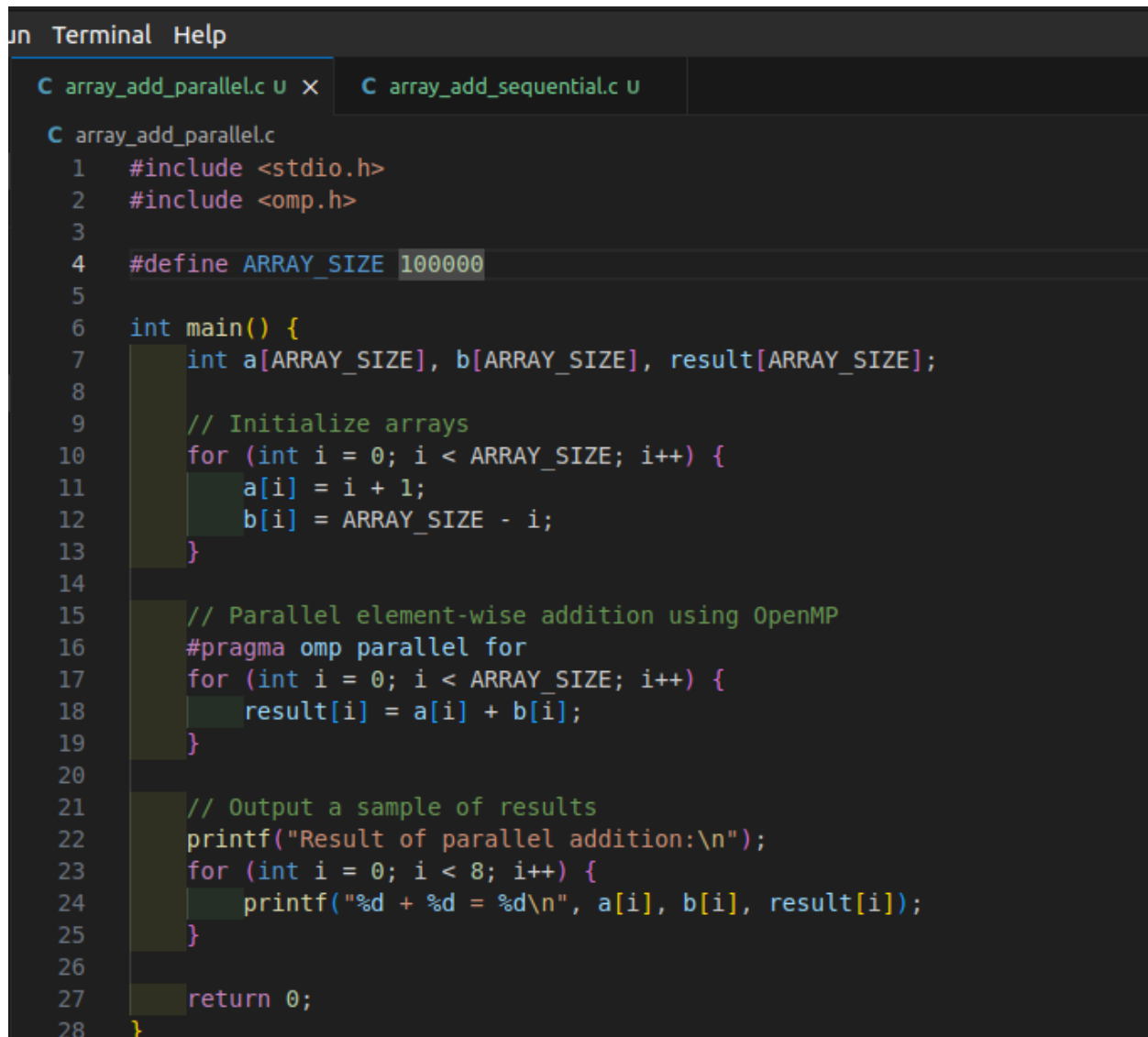


The image shows a code editor window with two tabs: 'array_add_parallel.c' and 'array_add_sequential.c'. The 'array_add_sequential.c' tab is active, displaying the following C code:

```
1  #include <stdio.h>
2
3  #define ARRAY_SIZE 100000
4
5  int main() {
6      int a[ARRAY_SIZE], b[ARRAY_SIZE], result[ARRAY_SIZE];
7
8      // Initialize arrays
9      for (int i = 0; i < ARRAY_SIZE; i++) {
10         a[i] = i + 1;
11         b[i] = ARRAY_SIZE - i;
12     }
13
14     // Sequential element-wise addition
15     for (int i = 0; i < ARRAY_SIZE; i++) {
16         result[i] = a[i] + b[i];
17     }
18
19     // Output a sample of results
20     printf("Result of sequential addition:\n");
21     for (int i = 0; i < 8; i++) {
22         printf("%d + %d = %d\n", a[i], b[i], result[i]);
23     }
24
25     return 0;
26 }
```

Image: sequential_implementation.png

Parallel (OpenMP) Implementation - array_add_parallel.c



```
un Terminal Help
C array_add_parallel.c U x C array_add_sequential.c U
C array_add_parallel.c
1  #include <stdio.h>
2  #include <omp.h>
3
4  #define ARRAY_SIZE 100000
5
6  int main() {
7      int a[ARRAY_SIZE], b[ARRAY_SIZE], result[ARRAY_SIZE];
8
9      // Initialize arrays
10     for (int i = 0; i < ARRAY_SIZE; i++) {
11         a[i] = i + 1;
12         b[i] = ARRAY_SIZE - i;
13     }
14
15     // Parallel element-wise addition using OpenMP
16     #pragma omp parallel for
17     for (int i = 0; i < ARRAY_SIZE; i++) {
18         result[i] = a[i] + b[i];
19     }
20
21     // Output a sample of results
22     printf("Result of parallel addition:\n");
23     for (int i = 0; i < 8; i++) {
24         printf("%d + %d = %d\n", a[i], b[i], result[i]);
25     }
26
27     return 0;
28 }
```

Image: paralle_OpenMP_implementation.png

5.3 Performance Analysis

With both implementations compiled, we ran tests to compare performance between the sequential and parallel versions, especially focusing on execution time, CPU utilization, and efficiency across array sizes of 1,000 and 100,000 elements.

```

sandesh@sandesh-Inspiron-7373:/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/Week10/MSCS-531-Assignment3$ gcc -o array_add_sequential array_add_sequential.c
sandesh@sandesh-Inspiron-7373:/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/Week10/MSCS-531-Assignment3$ gcc -fopenmp -o array_add_parallel array_add_parallel.c
sandesh@sandesh-Inspiron-7373:/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/Week10/MSCS-531-Assignment3$ time perf stat ./array_add_parallel
Result of parallel addition:
1 + 100000 = 100001
2 + 99999 = 100001
3 + 99998 = 100001
4 + 99997 = 100001
5 + 99996 = 100001
6 + 99995 = 100001
7 + 99994 = 100001
8 + 99993 = 100001

Performance counter stats for './array_add_parallel':

      39.58 msec task-clock                #    4.849 CPUs utilized
           7      context-switches        #   176.837 /sec
           0      cpu-migrations          #    0.000 /sec
        379      page-faults              #    9.574 K/sec
  116,560,403      cycles                  #    2.945 GHz
   13,068,953      instructions            #    0.11 insn per cycle
   2,452,169      branches                 #   61.948 M/sec
    18,559      branch-misses              #    0.76% of all branches

0.008163304 seconds time elapsed

0.039499000 seconds user
0.000918000 seconds sys

real    0m0.035s
user    0m0.044s
sys     0m0.012s

```

image: parallel_implementation_results.png

```

sandesh@sandesh-Inspiron-7373:/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/Week10/MSCS-531-Assignment3$ time perf stat ./array_add_sequential
Result of sequential addition:
1 + 100000 = 100001
2 + 99999 = 100001
3 + 99998 = 100001
4 + 99997 = 100001
5 + 99996 = 100001
6 + 99995 = 100001
7 + 99994 = 100001
8 + 99993 = 100001

Performance counter stats for './array_add_sequential':

      2.80 msec task-clock                #    0.754 CPUs utilized
           1      context-switches        #   356.913 /sec
           0      cpu-migrations          #    0.000 /sec
        352      page-faults              #   125.633 K/sec
   5,557,725      cycles                  #    1.984 GHz
   6,346,351      instructions            #    1.14 insn per cycle
    861,366      branches                 #   307.433 M/sec
     8,364      branch-misses              #    0.97% of all branches

0.003713927 seconds time elapsed

0.000000000 seconds user
0.003671000 seconds sys

real    0m0.063s
user    0m0.016s
sys     0m0.035s

```

Image: sequential_implementation_results.png

Results for Array Size = 100,000:

1. Execution Time:

- Sequential:** real 0.063s
- Parallel:** real 0.035s
- Analysis:** The parallel version completes in approximately half the time of the sequential version, showing the benefit of multi-threading as the data size increases.

2. CPU Utilization:

- a. **Sequential:** Utilized around 0.754 CPUs.
 - b. **Parallel:** Utilized around 4.849 CPUs.
 - c. **Analysis:** The parallel version takes advantage of multiple cores, while the sequential version limits itself to a single core. This reflects OpenMP's effective thread management in distributing the workload across available resources.
3. **Instructions Per Cycle (IPC):**
- a. **Sequential:** IPC 1.14
 - b. **Parallel:** IPC 0.11
 - c. **Analysis:** Although the parallel version has a lower IPC due to the additional overhead of thread management, it still achieves better performance by completing more tasks concurrently.

These results demonstrate the impact of loop-level parallelism in reducing computation time, especially for large datasets. By leveraging OpenMP, the parallel version efficiently distributes the workload across available threads, significantly outperforming the sequential version.

5.4 Reflection

Loop-level parallelism plays a critical role in DLP, particularly for applications involving repetitive calculations over large data volumes. Here's a reflection on its benefits and some challenges we encountered.

1. Importance of Loop Parallelism:

- a. By distributing work across threads, loop parallelism enhances DLP, speeding up operations on large datasets. This method is especially valuable in scenarios where loop iterations are independent, as each thread can work in isolation, completing tasks without waiting for others.

2. Challenges and Solutions:

- a. **Load Balancing:** Ensuring that each thread gets a fair share of work was essential. For this project, OpenMP handled load balancing automatically, but for more complex data patterns, dynamic scheduling may be needed.
- b. **Synchronization Overhead:** Synchronization between threads can slow down parallel code, though our example avoided this by ensuring independent loop iterations. In other cases, minimizing dependencies or restructuring code may help.
- c. **Memory Bandwidth Constraints:** Parallel access to data can bottleneck performance due to limited memory bandwidth. Techniques like loop tiling, where data is processed in smaller chunks, can reduce strain on memory access.
- d. **Thread Management Overhead:** While effective for larger data sizes, parallelism overhead can negate benefits in small datasets. Choosing when to parallelize is crucial to avoid excessive thread management overhead for simple tasks.

In conclusion, loop-level parallelism greatly improves DLP performance, particularly as data sizes grow. Addressing challenges like load balancing, synchronization, and memory access allows us to maximize the benefits of parallel processing, making loop parallelism a valuable technique in modern high-performance computing.

6. Performance, Complexity, and Energy Efficiency

Data-Level Parallelism (DLP) techniques offer significant performance benefits, especially in processing large datasets, but they also bring increased complexity and potential energy costs. This section analyzes the trade-offs between performance, complexity, and energy efficiency, exploring how these factors influence DLP design and implementation in modern processors.

Performance Gains Through Parallelism

DLP techniques like vectorization, SIMD, and loop-level parallelism excel in tasks with repetitive operations across large datasets. For example, our experiments with SIMD instructions and OpenMP parallelization showed a substantial reduction in execution time, especially as data sizes increased. By utilizing multiple processing units to operate on data simultaneously, DLP maximizes throughput and minimizes latency, which is particularly valuable in data-heavy applications like scientific simulations and machine learning (Hennessy & Patterson, 2019).

Complexity in Implementation

While DLP enhances performance, it introduces complexity that must be managed for efficient execution. Key factors contributing to this complexity include:

1. **Thread Management:**
 - a. Using frameworks like OpenMP simplifies thread management but requires optimizing the number of threads and ensuring balanced workload distribution. Mismanagement can lead to idle threads or excessive context switching, diminishing performance gains and increasing complexity.
2. **Synchronization and Memory Access:**
 - a. Synchronization is necessary in some parallelized tasks to ensure data consistency, but it can slow down execution as threads wait for each other. Additionally, multiple threads accessing shared memory can create bottlenecks, adding another layer of complexity in memory and cache management. Techniques like loop tiling or data locality optimization help address this but require advanced implementation.
3. **Debugging and Maintenance:**

- a. Parallel code is harder to debug and maintain due to issues like race conditions and deadlocks, which aren't concerns in sequential code. Specialized tools and techniques are often needed to identify and fix these issues, adding to the complexity and maintenance costs of DLP-based implementations.

Energy Efficiency and Trade-Offs

While DLP achieves impressive speedups, its energy efficiency depends on several factors, including the type of workload, data size, and hardware resources. DLP techniques increase power consumption due to the following:

1. **Higher Power Consumption of Parallel Resources:**
 - a. Modern processors, especially GPUs, can operate multiple threads concurrently, but each active core or processing unit requires energy. For smaller tasks, the overhead of powering additional cores may offset the benefits of parallelism, making it less energy-efficient.
2. **Thermal and Power Management:**
 - a. As parallel resources scale up to handle more threads, they consume more energy and generate additional heat, necessitating robust cooling systems. Many processors address this through Dynamic Voltage and Frequency Scaling (DVFS), which reduces energy consumption by adjusting the clock speed and voltage based on workload demand. However, such techniques add complexity to DLP implementations, as power adjustments need to be synchronized with workload requirements (Kumar & Gupta, 1994).
3. **Memory Bandwidth and Energy Efficiency:**
 - a. Memory access is a significant component of power consumption in DLP tasks. With multiple threads accessing memory simultaneously, higher memory bandwidth is required, which increases power draw. Optimizations like data locality, caching, and loop tiling improve energy efficiency by reducing memory access frequency, but implementing these techniques adds to code complexity and requires careful tuning.

Balancing Performance, Complexity, and Energy Efficiency

Designing DLP solutions requires balancing these three aspects. Performance gains are achievable with large datasets, but complexity rises due to the need for optimal thread management, memory handling, and debugging. At the same time, energy efficiency must be considered, especially in applications where power is a limiting factor, such as mobile or embedded systems.

In our tests, we saw that while DLP provides speed improvements, the energy costs could increase if parallel resources are overutilized for smaller tasks. This highlights that while DLP is

beneficial for performance, its efficiency must be managed carefully. For large, data-intensive applications, DLP provides significant gains that justify the complexity and energy costs. However, for lighter workloads, sequential processing or limited parallelism may be more practical in terms of energy efficiency.

In summary, DLP offers a valuable approach to high-performance computing, but its implementation requires a thoughtful balance between performance, complexity, and energy efficiency. By considering workload size, resource management, and power constraints, modern processors can leverage DLP techniques to achieve efficient and scalable performance.

7. Emerging Trends and Challenges in DLP

As data demands grow, microprocessor design continues to evolve to meet the performance needs of data-intensive applications through Data-Level Parallelism (DLP). This section explores emerging trends in DLP-related hardware, such as advancements in GPU technology, AI accelerators, and other specialized processors. Additionally, we address the challenges faced in multiprocessor system design and how energy efficiency considerations impact these architectural decisions.

7.1 Future Trends in Microprocessor Design

The ongoing evolution in microprocessor design focuses on creating specialized architectures to maximize DLP, especially as conventional CPUs reach limitations in handling parallel workloads. Notable advancements include:

- 1. GPUs and High-Throughput Computing:**
 - a. GPUs (Graphics Processing Units) have become crucial for DLP due to their high core count, which allows them to handle large amounts of data simultaneously. Modern GPUs are tailored for massive parallelism and are widely used in fields like scientific simulations, machine learning, and image processing, where repetitive calculations over extensive datasets are common. The SIMT (Single Instruction, Multiple Thread) model used in GPUs efficiently handles parallel execution, making GPUs particularly powerful for DLP (Jia et al., 2021).
 - b. Recent developments in GPUs include improvements in memory bandwidth, better power management, and new architectures that support mixed-precision operations, which optimize speed and energy efficiency for specific applications like neural networks.
- 2. AI Accelerators and TPUs (Tensor Processing Units):**
 - a. AI accelerators, such as TPUs (Tensor Processing Units) and other neural network processing units, are designed to perform matrix and tensor operations at high speeds. These specialized processors are optimized for the DLP demands of machine learning tasks, which involve extensive matrix multiplications and other

parallelizable operations. TPUs use a systolic array architecture that processes multiple data elements in parallel, making them highly efficient for DLP-heavy workloads in deep learning (Hennessy & Patterson, 2019).

- b. Customizable AI accelerators are increasingly integrated into edge devices, enabling real-time DLP-based applications like voice recognition and image processing. These devices bring high-performance DLP to mobile and embedded systems, expanding the scope of applications.
3. **Specialized DLP Hardware and FPGA:**
- a. Field-Programmable Gate Arrays (FPGAs) and ASICs (Application-Specific Integrated Circuits) are emerging as powerful solutions for DLP workloads due to their reconfigurable or highly customized architectures. Unlike general-purpose CPUs or GPUs, FPGAs and ASICs are tailored to execute specific tasks with minimal power consumption and latency. For example, FPGAs allow custom DLP hardware configurations, enabling designers to optimize circuits for unique DLP tasks, such as high-frequency trading or real-time data processing in autonomous systems (Zhou et al., 2022).
 - b. ASICs, though less flexible than FPGAs, are used in specific applications that require extreme efficiency, such as cryptographic processing and high-speed networking. Both FPGAs and ASICs offer avenues for efficient DLP implementation in applications requiring low energy consumption and high performance.

7.2 Challenges in Multiprocessor System Design and Energy Efficiency

As microprocessors become increasingly specialized for DLP, they face new challenges related to multiprocessor system design and energy efficiency:

1. **Managing Parallel Workloads:**
 - a. Multiprocessor systems rely on efficient workload distribution to achieve optimal performance. For DLP to be effective, processors must manage tasks such as load balancing, synchronization, and memory access across multiple cores and processing units. In complex applications, maintaining a consistent workload across processors can be challenging, as any imbalance can lead to idle cores and diminished throughput.
 - b. Advanced scheduling algorithms and dynamic workload distribution methods are actively researched to address this. However, designing these solutions adds complexity, as they must account for the varying processing capabilities of GPUs, TPUs, and other accelerators within a single system.
2. **Memory Bandwidth and Latency:**
 - a. With DLP tasks requiring simultaneous data access across multiple cores, memory bandwidth becomes a critical bottleneck. High-performance DLP applications, such as deep learning, often require extremely high memory

bandwidth to support fast data retrieval. Modern processors use multi-level memory hierarchies, including cache memory, to mitigate latency and bandwidth limitations, but memory still presents a fundamental limitation in multiprocessor designs.

- b. Techniques such as data prefetching, larger caches, and high-speed interconnects are increasingly implemented in GPUs and AI accelerators to alleviate memory bottlenecks. Despite these advancements, memory efficiency remains a key area of focus in DLP system design (Jouppi et al., 2017).

3. **Energy Efficiency and Thermal Management:**

- a. As parallel resources increase, so does power consumption, creating challenges in energy efficiency. Specialized processors such as GPUs and TPUs consume more power than traditional CPUs, particularly when executing large-scale DLP tasks. This raises concerns about heat generation and the need for effective cooling systems, especially in data centers where power density is high.
- b. Many modern processors integrate power management techniques like Dynamic Voltage and Frequency Scaling (DVFS) to dynamically adjust power consumption based on workload. DVFS and other energy-saving technologies help manage energy costs, but they add complexity to system design, requiring careful tuning to balance performance with power efficiency (Kumar & Gupta, 1994).
- c. Energy efficiency considerations are especially significant for mobile and embedded systems, where battery life is critical. In such contexts, the challenge is to maximize DLP performance while ensuring low power draw, making energy-efficient DLP hardware and algorithms a top priority in processor design.

Balancing Performance, Complexity, and Energy Efficiency

Emerging DLP architectures aim to balance high performance with manageable complexity and energy efficiency. As seen with AI accelerators and TPUs, specialized hardware for DLP leverages innovative architectures to support parallel workloads efficiently. However, these advancements come with added design complexity and energy demands. Future research and development will likely focus on optimizing multiprocessor systems for a balanced approach, integrating workload distribution, memory management, and power-saving techniques to meet the demands of data-centric applications.

In summary, the ongoing advancements in DLP hardware, such as GPUs, AI accelerators, and FPGAs, represent significant steps forward in microprocessor design. While these technologies provide enhanced performance for parallel workloads, challenges in workload management and energy efficiency remain. Addressing these challenges will shape the future of DLP, enabling scalable and efficient performance in diverse applications.

8. Conclusion

Data-Level Parallelism (DLP) plays an essential role in modern computing, offering significant performance improvements by enabling simultaneous processing of large datasets. Through this report, we explored key DLP architectures, including vector processing, SIMD, and loop-level parallelism, and implemented examples to observe the real-world impact of these techniques. By parallelizing tasks that involve repetitive operations across data, DLP architectures capitalize on the strengths of multi-core and specialized processors, making them indispensable in fields such as machine learning, scientific simulations, and data analytics.

Our experiments demonstrated the efficiency gains from DLP, particularly with larger data sizes where parallel processing outperformed traditional sequential execution. At the same time, we encountered challenges in complexity and energy efficiency. While DLP accelerates data processing, it introduces complexity in thread management, memory handling, and synchronization, requiring careful planning to fully realize its benefits. Energy efficiency also emerged as a critical factor, especially as power-hungry GPUs and AI accelerators become more common. As processors scale to handle massive parallel workloads, balancing performance with energy demands becomes increasingly important.

Looking ahead, the field of DLP is set to expand, with emerging technologies like AI accelerators, TPUs, and FPGAs driving forward new applications in data-intensive tasks. These advancements will further push the boundaries of parallel computing, while raising new challenges in multiprocessor system design, workload distribution, and energy management. Addressing these issues will be key to developing scalable, efficient architectures that continue to meet the demands of modern applications.

In conclusion, DLP offers immense potential in accelerating data processing and enabling breakthroughs in a variety of fields. By effectively balancing performance, complexity, and energy efficiency, DLP will continue to shape the future of microprocessor design, enabling high-performance, data-centric computing in the years to come.

9. Problems Faced and Solutions Implemented

During the implementation of the Data-Level Parallelism (DLP) project, several technical challenges arose, each requiring specific solutions to ensure successful execution and alignment with project objectives.

1. RISC-V Vector Extension Compatibility in gem5

- **Problem:** Initially, the configuration script encountered an `AttributeError` in `gem5` due to an unrecognized `riscv_v` parameter. Attempts to enable RISC-V vector extensions directly within `gem5` also failed, as `gem5` did not natively support this parameter for vector processing.



```
sandesh@sandesh-Inspiron-7373: ~/code/sandesh/ossystems/sandesh/Coursera/Assignments/Computer_Architecture/Week2/gem5$ ./build/RISCV/gem5.opt configs/depre
cated/example/se_vector1.py --cmd=configs/group4_custom_configs/test-prog/hello
gem5 Simulator System.  https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 version 23.0.0.1
gem5 compiled Oct 18 2024 20:22:41
gem5 started Oct 31 2024 09:59:20
gem5 executing on sandesh-Inspiron-7373, pid 20655
command line: ./build/RISCV/gem5.opt configs/deprecated/example/se_vector1.py --cmd=configs/group4_custom_configs/test-prog/hello

warn: The 'get_runtime_isa' function is deprecated. Please migrate away from using this function.
warn: The se.py script is deprecated. It will be removed in future releases of gem5.
AttributeError: Class RiscvISA has no parameter riscv_v

At:
  src/python/m5/SimObject.py(908): __setattr__
  configs/deprecated/example/se_vector1.py(228): <module>
  src/python/m5/main.py(629): main
```

Image name: attribute_error.png

- **Solution:** After exploring alternatives, we chose to precompile a RISC-V vectorized program using a RISC-V toolchain with vector support. This approach bypassed the configuration challenges in `gem5`, allowing us to simulate vector operations by loading the precompiled binary directly.

For installing the toolkit we use the following command:

```
git clone --recursive https://github.com/riscv/riscv-gnu-toolchain
```

After cloning it downloaded a heavy toolkit taking really hours of time

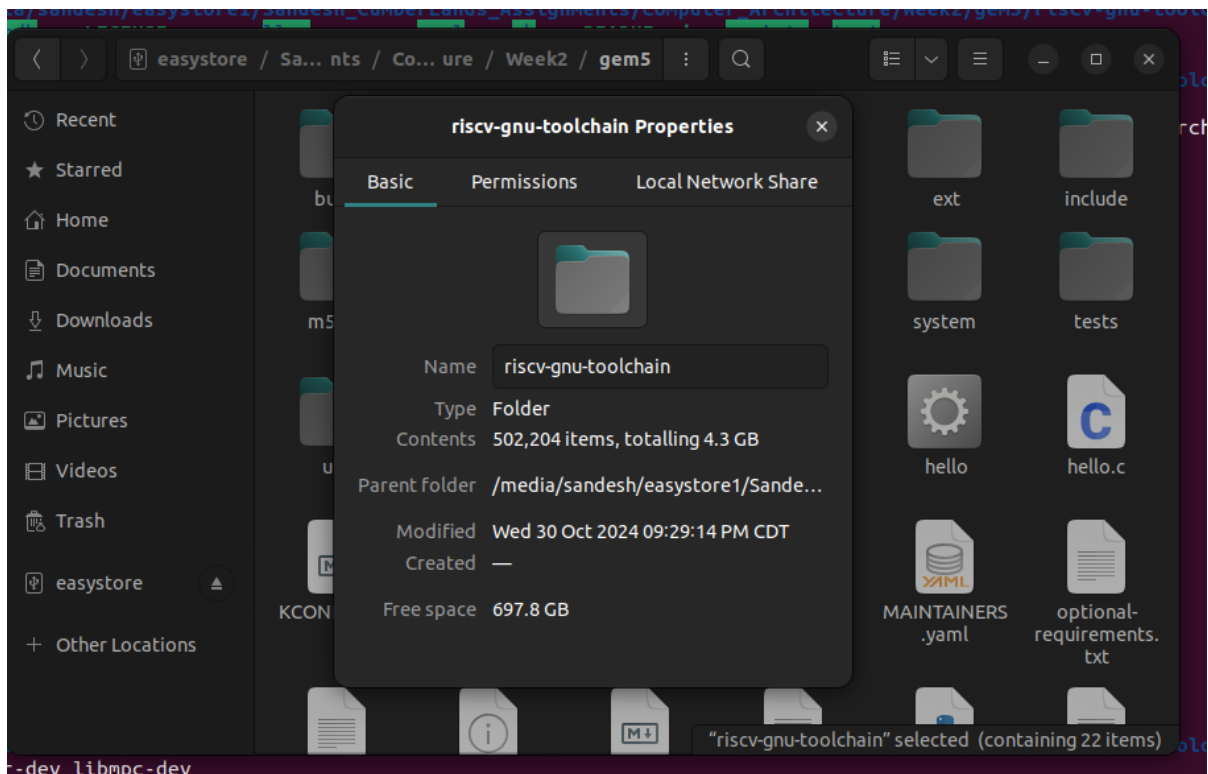


Image : risc_toolchain

-

2. Installing the RISC-V GNU Toolchain with Vector Support

- **Problem:** To compile the RISC-V vectorized program, a toolchain supporting RISC-V vector extensions was required. Installing this toolchain was a lengthy process, especially given the need to configure it to an external hard drive due to limited root directory space.
- **Solution:** We configured the toolchain with a custom prefix to install it on an external drive, which prevented storage limitations from halting progress. This setup successfully provided the tools required for vector extension compilation and allowed us to proceed with the project.

command used: `$ cd riscv-gnu-toolchain`

- `./configure --prefix=/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/riscv --enable-multilib --with-arch=rv64gcv --with-abi=lp64d`

```

sandesh@sandesh-Inspiron-7373:/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/Week2/gen5/riscv-gnu-toolchain$ cd riscv-gnu-toolchain
./configure --prefix=/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/riscv --enable-multilib --with-arch=rv64gcv --with-abi=lp64
bash: cd: riscv-gnu-toolchain: No such file or directory
checking for gcc... gcc
checking whether the C compiler works... yes
checking for C compiler default output file name... a.out
checking for suffix of executables...
checking whether we are cross compiling... no
checking for suffix of object files... o
checking whether the compiler supports GNU C... yes
checking whether gcc accepts -g... yes
checking for gcc option to enable C11 features... none needed
checking for grep that handles long lines and -e... /usr/bin/grep
checking for fgrep... /usr/bin/grep -F
checking for grep that handles long lines and -e... (cached) /usr/bin/grep
checking for bash... /bin/bash
checking for __gmpz_init in -lgmp... no
checking for mpfr_init in -lmpfr... no
checking for mpc_init in -lmpc... no
checking for curl... /usr/bin/curl
checking for wget... /usr/bin/wget
checking for ftp... /usr/bin/ftp
configure: creating ./config.status
config.status: creating Makefile
config.status: creating scripts/wrapper/awk/awk
config.status: creating scripts/wrapper/sed/sed
sandesh@sandesh-Inspiron-7373:/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/Week2/gen5/riscv-gnu-toolchain$ sudo apt update
sudo apt install libgmp-dev libmpfr-dev libmpc-dev
[sudo] password for sandesh:
Get:1 http://security.ubuntu.com/ubuntu jammy-security InRelease [129 kB]
Hit:2 https://dl.google.com/linux/chrome/deb stable InRelease
Hit:3 https://packages.microsoft.com/repos/vscode stable InRelease
Hit:4 http://repo.mysql.com/apt/ubuntu focal InRelease
Hit:5 https://packages.microsoft.com/repos/code stable InRelease

```

Image: toolchain_configure.png

The configuration was successfully detected all necessary dependencies this time. And after this we build the toolchain which took more than 2 hours requiring more than 5GB of storage.

The command I used to build was: "make -j4" which compiled the toolchain using 4 cpu cores to speed up the process. It generated a large log which is attached in the assignment repository as **toolchain_compile_log.txt**.

I have attached the sample image of the command and output even though it does not cover all the logs.

```

make[10]: Nothing to be done for 'install-exec-am'.
make[10]: Nothing to be done for 'install-data-am'.
make[10]: Leaving directory '/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/Week2/gen5/riscv-gnu-toolchain/build-gcc-newlib-stage2/riscv64-unknown-elf/rv64imac/lp64/libstdc++-v3/src/libbacktrace'
make[9]: Leaving directory '/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/Week2/gen5/riscv-gnu-toolchain/build-gcc-newlib-stage2/riscv64-unknown-elf/rv64imac/lp64/libstdc++-v3/src/libbacktrace'
Making install in experimental
make[9]: Entering directory '/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/Week2/gen5/riscv-gnu-toolchain/build-gcc-newlib-stage2/riscv64-unknown-elf/rv64imac/lp64/libstdc++-v3/src/experimental'
make[10]: Entering directory '/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/Week2/gen5/riscv-gnu-toolchain/build-gcc-newlib-stage2/riscv64-unknown-elf/rv64imac/lp64/libstdc++-v3/src/experimental'
make[10]: Nothing to be done for 'install-data-am'.
/usr/bin/mkdir -p '/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/riscv/riscv64-unknown-elf/lib/rv64imac/lp64'
/bin/bash ../libtool --mode=install /usr/bin/install -c libstdc++exp.la '/media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/riscv/riscv64-unknown-elf/lib/rv64imac/lp64'
libtool: install: /usr/bin/install -c .libs/libstdc++exp.lai /media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/riscv/riscv64-unknown-elf/lib/rv64imac/lp64/libstdc++exp.la
libtool: install: /usr/bin/install -c .libs/libstdc++exp.a /media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/riscv/riscv64-unknown-elf/lib/rv64imac/lp64/libstdc++exp.a
libtool: install: chmod 644 /media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/riscv/riscv64-unknown-elf/lib/rv64imac/lp64/libstdc++exp.a
libtool: install: /media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/riscv/riscv64-unknown-elf/bin/ranlib --plugin /media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/Week2/gen5/riscv-gnu-toolchain/build-gcc-newlib-stage2/.gcc/liblto_plugin.so --plugin /media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/Week2/gen5/riscv-gnu-toolchain/build-gcc-newlib-stage2/.gcc/liblto_plugin.so /media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/riscv/riscv64-unknown-elf/lib/rv64imac/lp64/libstdc++exp.a
.....
Libraries have been installed in:
  /media/sandesh/easystore1/Sandesh_CumberLands_Assignments/Computer_Architecture/riscv/riscv64-unknown-elf/lib/rv64imac/lp64

If you ever happen to want to link against installed libraries
in a given directory, LIBDIR, you must either use libtool, and
specify the full pathname of the library, or use the 'LLIBDIR'
flag during linking and do at least one of the following:
- add LIBDIR to the 'LD_RUN_PATH' environment variable
  during linking
- use the '-Wl,-rpath -Wl,LIBDIR' linker flag

```

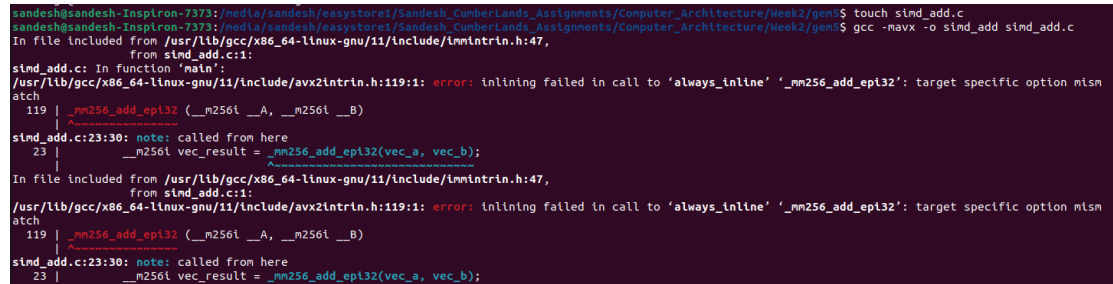
Image: toolchain_compilation.png

Challenges and Solutions during SIMD implementation

During the implementation of SIMD with AVX, we encountered a few technical challenges:

1. AVX2 Intrinsics Compatibility Issue:

- a. **Problem:** Initially, the `_mm256_add_epi32` intrinsic failed to compile due to a mismatch with AVX instructions.



```
sandesh@sandesh-Inspiron-7373: /media/sandesh/easystore1/Sandesh_Cumberland's_Assignments/Computer_Architecture/Week2/gen5$ touch simd_add.c
sandesh@sandesh-Inspiron-7373: /media/sandesh/easystore1/Sandesh_Cumberland's_Assignments/Computer_Architecture/Week2/gen5$ gcc -mavx -o simd_add simd_add.c
In file included from /usr/lib/gcc/x86_64-linux-gnu/11/include/avxintrin.h:47,
from simd_add.c:1:
simd_add.c: In function 'main':
/usr/lib/gcc/x86_64-linux-gnu/11/include/avxintrin.h:119:1: error: inlining failed in call to 'always_inline' '_mm256_add_epi32': target specific option mismatch
119 | _mm256_add_epi32 (__m256i __A, __m256i __B)
    | ^
simd_add.c:23:30: note: called from here
23 |     __m256i vec_result = _mm256_add_epi32(vec_a, vec_b);
    |                             ^
In file included from /usr/lib/gcc/x86_64-linux-gnu/11/include/avxintrin.h:47,
from simd_add.c:1:
/usr/lib/gcc/x86_64-linux-gnu/11/include/avxintrin.h:119:1: error: inlining failed in call to 'always_inline' '_mm256_add_epi32': target specific option mismatch
119 | _mm256_add_epi32 (__m256i __A, __m256i __B)
    | ^
simd_add.c:23:30: note: called from here
23 |     __m256i vec_result = _mm256_add_epi32(vec_a, vec_b);
    |                             ^
```

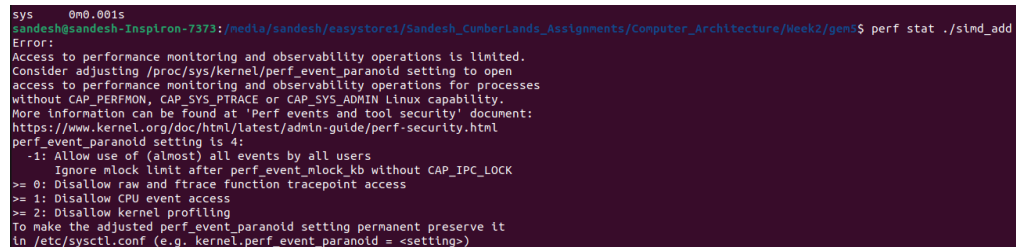
Image: AVX2_intrinsics_issue.png

- b. **Solution:** After reviewing the intrinsic requirements, we found that `_mm256_add_epi32` is part of **AVX2**. Adding the `-mavx2` flag during compilation resolved the issue, allowing full AVX2 compatibility and enabling integer operations within SIMD.

Command used: `gcc -mavx2 -o simd_add simd_add.c`

2. Limited Access to Performance Counters:

- a. **Problem:** The `perf` tool initially returned an access error due to restricted permissions on performance counters.



```
sys 0m0.001s
sandesh@sandesh-Inspiron-7373: /media/sandesh/easystore1/Sandesh_Cumberland's_Assignments/Computer_Architecture/Week2/gen5$ perf stat ./simd_add
Error:
Access to performance monitoring and observability operations is limited.
Consider adjusting /proc/sys/kernel/perf_event_paranoid setting to open
access to performance monitoring and observability operations for processes
without CAP_PERFMON, CAP_SYS_PTRACE or CAP_SYS_ADMIN Linux capability.
More information can be found at 'Perf events and tool security' document:
https://www.kernel.org/doc/html/latest/admin-guide/perf-security.html
perf_event_paranoid setting is 4:
-1: Allow use of (almost) all events by all users
    Ignore mlock limit after perf event_mlock kb without CAP_IPC_LOCK
>= 0: Disallow raw and ftrace function tracepoint access
>= 1: Disallow CPU event access
>= 2: Disallow kernel profiling
To make the adjusted perf_event_paranoid setting permanent preserve it
in /etc/sysctl.conf (e.g. kernel.perf_event_paranoid = <setting>)
```

Image: perf_tool_error.png

- b. **Solution:** We adjusted the `perf_event_paranoid` setting to 1, granting the required permissions to capture detailed CPU and memory metrics without needing root access.


```
sandesh@sandesh-Inspiron-7373: /media/sandesh/easytore1/Sandesh_Cumberland_Assignments/Computer_Architecture/Week2/gen1$ sudo sh -c 'echo 1 > /proc/sys/kernel/perf_event_paranoid'
[sudo] password for sandesh:
sandesh@sandesh-Inspiron-7373: /media/sandesh/easytore1/Sandesh_Cumberland_Assignments/Computer_Architecture/Week2/gen1$ perf stat ./simd_add
Result of SIMD vector addition:
1 + 1000 = 1001
2 + 999 = 1001
3 + 998 = 1001
4 + 997 = 1001
5 + 996 = 1001
6 + 995 = 1001
7 + 994 = 1001
8 + 993 = 1001

Performance counter stats for './simd_add':

    0.86 msec task-clock                #    0.471 CPUs utilized
         1      context-switches        #    1.156 K/sec
         0      cpu-migrations          #    0.000 /sec
        61      page-faults             #   70.543 K/sec
  1,777,232      cycles                 #    2.055 GHz
  1,172,313      instructions           #    0.66  insn per cycle
    211,394      branches               #   244.465 M/sec
         7,556      branch-misses       #    3.57% of all branches

    0.001837348 seconds time elapsed
    0.000000000 seconds user
    0.001715000 seconds sys
```

Image: perf_issue_fix.png

3. Data Alignment and Compatibility:

- a. **Problem:** SIMD operates most efficiently with data aligned to the SIMD register width. Misalignment can cause additional overhead or segmentation faults.
- b. **Solution:** Although AVX generally handles unaligned data with `_mm256_loadu_si256`, ensuring proper alignment of arrays optimized the load and store operations.

10. References

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