AI-Assisted Dynamic Power Estimation of an 8-bit ALU

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Abstract

This project presents an AI-assisted approach for estimating the dynamic power of an 8-bit Arithmetic Logic Unit (ALU) using real switching activity obtained from Verilog simulation. Switching data is extracted using Xilinx Vivado and processed using Python-based Machine Learning models. Linear Regression and Random Forest algorithms are trained to predict dynamic power. The results demonstrate high prediction accuracy at the RTL level.

1 Introduction

Power dissipation has become a primary design constraint in modern VLSI systems. Dynamic power dominates total CMOS power consumption and depends mainly on switching activity, supply voltage, and clock frequency. Traditional post-layout power estimation is accurate but time-consuming. This project proposes a fast and accurate AI-based method for dynamic power estimation at the RTL level.

2 Objectives

- Design and verify an 8-bit ALU using Verilog HDL.
- Extract real switching activity from RTL simulation.
- Generate a power dataset using the dynamic power equation.
- Train ML models for power estimation.
- Visualize and validate prediction accuracy.

3 Dynamic Power Model

Dynamic power in CMOS circuits is given by:

$$P_{dyn} \approx C \times V^2 \times f \times Activity \tag{1}$$

where C is capacitance, V is supply voltage, f is frequency and Activity is switching probability.

4 System Overview

The proposed system consists of RTL design, activity extraction, ML training and visualization.

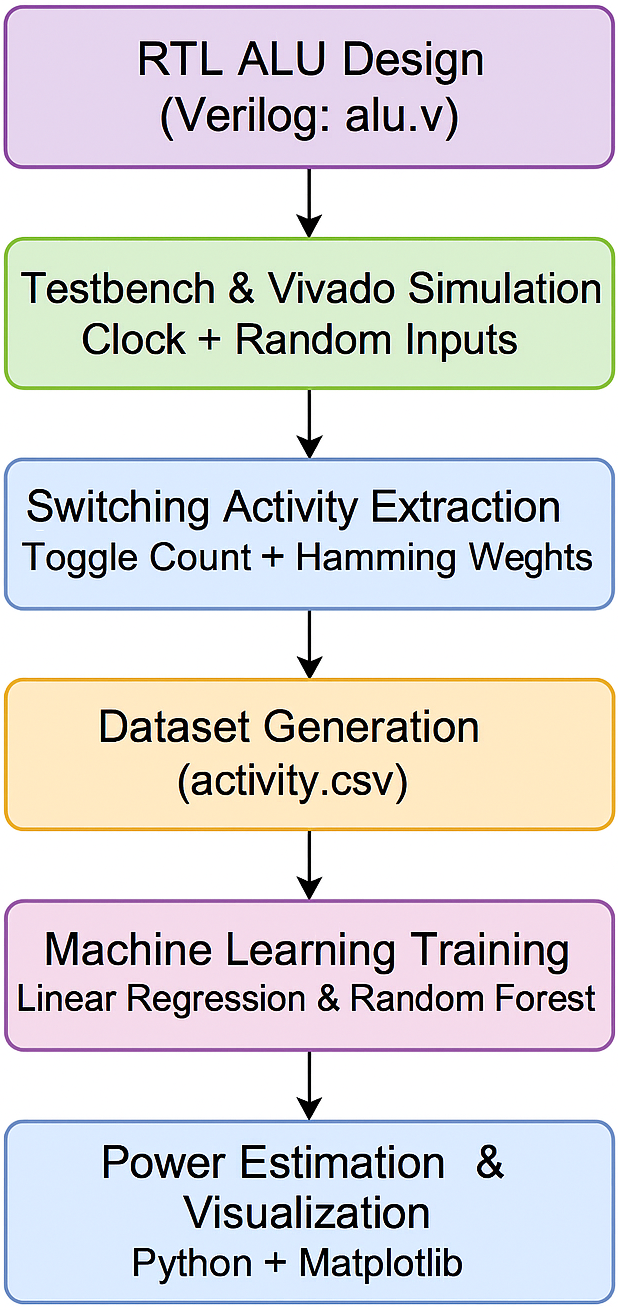

Figure 1: Overall System Block Diagram

5 RTL Design of 8-bit ALU

An 8-bit ALU was designed in Verilog to perform arithmetic and logical operations such as addition, subtraction, AND, OR and XOR.

6 Testbench and Simulation

A clocked random testbench was used for verification. The simulation was carried out in Xilinx Vivado. Output toggles and Hamming weights were logged per cycle into `activity.csv`.

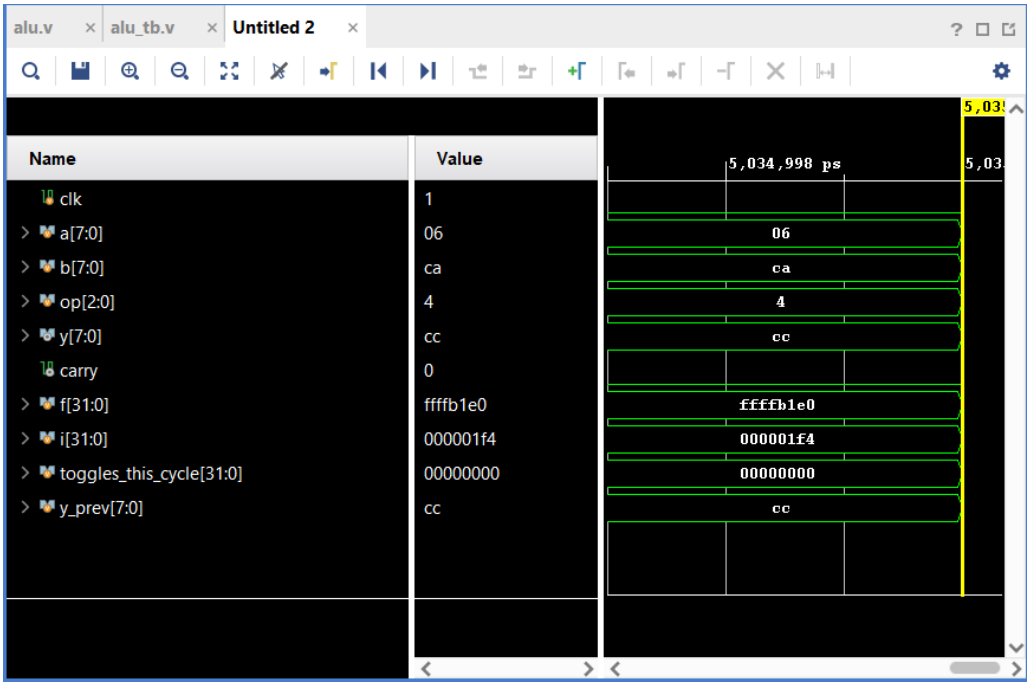

Figure 2: Vivado Simulation Waveform of 8-bit ALU

7 Dataset Generation

Using the extracted activity features, a synthetic but realistic power dataset was generated using the CMOS dynamic power equation with added noise.

8 Machine Learning Methodology

8.1 Feature Engineering

Features include input operands, output value, toggle count, Hamming weights and opcode encoding.

8.2 Model Training

The dataset was split into 80% training and 20% testing. Linear Regression and Random Forest models were trained.

8.3 Evaluation Metrics

Models were evaluated using R^2 Score and Mean Squared Error (MSE).

9 Results and Visualization

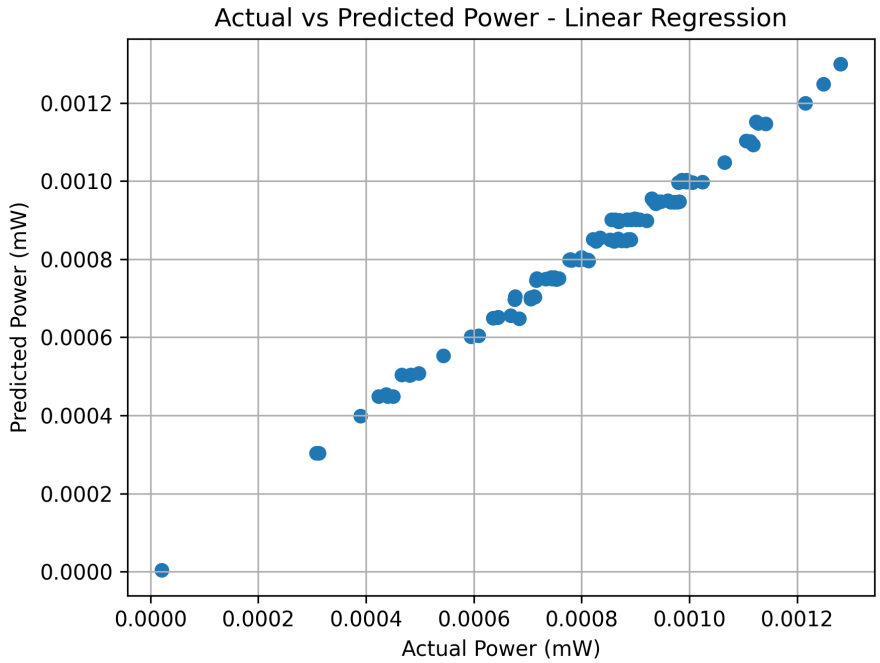

Figure 3: Actual vs Predicted Power using Linear Regression

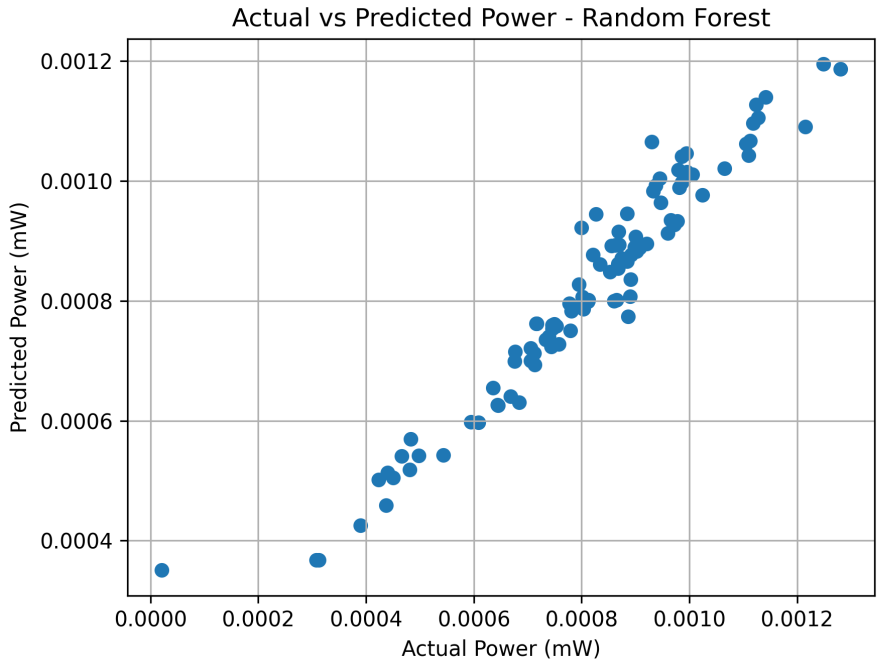

Figure 4: Actual vs Predicted Power using Random Forest

The Random Forest model achieved higher accuracy compared to Linear Regression, proving better suitability for non-linear power behavior.

10 Applications

- Early-stage power estimation
- AI-assisted low-power VLSI design
- RTL-level design optimization
- Academic research

11 Limitations

The current model uses synthetic power values and is limited to an 8-bit ALU only.

12 Future Scope

This framework can be extended to larger datapaths and real post-synthesis power data.

13 Conclusion

This project proves that Machine Learning can effectively estimate dynamic power at the RTL level using switching activity. The proposed AI-assisted framework enables fast and accurate power-aware VLSI design.

14 References

1. Weste & Harris, *CMOS VLSI Design*.
2. Xilinx Vivado User Guide.
3. Scikit-learn Documentation.