BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
WORK INTEGRATED LEARNING PROGRAMMES

COURSE HANDOUT

Part A: Content Design

Course Title	Computer Organization and Software Systems
Course No(s)	SS ZG516
Credit Units	5 (1 + 2 + 2) Unit split between Class Hours + Lab/Design/Fieldwork + Student preparation respectively; each unit translates to 32 hours
Course Author	Lucy J Gudino / Chandra Shekhar
Version No	1.0
Date	

Course Objectives

No	Course Objective
CO1	Introduce students to systems aspects (i.e. Computer Organization and Operating Systems) involved in software development
CO2	Equip the student to understand the computer architectural and operating systems related issues that affect the performance and nature of a software
CO3	To prepare students to be in a position to evaluate/correlate high level software performance based on its system level features (i.e. architectural and operating systems)

Text Book(s)

T1	Stallings William, Computer Organization & Architecture, Pearson Education, 9th Ed. 2013
T2	A Silberschatz, Abraham and others, Operating Systems Concepts, Wiley Student Edition, 8th Edition

Reference Book(s) & other resources

R1	**Patterson, David A & J L Hennenssy, Computer Architecture, A Quantitative Approach, Elsevier, 4th Ed.**
R2	Ghosal, Computer Organization and Architecture: From 8085 to core2Duo & Beyond (For JNTUK), Pearson Education, 2011 (Pearson Online)

R3	Tanenbaum, Modern Operating Systems: Pearson New International Edition, Pearson Education, 2013 (Pearson Online)
R4	Stallings, Operating Systems: Internals and Design Principles : International Edition, Pearson Education, 2013 (Pearson Online)

Modular Content Structure

1. **Computer System Components and Interconnections – T1 and R1**
   - 1.1. Organization and Architecture -**T1(Chpt1) , R1(Chpt1)**
   - 1.2. Structure and Functions of a computer system-**T1(Chpt1)**
   - 1.3. Computer Components **– T1(Chpt3)**
   - 1.4. Computer Functions
     - 1.4.1. Basic Instruction cycle state diagram **–T1(Chpt3)**
     - 1.4.2. Interrupts **– T1(Chpt3)**
     - 1.4.3. Instruction cycle state diagram with interrupts**- T1(Chpt3)**
     - 1.4.4. Interconnection Structures **- T1(Chpt3)**
     - 1.4.5. Bus Interconnection **- T1(Chpt3)**
   - 1.5. Performance Assessment **T1(Chpt2) and R1(Chpt1)**
     - 1.5.1. MIPS Rate **- T1(Chpt2) and R1(Chpt1)**
     - 1.5.2. Amdahl's Law**- T1(Chpt2) and R1(Chpt1)**

2. **Memory Organization – T1,R1**
   - 2.1. Computer Memory System Overview **-T1(Chpt4)**
     - 2.1.1. Characteristics of Memory Systems**-T1(Chpt4)**
     - 2.1.2. The Memory Hierarchy**-T1(Chpt4)**
   - 2.2. Cache Memory Principles**-T1(Chpt4)**
   - 2.3. Cache to Main Memory Mapping Functions: Direct, Associative, and Set Associative**-T1(Chpt4)**
   - 2.4. Replacement Algorithms**-T1(Chpt4)**
   - 2.5. Write Policy**-T1(Chpt4)**
   - 2.6. Multi-cache system**-T1(Chpt4)**
   - 2.7. Six Basic Cache optimisation techniques **– R1(Appendix C3)**

3. **Input/Output Organization- T1**
   - 3.1. I/O Modules **- T1(Chpt7)**
   - 3.2. Data Transfer Schemes **- T1(Chpt7)**
     - 3.2.1. Programmed I/O**- T1(Chpt7)**
     - 3.2.2. Interrupt-Driven I/O**- T1(Chpt7)**
     - 3.2.3. Direct Memory Access**- T1(Chpt7)**

4. **Instruction Set Architecture (x86 as an example) - T1,R1**
   - 4.1. Instruction Set: Characteristics and Functions **- T1(Chpt12)**
     - 4.1.1. Machine Instruction Characteristics**- T1(Chpt12)**
     - 4.1.2. Types of Operands (Intel x86 Data Types as an example) **- T1(Chpt12)**
     - 4.1.3. Types of Operations (Intel x86 Operation Types as an example) **- T1(Chpt12)**
   - 4.2. Instruction Set: Addressing Modes and Formats**- T1(Chpt13)**
     - 4.2.1. Addressing Modes (x86 Addressing Modes as an example) **- T1(Chpt13)**
     - 4.2.2. Instruction Formats (x86 Instruction Formats as an example) **- T1(Chpt13)**
   - 4.3 Instruction Pipeline **- T1(Chpt14), R1(Chpt2)**
     - 4.3.1 : Resource Hazard**- T1(Chpt14), R1(Chpt2)**
     - 4.3.2 : Data Hazard**- T1(Chpt14), R1(Chpt2)**

4.3.3: Control Hazard**- T1(Chpt14), R1(Chpt2)**

4.4 CISC Vs RISC- **T1 (Chpt15)**

5. Control Unit Operation

5.1. Hardwired Control Unit Implementation-

5.2. Micro programmed Control Unit Implementation-

6. Operating System Structure

6.1. Introduction to Operating System

6.2. Structure of a Operating System (Linux as an example OS)

6.3. Operating System Services

6.4. System Calls

7. Process Management

7.1. Concept of Process

7.2. Process State Diagram

7.3. Operations on Processes

7.4. Inter-process communications with examples

7.5. Process vs. Threads

7.6. Multithreading Models

7.7. Process Scheduling criteria

7.8. Process Scheduling Algorithms -FCFS, SJF, Priority, RR, Multilevel Queue, Multilevel Feedback Queue

8. Process Coordination

8.1. The Critical section problem

8.2. Peterson's Solution

8.3. Synchronization Hardware

8.4. Semaphores

8.5. Deadlock: System Model

8.6. Deadlock Characterization

8.7. Methods of Handling Deadlocks

8.7.1. Deadlock Prevention

8.7.2. Deadlock Avoidance: Banker's Algorithm

8.7.3. Deadlock Detection

8.7.4. Recovery from Deadlock

9. Memory Management

9.1. Memory-Management Strategies

9.2. Swapping

9.3. Contiguous memory Allocation

9.4. Paging

9.5. Segmentation

9.6. Virtual-Memory Management

9.7. Demand Paging

9.8. Page Replacement Algorithms: FIFO, Optimal, LRU, LFU

9.9. Thrashing

10. File System

10.1. File Concept

10.2. Access Methods

10.3. Directory Structure

10.4. File System Mounting

10.5. File System Structure

10.6. File System Implementation

10.7. Directory Implementation

Learning Outcomes:

No	Learning Outcomes
LO1	To **apply** the knowledge of performance metrics to find the performance of systems.
LO2	To **Investigate** high performance architecture design
LO3	To **Examine** different computer architectures and hardware
LO4	Students will **Analyze and Compare** of process management concepts including scheduling, synchronization ,deadlocks
LO5	Students will **Examine** multithreading and system resources sharing among the users
LO6	Students will **Outline** of file system interface and implementation

Part B: Contact Session Plan

Academic Term	
Course Title	Computer Organization and Software Systems
Course No	
Lead Instructor	

Course Contents

Contact Hour	List of Topic Title (from content structure in Part A)	Topic # (from content structure in Part A)	Text/Ref Book/external resource
1-2	**Computer System Components and Interconnections:** Organization and Architecture, Structure and Functions of a computer system, Computer Components, Computer Functions: Basic Instruction cycle state diagram, Interrupts, Instruction cycle state diagram with interrupts.	1.1-1.3, 1.4.1-1.4.3	T1 and R1
2-4	Interconnection Structures and Bus Interconnection Performance Assessment : MIPS Rate, Amdahl's Law **Memory Organization :** Computer Memory System Overview : Characteristics of Memory Systems and The Memory Hierarchy. Cache Memory Principles.	1.4.4-1.4.5, 1.5,2.1-2,2	T1(Chap 3), R1(Chap 3)
5-6	Cache to Main Memory Mapping Functions: Direct, Associative, and Set Associative.	2.3-2.6	T1,R1

	Replacement Algorithms, Write Policy, Multi-cache system.		
7-8	**Input/Output Organization :** I/O Modules, Data Transfer Schemes : Programmed I/O, Interrupt-Driven I/O, Direct Memory Access	3.1-3.2	T1
9-10	**Instruction Set Architecture (x86 as an example):** Instruction Set: Characteristics and Functions : Machine Instruction Characteristics, Types of Operands, Types of Operations, Instruction Set: Addressing Modes and Formats: Addressing Modes, Instruction Formats	4.1-4.2	T1
11-12	Instruction Pipeline :Resource Hazard, Data Hazard and Control Hazard	4.3	T1
13-14	CISC Vs RISC. **Control Unit Operation** : Hardwired Control Unit Implementation, Micro programmed Control Unit Implementation	4.4, 5.1-5.2	T1
15-16	**Operating System Structure :** Introduction to Operating System, Structure of a Operating System (Linux as an example OS), Operating System Services , System Calls	6.1-6.4	T2
17-18	**Process Management :** Concept of Process, Process State Diagram, Operations on Processes, Inter-process communications with examples, Process vs. Threads, Multithreading Models	7.1-7.6	T2
19-20	Process Scheduling criteria, Process Scheduling Algorithms -FCFS, SJF, Priority, RR, Multilevel Queue, Multilevel Feedback Queue	7.7-7.8	T2
21-22	**Process Coordination:** The Critical section problem, Peterson's Solution, Synchronization Hardware	8.1-8.3	T2
23-24	Semaphores. Deadlock: System Model, Deadlock Characterization, Methods of Handling Deadlocks: Deadlock Prevention	8.4-8.6, 8.7.1	T2
25-26	Deadlock Avoidance: Banker's Algorithm, Deadlock Detection, Recovery from Deadlock	8.7.2 – 8.7.4	T2
27-28	**Memory Management :** Memory-Management Strategies, Swapping, Contiguous memory Allocation, Paging, Segmentation	9.1-9.5	T2
29-30	Virtual-Memory Management, Demand Paging, Page Replacement Algorithms: FIFO, Optimal, LRU, LFU Thrashing.	9.6 – 9.9	T2

31-32	**File System :** File Concept, Access Methods, Directory Structure, File System Mounting, File System Structure, File System Implementation, Directory Implementation	10.1 – 10.7	T2

Evaluation Scheme

Evaluation Component	**Name** (Quiz, Lab, Project, Midterm exam, End semester exam, etc)	**Type** (Open book, Closed book, Online, etc.)	**Weight**	**Duration**	**Day, Date, Session, Time**
EC - 1	Quizzes / Assignment		25%		To be announced
EC - 2	Mid-term Exam	Closed book	25%	2 hours	To be announced
EC - 3	End Semester Exam	Open book	50%	3 hours	To be announced

Note *- Evaluation components can be tailored depending on the proposed model.*

Important Information

Syllabus for Mid-Semester Test (Closed Book): Topics in Weeks 1-8 (1-18 Hours)
Syllabus for Comprehensive Exam (Open Book): All topics given in plan of study

Evaluation Guidelines:

1. EC-1 consists of either two Assignments or three Quizzes. Announcements regarding the same will be made in a timely manner.
2. For Closed Book tests: No books or reference material of any kind will be permitted. Laptops/Mobiles of any kind are not allowed. Exchange of any material is not allowed.
3. For Open Book exams: Use of prescribed and reference text books, in original (not photocopies) is permitted. Class notes/slides as reference material in filed or bound form is permitted. However, loose sheets of paper will not be allowed. Use of calculators is permitted in all exams. Laptops/Mobiles of any kind are not allowed. Exchange of any material is not allowed.
4. If a student is unable to appear for the Regular Test/Exam due to genuine exigencies, the student should follow the procedure to apply for the Make-Up Test/Exam. The genuineness of the reason for absence in the Regular Exam shall be assessed prior to giving permission to appear for the Make-up Exam. Make-Up Test/Exam will be conducted only at selected exam centres on the dates to be announced later.

It shall be the responsibility of the individual student to be regular in maintaining the self-study schedule as given in the course handout, attend the lectures, and take all the prescribed evaluation components such as Assignment/Quiz, Mid-Semester Test and Comprehensive Exam according to the evaluation scheme provided in the handout.