

COL215 Lab Assignment 3

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1 Objective

Extending the design in previous assignment to a multi-digit display by introducing proper timing and refreshing signals.

2 Procedure

1. The basic idea is to display one digit at a time in rapid succession so that the eye perceives that the digits are actually displayed simultaneously.
2. We maintain a counter of 4 possible values that is incremented at each rising clock edge. With the counter as a control signal, we multiplex the bcd value to the four available digits and also multiplex the anode values to decide where the digit is displayed.
3. Finally, we ran synthesis, generated the bitstream and ran it on the board. Images of different inputs to the board can be seen in Fig 2.
4. We keep a refresh period of 20ms. We observe that the digits seamlessly appear to be displayed simultaneously to our eyes. The refresh rate is also implemented by maintaining another counter that gets incremented every clock cycle, being reset every 20ms.

3 Simulation

We simulated the code on EDA Player, for some possible the inputs and observed outputs for them. The outputs are shown in Fig 1. The an signal goes from "1110" to "0111" to display the lsb to msb of the digits. The output seg changes corresponds to one of the four bcd_i signals at a time.

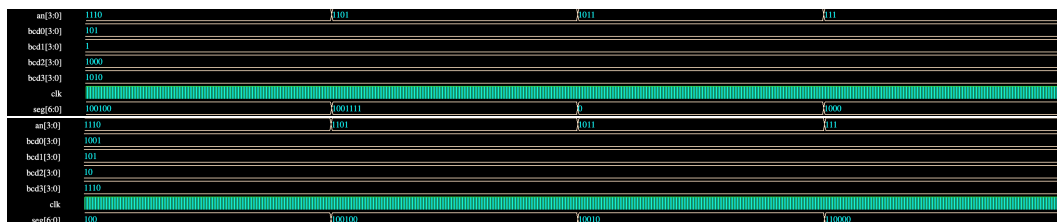


Figure 1: Simulation for some inputs

4 Running on Board

After simulation, running on the actual board also gave us expected outputs. The images for some possible inputs can be seen in Fig 2.

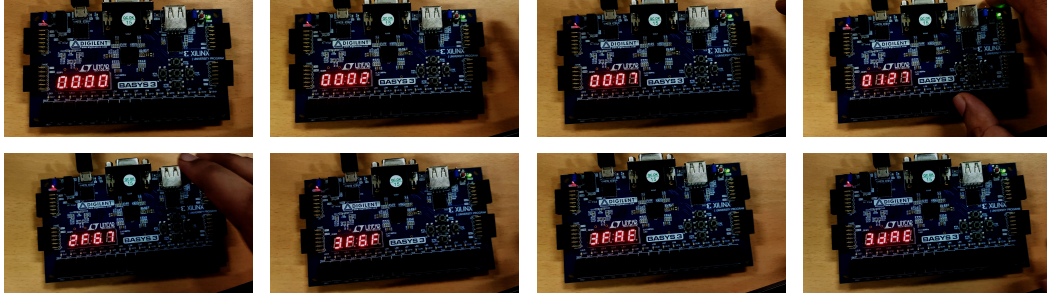


Figure 2: Running on Board

5 Resource Count

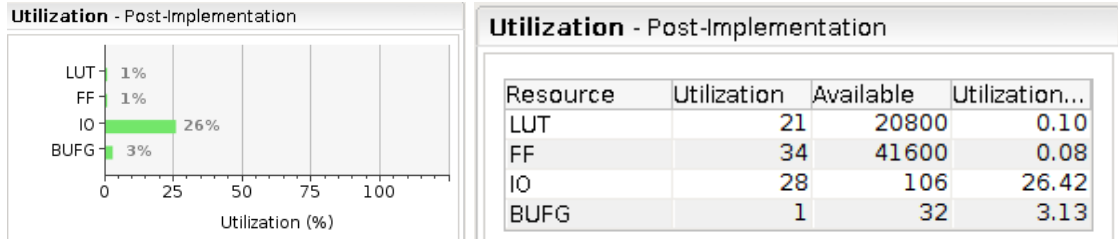


Figure 3: Resource Utilisation

Component	Count
Flip-flops	34
LUT	21
BRAM	0
DSP	0

Table 1: Different components of the Digital Circuit and the counts of each of these components used.