

Experiment 2 : Logic Gates

Digital Systems and Microcontrollers | Monsoon 2024

Instructions

- There are two parts in this Lab Experiment.
- Submit a separate tinkercad circuit project for each part.
- Make sure to answer the extra question in each part of the experiment in the report.
- Name the output LED's(SUM, CARRY et cetera) appropriately.
- The inputs to the circuit would be of the form AB when there are two inputs i.e 01 means $A = 0$ and $B = 1$ and ABC when there are three inputs. i.e 100 $\Rightarrow A = 1, B = 0, C = 0$.
- Sample circuit for each experiment is given in the Appendix for reference.

In this experiment, you will be introduced to some of the basic logic gates (NOT, AND, OR, NAND, NOR, XOR etc) available commercially in the IC (Integrated Circuit) form. Two families of digital ICs are commonly used: the TTL 74LSxx series and the CMOS CD 40xx series. Many of these ICs have 14 pins, and some have 16 or more. Two pins are used for power supply connections. Thus 12 pins are available in a 14-pin IC for gate inputs and outputs. A 2-input gate requires three pins per gate (two for inputs and one output), and so ICs that implement 2-input logic functions generally have 4 gates per IC. TTL ICs require a fixed d-c power supply voltage VCC having the nominal value of 5V and a tolerance of 5%. Thus these ICs are not guaranteed to function with VCC below 4.75V and VCC in excess of 5.25V can damage the IC. A $0.1\mu\text{F}$ ceramic capacitor should be connected between the VCC and Ground pins of each TTL IC to suppress spikes that may otherwise be created due to the current drawn from the power supply. Most CMOS ICs can work with $3\text{V} \leq \text{VCC} \leq 15\text{V}$ and do not require capacitors at each VCC pin.

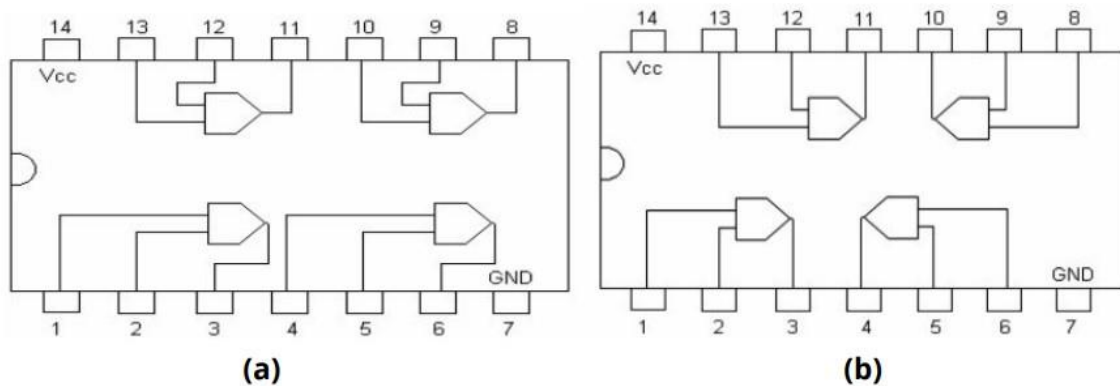


Figure 1: Two types of input connections for Quad-2-Input Gates a). TTL 74xx ICs b). CMOS CDXX ICs

Part A : Verifying the truth table of Logic Gates

The goal of this part of the experiment is to take input from the serial monitor and verify the truth table of logic gates: (NOT, OR, AND, XOR, NOT, NAND) using TTL 74XX family of ICs.

1. Place the IC on breadboard and give V_{cc} and Gnd connection to it.
2. Take inputs from the Serial Monitor for values of A and B and route them to the input pins of the IC.
3. Connect an LED with appropriate resistor to the output of the GATE.
4. Note the output of the chosen gate for different values of input in a truth table.

You can take an input of 0 to 10 from the Serial Monitor to a variable x the following way:

```
int x; void setup()
{
    Serial.begin(9600); //opens serial port, sets data rate to 9600 bps
} void loop() { if(Serial.available() > 0) { x = Serial.read(); // x would be an integer between
0 and 255
    // depending on the ascii value of the character read x = x - '0'; //
    Subtracting ascii value of 0 from x.

    }

    //Use the value of x in code.
}
```

Part B : De Morgan's Law

De Morgan's theorems state that $(A + B)^0 = A^0 \cdot B^0$ and $(A \cdot B)^0 = A^0 + B^0$. Verify these theorems by proceeding step by step as follows:

1. Set up a circuit consisting of two NOT gates and one AND gate to perform function $Y = A^0 \cdot B^0$,
2. Obtain the truth table of this circuit by noting the output of the function for different values of A and B . Verify that the output of the function is same as that of the NOR gate.
3. Repeat steps 1 and 2 using an OR gate instead of an AND gate to verify that the truth table is same as that of the NAND gate.

How would you realise the above circuit if you have only NAND gates instead of NOT gates? i.e How would you use NAND gates to perform function of NOT gates?

Appendix

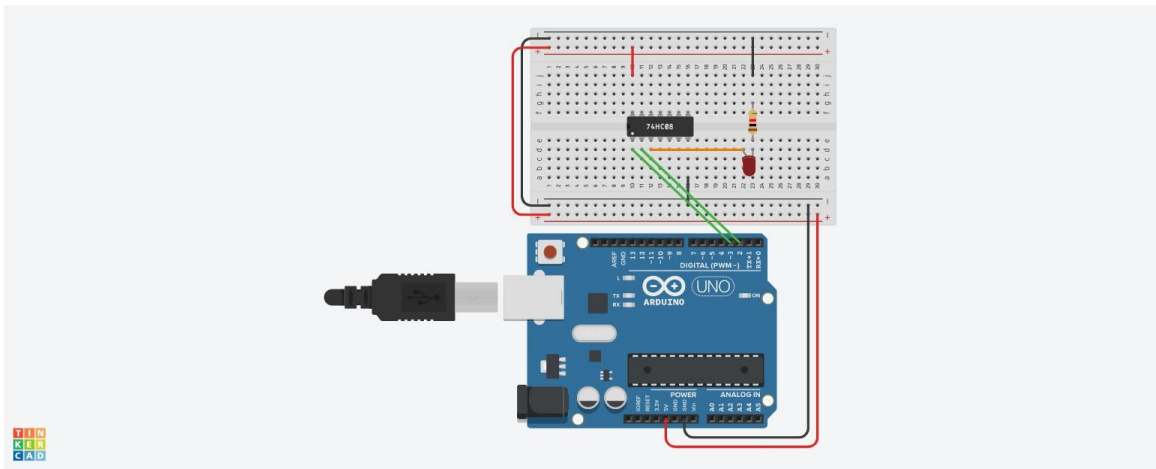


Figure 4: Part A: Verifying AND Gate

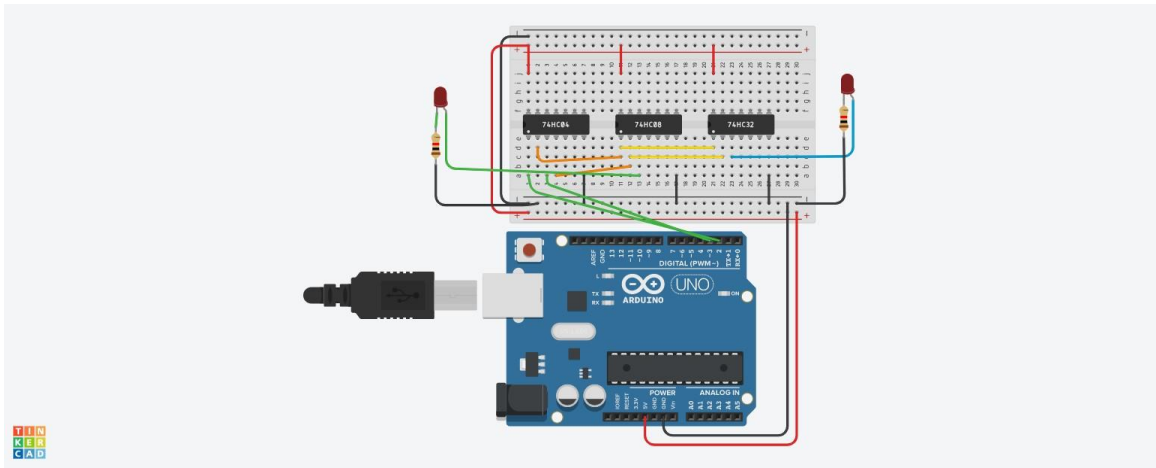


Figure 5: Part B: De Morgan's Law