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Internal - II

Computer Organization

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6. Direct memory access(DMA):

Direct memory access is a mode of data transfer between the memory and I/O devices. The happens without the involvement of the processor. we have two other methods of data transfer, programmed I/O and interrupt driven I/O. Let's revise each and get acknowledge with their drawbacks

In programmed I/O, the processor keeps on Scanning whether any device is ready for data transfer. If an I/O device is ready. The processor fully dedicates itself in transferring the data between I/O and memory. It transfers data at a high rate, but it can't get involved in any other activity during data transfer. This is the major drawback of programmed I/O.

In Interrupt driven I/O, whenever the device is ready for data transfer, then it raises an interrupt to processor. processor completes executing its ongoing instruction and saves its current state. It then switches to data transfer which causes a delay. Here, the processor doesnt keep scanning for peripherals ready for data transfer

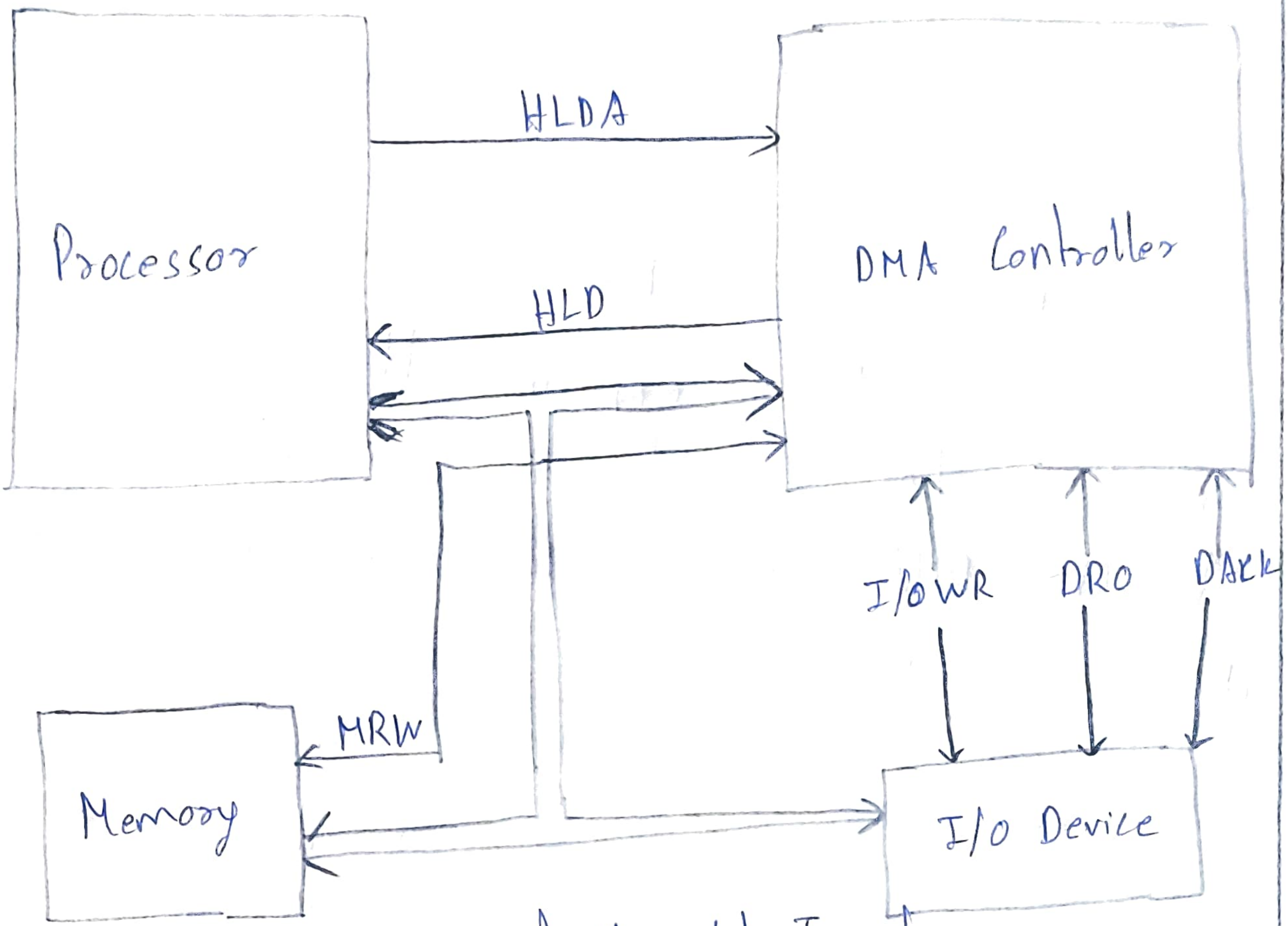
The DMA controller transfers the data in three modes:

1) **Burst mode:**
Here, once the DMA controller gains the charge of the system bus, then it releases the system bus only after completion of data transfer. Till then the cup has to wait for the system buses.

2) **Cycle stealing mode:** In this mode, the DMA controller forces the CPU to stop its operation and relinquish the control over the bus for a short term to the DMA controller

Direct Memory Access Controller & It's working:

DMA controller is a hardware unit that allows I/O devices to access memory directly without the participation of the processor. Here we will discuss the working of the DMA controller. Below we have the diagram of DMA controller that explains its working.



DMA Controller data Transfer

* whennever an I/o device wants to transfer the data to or from memory, it sends the DMA request (DRQ) to the DMA controller.

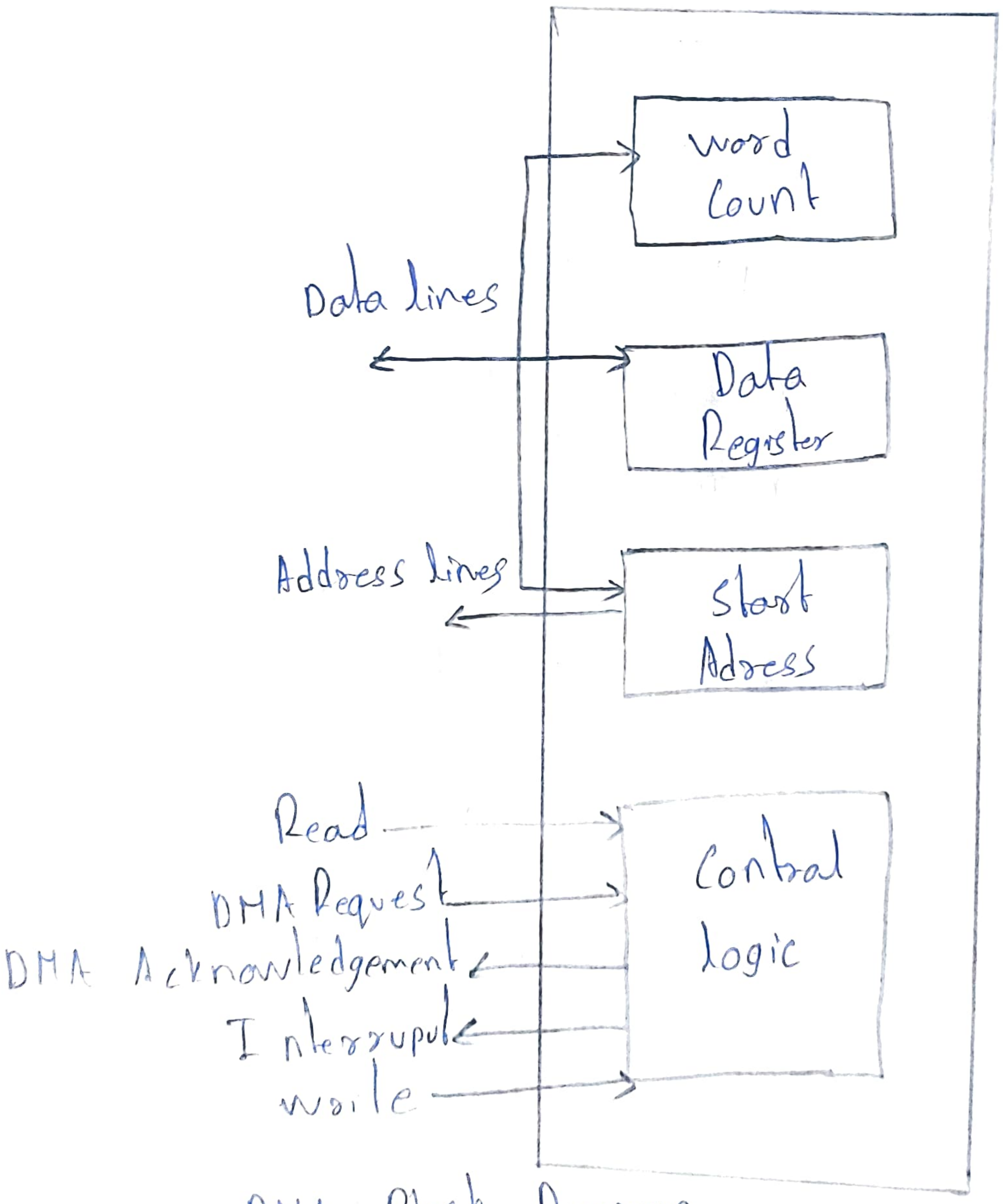
* CPU receives the Hold request (HLD) from DMA controller and relinquishes the bus and sends the Hold acknowledgement (HLDA). DMA Controller.

* After receiving the hold acknowledgement (HLDA). that the data transfer can be performed and DMA controller takes the charge of the system bus and transfers the data to or from memory.

Now the DMA controller can be separate unit that is shared by various I/O devices, or it can also be a part of the I/O device interface.

Direct memory Acess Diagram:

After exploring the working of DMA controller. Let us discuss the block diagram of the DMA controller. Below we have a block diagram of DMA controller.



DMA Block Diagram.

whenever a processor is requested to read or write a block of data. i.e. transfer a block of data

5) Synchoronous Buses;

In Synchonous Buses, the steps of data transfer take place a fixed clock cycles. everything is synchoronused bus ~~the~~ clock and clock signals are made available to both master and slave. The bus clock is a square wave singal. A cycle starts at one rising edge of the clock and ends at the next rising edge. which is the begining of the next cycle. A transfer may take multiple bus cycle depending on the speed parameters of the bus and the two ends of the transfer. one scenario would be that on the first clock cycle, the master puts an address on the adress bus, puts data on the data bus, and asserts the appropriate control lines. slave recognizes, its adress on the adress bus on the first cycle and reads the new value for the bus in the second cycle. Synchoronous buses are simple and easily implemented. However, when connecting devies with varying speed to a

Synchronous bus, the slowest device will determine the speed of the bus. Also the synchronous bus length could be limited to avoid clock-skewing problem

Asynchronous Buses:

There are no fixed clock cycles in asynchronous buses. Handshaking is used instead shows the handshaking protocal. The master asserts the data-read line.

An asynchronous bus has no system clock. Handshaking is done to properly conduct the transmission of data between the sender and the receiver. The process is illustrated. For example, In an asynchronous read operation, the bus master puts the address and control signals on the bus and then asserts a synchronization signal. The slave's synchronization signal indicates to the processor that there is valid data on the bus and it read the data. The master then deasserts its synchronization signal, which indicates to the slave that the master has read the

the data. The slave then deasserts its synchronization signal. This method of synchronization is referred to as a full handshake. Note that there is no clock and that starting and ending of the data transfer and indicated by special synchronization signals. An asynchronous communication protocal can be considered as a pair of finite state machines (FSMs) that operate in such away that one does not proceed until the other FSM has reached a certain state

2) Interface Circuits:

An I/O interface consists of the circuits required to connect an I/O device to a computer bus. On the side of the interface we have to bus signals for address, data and control, on the other side we have data path with its associated controls to transfer data between the interface and the I/O device.

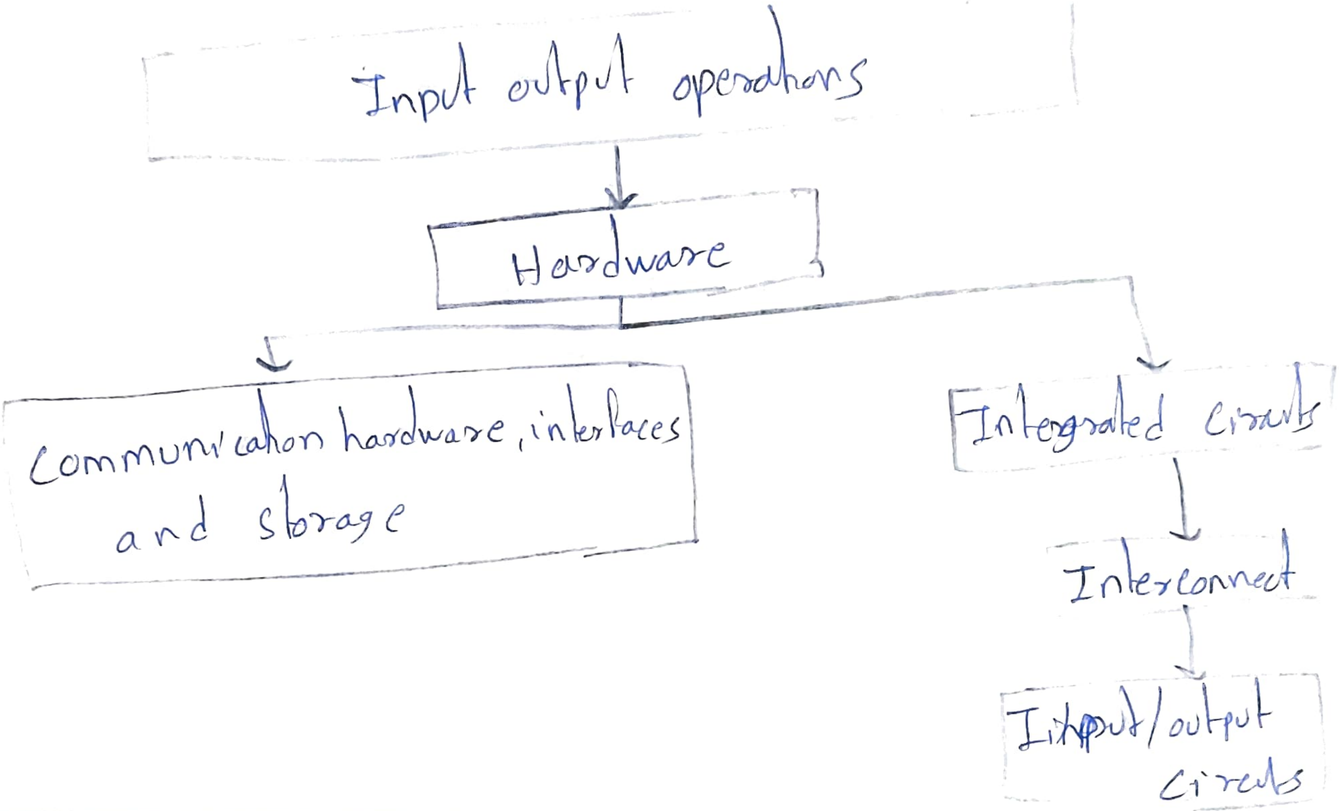
- provides a storage buffer for a least one word of data (or one byte, in the case of byte-oriented devices,

- Contains status flags that can be accessed by the processor to determine whether the buffer is full (for input) or empty (for output)
- Contains address-decoding circuitry to determine when it is being adressed by the processor.
- Generates the appropriate ~~their~~ timing signals required by the bus control scheme.

i) Input-operations:

Input-output (I/O) System transfers information between computer main memory and the outside world. An I/O system is composed of I/O devices (peripherals), I/O control units, and software to carry out the I/O transaction(s) through a sequence of I/O operations. I/O devices can be classified as serial, able to transfer bit streams one bit at a time, or parallel. parallel devices have a wider data bus and can therefore transfer data in words of one or more bytes like any other activity in a computer system. I/O is a concerted work of both hardware and software

The Software which is exculed to carry out an I/o transaction for a specific I/o device is called a device driver.

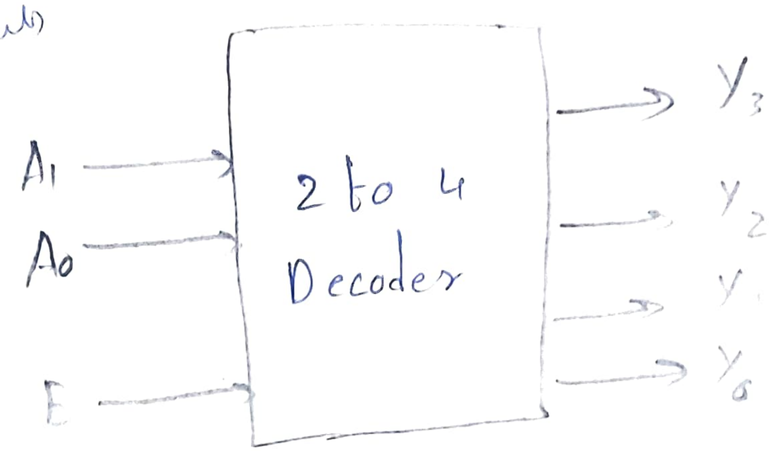

Input output operations
Hardware
communication hardware, interfaces and storage
Integrated circuits
Interconnect
~~I~~ Input/output circuts

ii) Decoder:

Decoder is a combinatontional circuit that has 'n' input lines and maximum of 2^n output lines one of these outputs will be active high based on the combination of inputs present, when the decoder is enabled. That means decoder detectes a particular code. The outpus of the decoder are nothing but the min terms of 'n' input varibls lines, when it is enabled

2 to 4 decoder

Let 2 to 4 decoder has two inputs A_1 and A_0 and four outputs Y_3, Y_2, Y_1 & Y_0. The block diagram



One of these four outputs will be '1' for each combination of inputs when enable E is '1'. The Truth table of 2 to 4 decoder is shown below.

Enable	Inputs		outputs			
E	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	0	1	0	1	0	0
1	1	0	1	0	0	0
1	1	1	0	0	0	0