

# Design of Two Stage Operational Amplifier

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## Background Theory

### 12.8.1 Review of Bode's Rules

In our review of Bode's rules in Chapter 11, we noted that the slope of the magnitude of a transfer function decreases (increases) by 20 dB/dec as the frequency passes a pole (zero). We now review Bode's rule for plotting the phase of the transfer function:

The phase of a transfer function begins to decrease (increase) at one-tenth of the pole (zero) frequency, incurs a change of  $-45^\circ$  ( $+45^\circ$ ) at the pole (zero) frequency, and experiences a total change of nearly  $-90^\circ$  ( $+90^\circ$ ) at ten times the pole (zero) frequency.<sup>14</sup>

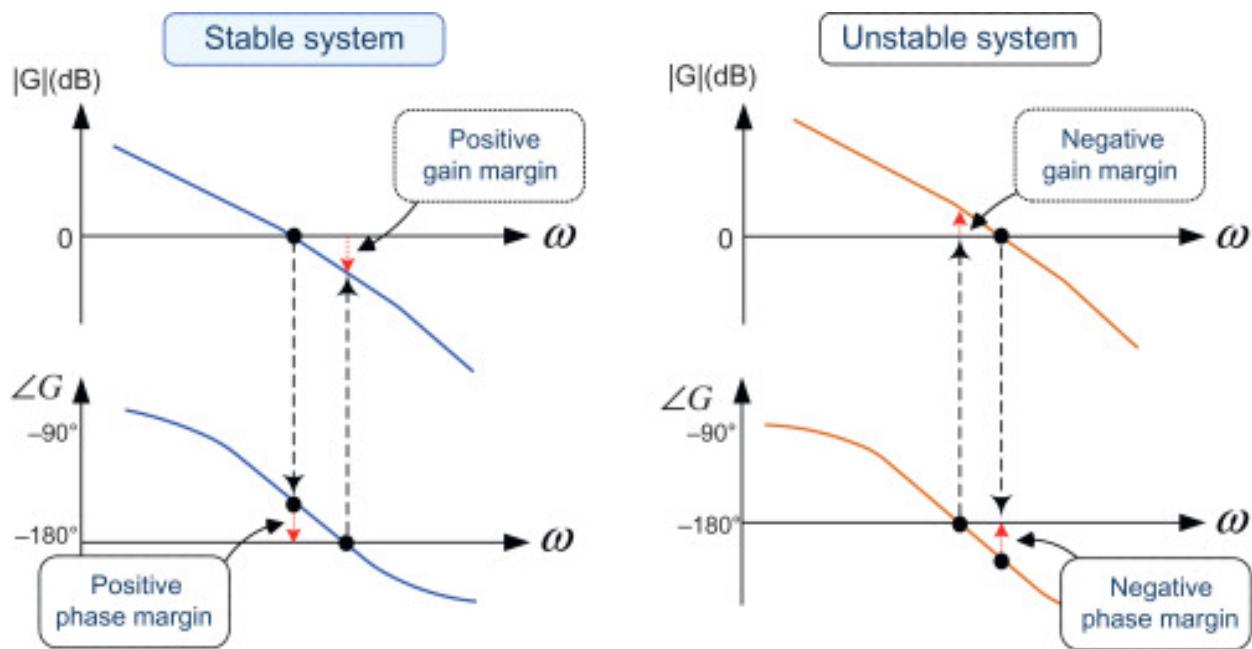
Since the phase begins to change at one-tenth of a pole or zero frequency, even poles or zeros that seem far may affect it significantly—a point of contrast to the behavior of the magnitude.

#### Gain Margin/Phase Margin:

##### Stability Condition:

- Our foregoing investigation indicates that if  $|KH(j\omega_1)| \geq 1$  and  $H(j\omega_1) = -180^\circ$ , then the negative feedback system oscillates. Thus, to avoid instability, we must ensure that these two conditions do not occur at the same frequency.
- In summary, to guarantee stability in negative-feedback systems, we must ensure that the loop gain falls to unity before the phase shift reaches  $-180^\circ$  so that Barkhausen's criteria do not hold at the same frequency.
- The frequencies at which the loop gain falls to unity or the phase shift reaches  $-180^\circ$  play such a critical role as to deserve specific names. The former is called the “gain crossover frequency” ( $\omega_{GX}$ ) and the latter, the “phase crossover frequency” ( $\omega_{PX}$ ). Stability requires that:

$$\omega_{GX} < \omega_{PX}$$



### Miller's Theorem:

Consider the general circuit shown in Fig. 11.13(a), where the floating impedance,  $Z_F$ , appears between nodes 1 and 2. We wish to transform  $Z_F$  to two grounded impedances as depicted in Fig. 11.13(b), while ensuring all of the currents and voltages in the circuit remain unchanged. To determine  $Z_1$  and  $Z_2$ , we make two observations: (1) the current drawn by  $Z_F$  from node 1 in Fig. 11.13(a) must be equal to that drawn by  $Z_1$  in Fig. 11.13(b); and (2) the current injected to node 2 in Fig. 11.13(a) must be equal to that injected by  $Z_2$  in Fig. 11.13(b). (These requirements guarantee that the circuit does not “feel” the transformation.) Thus,

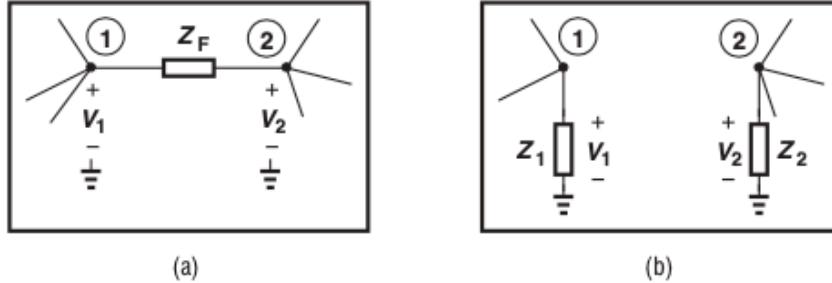
$$\frac{V_1 - V_2}{Z_F} = \frac{V_1}{Z_1} \quad (11.19)$$

$$\frac{V_1 - V_2}{Z_F} = -\frac{V_2}{Z_2}. \quad (11.20)$$

Denoting the voltage gain from node 1 to node 2 by  $A_v$ , we obtain

$$Z_1 = Z_F \frac{V_1}{V_1 - V_2} \quad (11.21)$$

$$= \frac{Z_F}{1 - A_v} \quad (11.22)$$



**Figure 11.13** (a) General circuit including a floating impedance, (b) equivalent of (a) as obtained from Miller's theorem.

and

$$Z_2 = Z_F \frac{-V_2}{V_1 - V_2} \quad (11.23)$$

$$= \frac{Z_F}{1 - \frac{1}{A_v}}. \quad (11.24)$$

Called Miller's theorem, the results expressed by Eqs. (11.22) and (11.24) prove extremely useful in analysis and design. In particular, Eq. (11.22) suggests that the floating impedance is reduced by a factor of  $1 - A_v$  when “seen” at node 1.

- Capacitance at the input node is amplified whereas Capacitance seen at the output node is attenuated.
- Miller's approximation does not tell us about the zero introduced.

As an important example of Miller's theorem, let us assume  $Z_F$  is a single capacitor,  $C_F$ , tied between the input and output of an **inverting amplifier** [Fig. 11.14(a)]. Applying Eq. (11.22), we have

$$Z_1 = \frac{Z_F}{1 - A_v} \quad (11.25)$$

$$= \frac{1}{(1 + A_0)C_F s}, \quad (11.26)$$

where the substitution  $A_v = -A_0$  is made. What type of impedance is  $Z_1$ ? The  $1/s$  dependence suggests a capacitor of value  $(1 + A_0)C_F$ , as if  $C_F$  is “amplified” by a factor of  $1 + A_0$ . In other words, a capacitor  $C_F$  tied between the input and output of an inverting amplifier with a gain of  $A_0$  **raises the input capacitance** by an amount equal to  $(1 + A_0)C_F$ . We say such a circuit suffers from “Miller multiplication” of the capacitor.

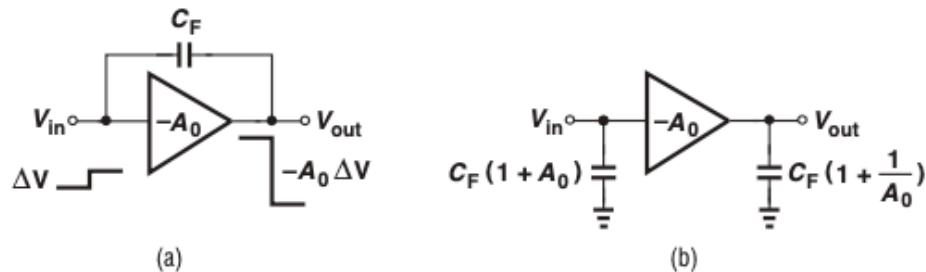
The effect of  $C_F$  at the *output* can be obtained from Eq. (11.24):

$$Z_2 = \frac{Z_F}{1 - \frac{1}{A_v}} \quad (11.27)$$

$$= \frac{1}{\left(1 + \frac{1}{A_0}\right)C_F s}, \quad (11.28)$$

which is close to  $(C_F s)^{-1}$  if  $A_0 \gg 1$ . Figure 11.14(b) summarizes these results.

The Miller multiplication of capacitors can also be explained intuitively. Suppose the input voltage in Fig. 11.14(a) goes up by a small amount  $\Delta V$ . The output then goes *down* by  $A_0\Delta V$ . That is, the voltage across  $C_F$  increases by  $(1 + A_0)\Delta V$ , requiring that the input provide a proportional charge. By contrast, if  $C_F$  were not a floating capacitor and its right plate voltage did not change, it would experience only a voltage change of  $\Delta V$  and require less charge.



**Figure 11.14** (a) Inverting circuit with floating capacitor, (b) equivalent circuit as obtained from Miller's theorem.

### Miller Compensation Technique Principles:

- Miller compensation is one of the most popular techniques that is used to increase the stability of the Multi-stage amplifier.
- The compensation capacitor is connected between the output of these two stages(input of second stage and output of second stage), so this Compensation Capacitor  $C_C$  is also called a Miller Capacitor.
- The working principle of Miller compensation is to split the poles so a higher phase margin can be reached at the unity gain frequency. However, a right-hand-plane (RHP) zero was generated due to a feed forward current from the output of the first stage to the output of the second stage.
- Before compensating the circuit, the two stage operational amplifier has two poles which are located at  $p_1 = 1/(R_1 C_1)$ , and  $p_2 = 1/(R_2 C_2)$ , where R and C are the resistance and capacitance respectively at the corresponding nodes shown in the Figure. The capacitors  $C_1$  and  $C_2$  are mainly formed by the parasitic capacitance of corresponding connected MOSFETs of each node.
- The Miller effect makes one pole more dominant by moving the pole down in frequency, while the other becomes less dominant by moving the pole up in frequency (pole splitting).
- The new values of poles are: ( $gm_7=gm_2$ )

$$p_1 = \frac{-1}{(C_2 + C_C)R_2 + (C_1 + C_C)R_1 + g_{m7}R_1R_2C_C}$$

$$\cong \frac{-1}{g_{m7}R_1R_2C_C}$$

$$p_2 = -\frac{(C_2 + C_C)R_2 + (C_1 + C_C)R_1 + g_{m7}R_1R_2C_C}{R_1R_2(C_1C_2 + C_1C_C + C_2C_C)}$$

$$\cong -\frac{g_{m7}C_C}{C_1C_2 + C_1C_C + C_2C_C}$$

$$\cong -\frac{g_{m7}}{C_2 + C_1} \quad \text{or,} \quad -\frac{g_{m7}}{C_2} \quad \text{for} \quad C_2 > C_C > C_1$$

- As shown in figure below poles are split to new position:

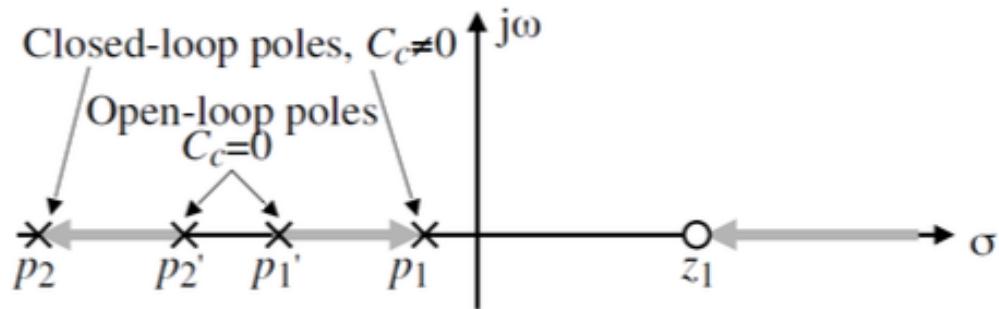
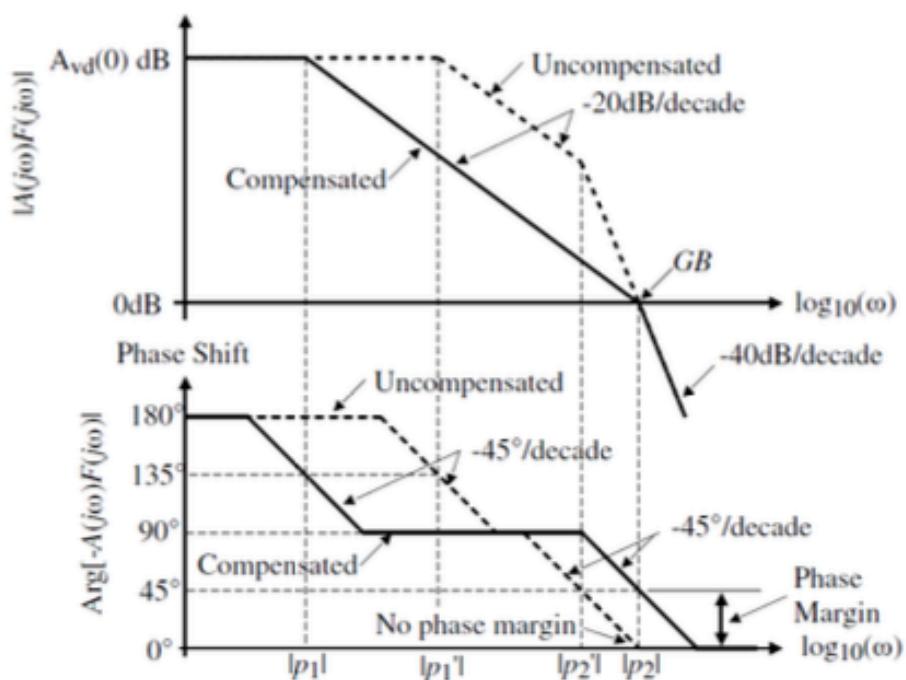


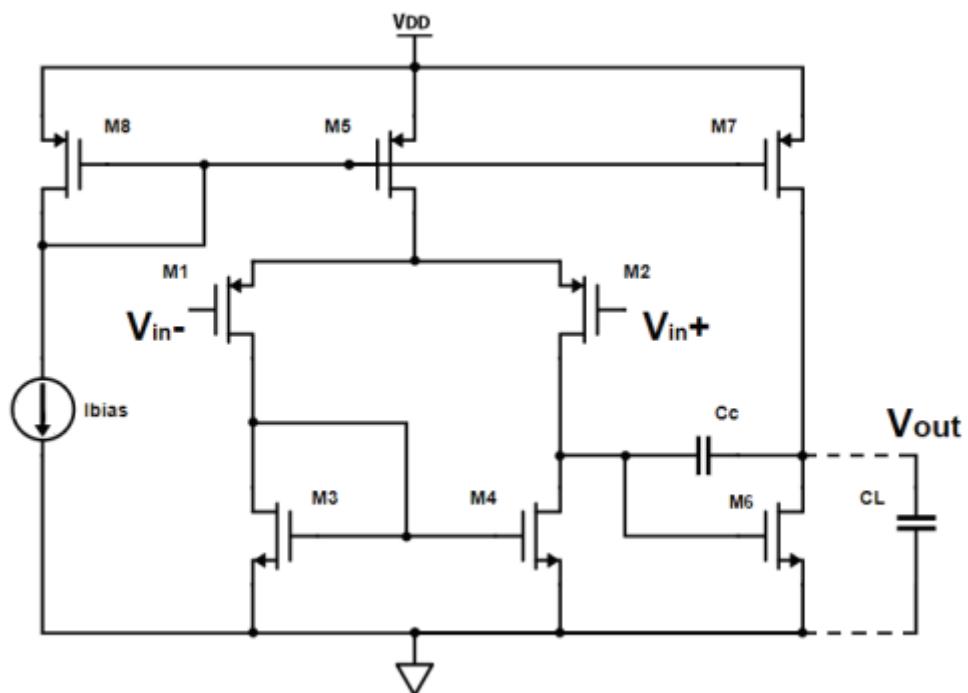
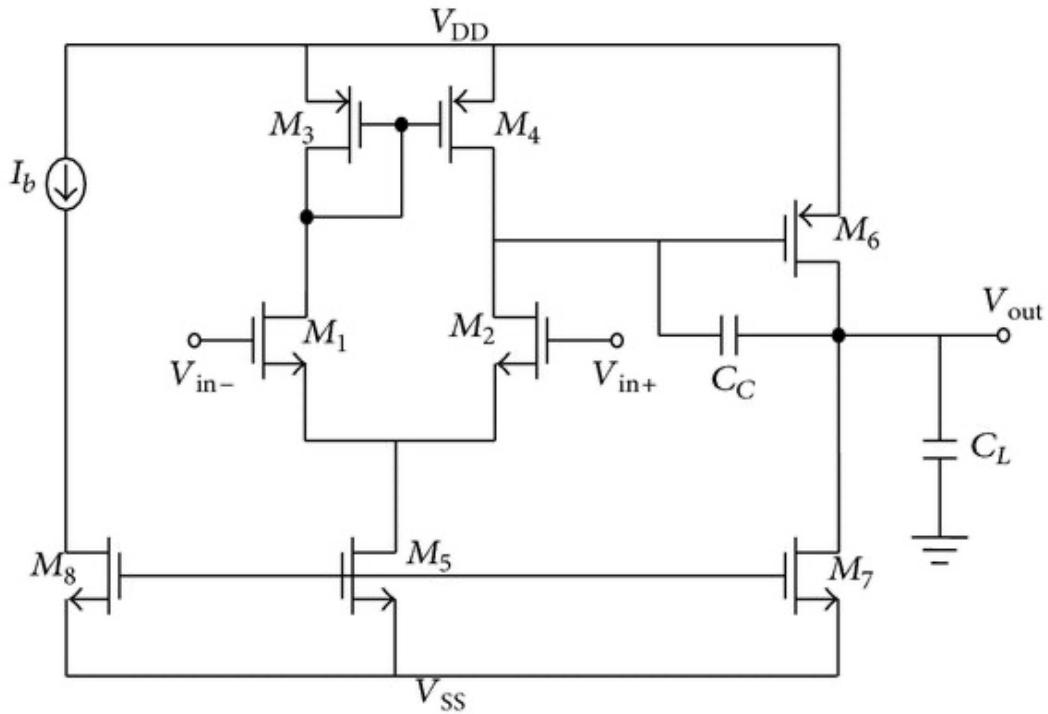
Figure 2.7: Pole Splitting Demonstration [2]

- $p_1$  becomes more dominant than it used to be, which results in the system starting to behave as a first order system in low frequency range. On the contrary,  $p_2$  moves to the other direction which makes it more non-dominant.
- The goal of splitting both poles is achieved, however, a RHP zero  $z_1$  is generated, which is undesirable because it boosts the gain while decreasing the phase. One approach to address this issue is to make sure its frequency is 10 times larger than the unity gain bandwidth frequency by adjusting the corresponding parameter of  $z$ .



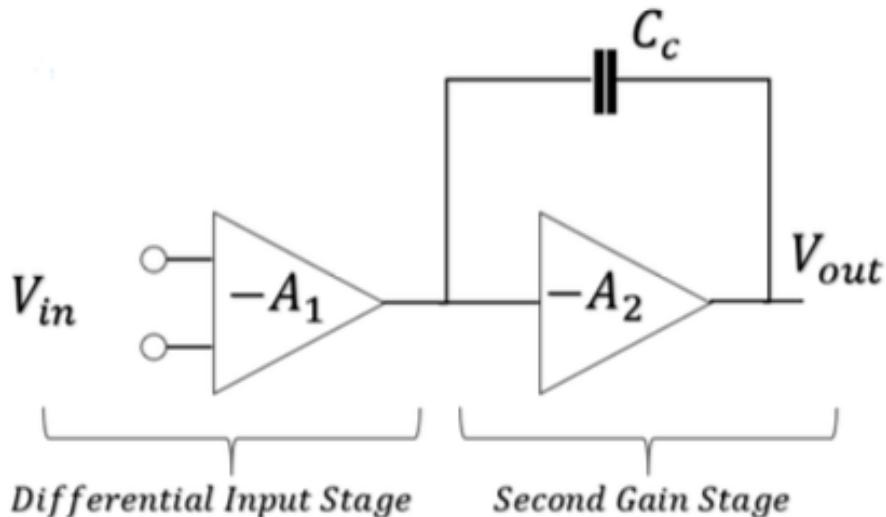
- Slew rate:
- CMRR: Common mode rejection ratio:
- PSRR:

2 Stage Opamp: N-type/P-type input: (lower common mode i/p voltages-N-type)



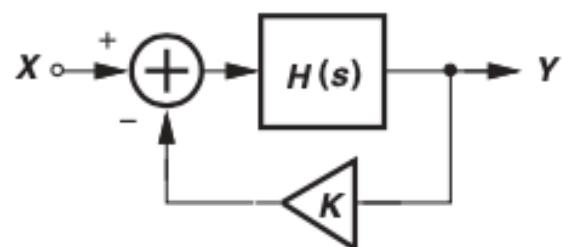
## Background of Amplifier System Stability

- Two or more stages amplifiers can be implemented to achieve high gain and high output swing regardless of the limitations of the power supply voltage or power consumption compared to single stage amplifiers.
- An uncompensated two-stage operational amplifier has a two-pole transfer function, and both poles are located below the unity gain frequency.



2.1: Block diagram of a Miller compensated operational amplifier

- Therefore, a compensation circuitry must be implemented to enlarge the phase margin so does the stability.
- As shown in the Figure 2.1, the Miller capacitor is used as a negative feedback network to compensate the system, which feeds a current back from the output to the middle of the two stages A1 and A2
- However, Operational amplifiers operating on a close-loop with a negative-feedback system are susceptible to oscillation.



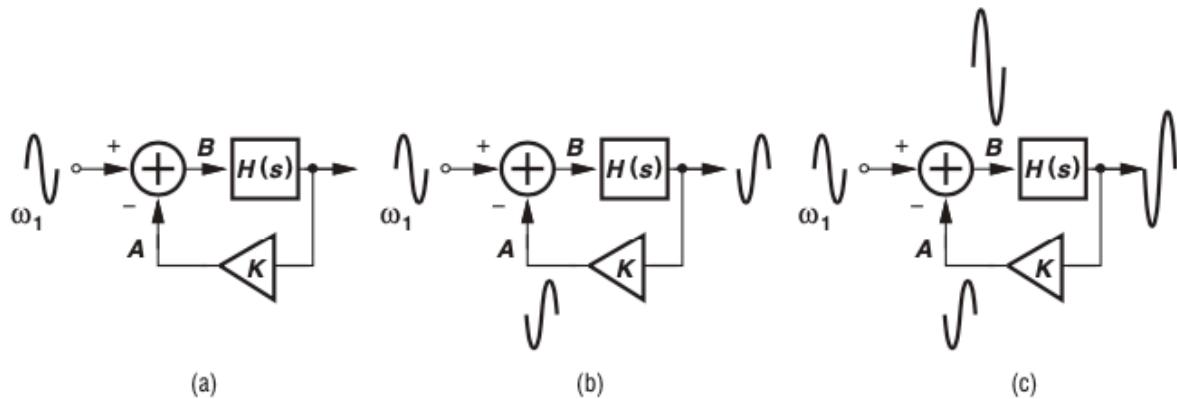
**Figure 12.63** Negative feedback system.

- Suppose an amplifier having a transfer function  $H(s)$  is placed in a negative feedback loop (Fig. 12.63).
- As with the cases studied in Section 12.1, we write the closed-loop transfer function as :

$$\frac{Y}{X}(s) = \frac{H(s)}{1 + KH(s)},$$

- where  $KH(s)$  is sometimes called the “loop transmission” rather than the loop gain to emphasize its frequency dependence.
- that for a sinusoidal input,  $x(t) = A \cos \omega t$ , we simply make the substitution  $s = j\omega$  in the above transfer function.
- An interesting question that arises here is, what happens if at a certain input frequency  $\omega_1$ , the loop transmission,  $KH(j\omega_1)$ , becomes equal to  $-1$ ? Then, the closed-loop system provides an infinite gain (even though the open-loop amplifier does not).
- To understand the consequences of infinite gain, we recognize that even an infinitesimally small input at  $\omega_1$  leads to a finite output component at this frequency.
- A small noise component at  $\omega_1$  therefore experiences a very high gain and emerges as a large sinusoid at the output. We say the system oscillates at  $\omega_1$ .
- Viewing  $KH$  as a complex quantity, we recognize that this condition (“Barkhausen’s criteria” for oscillation) is equivalent to:

$|KH(j\omega_1)| \geq 1$  : ensures sufficient loop gain for the circulating signal to grow  
 $|KH(j\omega_1)| = -180^\circ$



**Figure 12.64** Evolution of oscillatory system with time: (a) a component at  $\omega_1$  is sensed at input, (b) the component returns to subtractor with a  $180^\circ$  phase shift, (c) the subtractor enhances the signal at node B.

In summary, a negative feedback system may become unstable if the forward amplifier introduces a phase shift of  $-180^\circ$  at a finite frequency,  $\omega_1$ , and the loop transmission  $|KH|$  is equal to unity at that frequency. These conditions become intuitive in the time domain as well. Suppose, as shown in Fig. 12.64(a), we apply a small sinusoid at  $\omega_1$  to the system and follow it around the loop as time progresses. The sinusoid incurs a sign reversal as it emerges at the output of the forward amplifier [Fig. 12.64(b)]. Assumed frequency-independent, the feedback factor simply scales the result by a factor of  $K$ , producing an inverted replica of the input at node  $A$  if  $|KH(j\omega_1)| = 1$ . This signal is now *subtracted* from the input, generating a sinusoid at node  $B$  with *twice* the amplitude [Fig. 12.64(c)]. The signal level thus continues to grow after each trip around the loop. On the other hand, if  $|KH(j\omega_1)| < 1$ , then the output cannot grow indefinitely.

- Shown on Figure 2.3, smaller phase margin tends to have larger overshoot and longer settling time to a step response input while larger phase margin can settle the output down quicker and has less output oscillation:

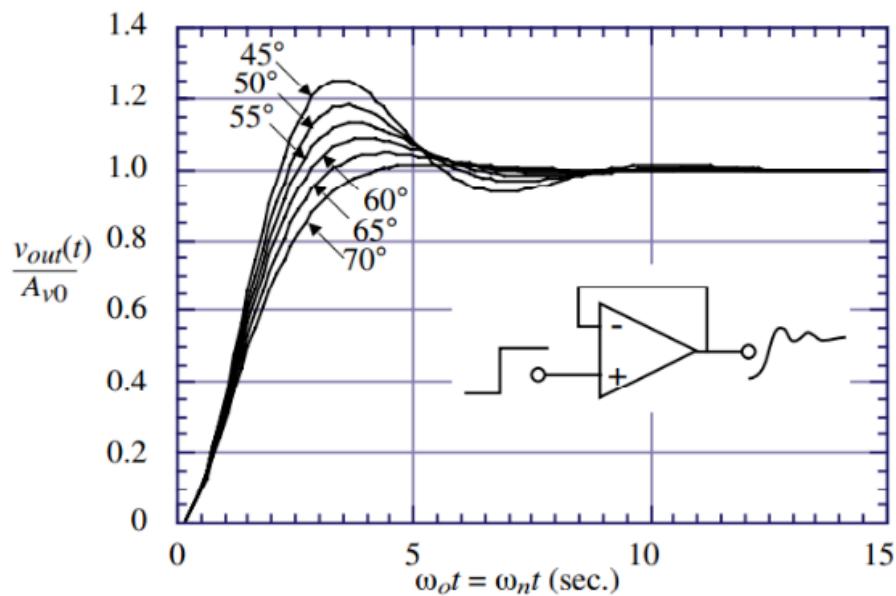
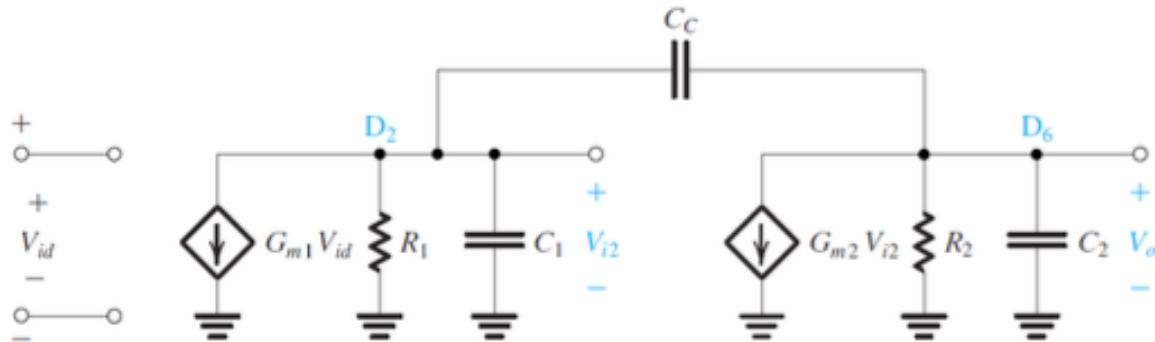


Figure 2.3: Phase Margin Demonstration [8]



## Small Signal Derivation

- Small Signal circuit of 2-stage differential amplifier:



- $gm_1$  is the transconductance of FET of first stage to which i/p is applied, similarly for  $gm_2$
- where R and C are the  $R_1$   $C_1$   $R_2$   $C_2$  resistance and capacitance respectively at the corresponding nodes shown in the Figure.
- The capacitors  $C_1$  and  $C_2$  are mainly formed by the parasitic capacitance of corresponding connected MOSFETs of each node.

$V_{in} = V_{in^+} - V_{in^-}$

gm2 represents gm of second stage

Step 1 : DERIVE TRANSFER FUNCTION MANUALLY

KCL:

$$\frac{V_i}{sC_1} + \frac{V_i}{R_1} + g_{m1}V_{in} + \frac{V_o - V_i}{sC_c} = 0$$

R1,R2=o/p resistances of 1 and 2 stages  
C1,C2=parasitic Capacitances of 1 and 2 stages

$$V_i \left( sC_1 + \frac{1}{R_1} + sC_c \right) + g_{m1}V_{in} - V_o sC_c = 0$$

$$V_i = \frac{R_1 \cdot V_o sC_c - R_1 g_{m1} V_{in}}{1 + sR_1 (C_1 + C_c)} \quad \text{--- (1)}$$

$$\frac{V_o}{sC_2} + \frac{V_o}{R_2} + g_{m_2} V_i + \frac{V_o - V_i}{sC_c} = 0$$

$$V_o \left[ \frac{1}{sC_2} + \frac{1}{R_2} + \frac{1}{sC_c} \right] = V_i \left[ \frac{1}{sC_c} - g_{m_2} \right]$$

$$V_o \left[ R_2 \cdot s \cdot (C_c + C_2) + 1 \right] \cdot \frac{1}{R_2} = \frac{\left( V_o s C_c R_1 - g_{m_2} V_{in} \right)}{\left( s C_c - g_{m_2} \right)}$$

$$V_o \left[ 1 + R_2 \cdot s \cdot (C_c + C_2) \right] \left[ 1 + R_1 \cdot s \cdot (C_c + C_1) \right]$$

$$= \left[ V_o s C_c R_1 - g_{m_2} R_1 V_{in} \right] \cdot \left[ s C_c R_2 - g_{m_2} R_2 \right]$$

$$V_o \left[ \frac{\left( 1 + R_2 \cdot s \cdot (C_c + C_2) \right) \cdot \left( 1 + R_1 \cdot s \cdot (C_c + C_1) \right)}{s C_c R_2 - g_{m_2} R_2} \right] = \left[ V_o s C_c R_1 - g_{m_2} R_1 V_{in} \right]$$

$$g_{m_1} R_1 V_{in} = V_o s C_c R_1 - V_o \left[ \frac{\left( 1 + R_2 \cdot s \cdot (C_c + C_2) \right) \cdot \left( 1 + R_1 \cdot s \cdot (C_c + C_1) \right)}{s C_c R_2 - g_{m_2} R_2} \right]$$

$$V_{in} \left[ -g_{m_1} \cdot R_1 \cdot [s C_c R_2 - g_{m_2} R_2] \right]$$

$$= V_o \left[ s C_c R_1 [s C_c R_2 - g_{m_2} R_2] \right]$$

$$- V_o \left[ \left( 1 + R_2 \cdot s \cdot (C_c + C_2) \right) \cdot \left( 1 + R_1 \cdot s \cdot (C_c + C_1) \right) \right]$$

$$\frac{V_o}{V_{in}} = \frac{g_{m_1} \cdot R_1 \cdot g_{m_2} \cdot R_2 \cdot \left[ 1 - \frac{s C_c}{g_{m_2}} \right]}{s^2 \left[ R_1 \cdot R_2 \cdot (C_1 C_2 + C_1 C_c + C_2 C_c) + s \left[ R_2 (C_c + C_2) + R_1 (C_c + C_1) + C_c g_{m_2} R_1 R_2 \right] + 1 \right]}$$

$$\frac{V_o(s)}{V_{in}(s)} = g_{m_1} g_{m_2} R_2 R_1 \left[ 1 - \frac{s C_c}{g_{m_2}} \right]$$

$$= \frac{s^2 [R_1 R_2 + s C_1 + s^2 b]}{s^2 [R_1 R_2 + s C_1 + s^2 b] +}$$

$$a = (C_2 + \epsilon) R_2 + (C_1 + C_c) R_1 + g_{m_2} R_1 R_2 C_c$$

$$b = R_1 R_2 [C_1 C_2 + C_1 C_c + C_2 C_c]$$

$$\frac{V_o(s)}{V_{in}(s)} = \frac{A_{DC} \left[ 1 - \frac{s}{Z} \right]}{(1 + \frac{s}{P_1})(1 + \frac{s}{P_2})} ; P_1, P_2 \text{ have to be}$$

in -ve X-axis

① DC gain: [ $s \approx 0$ ]

$$\frac{V_o(s \approx 0)}{V_{in}(s \approx 0)} = g_{m_1} g_{m_2} R_1 R_2$$

② Zeros:  $1 - \frac{s}{Z} = 0$

$$s = Z ; Z = g_{m_2} / \epsilon_c$$

③ Poles:

$$\begin{aligned} D(s) &= \left(1 + \frac{s}{P_1}\right) \cdot \left(1 + \frac{s}{P_2}\right) \\ &= 1 + s \left[ \frac{1}{P_1} + \frac{1}{P_2} \right] + \frac{s^2}{P_1 P_2} \end{aligned}$$

Dominant pole approximation:

$$P_1 \ll P_2$$

$$D(s) \approx 1 + s \left[ \frac{1}{P_1} \right] + \frac{s^2}{P_1 P_2}$$

Transfer function after applying dominant pole approximation:

$$\frac{V_o(s)}{V_{in}(s)} \approx \frac{g_{m1} g_{m2} R_2 R_1 \left[ 1 - \frac{s C_c}{g_{m2}} \right]}{1 + s \cdot \frac{1}{P_1} + \frac{s^2}{P_1 P_2}}$$

Comparing with transfer function:

$$P_1 = \frac{1}{a} = \frac{-1}{(C_2 + C_c) R_2 + (C_1 + C_c) R_1 + g_{m2} R_1 R_2 C_c}$$

$$P_2 = \frac{-1}{g_{m2} R_1 R_2 C_c}$$

$$P_2 = \frac{\frac{1}{P_1} \cdot \frac{1}{(b)}}{-R_2(C_2 + C_c) + (C_1 + C_c)R_1 + g_{m2} R_1 R_2 C_c}$$

$$= \frac{-R_2 [C_1 C_2 + C_1 C_c + C_2 C_c]}{R_1 R_2 [C_1 C_2 + C_1 C_c + C_2 C_c]}$$

$$= -g_{m2} R_1 R_2 C_c$$

$$= \frac{-g_{m2} C_c}{C_1 C_2 + C_1 C_c + C_2 C_c} \approx \frac{-g_{m2}}{C_1 + C_2} \approx \frac{-g_{m2}}{C_2} \quad \boxed{\text{for: } C_2 > C_c > C_1}$$

$$\bullet Z = g_{m_2}/C_C \quad \bullet G_{BW} = g_{m_1}/C_C$$

$$\bullet P_1 \approx \frac{1}{g_{m_2} R_1 R_2 C_C}$$

$$\bullet P_2 \approx g_{m_2}/C_2$$

$$\bullet A_{DC} = g_{m_1} g_{m_2} R_1 R_2$$

\* Both frequency and amplitude are in log scale

\* magnitude of transfer function falls at  $20dB/decade$  after pole frequency:

$$20 \times \log_{10} \left( \frac{\omega}{\omega_p} \right)$$

$$\textcircled{1} \text{ Change in gain: } 20 \times \log_{10} \left( \frac{\omega_2}{P_1} \right)$$

$$\textcircled{2} \text{ Gain at } G_{BW} = 0 \text{ dB}$$

$$\textcircled{3} \text{ Gain at } P_1 = 20 \log_{10} A_{DC}$$

$$20 \log_{10} A_{DC} - 0 = 20 \times \log_{10} \left( \frac{\omega_2}{P_1} \right)$$

$$A_{DC} = \frac{G_{BW}}{P_1}$$

$$G_{BW} = P_1 \times A_{DC} = g_{m_1}/C_C$$

Phase margin:

$$\left| \frac{V_o}{V_{in}} \right| = -\tan^{-1}\left(\frac{\omega}{|Z_1|}\right) - \tan^{-1}\left(\frac{\omega}{|P_1|}\right) - \tan^{-1}\left(\frac{\omega}{|P_2|}\right)$$

To shrink effect of  $Z_1$  on phase margin.

$$Z_1 = 10 \cdot GB$$

$$\left| \frac{V_o}{V_{in}} \right| \Bigg|_{\omega=GB} = -\tan^{-1}\left(\frac{GBW}{|Z_1|}\right) - \tan^{-1}\left(\frac{GBW}{|P_1|}\right) - \tan^{-1}\left(\frac{GBW}{|P_2|}\right)$$

$$= -\tan^{-1}\left(\frac{1}{10}\right) - \tan^{-1}(ADC) - \tan^{-1}\left(\frac{GBW}{|P_2|}\right)$$

From definition of Phase Margin:

$$-180^\circ + PM = -5.71 - 90^\circ - \tan^{-1}\left(\frac{GBW}{|P_2|}\right)$$

$$PM = 84.29^\circ - \tan^{-1}\left(\frac{GBW}{|P_2|}\right)$$

Assuming  $PM \geq 60^\circ$

$$84.29^\circ - \tan^{-1}\left(\frac{GBW}{|P_2|}\right) \geq 60^\circ$$

$$\tan^{-1}\left(\frac{GBW}{|P_2|}\right) \leq 24.29$$

$$\frac{GBW}{|P_2|} \leq \tan(24.29)$$

$$|P_2| \geq 2.2 GBW$$

$$Z = 10 \cdot G_B W$$

$$\frac{g_{m_2}}{C_C} = 10 \cdot \frac{g_{m_1}}{C_C}$$

$$g_{m_2} = 10 \cdot g_{m_1}$$

For  $P_M \geq 60^\circ$

$$P_2 = \frac{g_{m_2}}{C_2} \geq 2.2 \frac{g_{m_1}}{C_C}$$

$$10 \cdot \frac{g_{m_1}}{C_2} \geq 2.2 \frac{g_{m_1}}{C_C}$$

$$10 \cdot C_C \geq 2.2 C_2$$

$$C_C \geq 0.22 C_2$$

$$C_2 \approx C_L$$

$$C_C \geq 0.22 C_L$$

- $\omega$  is the angular frequency which unit is rad/sec.  $1\text{Hz} = 2\pi \text{ rad/sec}$ . In the derivations above frequencies are given in rad/sec.
- For the calculations we need to convert to Hz.

Alternate derivation for Phase Margin:

$$-180^\circ + PM = < \frac{V_o(s)}{V_{in}(s)}$$

$$= -\tan^{-1}\left(\frac{GBW}{|Z_1|}\right) - \tan^{-1}\left(\frac{GBW}{|P_1|}\right) - \tan^{-1}\left(\frac{GBW}{|P_2|}\right)$$

$$A_{DC} = \frac{GBW}{|P_1|}$$

$$-180^\circ + PM = -\tan^{-1}\left(\frac{GBW}{|Z_1|}\right) - \tan^{-1}(A_{DC}) - \tan^{-1}\left(\frac{GBW}{|P_2|}\right)$$

$A_{DC}$  very large value hence  
 $\tan^{-1}(x \rightarrow \infty) = 90^\circ$

$$-180^\circ + PM = -\tan^{-1}\left(\frac{GBW}{|Z_1|}\right) + 90^\circ - \tan^{-1}\left(\frac{GBW}{|P_2|}\right)$$

$$PM = 90^\circ - \tan^{-1}\left(\frac{GBW}{|P_2|}\right) - \tan^{-1}\left(\frac{GBW}{|Z_1|}\right)$$

$$|P_2| = \frac{g_{m_2} \cdot C_C}{C_1 C_2 + C_1 \xi + C_2 \xi} ; |Z_1| = \frac{g_{m_2}}{C_C}$$

$$GBW = \frac{g_{m_1}}{C_C}$$

$$PM = 90^\circ - \tan^{-1}\left(\frac{\frac{g_{m_1}}{I_{D_1}} \cdot \frac{C_1 C_2 + C_1 C_C + C_2 C_C}{\xi^2} \cdot \frac{I_{D_2}}{I_{D_1}}}{\frac{g_{m_2}}{I_{D_2}} \cdot \frac{I_{D_2}}{I_{D_1}}}\right)$$

$$- \tan^{-1}\left(\frac{\frac{g_{m_1}}{I_{D_1}} \cdot \frac{I_{D_2}}{I_{D_1}}}{\frac{g_{m_2}}{I_{D_2}}}\right)$$

Using approximate values:

$$PM = 90^\circ - \tan^{-1}\left[\frac{\frac{g_{m_1}}{I_{D_1}} \cdot \frac{I_{D_1}}{I_{D_2}} \cdot \frac{C_L}{C_C}}{\frac{g_{m_2}}{I_{D_2}} \cdot \frac{I_{D_2}}{I_{D_1}}}\right]$$

$$- \tan^{-1}\left[\frac{\frac{g_{m_1}}{I_{D_1}} \cdot \frac{I_{D_1}}{I_{D_2}}}{\frac{g_{m_2}}{I_{D_2}}}\right]$$

$$\text{using } k = \frac{g_{m1}}{I_{D1}}$$

$$\frac{g_{m2}}{I_{D2}}$$

$$PM = 90^\circ - \tan^{-1} \left( k \cdot \frac{I_{D1}}{I_{D6}} \cdot \frac{C_L}{C_C} \right) - \tan^{-1} \left( k \cdot \frac{I_{D1}}{I_{D6}} \right)$$

$$PM = 60^\circ : \tan^{-1}(A) + \tan^{-1}(B) = \tan^{-1} \left( \frac{A+B}{1-AB} \right)$$

$$\tan 30^\circ = \frac{1}{\sqrt{3}} = \frac{k \cdot \left( 1 + \frac{C_L}{C_C} \right) \cdot \frac{I_{D1}}{I_{D6}}}{1 - k^2 \frac{C_L}{C_C} \left( \frac{I_{D1}}{I_{D6}} \right)^2}$$

- DC gain (cap=infinite impedance at low frequency) of first and second stages:

Find the gain of the opamp shown in Fig. 6.3. Assume the power supply is  $V_{DD} = 1.8$  V and a purely capacitive load. Assume the process parameters for the 0.18- $\mu$ m process in Table 1.5.

$$I_{D8} = 20 \mu\text{A}, \quad I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{D5}/2 = (W_5/2W_s)I_{D8} = 100 \mu\text{A}$$

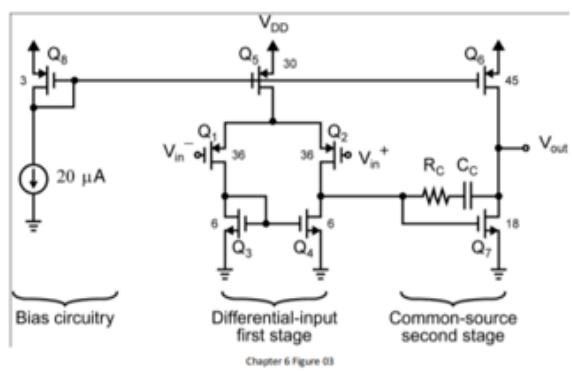
$$I_{D6} = I_{D7} = (W_6/W_s)I_{D5} = 300 \mu\text{A}$$

$$g_{m1} = g_{m2} = 1.30 \text{ mA/V, and } g_{m7} = 3.12 \text{ mA/V.}$$

$$r_{ds} = \frac{1}{\lambda I_{D,out}} \cong \frac{1}{\lambda I_D} \quad r_{ds1} = r_{ds2} = r_{ds3} = r_{ds4} = 37.5 \text{ k}\Omega \quad r_{ds6} = r_{ds7} = 12.5 \text{ k}\Omega$$

$$A_{v1} = -g_{m1}(r_{ds2} \parallel r_{ds4}) = -24.4 \text{ V/V}$$

$$A_{v2} = -g_{m7}(r_{ds6} \parallel r_{ds7}) = -19.5 \text{ V/V}$$



It should be noted again that the hand calculation using the approximate equations above is of only moderate accuracy, especially the output resistance calculation on  $r_{ds}$ . Therefore, later they should be verified by simulation by SPICE/SPECTRE.

However, the benefit of performing a hand calculation is to give an initial (hopefully good) design and also see what parameters affect the gain.



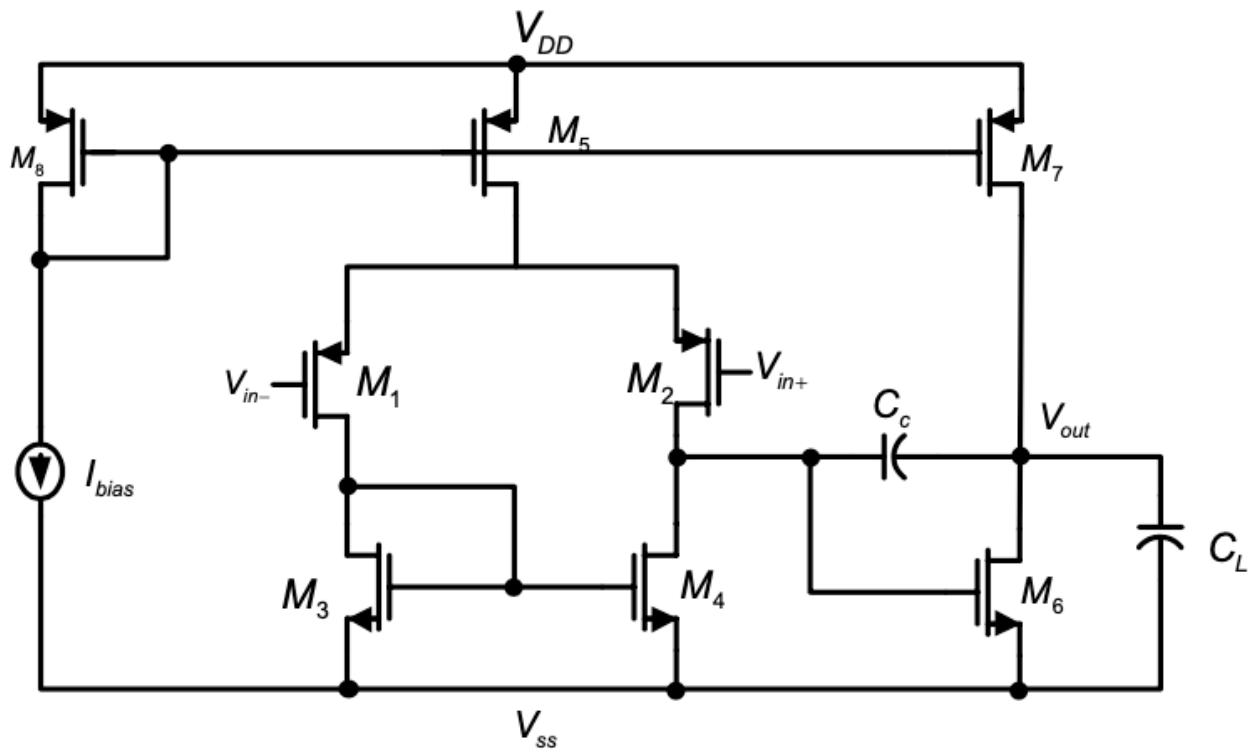
## Design Procedure

Amplifier Design Procedure	
<b>Step 1: Choose <math>g_{m1}/I_{D1}</math></b>	$GBW = \frac{1}{2} \left( \frac{g_{m1}}{I_{D1}} \right) * SR$
<b>Step 2: Choose <math>g_{m6}/I_{D6}</math></b>	$k = \frac{g_{m1}/I_{D1}}{g_{m6}/I_{D6}}$
<b>Step 3: Choose <math>I_{D1}/I_{D6}</math></b>	$\frac{I_{D1}}{I_{D6}} \leq \frac{C_c}{2(C_L + C_c)}$
<b>Step 4: Calculate <math>C_c</math></b>	$\sqrt{3k(1 + \frac{C_L}{C_c})} \left( \frac{I_{D1}}{I_{D6}} \right) = 1 - k^2 \left( \frac{C_L}{C_c} \right) \left( \frac{I_{D1}}{I_{D6}} \right)^2$
<b>Step 5: Check the validity of <math>C_c</math></b>	$\frac{I_{D1}}{I_{D6}} \leq \frac{C_c}{2(C_L + C_c)}$
<b>Step 6: Size M1 &amp; M6</b>	$(\frac{W}{L})_1 = \frac{I_{D1}}{I_{du1}} \quad (\frac{W}{L})_6 = \frac{I_{D6}}{I_{du6}}$
<b>Step 7: Size M3 &amp; M4</b>	
<b>Step 8: Size M5 &amp; M7</b>	

Step 0: Characterize FET find Vdsat, Vth

- M5: 2x size of M1,M2 as it carries twice the current of M1,M2 .
- M8: for a current source of 55uA, sized according to M5 (1/2 of M5).
- M7: sized according to current mirror.
- M3,M4: sized in such a way that the Vgs of M6 will give gm/Id ratio of 10: Vgs=353 mV . (calculations were based on this gm/Id ratio). hint: assume Id proportional to W/L, Vgs: larger W/L for same current then Vgs will go down.

Specs	Specification	Simulated Value
<b>Supply Voltage</b>	1.2 V	1.2 V
<b>Load Capacitor (CL)</b>	5 pF	5 pF
<b>DC Gain</b>	75dB	60dB (Did not design for this assumed Very high value )
<b>Gain Bandwidth</b>	80 MHz	68 MHz
<b>Phase Margin</b>	60°	54.3°
<b>Slew Rate</b>	100 V/ $\mu$ s	



$$C_L = 5 \text{ pF}$$

$$GBW = 80 \text{ MHz}$$

$$SR = 100 \text{ V/μs}$$

$$1] \quad GBW = Y_2 \times \left( \frac{g_{m_1}}{I_{D_1}} \right) \times SR$$

$$\begin{aligned} \frac{g_{m_1}}{I_{D_1}} &= \frac{2 \times 80 \times 10^6 \times 2\pi}{100 \times 10^6} \\ &= 4\pi \times 4/5 = 16\pi/5 = 10 \end{aligned}$$

$$2] \quad \text{Assume } k=1 \quad \frac{g_{m_6}}{I_{D_6}} = 10$$

From  $\text{PM} = 60^\circ$  and placing  $360^\circ > 10 \text{ GBW}$

$$g_{m_6} \geq 10 \cdot g_{m_1}$$

$$\frac{I_{D_1}}{I_{D_6}} = 0.1$$

$$3] \quad \sqrt{3} \times \left( 1 + \frac{C_L}{C_C} \right) \frac{I_{D_1}}{I_{D_6}} = 1 - k^2 \left( \frac{C_L}{C_C} \right) \left( \frac{I_{D_1}}{I_{D_6}} \right)^2$$

$$\begin{aligned} C_C &= 0.22 C_L \\ &= 1.1 \text{ pF} \end{aligned}$$

$$4] \quad SR = \frac{100 \times 10^6}{1/5} \text{ V/μs} = \frac{2 I_D}{C_C}$$
$$= \frac{100 \times 10^6 \times 1/1 \times 10^{-12}}{1/5}$$

$$I_{D_1} = \frac{110 \text{ mA}}{2} = 55 \text{ mA}$$

$$I_{D_6} = 550 \text{ μA}$$

$$\text{Verify } \frac{I_{D_1}}{I_{D_6}} \leq \frac{C_C}{2(C_C + C_L)}$$

$$0.1 < \frac{1.1}{12.2} = 0.09$$

5]  $\frac{g_{m_1}}{I_{D_1}} = 10$

10

$$V_{GS} = -340.1 \text{ mV}$$

PMOS:  $I_{D_1} = -2.167 \text{ A}$   $\frac{W}{L} = \frac{600\text{n}}{500\text{n}}$

$$W = \frac{55}{2.167} = \underline{25.3 \times 600\text{n}}$$

10GBW

NMOS:  $I_{D_6} = V_{GS} = 353.2 \text{ mV}$   $\frac{W}{L} = \frac{600\text{n}}{500\text{n}}$   
 $= 4.8 \text{ A}$

$$W = \frac{550}{4.8} = 114.58 \times 600\text{n}$$

$M_3, M_4$ : sized for  $V_{GS}/V_{DS} = 353.2 \text{ mV}$   
 so  $M_6$  is appropriately biased

$$\left| \frac{I_{D_1}}{I_{D_6}} \right|^2$$

$M_7$ : for current to be copied from current source

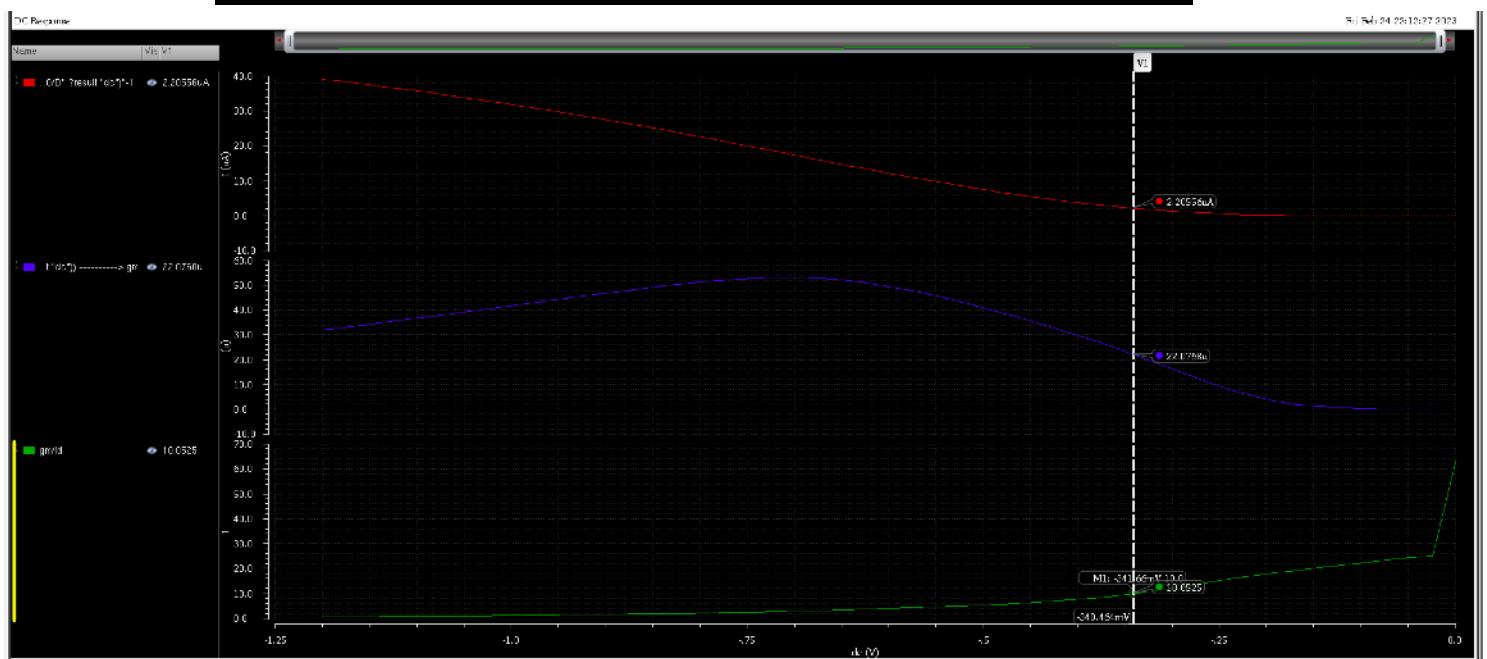
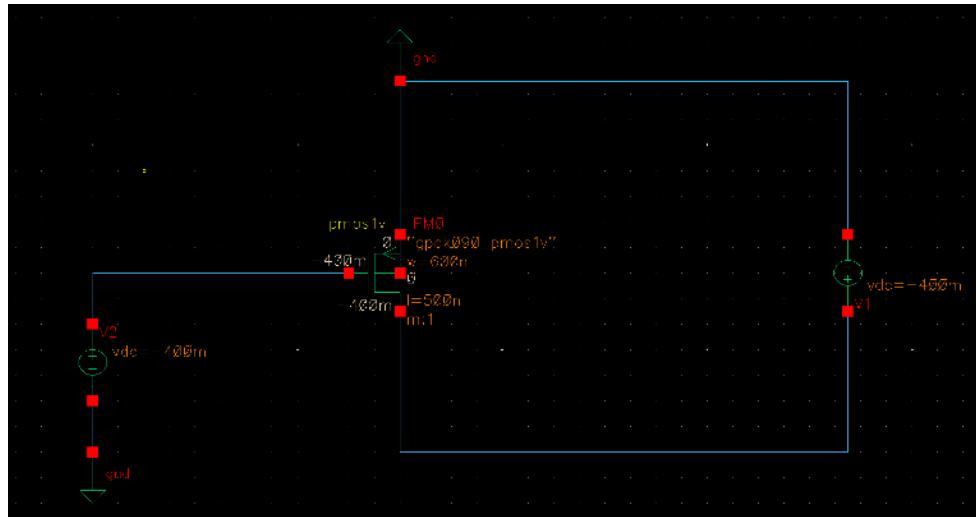
## Simulation and Results

### 1. Characterize FETs (DC Simulations)

For both PMOS and NMOS use W/L=600n/500

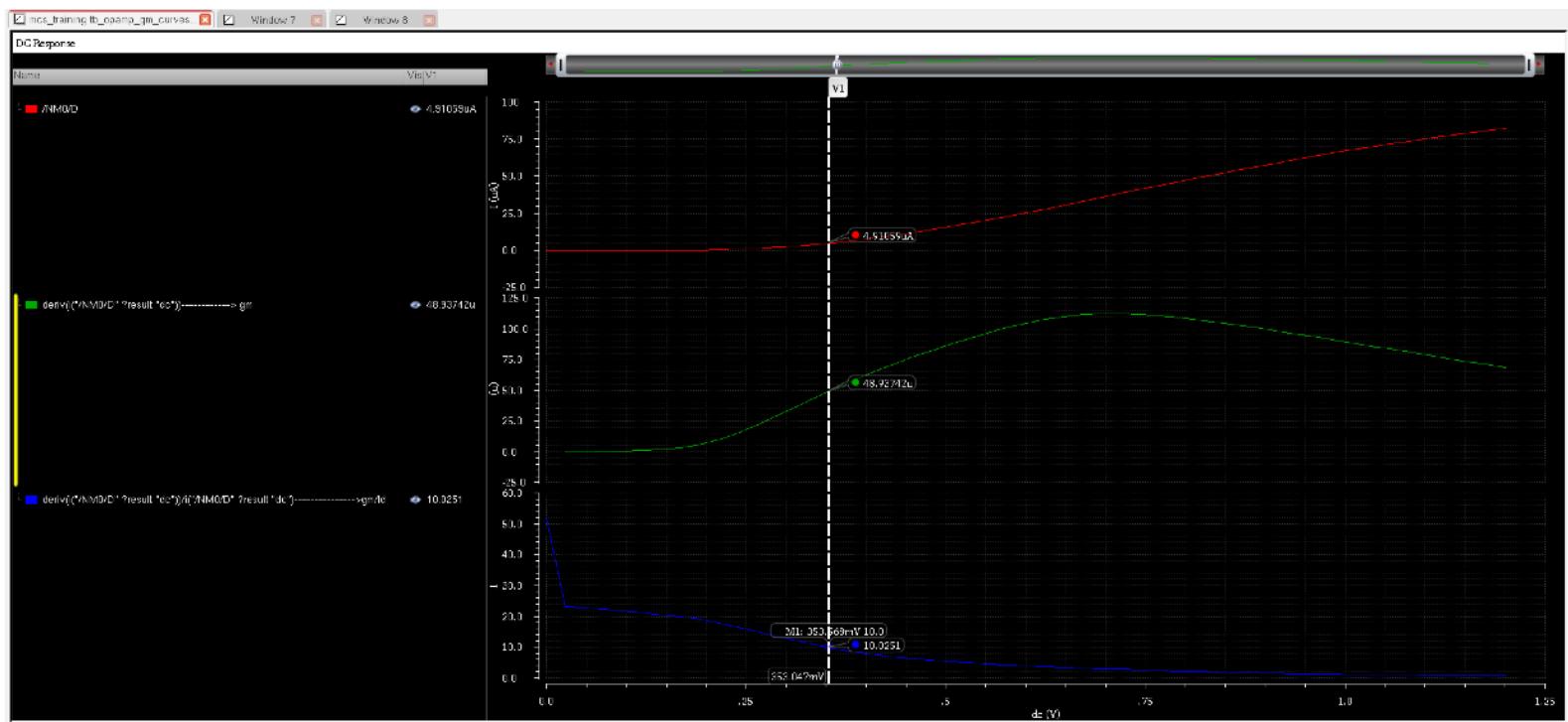
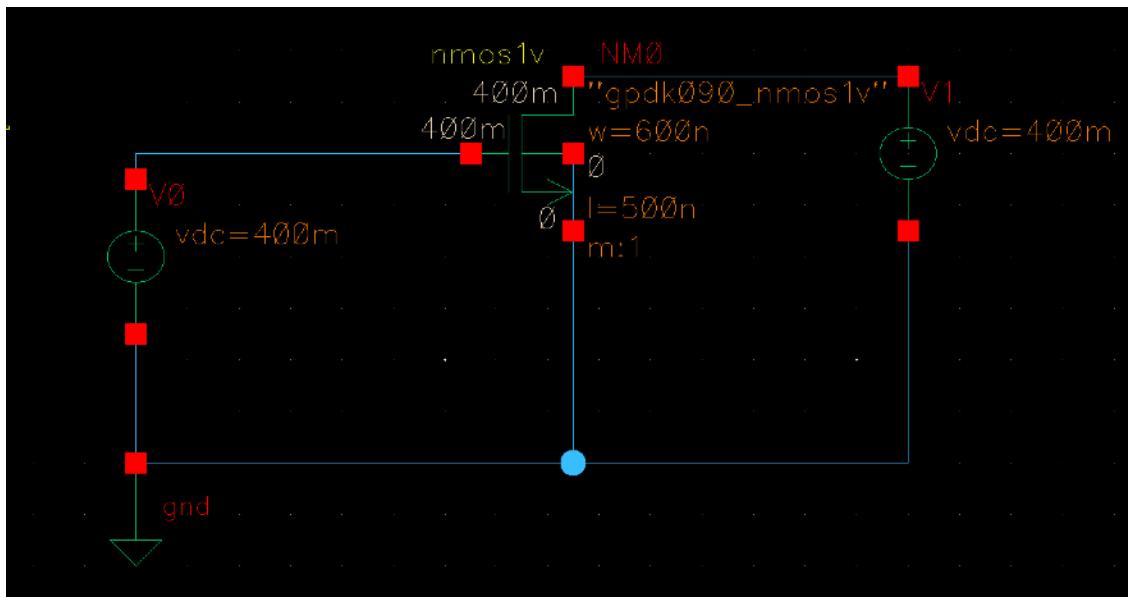
#### a. PMOS:

- use schematic shown with  $V_{DS} = -400\text{mV}$ , sweep  $V_{GS}$  ( $V_g$  from 0 to -1.2 V)
- plot  $I_d$  vs  $V_{GS}$  > using  $I_d$  vs  $V_{GS}$  curve plot  $g_m$  (use derive function in calculator, derive  $I_d$  vs  $V_{GS}$  > plot  $g_m/I_d$  vs  $V_{GS}$ )
- while plotting can multiply y-axis components by -1 for easier viewing
- note down  $V_{th}$ ,  $V_{dsat}$ : -185 mV, -150mV.



b. similarly for NMOS:

- $V_{th}$ ,  $V_{dsat}$ : 191.9 mV, 193.75mV



## 2. Complete Opamp

- a. AC response: ac magnitude 10mV for Vin+ and 0 ac magnitude for Vin-.
- b. DC simulation with Vcm=400mV.

- M5: 2x size of M1,M2 as it carries twice the current of M1,M2 .
- M8: for a current source of 55uA, sized according to M5 (1/2 of M5).
- M7: sized according to current mirror.
- M3,M4: sized in such a way that the Vgs of M6 will give gm/Id ratio of 10: Vgs=353 mV .  
(calculations were based on this gm/Id ratio). hint: assume Id proportional to W/L, Vgs:  
larger W/L for same current then Vgs will go down.
- Finally verify that all transistors are in saturation region.

