



PHASE LOCKED LOOP DESIGN

CpE-6230-Advanced VLSI Design

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ACKNOWLEDGEMENT

We would like to thank Dr.Betner for giving us this opportunity. This project helped us gain an intuitive understanding of a PLL.

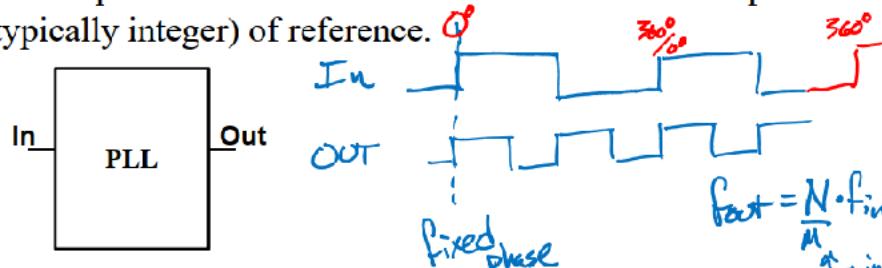
CONTENTS

This report contains the design and simulation results of the following components:

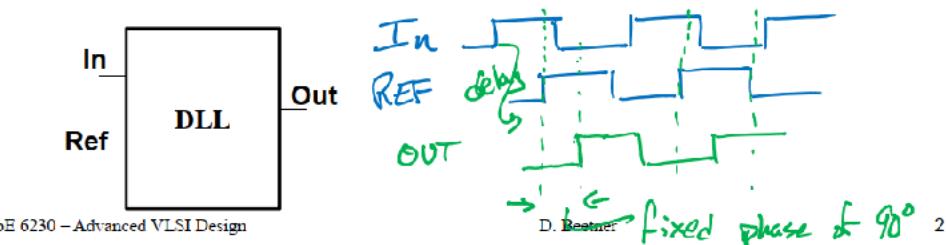
1. Complete PLL design
2. Voltage Controlled Oscillator
3. Charge Pump and Loop Filter
4. Phase and Frequency Detector
5. Frequency Divider
6. Appendix (contains design and simulation of basic gates and D-flipflop)

PLLs and DLLs

- Phase Locked Loop: generates a clock signal with fixed phase with respect to a reference. Could be at a fixed multiple (typically integer) of reference.

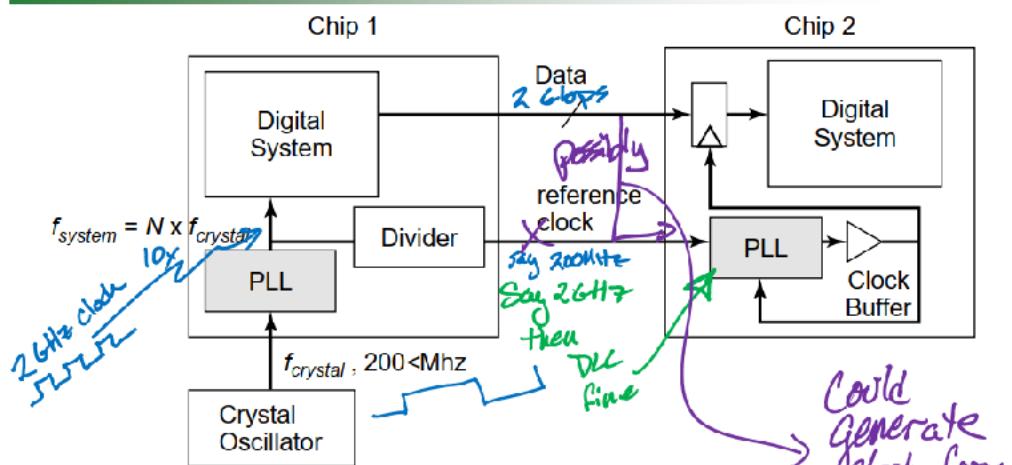


- Delay Locked Loop: generates a clock signal with fixed phase with respect to a reference. Same signal at in and out.



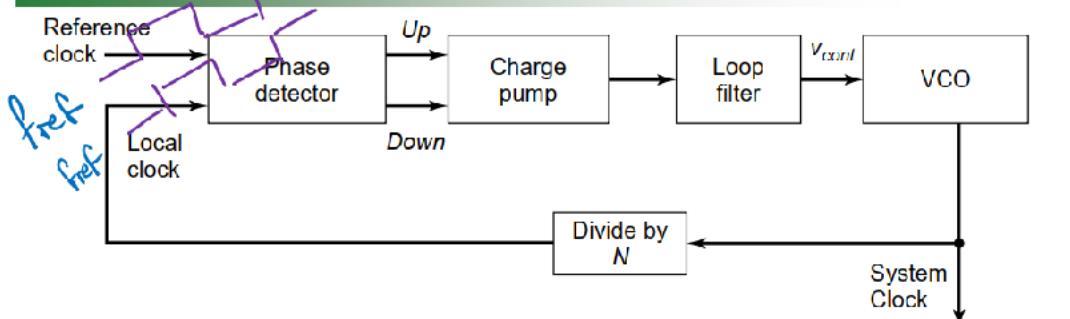
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PLL-Based synchronization and clock multiplication



PLL provides high-frequency internal clock. PLL could also provide high-frequency I/O clock from a reference with optimal phase for sampling data (possibly oversampling). PLL could also be used to generate I/O clock from data. If I/O clock reference same frequency as data, DLL could be used to provide correct phase rather than PLL.

PLL Block Diagram



- VCO – Voltage Controlled Oscillator. Generates a clock signal whose frequency depends on input voltage (V_{cont}).

e.g. $V_{\text{cont}} \text{ low}$

$\text{clock} \rightarrow$ low-freq

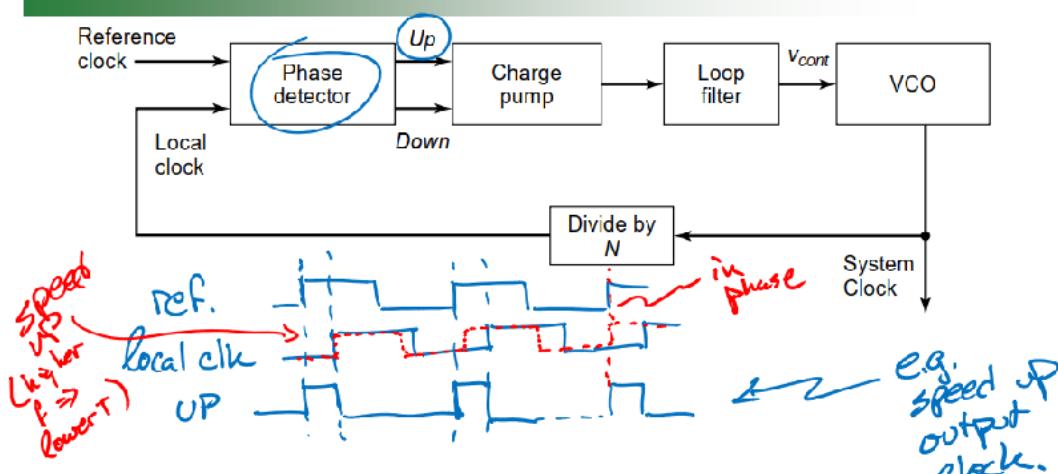
$V_{\text{cont}} \text{ high}$

high-freq.

- Output divided by ‘N’ to compare to reference

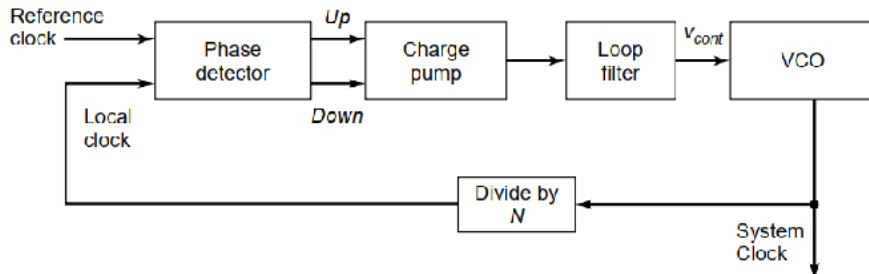
a counter

Phase detector

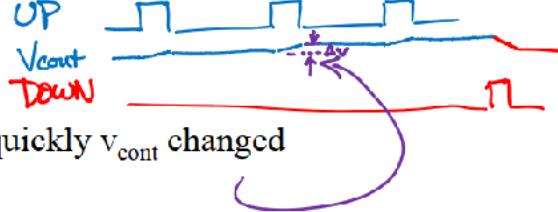


- Phase detector: Compares clock and reference. Generates:
 - “up” if output should speed up (phase lags)
 - “down” if output should slow down (phase leads)

Charge pump and loop filter



- Charge pump + filter: turns “up” + “down” into analog output voltage or current



Applications of PLL:

After some final modifications and fine tuning the PLL design mostly works. The phase detector correctly compares the reference clock with the local clock, and produces the correct speed up and slow down signals when the inputs are not synced. **The charge pump operates to a reasonable extent, and produces the correct control voltage range for the VCO, which in turn generates an output frequency centered at roughly 395MHz.** Finally, the divider successfully provides a correct local clock to be fed back into the phase detector. It takes the PLL roughly 5 microseconds to sync the clock signals.

Unfortunately, the design is not without flaws. After the 5 microsecond mark the clock signals de-sync from each other due to the inability of the up signal to release on time. As to why this event occurs it seems that the control voltage cannot decay fast enough between cycles, likely due to the incredibly large RC network in the loop filter. As a consequence the PLL appears to be stuck in an endless speed up loop. Secondly, the output gain is still absurdly large at roughly 900MHz/V due to the very large 180MHz bandwidth.

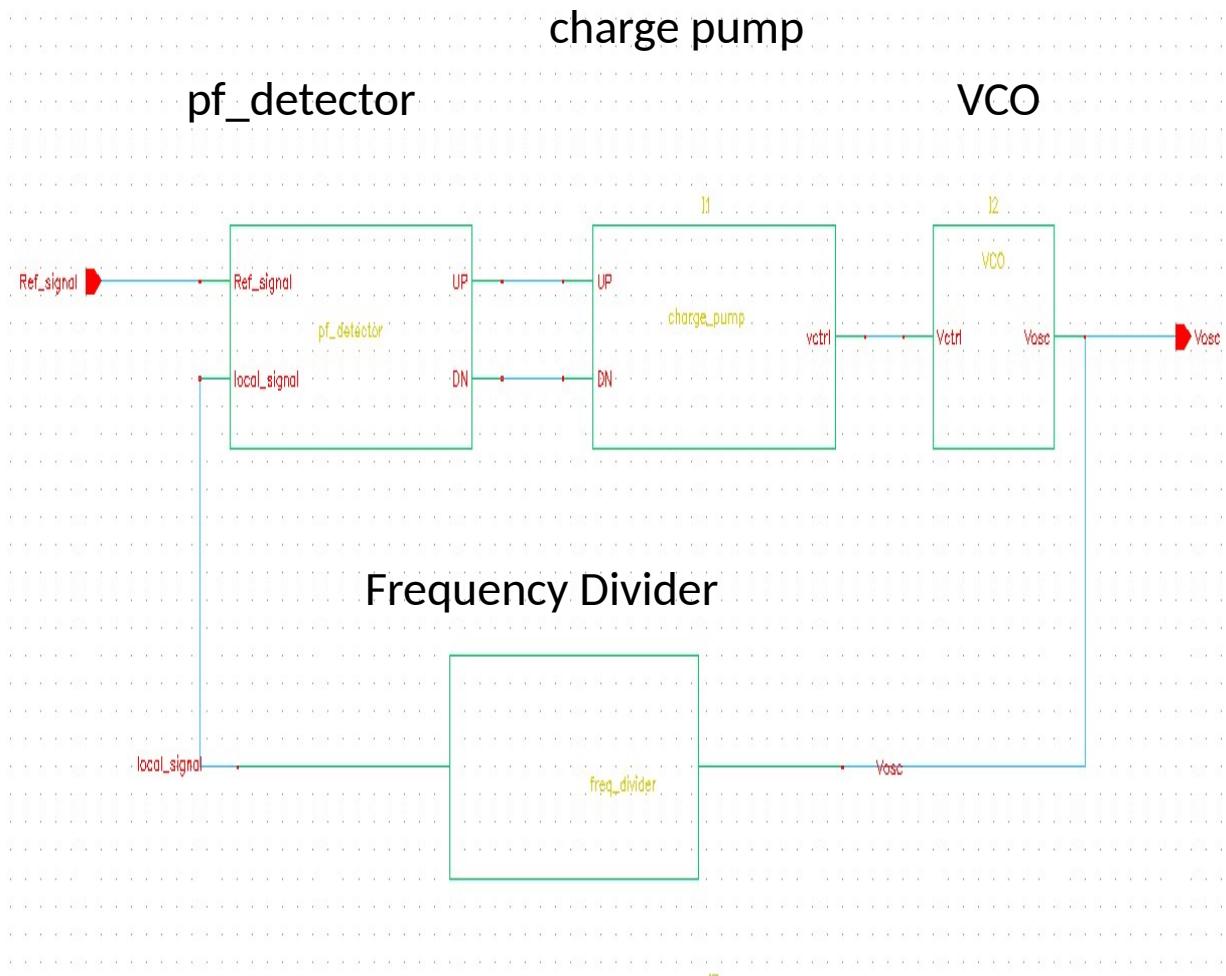
Specifications:	To be Designed	Simulation Results
Vdd		1.0 V
VCO i/p voltage:		0.8 to 1.0 V
Bandwidth (output freq range):		290 MHz – 470 MHz
Settling/Lock time:		4 uS
Output Gain:		900MHz/V

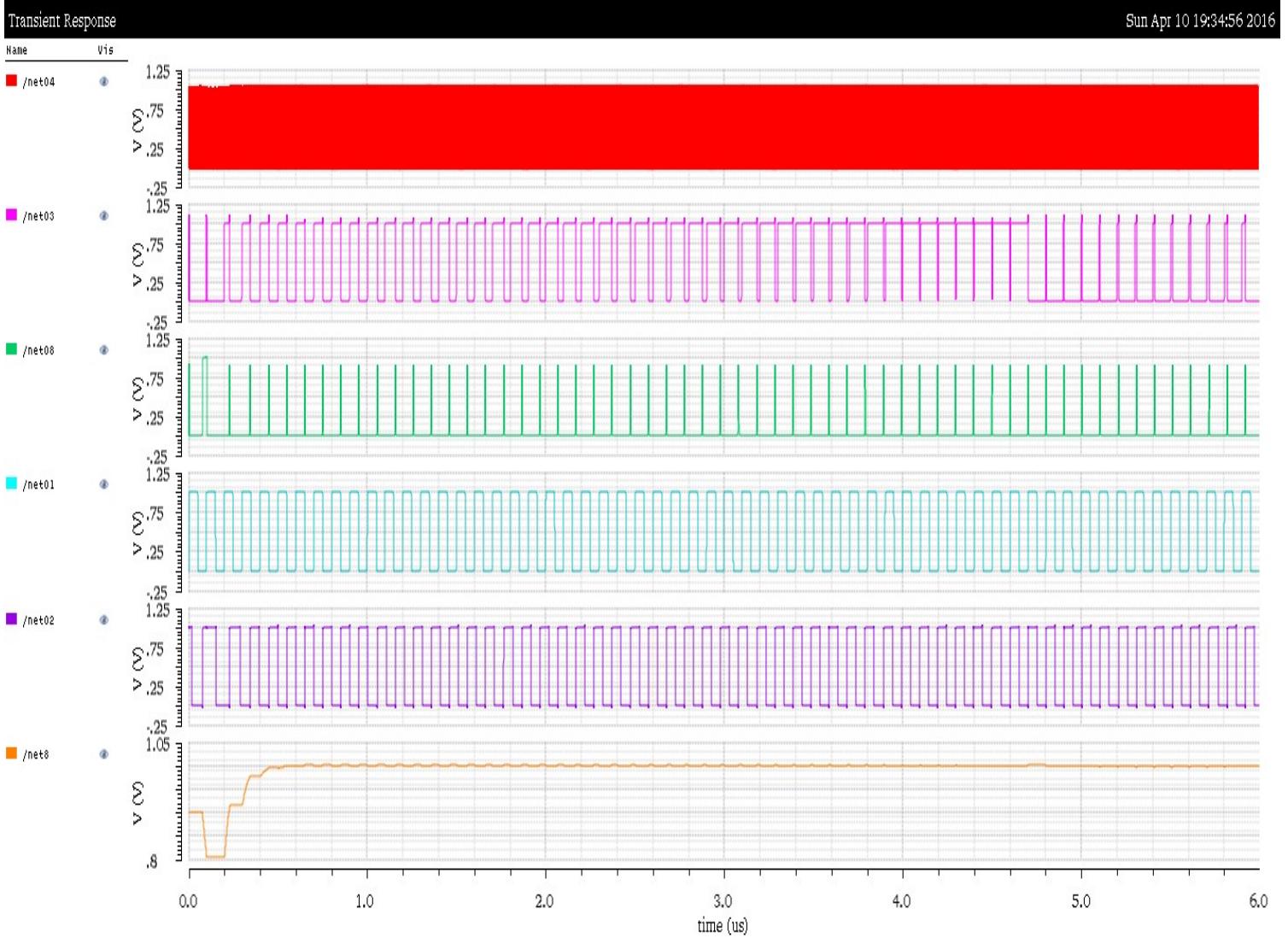
Settling time/lock time/bandwidth definitions???Do some research on technical specifications

For complete PLL simulation, pwl waveform added in feedback of VCO, for input initial condition (for more details look at VCO_final.docx). (<https://www.youtube.com/watch?v=VvkHPoSVpVc>). Initially did not give any phase difference b/w reference and local clock.

Changes made from individual simulation: (VCO and loop filter)

Complete PLL Schematic

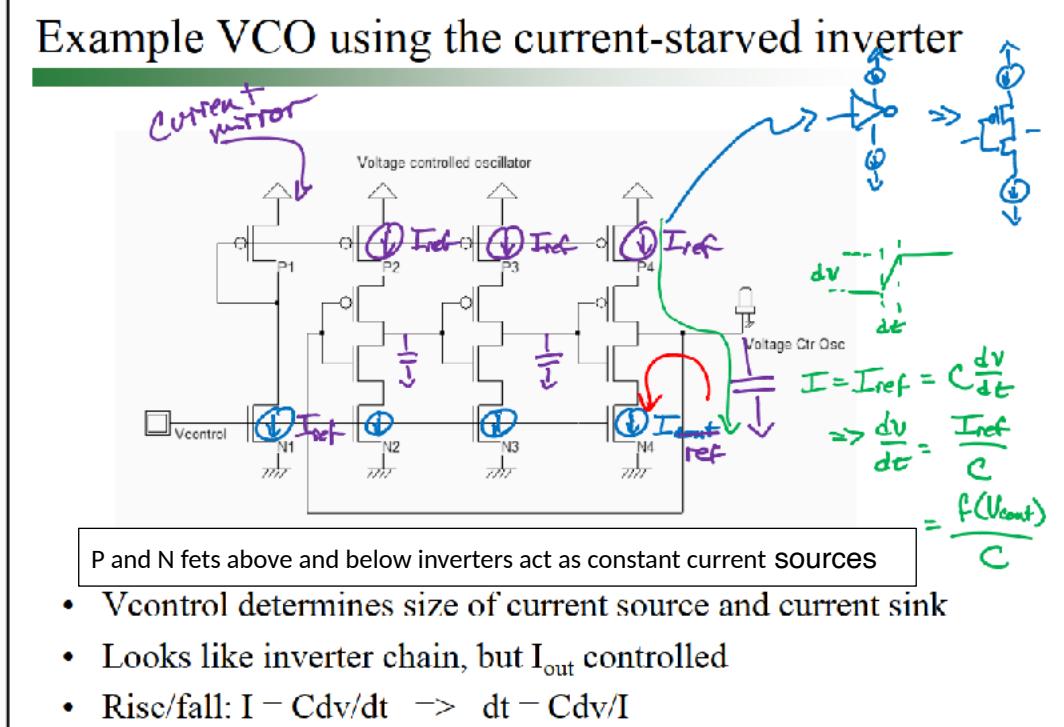
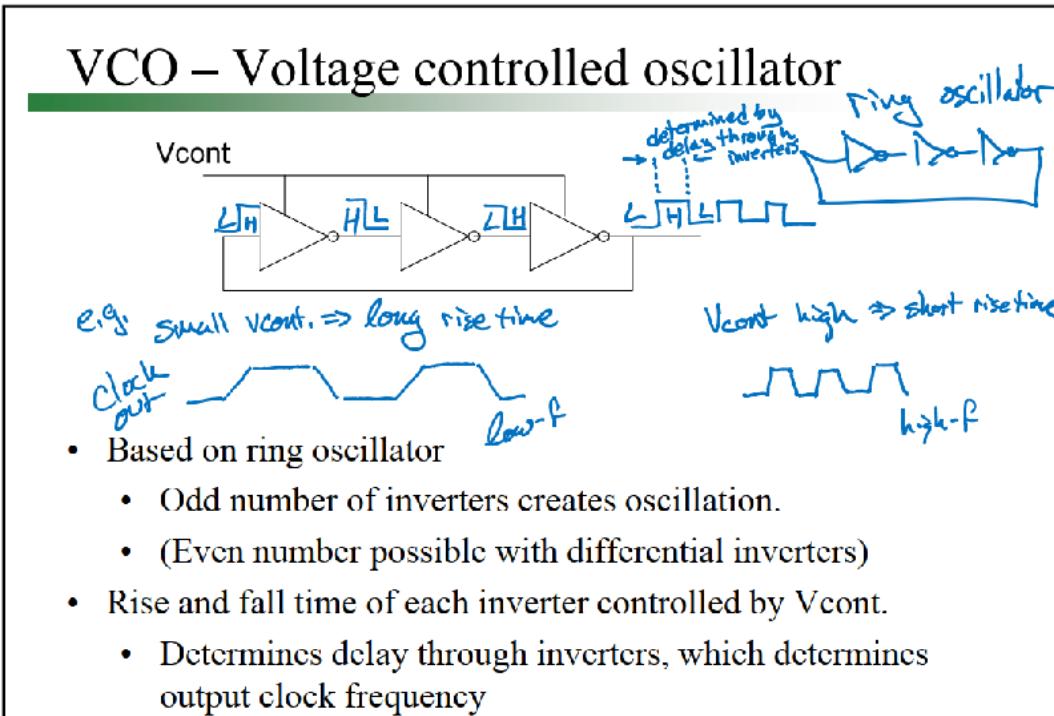


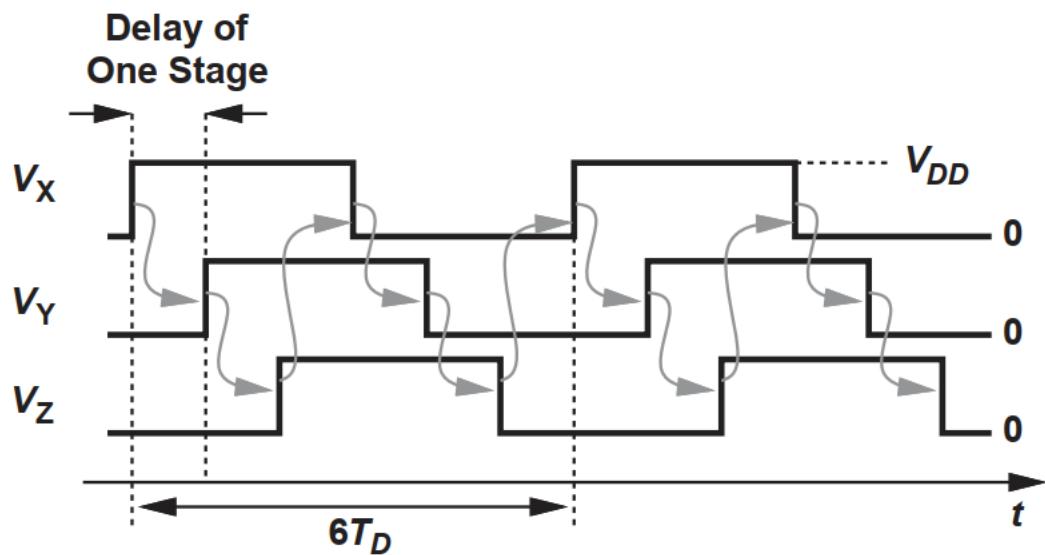
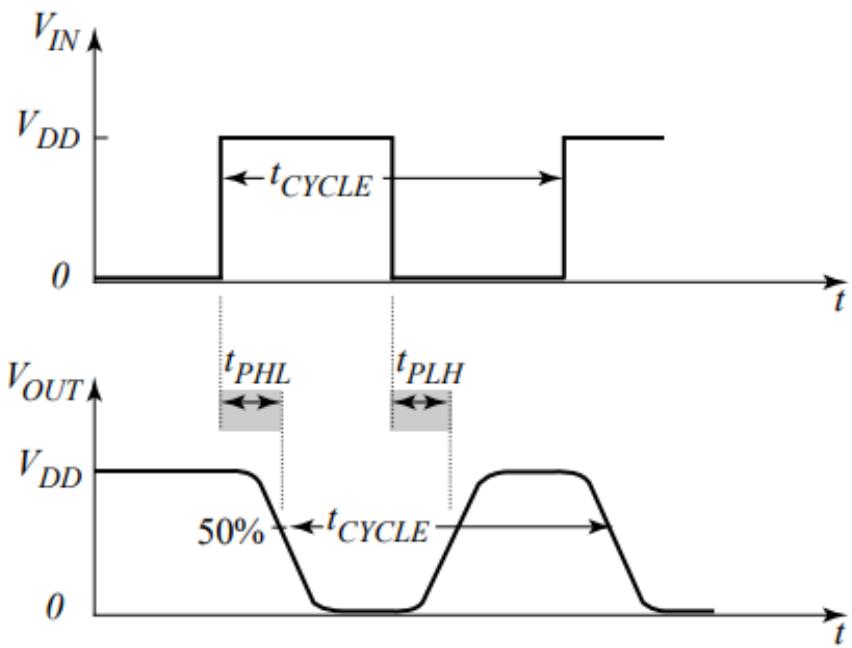


PLL Simulation Results. The above signals from top to bottom are: Output oscillator frequency, Up Signal, Down Signal, Reference Clock, Local Clock, Control Voltage.

1. Voltage Controlled Oscillator

Background Theory:





Ring oscillator waveforms.

Donot use inverter delay equations derived at the end, as the next stage is charged/discharged by a constant current source.

VCO

- For low power consumption using min-sized FETs for current source/sink. [$W/L = \frac{120}{45}$]
- $V_{ctrl} : 0.8V - 0.1V$ [to keep NMOS in saturation]
- O/p Frequency: 400MHz
- $4n C_{ox} = 116.81 \text{ nA/V}^2$
- $V_{thn} = 0.45V$
- Short channel FET, hence used V_{ctrl} and simulated I_o vs V_{ds} graph.
- Found $I_o = 21.34\text{A}$

$V_{se} = I_o = 18\text{mA}$ [use a smaller value as current mirror wont copy]

$$f = 400\text{MHz} =$$

$$2 \times N \times T_p = \frac{1}{400 \times 10^{-6}}$$

$$T_p = 0.25 \times 10^{-9} \text{ seconds}$$

$$T_p = 0.25 \times 10^{-9} \text{ s}$$

$$I_{D,n} = C_L \times \frac{dV}{dt} = C_L \times \frac{V_{DD}/2 - 0}{T_p - 0}$$

$$C_L = \frac{I_{D,n} \times T_p \times 2}{V_{DD}} = 9\text{fF}$$

$$C_L = C_{out} + C_{in} = C_{ox} (W_p L_p + W_n L_n) + \frac{3}{2} C_{ox} [W_p L_p + W_n L_n]$$

$$C_L = \frac{5}{2} \times C_{ox} \times [W_p L_p + W_n L_n]$$

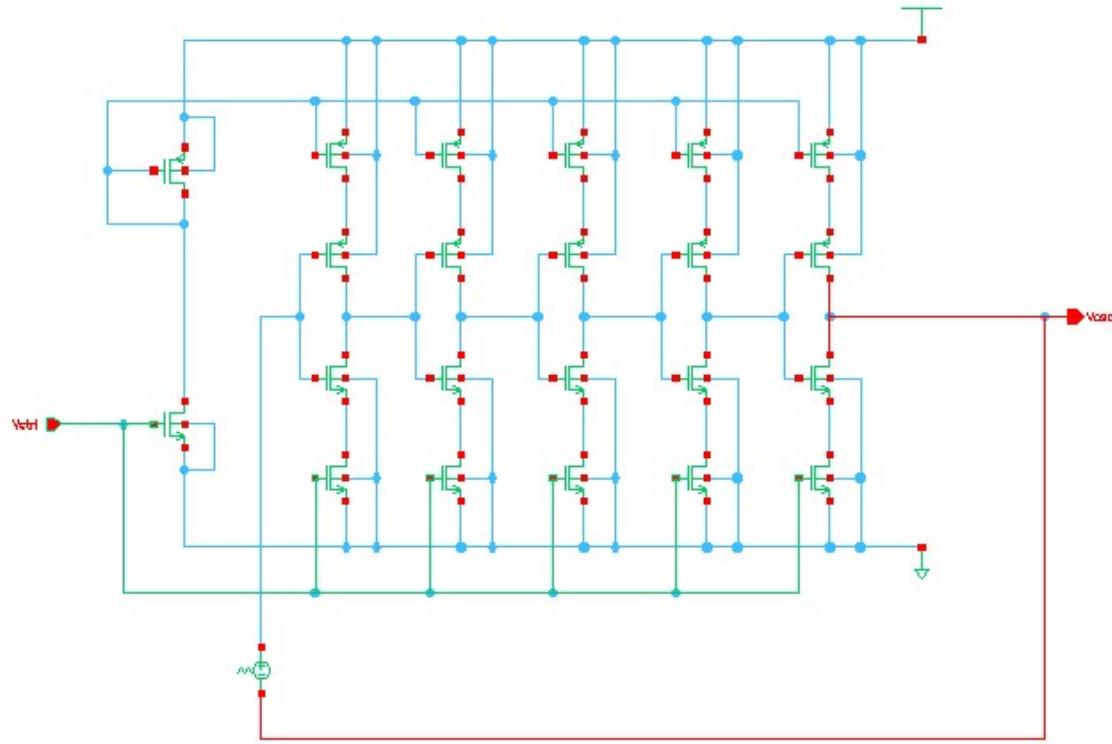
$$9 \times 10^{-15} = \frac{5}{2} \times 15FF \times \frac{1}{4m^2} [W_p + W_n] \times 45 \times 10^{-9}; C_{ox} = \frac{15FF}{4m^2}$$

$$9.0 \text{ fF} = 2.5 \times \frac{15.0 \times 10^{-15}}{10^{-12}} \times [2 \times W_p] \times 45 \times 10^{-9}$$

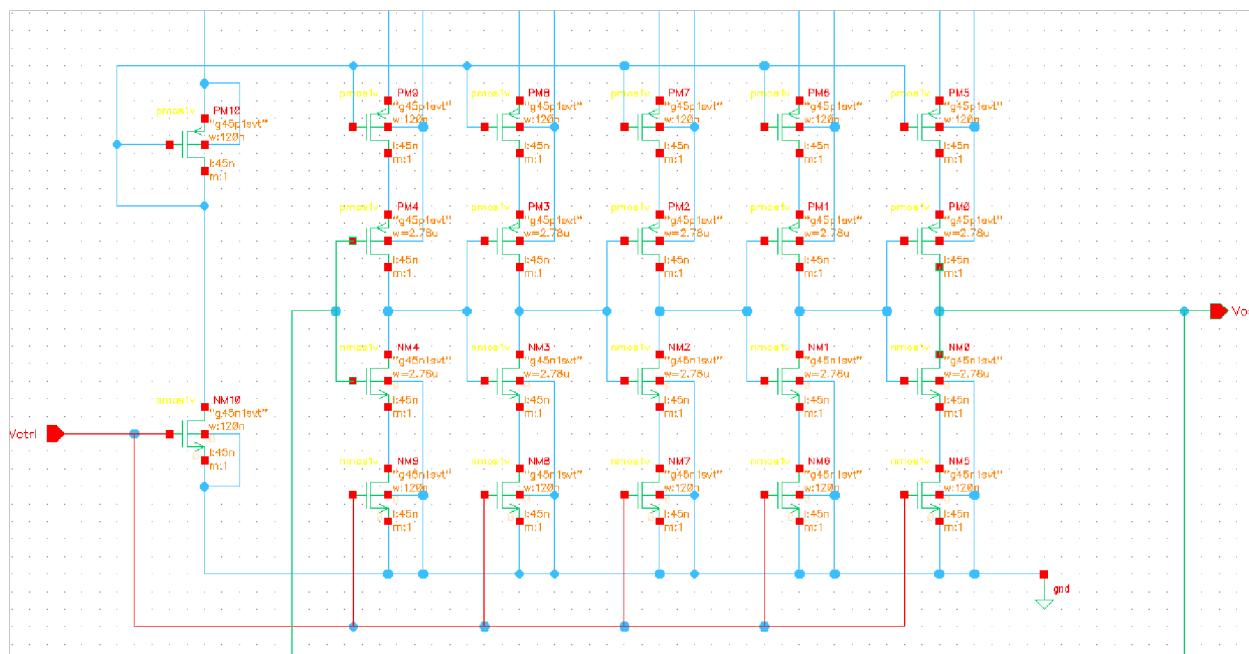
~~*~~ $W_p = 2.66 \text{ } \mu\text{m}$

How is this Capacitance derived?

The VCO follows a current starved inverter design using a five stage inverter ring for the oscillator. All of the FETs are minimum sized except for the NFETs and PFETs that make up the ring oscillator inverters. The width of these FETs have been scaled up to $2.78\mu\text{m}$ (roughly 125 lambda) in order to reach a center frequency of 400MHz.

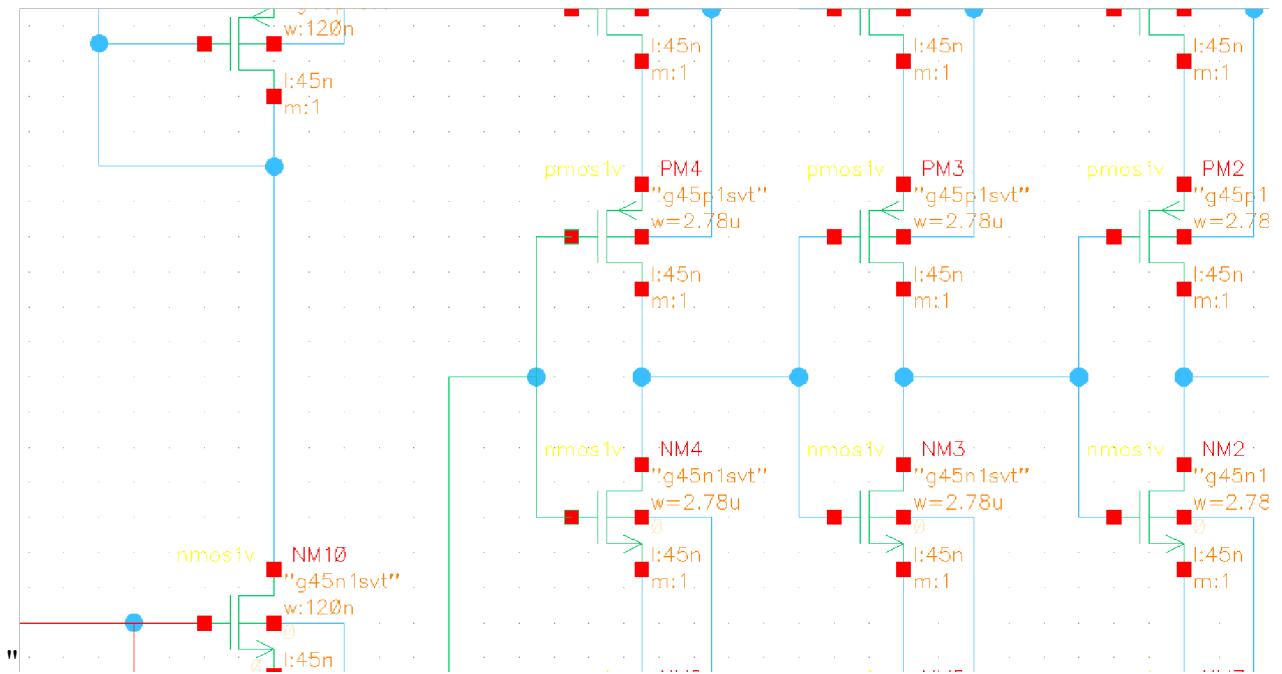


Full schematic of VCO (used in complete PLL simulation, pwl source added)



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Full schematic of VCO demonstrating transistor sizes



Enhanced image demonstrating section of VCO

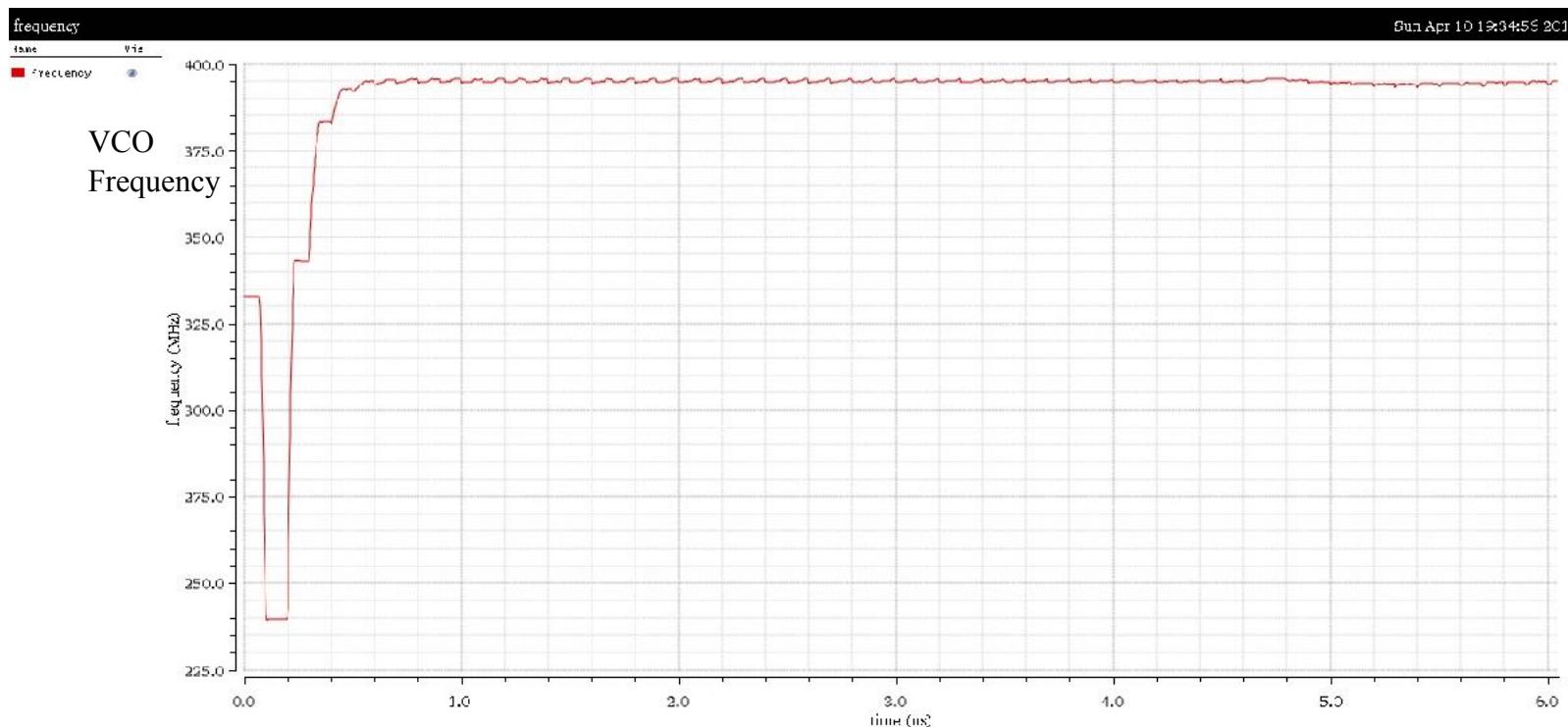
Enhanced image of step voltage source on the ring oscillator

The VCO input voltage is 0.8V to 1V with the center voltage at 0.9V. This new range was selected based on earlier problems that arose from the large difference in current at the 0.4V to 0.6V control voltage range. At 0.4V the NFETs that are part of the current sinks are barely turned on because the threshold voltage is about 0.35V. However, at 0.6V the NFETs were pulling much more current at values ranging from 10 to 20 times greater than at the 0.4V input. This exponential increase in current created a very large oscillation frequency bandwidth that was usually at least 500MHz wide. To decrease this bandwidth, the input voltage was scaled up so that the NFETs could fully turn on. As expected the total bandwidth decreased significantly to roughly 180MHz (~290MHz to ~470MHz).

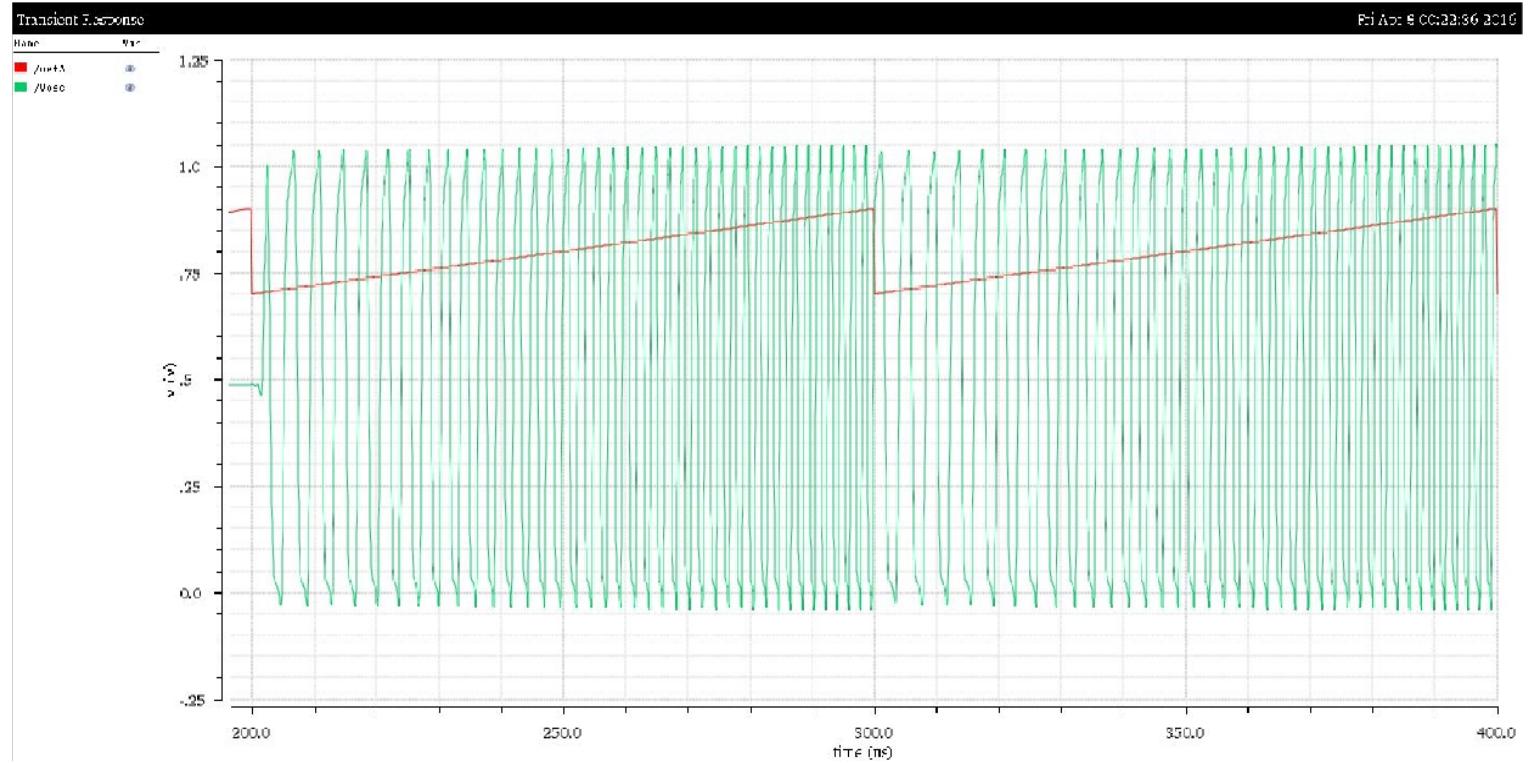
Simulation method for VCO:

One issue that persisted since the beginning of the design had to do with simulating the VCO with a DC input. The problem was that any DC input used for the control voltage, whether it be a flat DC voltage or a DC sweep, gave a flat output of VDD, VSS, or VDD/2. The cause of this problem is still unknown, but two workarounds were eventually discovered. One solution was to use a modified voltage pulse input to represent the control voltage. In this case a periodic signal ranging from 0.8V to 1V was given a rise time equal to the period so that the entire output frequency range could be evaluated. The second case involved setting a step voltage in the feedback loop as an input condition.

VCO Frequency vs time

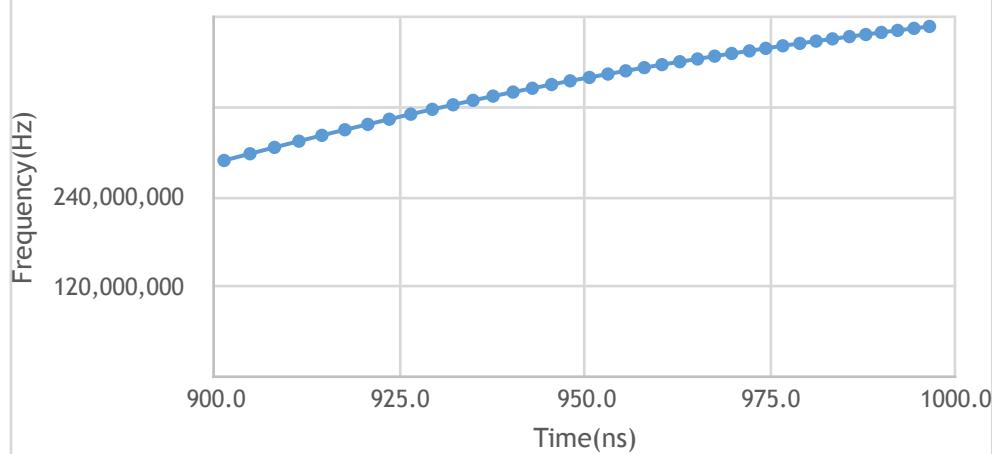


VCO output waveform. Vctrl is the red line increasing from 0.7V to 0.9V.



Note: this simulation is for the individual VCO component only, not the entire PLL design

VCO Component Sim (Vctrl is 0.8 to 1V)



As mentioned before the output bandwidth happens to be roughly 180MHz. Far from the acceptable range of 2MHz, improving the bandwidth was one of the most challenging aspects of the VCO design. While increasing the control voltage helped significantly, it was still not enough. Some other VCO experiments were performed to mitigate the large current differences. One experiment involved changing the lengths of the ring oscillator FETs. This worked to a small extent, but nowhere near enough to justify increasing the FET lengths. The second experiment involved narrowing the control voltage range, which actually did work fantastically at managing the bandwidth. Unfortunately, due to the already strained design limits of the charge pump and loop filter, this method could not be implemented in the PLL without great difficulty, and it would make the already insane component sizes even larger. With some additional current limiting circuitry the output frequency bandwidth could probably be limited to an acceptable range.

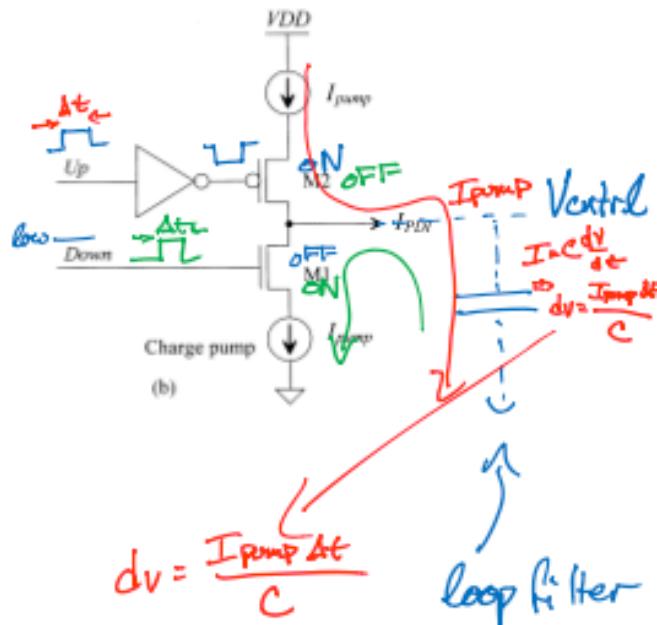
Plot of VCO bandwidth from 900ns to 1000ns. At 900ns Vctrl is 0.8V increasing to 1V by 1000ns

2. Charge Pump and Loop Filter

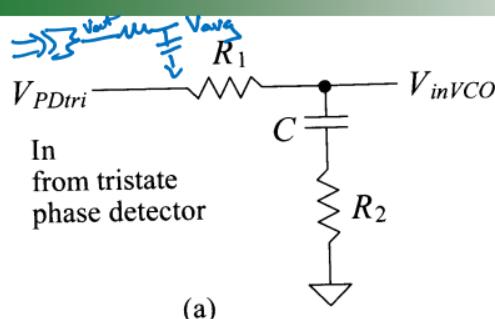
Background Theory:

Charge pump converts “up-down” to analog signal

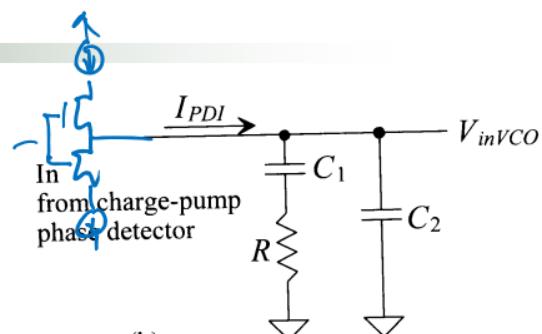
- I_{PDI} used to charge/discharge filter capacitor
 - Up on more than down \rightarrow capacitor charges up, V_{out} rises
- Relatively insensitive to power supply noise



Loop filter



Loop filter for tristate phase detector, or for XOR phase detector



Loop filter for charge pump

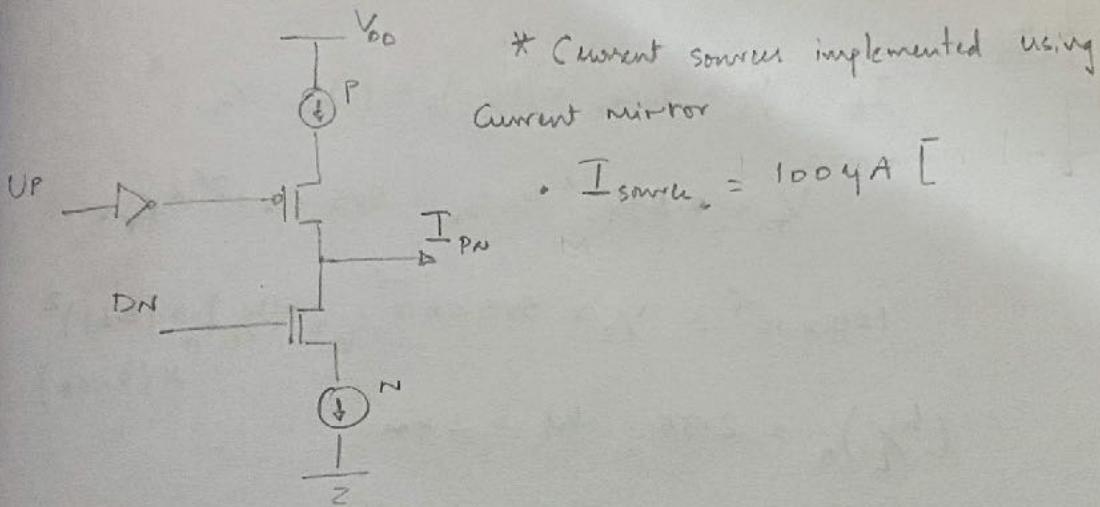
- A slow response time (i.e. low-pass loop filter) is required for good PLL stability and low jitter
 - $RC \gg$ reference clock period
 - Typically takes 10s of cycles or more to adjust
 - Filter can be more complex

*100s of
1000s of
clocks.*

Calculations:

Charge Pump:

- Long channel FETs: $L = 850 \text{ nm}$
- Square law model valid



Current mirror P: $\textcircled{1} P : I_0 = 1004 \text{ A}$

$$-V_{DD} + V_{SD} + I_D \times R = 0$$

$$V_{SD} = V_{SG} = V_{DD} - I_D \times R$$

$$V_{GS} = I_D \times R - V_{DD} = -0.9 \text{ V}$$

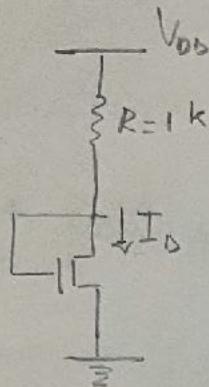
$$R = 1 \text{ k}\Omega \quad V_{DD} = 1.0 \text{ V} ; V_{TP} = -0.47 \text{ V} ; k_p = 385.0 \frac{\text{A}}{\text{V}^2}$$

$$I_{D,P} = \gamma_2 \times \mu_p C_{op} \times \left(\frac{W}{L} \right)_P \times (V_{GS} - V_{TP})^2$$

$$100 \times 10^{-6} = \gamma_2 \times \left(\frac{W}{L} \right)_P \times 385.0 \times 10^{-6} \frac{\text{A}}{\text{V}^2} \times (-0.9 \text{ V} + 0.47)^2$$

$$\left(\frac{W}{L} \right)_P = 2.88 ; \quad W_p = 2.45 \text{ } \mu\text{m}$$

Current Source N: $\textcircled{1}_N$ $I_D = 100\mu\text{A}$



$$-V_{DD} + I_D \times R + V_{DS} = 0$$

$$V_{DS} = V_{GS} = V_{DD} - I_D \times R = 1 - 0.1 = 0.9\text{V}$$

$$I_D = \gamma_2 \times 4_n C_{ox} \times (W_L)_{n} \times (V_{GS} - V_{Tr})^2$$

$$V_{Tr} = 0.49\text{V}; \quad 4_n C_{ox} = 505.0 \times 10^{-6} \text{A/V}^2$$

$$100 \times 10^{-6} = \gamma_2 \times 505.0 \times 10^{-6} / \text{V}^2 \times (W_L)_n \times (0.41)^2 \times (0.168)$$

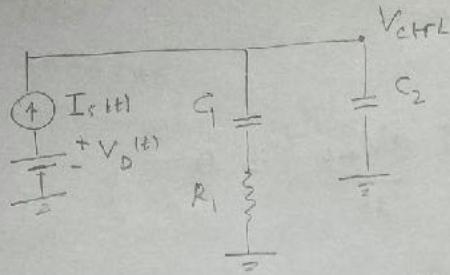
$$(W_L)_n = 2.35; \quad W_n = 2.4\text{m}$$

$I_D = 100\mu\text{A}$ larger current will help reach Vcenter.

Current mirror not copying current properly. Adjusted sizes to match current. Because of the voltage at capacitive node DS drop not large enough to operate in saturation region.

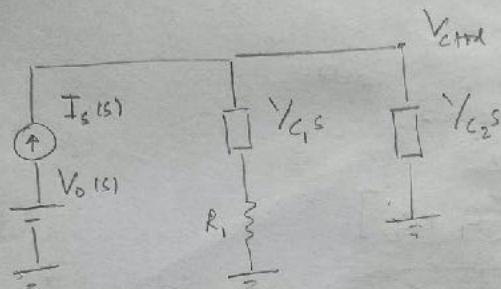
Loop Filter Design : From Razavi (reason for using C2)/PDF

Loop Filter:



$$I_s(t) = I_s [u_1(t) - u_1(t - \tau)]$$

Assuming zero initial conditions:



$$\begin{aligned} I_s(s) &= I_s \left[Y_s - e^{-\tau s} \cdot \frac{1}{s} \right] \\ &= \frac{I_s}{s} \left[1 - e^{-\tau s} \right] \\ &= V_{CTRL} \left[\frac{1}{R_1 + Y_{C_1}} + \frac{1}{Y_{C_2}} \right] \\ &= V_{CTRL} \left[\frac{C_1 s}{R_1 C_1 s + 1} + C_2 s \right] \\ &= V_{CTRL}(s) \left[\frac{C_1 s + R_1 C_1 C_2 s^2 + C_2 s}{1 + R_1 C_1 s} \right] \end{aligned}$$

$$\begin{aligned} V_{CTRL}(s) &= \frac{1 + R_1 C_1 s}{R_1 C_1 C_2 s^2 + (C_1 + C_2)s} \times \frac{I_s}{s} \times \left[1 - e^{-\tau s} \right] \\ &= \frac{R_1 C_1}{R_1 C_1} \left[\frac{1}{R_1 C_1} + s \right] \times \left[1 - e^{-\tau s} \right] \\ &= \frac{1}{R_1 C_1 C_2 s^2 \left[s + (C_1 + C_2) \right]} \times \left[1 - e^{-\tau s} \right] \end{aligned}$$

$$\left[s + \frac{1}{R_1 C_1} \right]$$

$$x [1 - e^{-Is}]$$

$$\frac{C_2 \cdot s^2 \left[s + \frac{C_1 + C_2}{R_1 C_1 C_2} \right]}{}$$

$$= \left[\frac{A}{s} + \frac{B}{s^2} + \frac{C}{s + \frac{C_1 + C_2}{R_1 C_1 C_2}} \right] \cdot [1 - e^{-Is}] \times \frac{I_s}{C_2}$$

$$\frac{s + \frac{1}{R_1 C_1}}{C_2 \cdot s^2 \left[s + \frac{C_1 + C_2}{R_1 C_1 C_2} \right]} = \frac{A}{s} + \frac{B}{s^2} + \frac{C}{s + \frac{C_1 + C_2}{R_1 C_1 C_2}}$$

$$B = \frac{1}{C_1 + C_2} - \frac{C_1 + C_2}{R_1 C_1 C_2} e^{-\frac{C_1 + C_2}{R_1 C_1 C_2} t}$$

$$V_{ctrl}(t) = \left[\left[A \cdot u(0) + B \cdot t + C \cdot e^{-\frac{C_1 + C_2}{R_1 C_1 C_2} (t - \tau)} \right] - \left[A u(t - \tau) + B (t - \tau) + C e^{-\frac{C_1 + C_2}{R_1 C_1 C_2} (t - \tau)} \right] \right] \cdot \frac{I_s}{C_2}$$

Time constant while charging : $\frac{R_1 C_1 C_2}{C_1 + C_2} = \tau$

$$B = \frac{1}{C_1 + C_2}$$

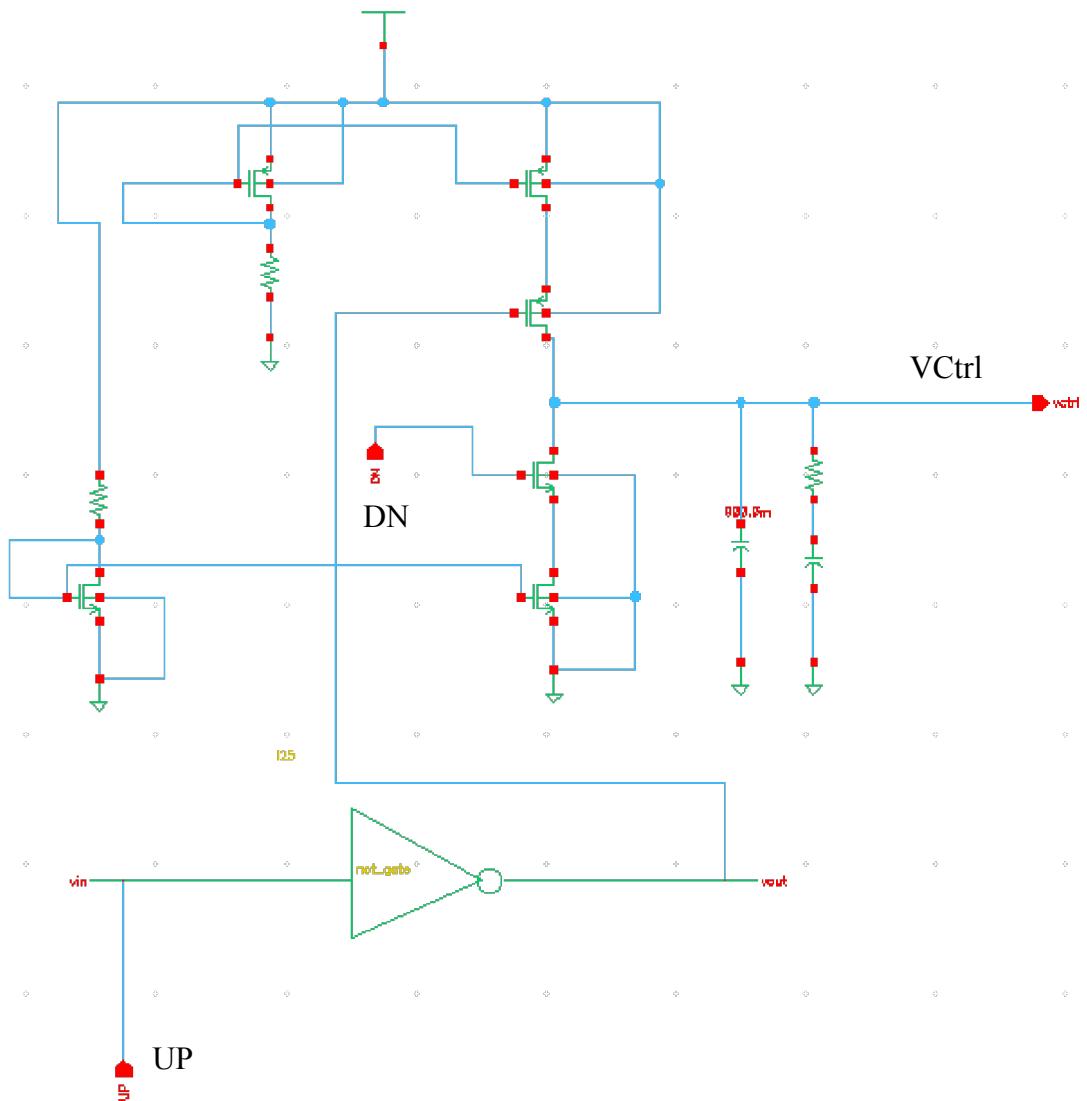
C will be negative,

* larger I_s then $V_{ctrl}(t)$ will reach $V_{control}$
more easily

- Keep capacitors in pico farad range so it will not be affected by the gate capacitance of the next stage (VCO).
- Time constant \gg reference clock period (100ns), constraint taken from slide, from the values used we get 0.9 ms \gg 100 ns.

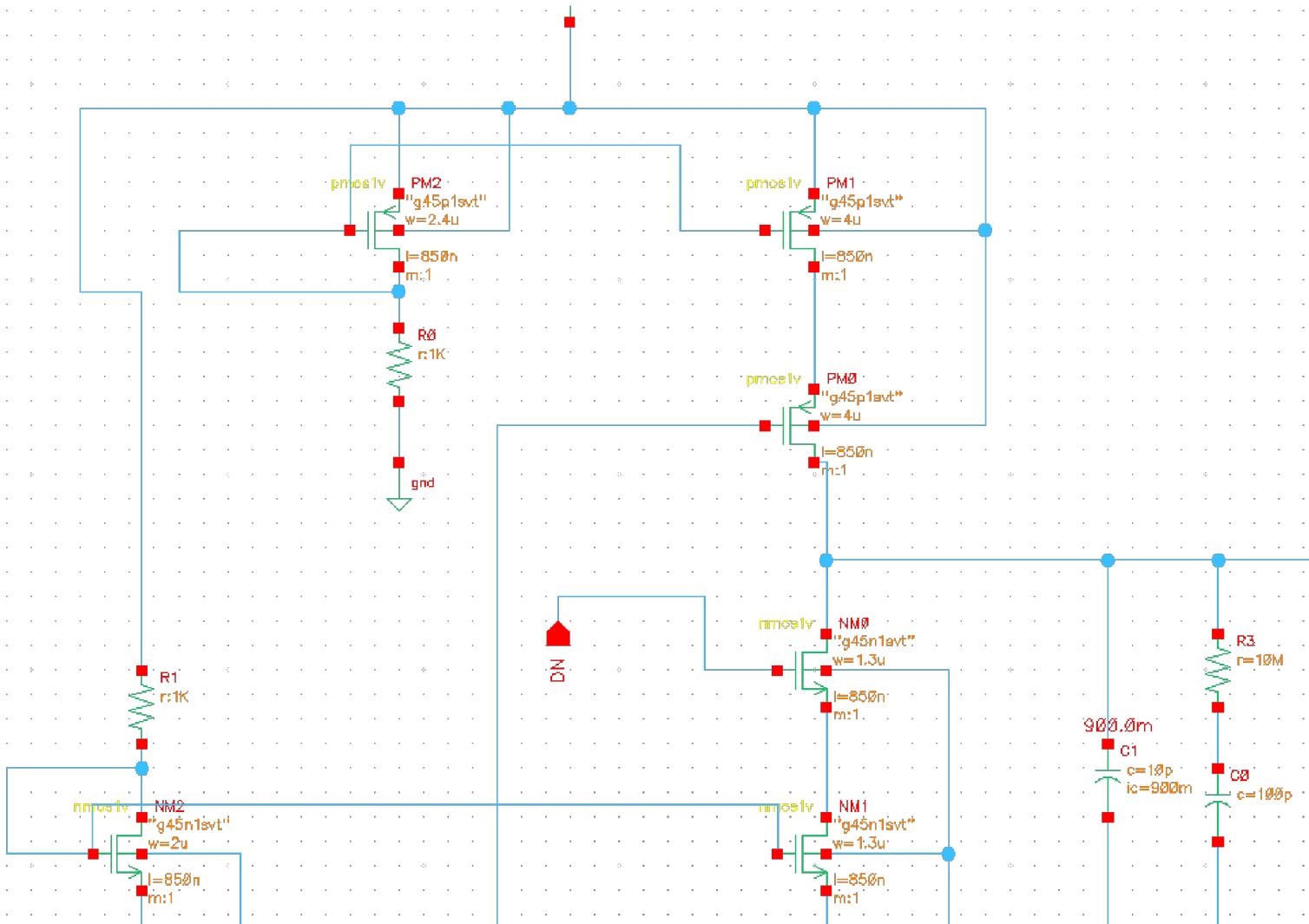
Charge pump is used to convert the UP and DN signals to a control voltage that is fed to the voltage controlled oscillator. Charge pump used a current mirror to produce a constant current to pFET and nFET connected to the UP and DN inputs. The current was set by the adjusting the value of the resistor and size of the transistors. FET sizes were calculated using mathematical formulae and then optimized in cadence to get desired level of current. For control voltage to vary from 0.8V-1V initial condition (0.9V) was set on the control voltage, 0.9V being the center voltage.

Loop filter component values were optimized such that the control voltage varies slowly. Schematic of the charge pump is shown below.



Charge pump schematic

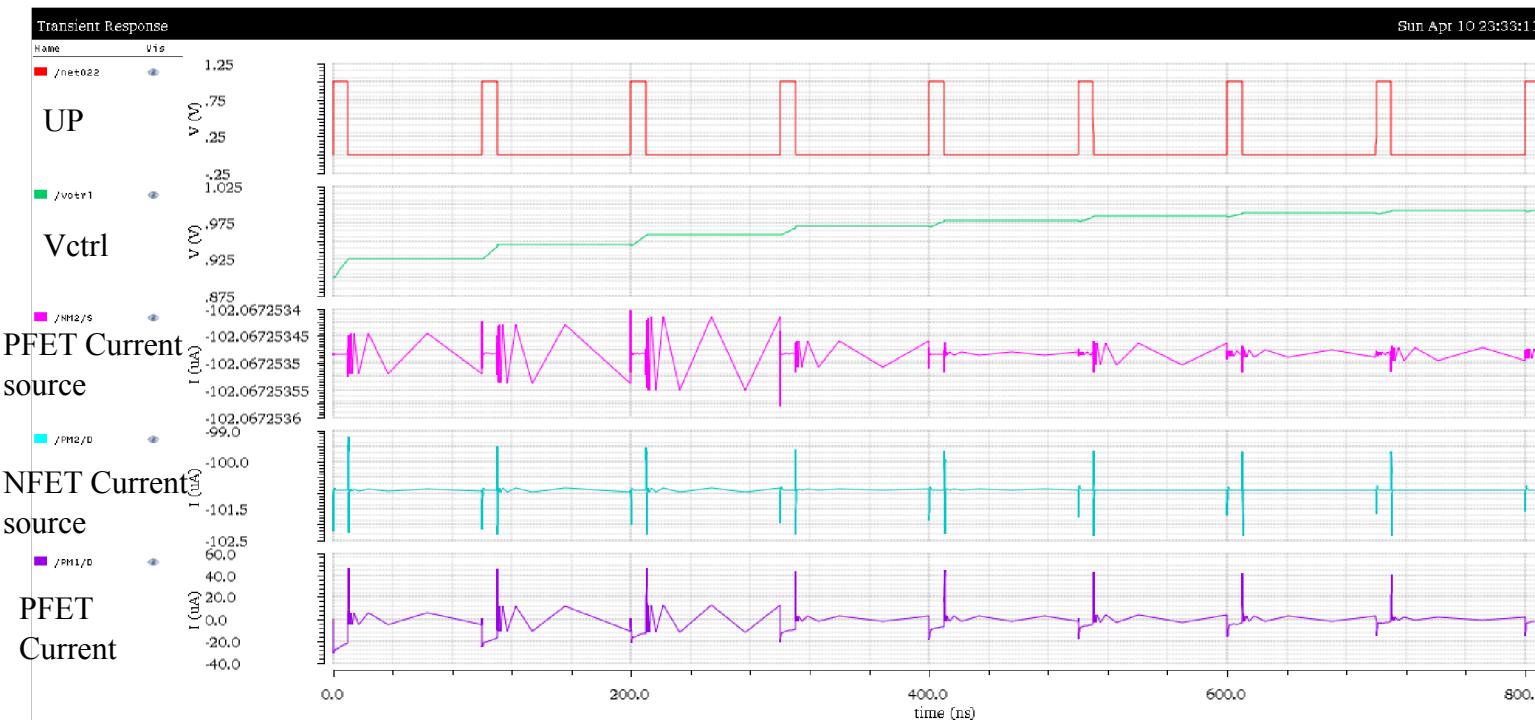
Charge pump schematic close up view



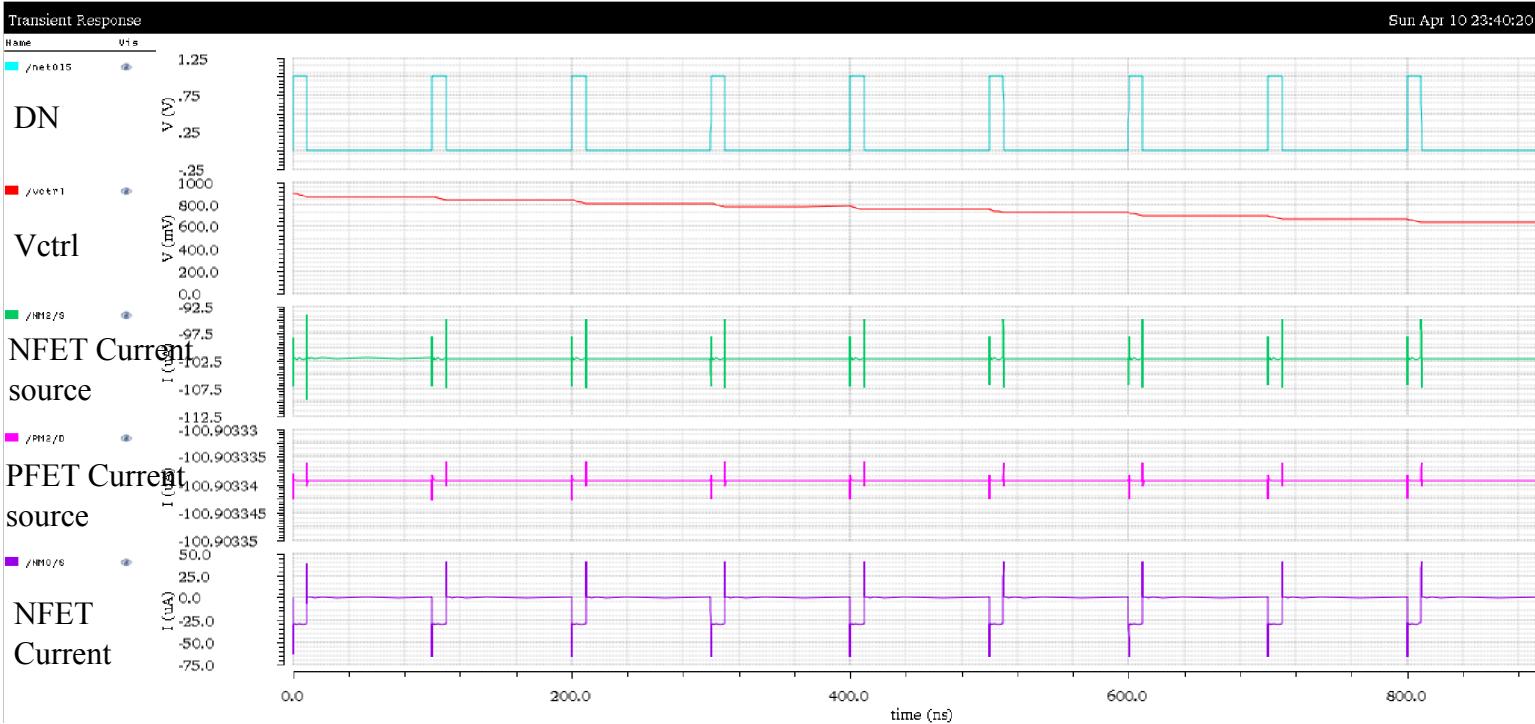
UP and DN signals were given a frequency of 10MHz and pulse width of 10ns for the simulations. The current source FETs produced a current of 100μA with a mismatch of 2μA. NFETs and PFETs connected to UP and DN were sized down to get vcontrol to change slowly.

With NFETS and PFETS sized down the NFET passed a current of 30μA while the PFET passed a current of 15μA. Attempting to optimize the size of the PFET to pass a larger current through it resulted in the PFET being nearly twenty times larger than its current size. This mismatch in current resulted in vcontrol to change more rapidly when the DN signal was high. The PFETs couldn't pass as much current as NFET probably because of the initial condition set on the control voltage, which prevented it from operating in the pinch-off region. (VDS being very low).

The capacitor and resistor values were designed such that $RC \gg 100\text{ns}$, to obtain a vcontrol that changes slowly. The values of resistor and capacitor obtained from Texas Instrument tool could not be implemented as the control voltage changed very rapidly.



PFET connected to UP signal passes a current of $8\mu\text{A}$ when the UP signal is on. It takes approximately three cycles for the control voltage to reach seventy percent of its final value (0.9V - 0.97V).



Simulation results when DN signal is high

When DN signal is high and UP signal is low, the NFETS connected to the DN signal are turned on. It can be seen that the NFET conducts a current of nearly $30\mu\text{A}$ when DN signal is high. Due to mismatch in currents the control voltage reaches its minimum final value in three cycles. With the current already so low and the RC values very large it is difficult to get the NFET to discharge any slower.

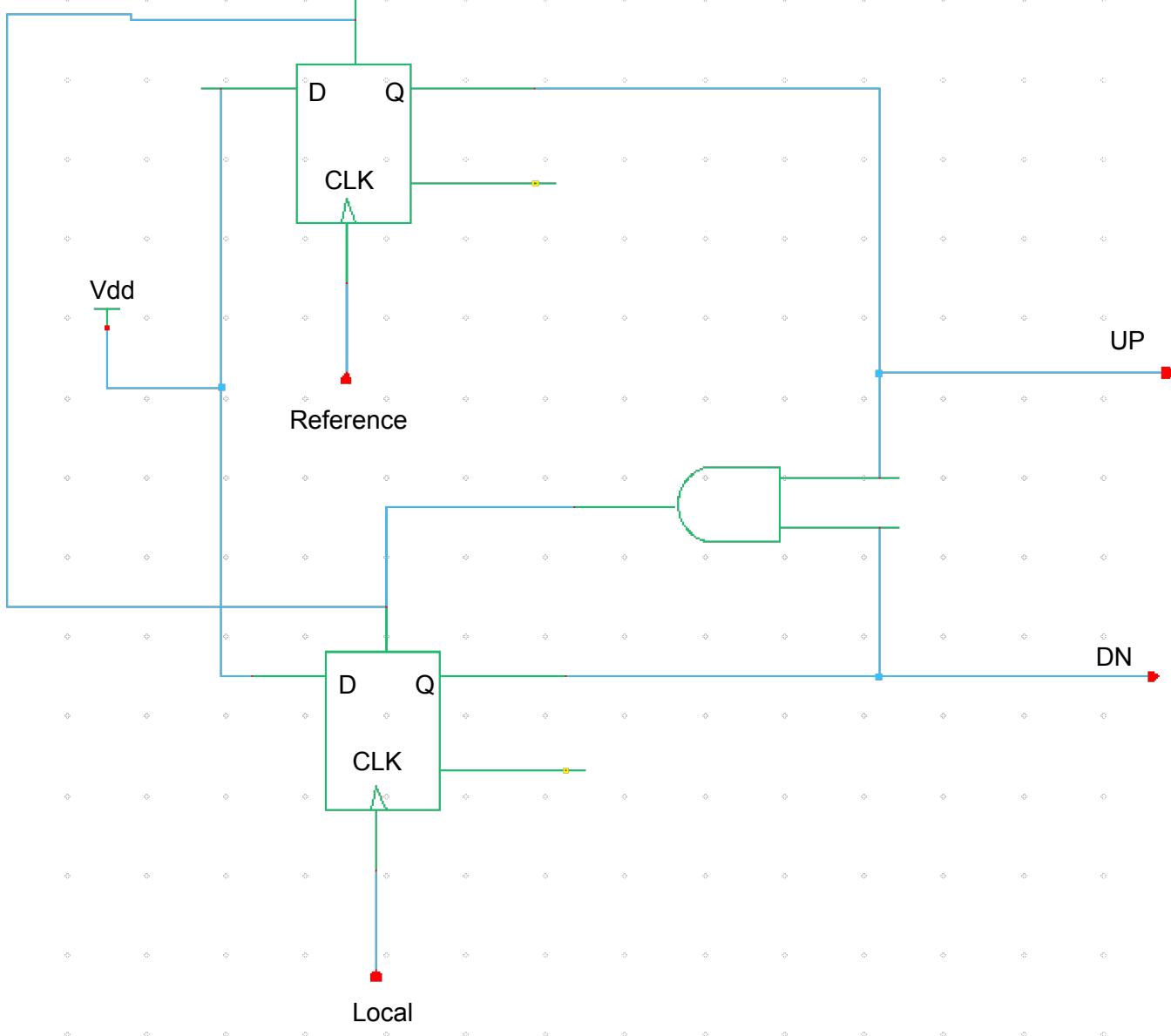
Some more optimization needs to be done to match the current of the current source and that of the FETs. The PFET and NFET current sources could be sized down and the PFET could be fixed so that it passes the same current as the NFET.

3. Phase and Frequency Detector

Background Theory: (take from AVLSI Slides)

Mention/Study types of Detectors

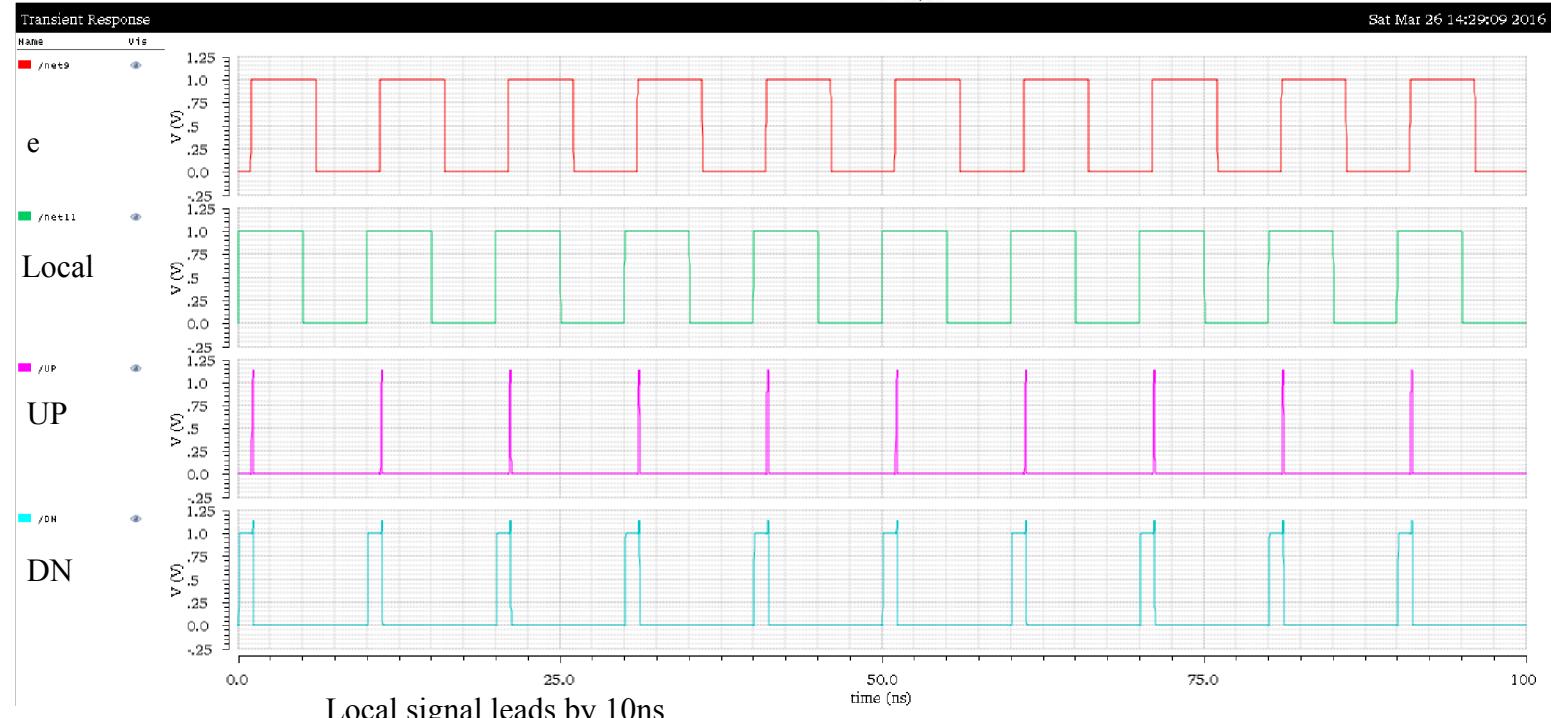
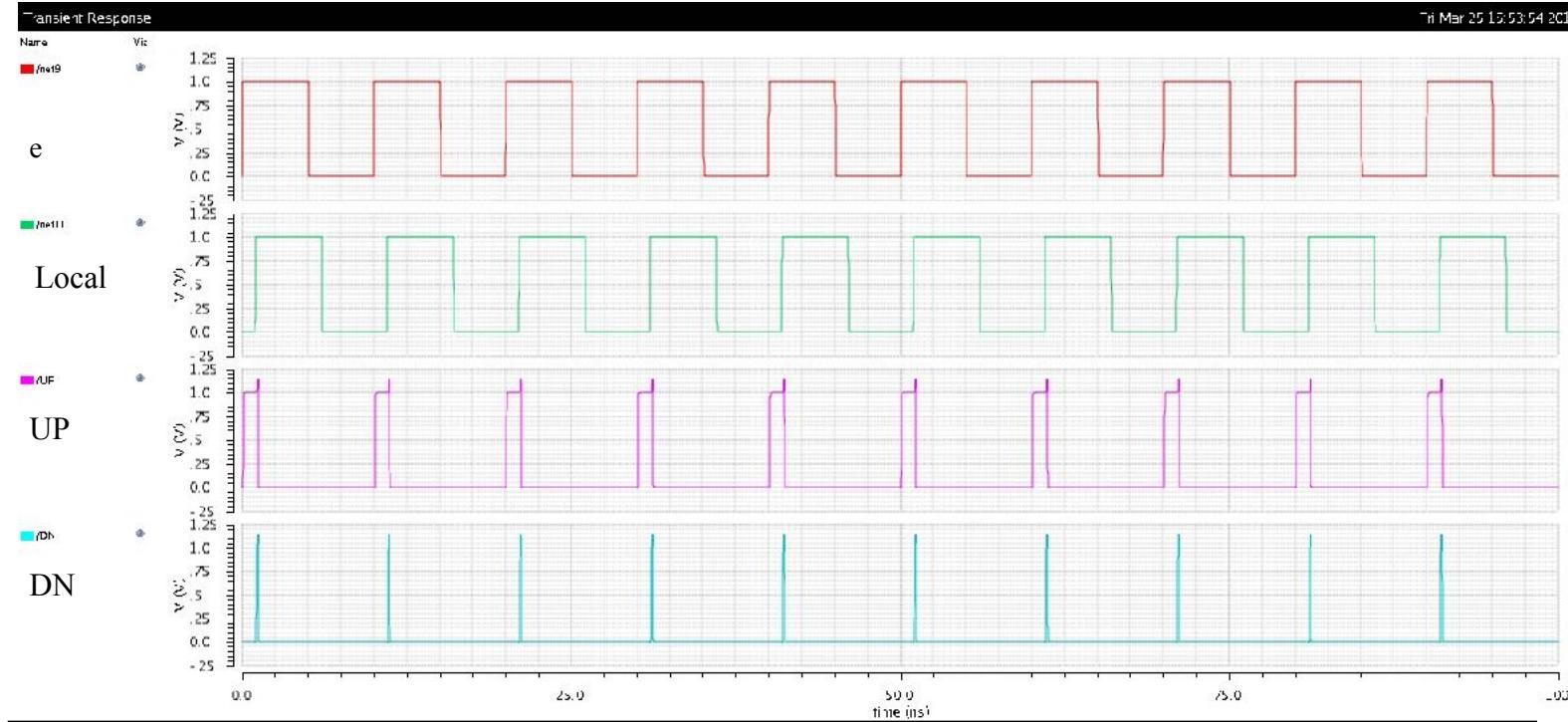
Phase and Frequency detector was used to detect phase difference due to its simplicity and ability to differentiate between lead and lag of the local and reference signals. The schematic is shown in the figure below. The detector was implemented with positive edge triggered D-flipflops with active high reset pin. Input D of both flip-flops is connected to Vdd.



Schematic of Phase and Frequency Detector

Both signals have a frequency of 10MHz. Time delay of 10ns was given between reference and local signals. Two simulations are presented below one for the case where local signal leads and the other where the local signal lags.

Simulation result when Local signal lags by 10ns



4. Frequency Divider

Derivation:

Need to consider how the duty cycle changes , extra circuitry added to get 50% duty cycle.

Explanation of divide by N (odd) and duty cycle aduster:

- <https://www.youtube.com/watch?v=OzesYnxI9Rg>
- https://www.mikrocontroller.net/attachment/177198/Clock_Dividers_Made_Easy.pdf

Divide by 5:

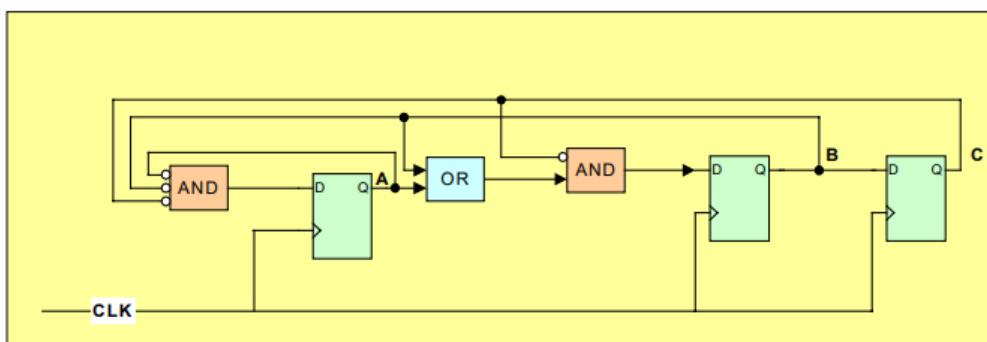


Figure 12: Divide by 5 (Duty cycle not 50%)

[Figure 13](#) shows the timing for the above Divide by 5 circuit.

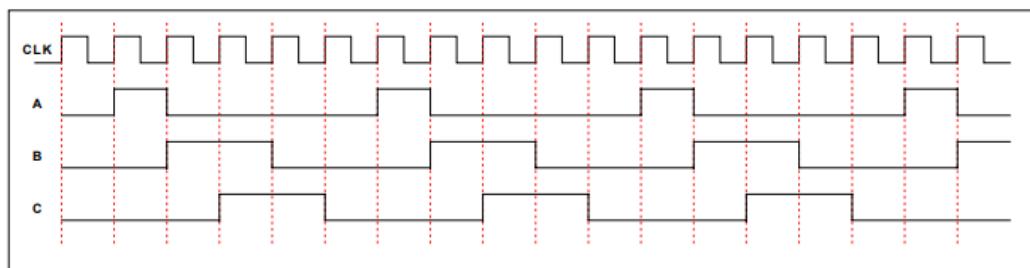


Figure 13: Timing diagram for Divide by 5 (duty cycle not 50%)

As seen from the timing diagram in [Figure 13](#) that the flip-flop outputs B and C are both Divide by 5 where C is a one clock delayed version of B.

A	B	C
0	0	0
1	0	0
0	1	0
0	1	1
0	0	1

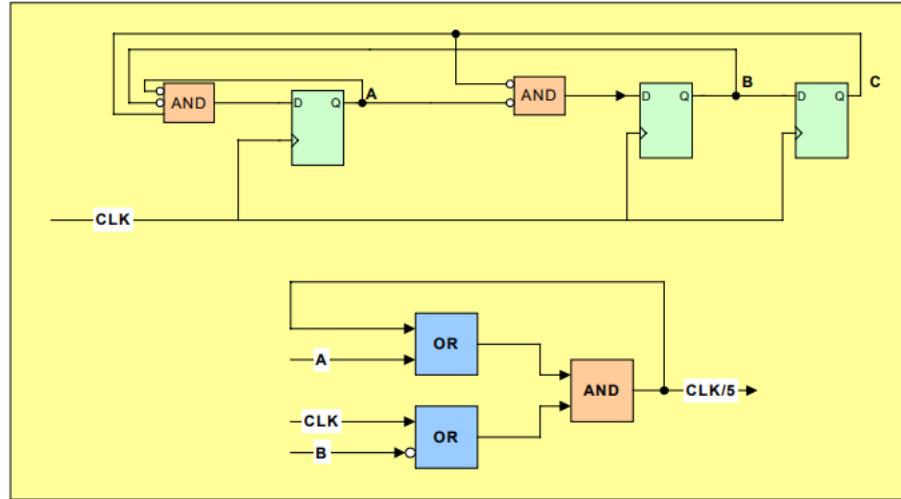


Figure 18: LUT Implementation for Divide by 5 (50% duty cycle output)

[Figure 19](#) shows the timing diagram for the above Divide by 5 circuit.

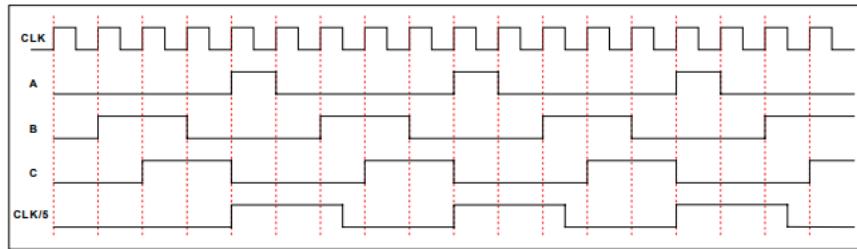


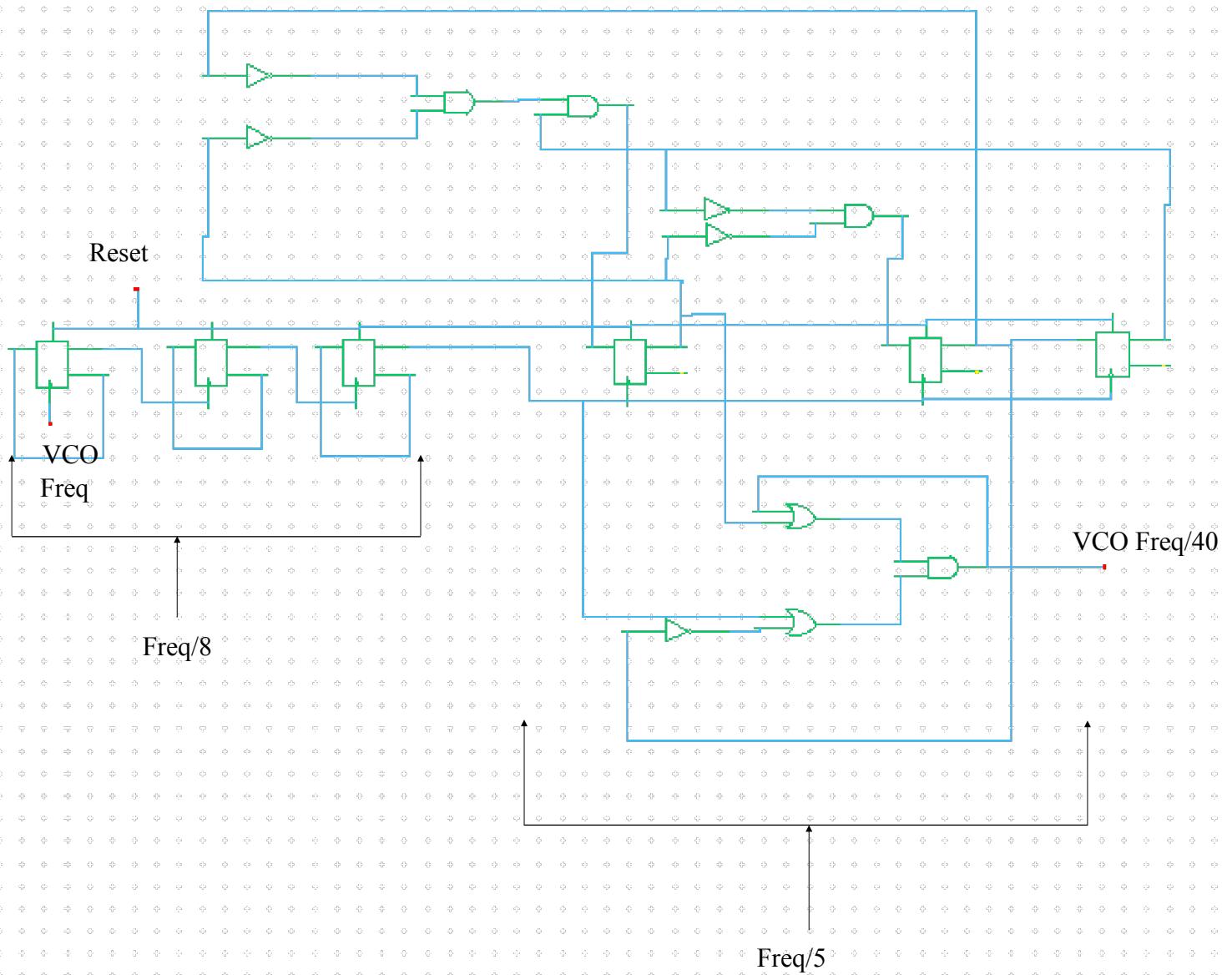
Figure 19: Timing diagram for Divide by 5 (LUT implementation)

Here above the first output pulse is started by the A flip-flop and terminated by the B flip-flop when the clock is low.

CLK	A	B	C	CLK/5
1	0	0	0	1
0	0	0	0	1
1	0	1	0	1
0	0	1	0	0
1	0	1	1	0
0	0	1	1	0
1	0	0	1	0
0	0	0	1	0
1	1	0	0	1
0	1	0	0	1

Table 4: LUT output table for Divide by 5 circuit

Frequency divider was used to down convert VCO target frequency of 400MHz to 10MHz. This was achieved by cascading divide by 8 frequency divider and a divide by 5 divider.



Simulation result below shows the proper functioning of the divider. Input frequency of 400MHz was supplied to the divider and an output frequency of 10MHz (T=100ns) was obtained.



Divide by 40 Frequency Divider

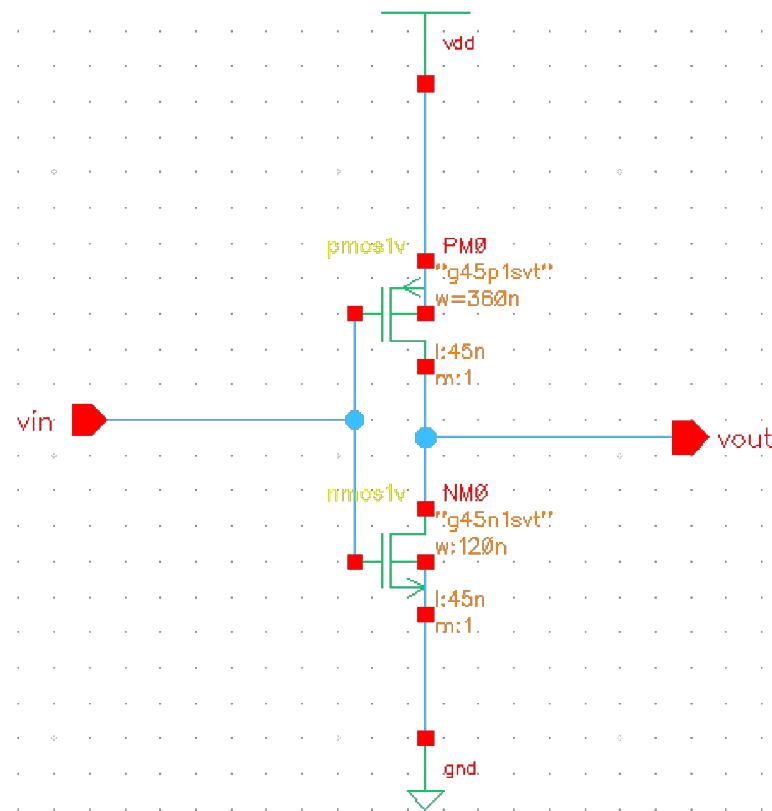
5.Appendix

The following components transistor level schematics and simulations that describe its functionality are included:

- a.NOT gate
- b.AND gate
- c.OR gate
- d.2 input NAND gate
- e.3 input NAND gate
- f.D-flipflop (positive edge triggered with active high reset pin)
- g.nMOS and pMos parameters estimation

a.NOT Gate

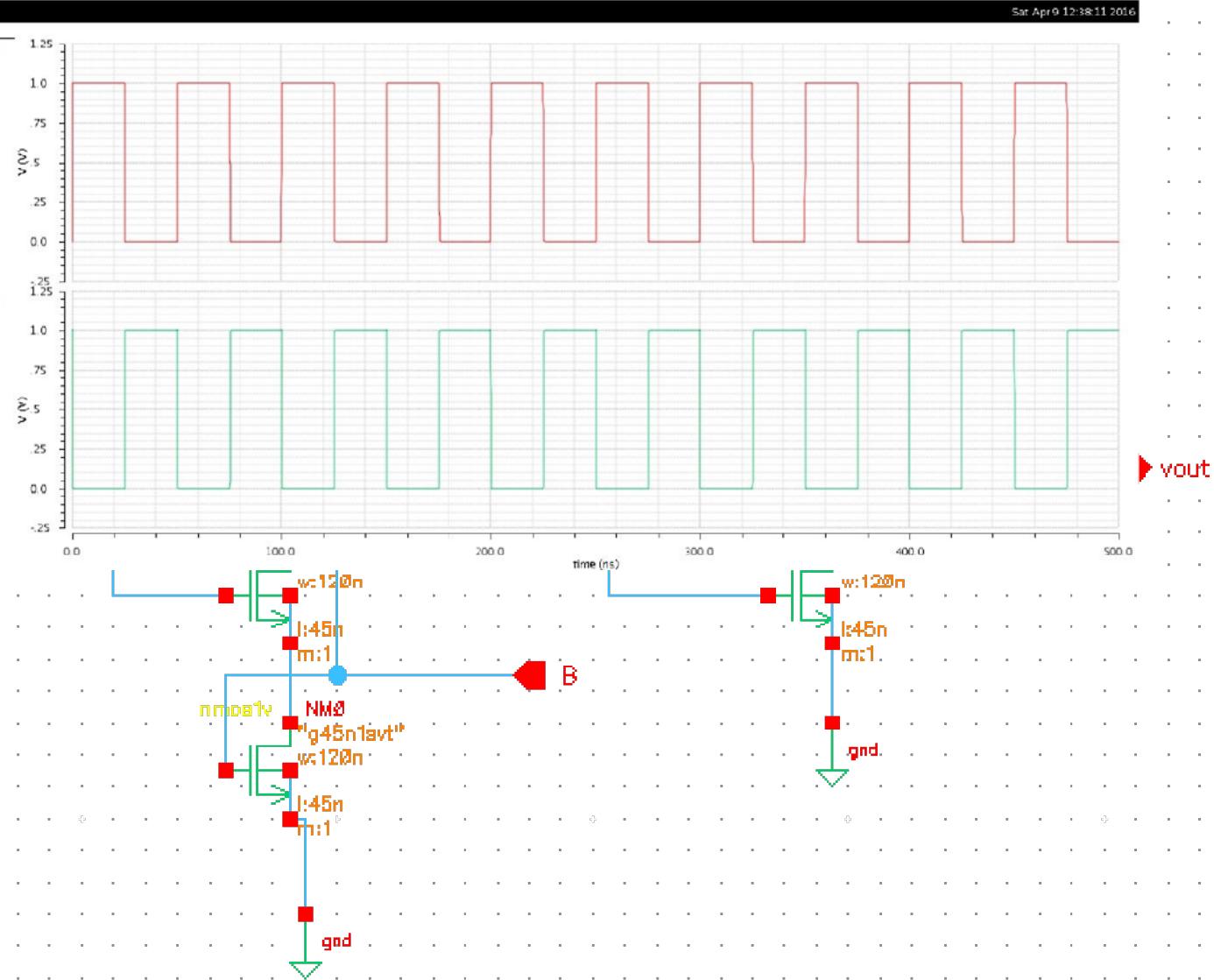
Active high logic is used for the gates. Bit ‘1’ is represented by 1v voltage level and bit ‘0’ is represented by 0v voltage level.



Transistor level diagram of NOT gate

b. AND Gate

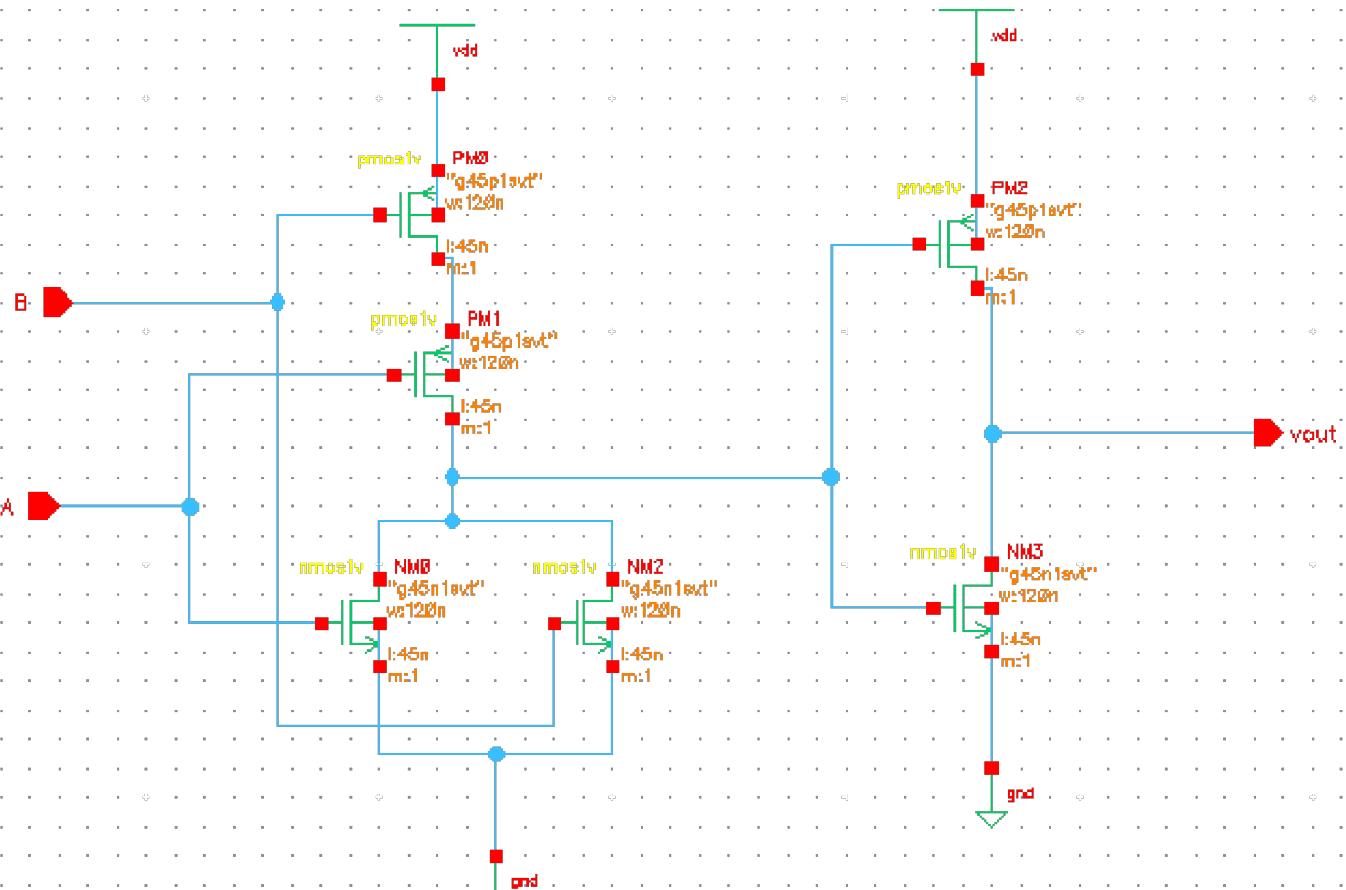
The simulation result shown below verifies the proper working of the NOT gate. Bit ‘1’ is seen at output when input bit is ‘0’ and bit ‘0’ is seen at output when input is bit ‘1’.



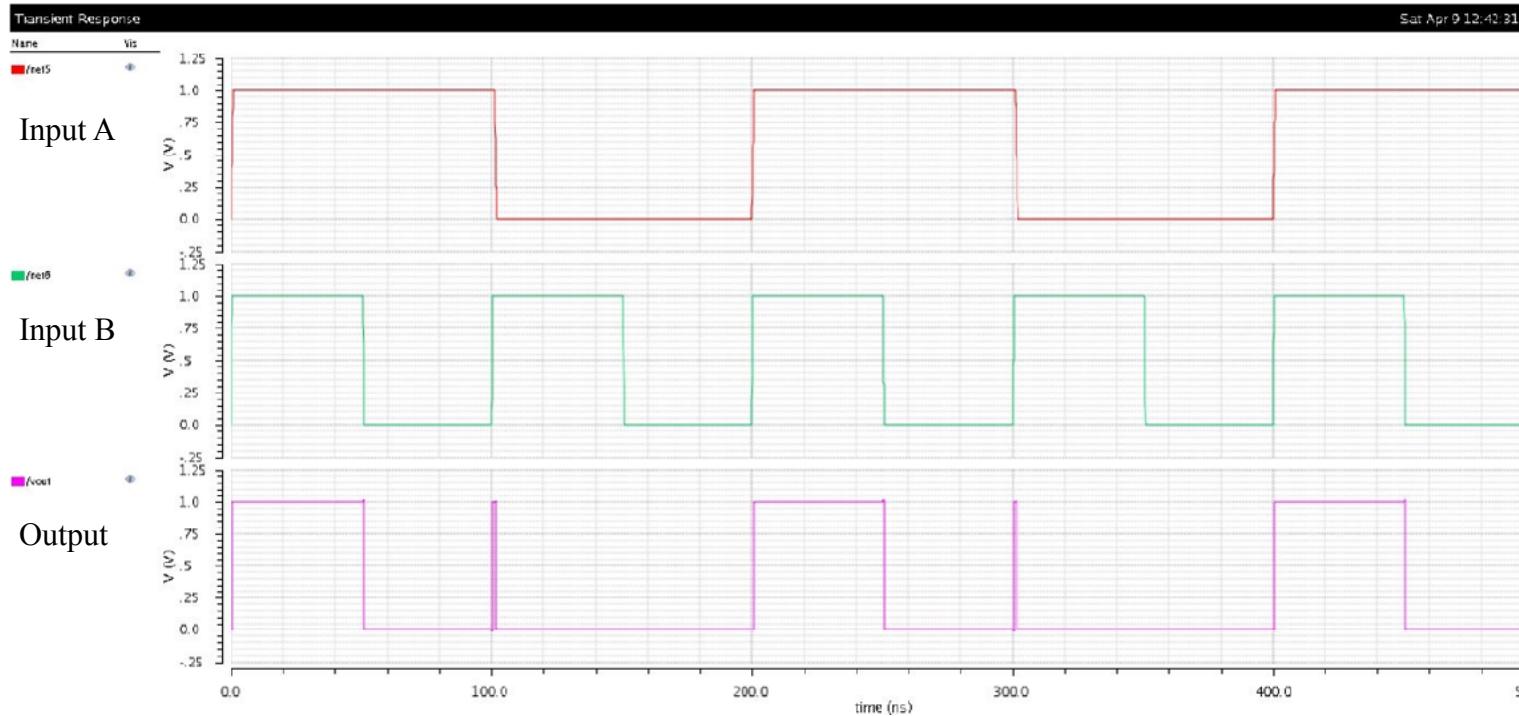
Transistor level of 2. input AND gate

Simulation verifying functionality of NOT gate

The simulation result shown below verifies the proper working of AND gate. Bit ‘1’ is seen at output when both input bits are ‘1’ and bit ‘0’ is seen at output when either of input bit is ‘0’.



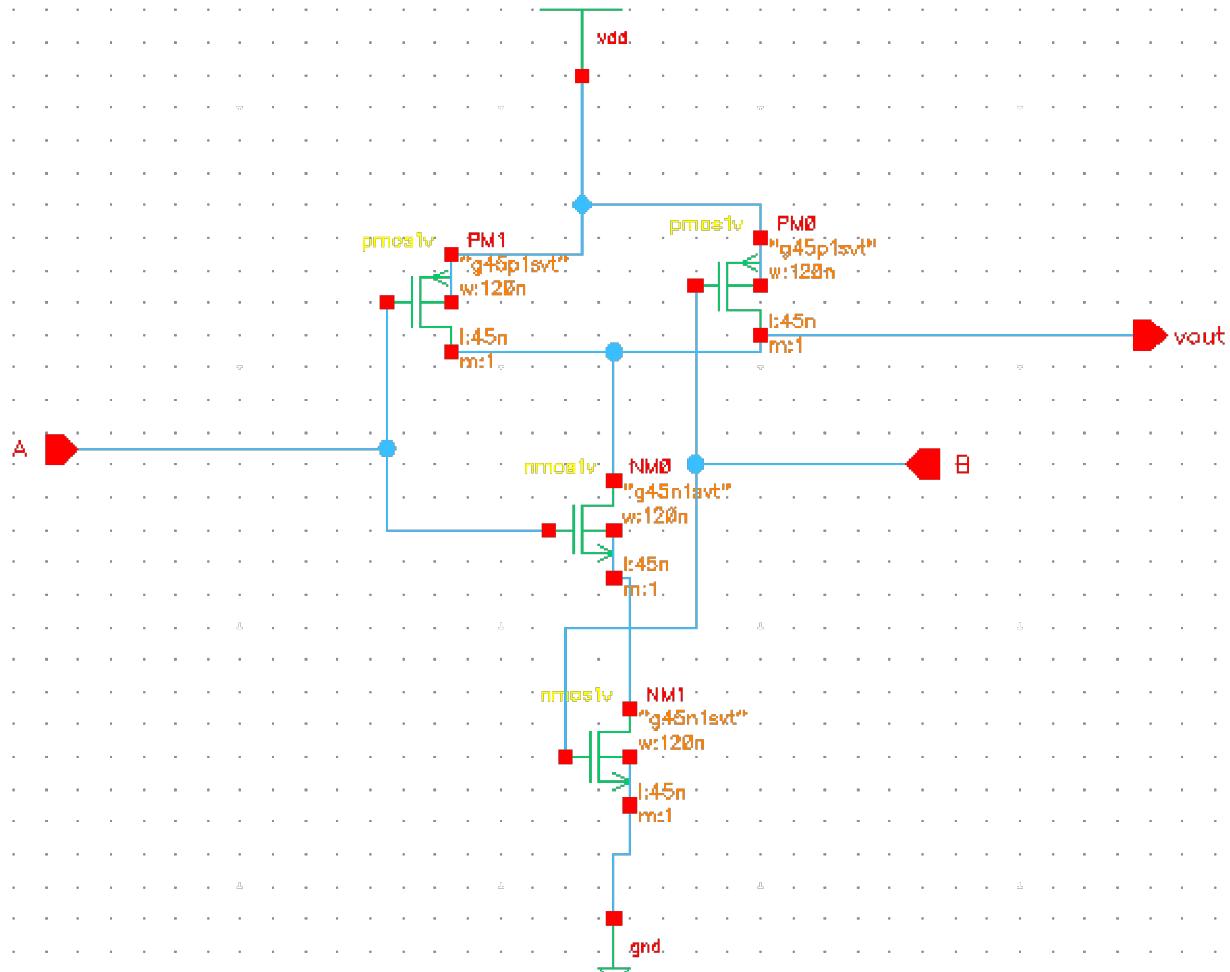
Transistor level schematic of 2 input
OR gate



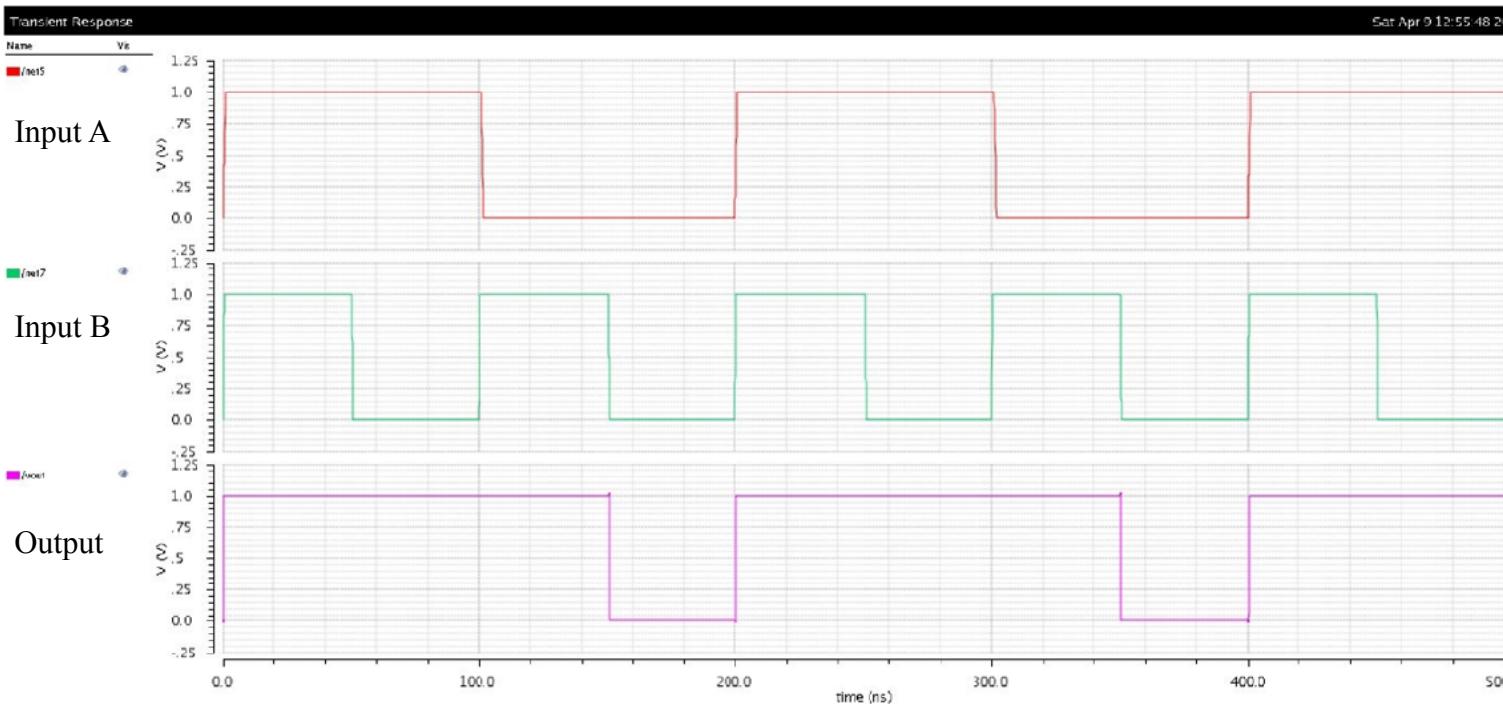
Simulation verifying functionality of AND gate

c. OR Gate

The simulation result shown below verifies the proper working of OR gate. Bit ‘0’ is seen at output when both input bits are ’0’ and bit ‘1’ is seen at output when either of the input bit is ‘1’.



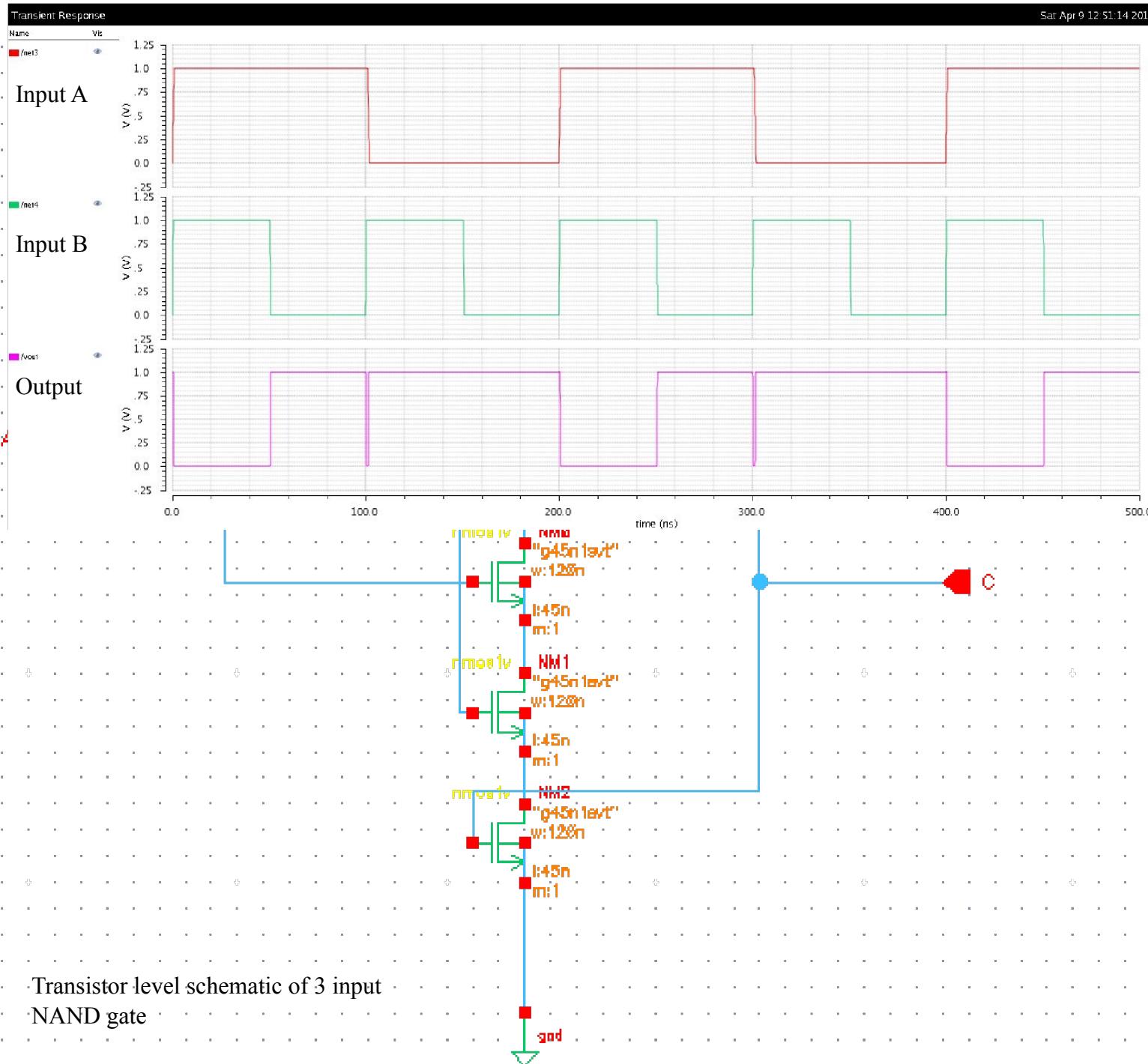
Transistor level schematic of 2 input
NAND gate



Simulation verifying functionality of OR gate

d. two input NAND Gate

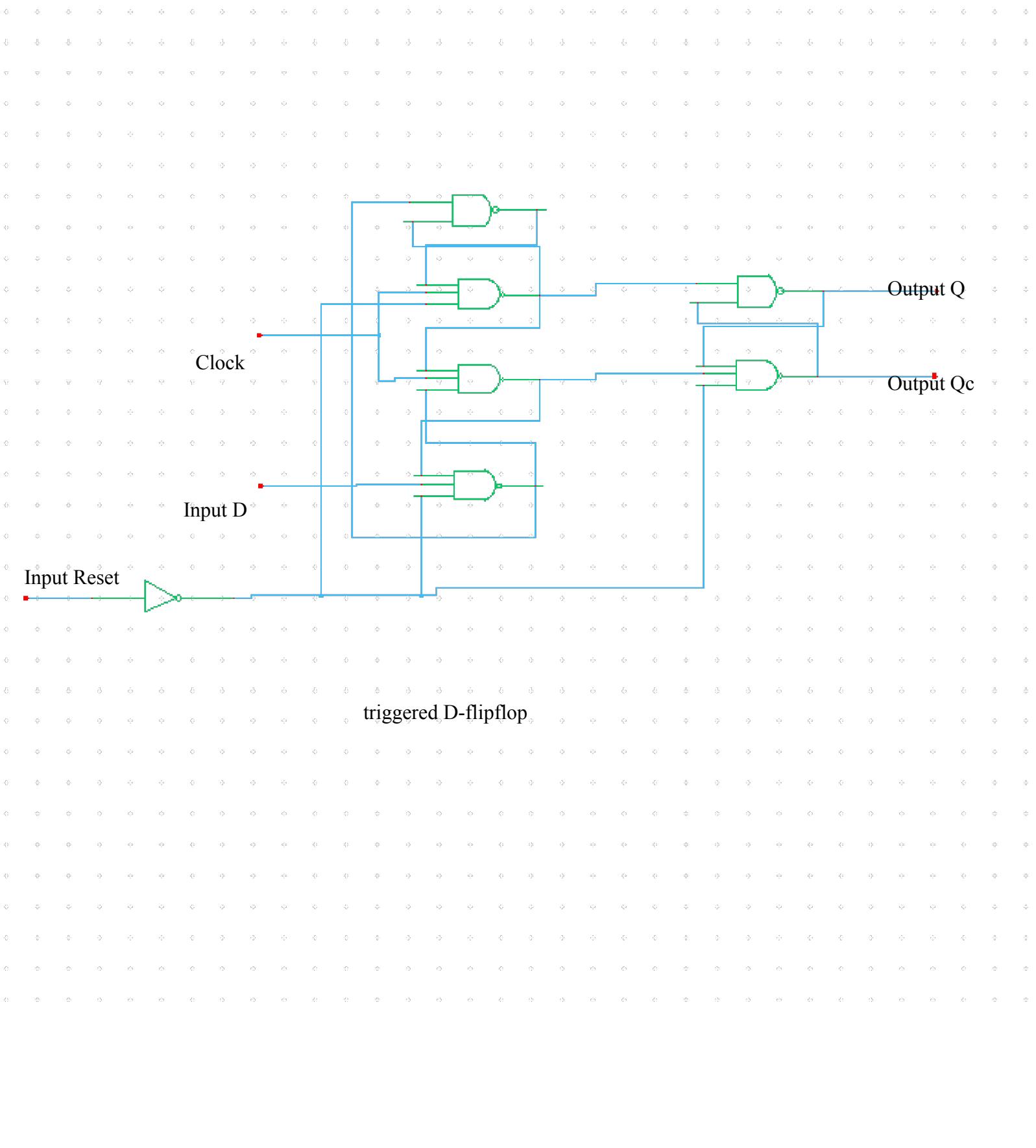
The simulation result shown below verifies the proper working of NAND gate. Bit '0' is seen at output when both input bits are '1' and bit '1' is seen at output when either of the input bit is '0'.

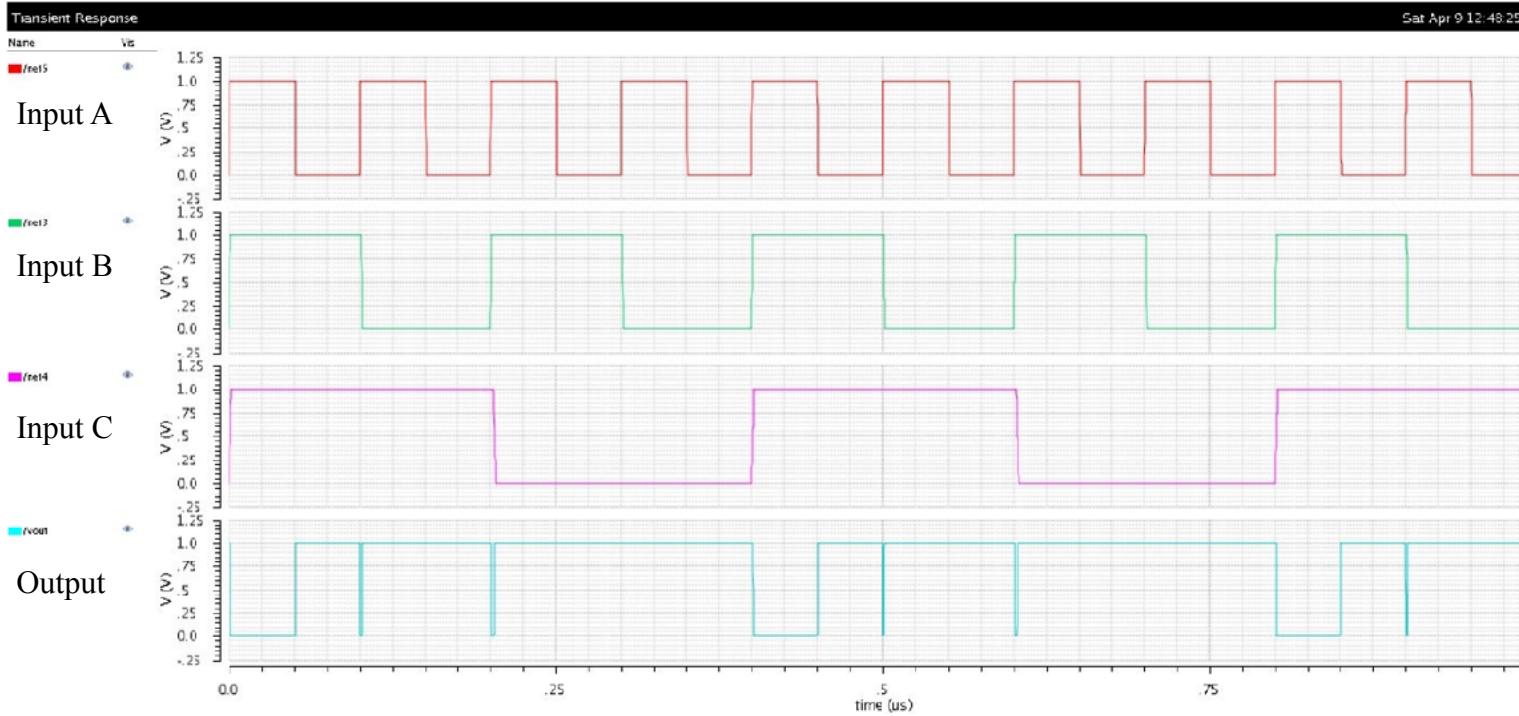


Simulation verifying functionality of NAND gate

e. three input NAND Gate

The simulation result shown below verifies the proper working of NAND gate. Bit '0' is seen at output when all input bits are '1' and bit '1' is seen at output when either of the input bit is '0'.

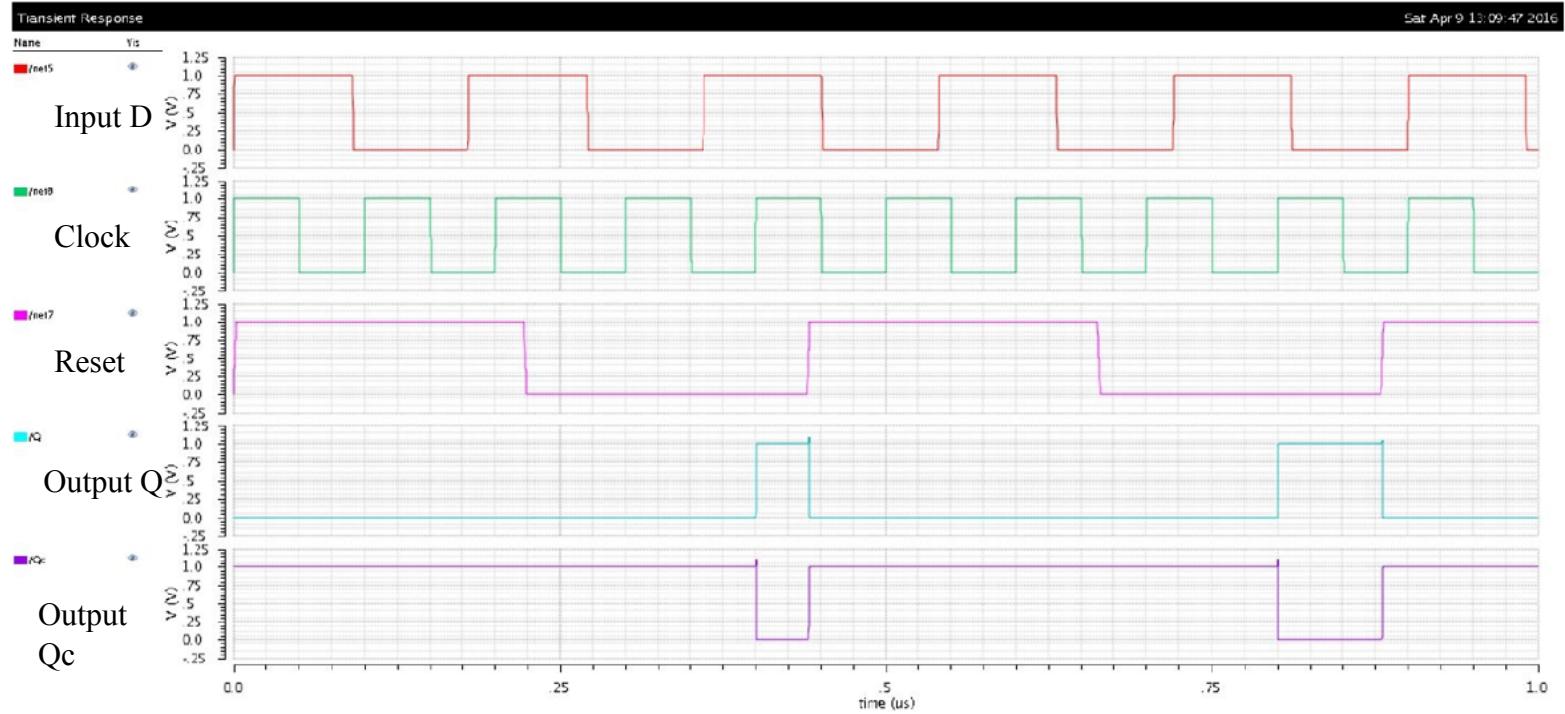




Simulation verifying functionality of NAND gate

f. d flipflop

D-flipflop functionality is described in the truth table shown below. Output Q changes to input D only at the rising edge of the clock given that the reset pin is at bit ‘0’. When Reset pin is high output Q is ‘0’. Output Q and Qc always take complementary values in a D-flipflop.



Simulation verifying functionality of D-flipflop

Reset	D	CLK	Q	Qc
1	X	X	0	1
0		0 ↑	0	1
0		1 ↑	1	0

Truth Table: D-flipflop

g. nMOS and pMOS FET Parameters Estimation

Transistors ($W/L = 2\mu/850n$ for nMOS and $W/L=2\mu/850n$ for pMOS) were simulated to estimate the parameters. Threshold voltage was calculated with V_{DS} at $|1V|$. With V_{GS} at $|1V|$, V_{DS} was swept to calculate current through the FET at various regions and V_{Dsat} was calculated. The parameters given below were obtained and used to design the charge pump. SVT cells were used in design.

	V_t	K'	V_{Dsat}
pMOS	-0.47V	$86.22 \mu A/V^2$	0.5V
nMOS	0.45V	$116.81 \mu A/V^2$	-0.5V

Table: FET Parameters (estimated) (NOT ACCURATE)

For calculations used the values given below: (V_t will different in the FET's used in design)

- $V_{tp} = -0.47V$, $V_{tn} = 0.49V$
- $K' = \beta_{eff} = k' * (W/L)$, for nmos=505.0/ V^2 , pmos=375.0/ V^2 , for $L=0.85\mu m$: back calculated from charge pump source
- Cox: $C_{gs} = (2/3)C_{ox} \cdot W \cdot L + C_{ov1gs}$, $C_{gd} = C_{ov}$, if the device is in strong inversion (above-threshold, i.e. $VG-VTO > 0$) and saturated ($VD > VG-VTO$). $C_{ox} = 15.00 \text{ fF}/\mu m^2$ (process dependednt used the figure below)
- Capacitor values: (<http://rfsilicon.com/index.html>?<http://rfsilicon.com/home/modeling/mos/simple.htm>)
- (45nm 2 stage Opamp Design : www.youtube.com/watch?v=hOuBGcZ5m58)

$W=7.04\mu m, L=200nm$

<code>cdsbo</code>	11.7249a
<code>cgb</code>	-361.404a
<code>cgd</code>	-1.34985f
<code>cgdbo</code>	27.2914a
<code>cgg</code>	17.0976f
<code>cggbo</code>	14.3804f
<code>cgs</code>	-15.3863f
<code>cgsbo</code>	-13.9663f
<code>cjd</code>	5.33853f
<code>cjs</code>	9.12731f
<code>covlgb</code>	0
<code>covlgd</code>	1.37714f
<code>covlgs</code>	1.42008f
<code>csb</code>	-1.7182f
<code>csd</code>	-38.7548a
<code>csg</code>	-13.0065f
<code>css</code>	14.7634f

Only for reference(ball park) do not use these values: **betaeff will change for long and short channel FETs in same process.**

2. 45nm CMOS (1V_Ivt) (L=1u, W=1u), long-channel device

Table 3 Electrical Parameters

	V _{T0} (V)	k' ($\mu\text{A}/\text{V}^2$)	V _{dsat} (V)	$\lambda (\text{V}^{-1})$	$\gamma (\sqrt{\text{V}})$
NMOS	0.285	309.86	0.74	0.082	0.24
PMOS	-0.244	-205.7	-0.7	-0.103	-0.197

Table 4 Capacitance parameters

	C _{ox} (fF/ μm^2)	C _{ov} (fF/ μm)	C _{jo} (fF/ μm^2)	C _{jsw} (fF/ μm)	C _{jswg} (fF/ μm)	m _j	m _{jsw}	m _{jswg}	V _B	V _{BSW}	V _{BSWG}
NMOS	10.8	0.16	0.69	0.057	0.2	0.25	0.011	0.5	0.51	0.78	0.44
PMOS	10.2	0.18	0.82	0.071	0.293	0.31	0.012	0.81	0.75	.49	0.54

tfin	15n
tfin_base	15n
tfin_top	15n
tfindrw	10n
tgate	10n
...	-
tmask	30n
...	-
toxg	1.2n
toxp	2n
toxref	1.2n
tsili	10n

Generic PDK Device Parameters

45nm CMOS

1. 45nm CMOS (1V_Ivt) (L=45nm, W=120nm), minimum transistor size

Table 1 Parameters for manual model

	V _{T0} (V)	k' ($\mu\text{A}/\text{V}^2$)	V _{dsat} (V)	$\lambda (\text{V}^{-1})$	$\gamma (\sqrt{\text{V}})$
NMOS	0.49	128	0.35	0.26	0.195
PMOS	-0.48	-112.5	-0.334	-0.18	-0.203

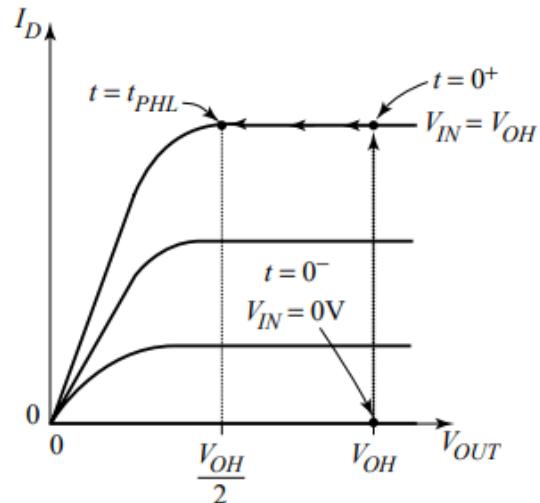
Table 2 Capacitance parameters

	C _{ox} (fF/ μm^2)	C _{ov} (fF/ μm)	C _{jo} (fF/ μm^2)	C _{jsw} (fF/ μm)	C _{jswg} (fF/ μm)	m _j	m _{jsw}	m _{jswg}	V _B	V _{BSW}	V _{BSWG}
NMOS	10.8	0.16	0.69	0.057	0.2	0.25	0.011	0.5	0.51	0.78	0.44
PMOS	10.2	0.18	0.82	0.071	0.293	0.31	0.012	0.81	0.75	.49	0.54

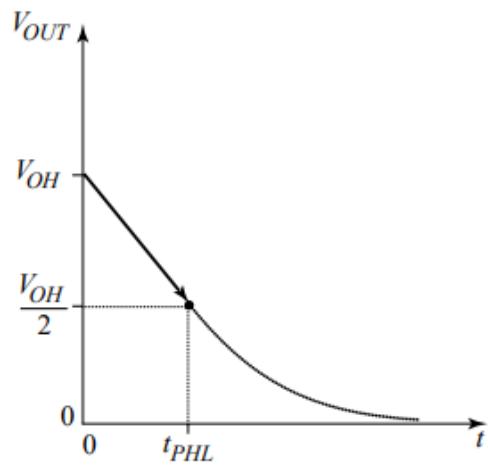


Problems/Challenges Faced:

Graphical Interpretation



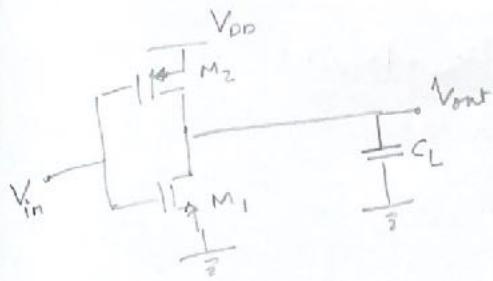
(a)



(b)

Donot use inverter delay equations derived below, as the next stage is charged/discharged by a constant current source.

INVERTER DELAY



① $V_{in} = 0, V_{out} = 0$

$$M_2 : \quad V_{GS} = 0 - V_{DD} = -V_{DD}$$

$$V_{DS} = 0 - V_{DD} = -V_{DD}$$

$V_{DS} < V_{GS} - V_{TH}$; saturation region

$-V_{DD} < -V_{DD} - V_{TH_2}$; $V_{TH_2} = -V_C$ so this condition is true

$$|I_{D_2}| = \frac{1}{2} \mu_P C_{ox} \left(\frac{W}{L} \right)_2 (V_{DD} - |V_{TH_2}|)^2$$

$$I = C_L \frac{dV}{dt} = C_L \times \frac{V_{out} - 0}{t - 0}$$

$$V_{out}(t) = \frac{|I_{D_2}| t}{C_L}$$

$$V_{out}(t) = \frac{1}{2} \mu_P \frac{C_{ox}}{C_L} \left(\frac{W}{L} \right)_2 (V_{DD} - |V_{TH_2}|)^2 \cdot t$$

$$V_{out}(t) = V_{D_2} = |V_{TH_2}| ; \text{ the } M_2 \text{ enters triode}$$

Region :

$V_G =$	$\left\{ \begin{array}{l} \cdot V_{GS} - V_{TH_2} \\ \cdot V_G - V_{DD} + V_{TH_2} \\ \cdot V_{BS} : \\ \quad V_{TH_2} - V_{DD} \end{array} \right.$
$V_S = V_{DD}$	
$V_B = V_{TH_2} $	

$$V_{DS} = V_{GS} - V_{TH_2} ; V_G = 0 \text{ assuming}$$

as V_{out} increases above $|V_{TH_2}|$, M_2 enters triode region

$$T_{PLH_1} = \frac{2 |V_{TH_2}| C_L}{4 \mu_p C_{ox} \left(\frac{W}{L}\right)_2 (V_{DD} - |V_{TH_2}|)^2}$$

② M₂ in triode region :

$$|I_{D_2}| = C_L \frac{dV_{out}}{dt}$$

$$\gamma_2 \mu_p C_{ox} \left(\frac{W}{L}\right)_2 \left[2 (V_{DD} - |V_{TH_2}|) (V_{DD} - V_{out} - (V_{DD} - V_{out})^2) \right]$$

$$= C_L \frac{dV_{out}}{dt}$$

$$\frac{dV_{out}}{2(V_{DD} - |V_{TH_2}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2} = \gamma_2 \mu_p \frac{C_{ox}}{C_L} \left(\frac{W}{L}\right)_2 dt$$

$$V_{DD} - V_{out} = 4$$

$$\int \frac{du}{au - u^2} = \frac{1}{a} \ln \frac{u}{a-u}$$

$$\frac{-1}{2(V_{DD} - |V_{TH_2}|)} \ln \frac{V_{DD} - V_{out}}{V_{DD} - 2|V_{TH_2}| + V_{out}}$$

$V_{out} = V_{DD}/2$
 $V_{out} = |V_{TH_2}|$

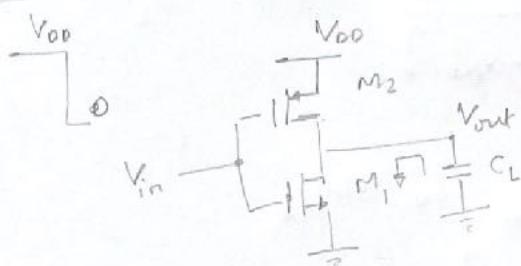
$$= \gamma_2 \mu_p \frac{C_{ox}}{C_L} \left(\frac{W}{L}\right)_2 T_{PLH_2};$$

* T_{PLH_2} is measured from T_{PLH_1} ($V_{out} = |V_{TH_2}|$)

time to charge from $|V_{TH_2}|$ to $V_{DD}/2$

$$T_{PLH_2} = \frac{C_L}{4p C_{ox} \left(\frac{W}{L} \right)_2 [V_{DD} - |V_{TH_2}|]} \ln \left(3 - 4 \frac{|V_{TH_2}|}{V_{DD}} \right)$$

$$T_{PLH} = T_{PLH_1} + T_{PLH_2}$$



- $V_{out} = V_{DD} = V_D$
- $V_{DS} > V_{GS} - V_{TH_1}$: M₁ in saturation
- $V_S = 0$

- $V_G = V_{DD}$
- $V_{DD} > V_{DD} - V_{TH_1}$ saturation

- M₂ = OFF

$$I_{D_1} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_1 (V_{DD} - V_{TH_1})^2$$

$$= C_L \cdot \frac{V_{out} - V_{DD}}{t}$$

M₁ : enters triode region at $V_{out} = V_{DD} - V_{TH_1}$

- $V_D = V_{DD} - V_{TH_1}$
- $V_{DS} = V_{GS} - V_{TH_1}$

- $V_G = V_{DD}$
- $V_{DD} - V_{TH_1} = V_{DD} - V_{TH_1}$

- $V_S = 0$
- V_{DS} decreases from this point

$$t = T_{PHL_1}$$

$$T_{PHL_1} = \frac{2 V_{TH_1} C_L}{\left(\mu_n C_{ox} \frac{W}{L} \right)_1 (V_{DD} - V_{TH_1})^2}$$

$$M_1 \text{ in triode region : } V_{AS} - V_t = \frac{V_{DS}}{2} - \frac{V_{DS}^2}{V_{DD}}$$

$$\gamma_2 \mu_n C_{ox} \left(\frac{W}{L} \right)_1 \left[2(V_{DD} - V_{TH_1}) V_{out} - V_{out}^2 \right]$$

$$= -C_L \frac{dV_{out}}{dt}$$

$$\frac{dV_{out}}{\left[2(V_{DD} - V_{TH_1}) V_{out} - V_{out}^2 \right]} = -\gamma_2 \mu_n \frac{C_{ox}}{C_L} \left(\frac{W}{L} \right)_1 dt$$

V_{out} from $V_{DD} - V_{TH_1}$ to $V_{DD}/2$

$t = T_{PHL_1}$ [reference]

$$-\frac{1}{2(V_{DD} - V_{TH_1})} \ln \frac{V_{out}}{2(V_{DD} - V_{TH_1}) - V_{out}} \quad \begin{cases} V_{out} = V_{DD}/2 \\ V_{out} = V_{DD} - V_{TH_1} \end{cases}$$

$$T_{PHL_2} = \frac{C_L}{\gamma_n C_{ox} \left(\frac{W}{L} \right)_1 \left[V_{DD} - V_{TH_1} \right]} \cdot \ln \left(3 - 4 \cdot \frac{V_{TH_1}}{V_{DD}} \right)$$

$$T_{PHL} = \frac{C_L}{\gamma_n C_{ox} \left(\frac{W}{L} \right)_1 \left[V_{DD} - V_{TH_1} \right]} \left[\frac{2V_{TH_1}}{V_{DD} - V_{TH_1}} + \ln \left(3 - 4 \frac{V_{TH_1}}{V_{DD}} \right) \right]$$

**Example
16.22**

Compare the two terms inside the square brackets in Eq. (16.82) as V_{TH1} varies from zero to $V_{DD}/2$.

Solution For $V_{TH1} = 0$, the first term is equal to 0 and the second equal to $\ln 3 \approx 1.1$. As V_{TH1} increases, the two terms converge, both reaching 0.684 for $V_{TH1} = 0.255V_{DD}$. Finally, for $V_{TH1} = V_{DD}/2$, the first term rises to 2 and the second falls to 0. Figure 16.24 plots each term and the sum of the two, suggesting that low thresholds improve the speed.

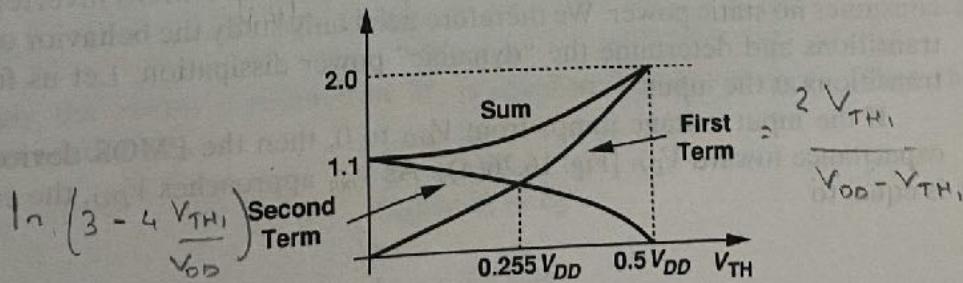


Figure 16.24

Exercise

Repeat the above example if V_{TH1} varies from 0 to $3V_{DD}/4$.