

INTRODUCTION TO VLSI DESIGN

Project Part 4

Under the Guidance of

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For XOR, Half-adder and Full-adder the following have been included:

1. Schematic
2. Layout
3. DRC
4. LVS
5. Symbol
6. Test bench schematic
7. Simulations for given binary inputs (pulse input)

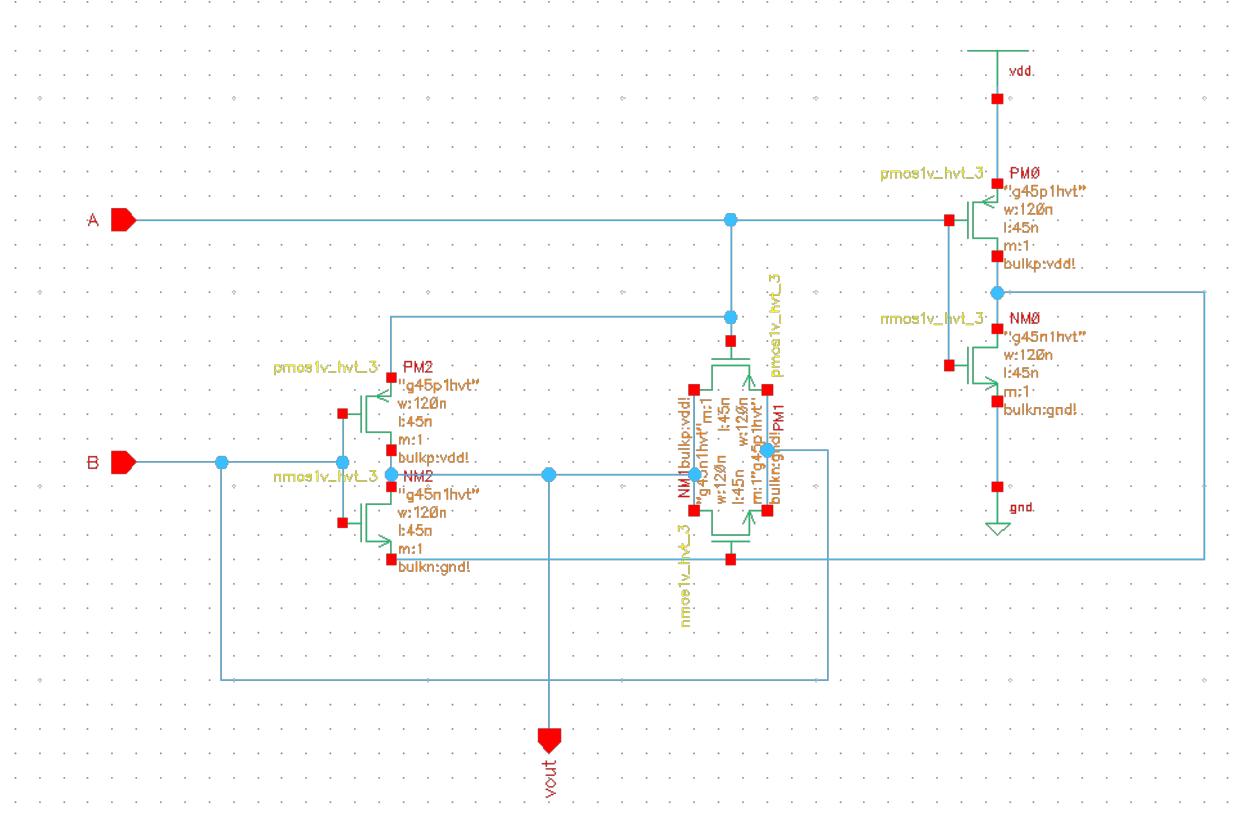
For Wallace tree multiplier the following have been included:

1. Layout (showing area)
2. Simulations
3. Time delay for 101101×100111

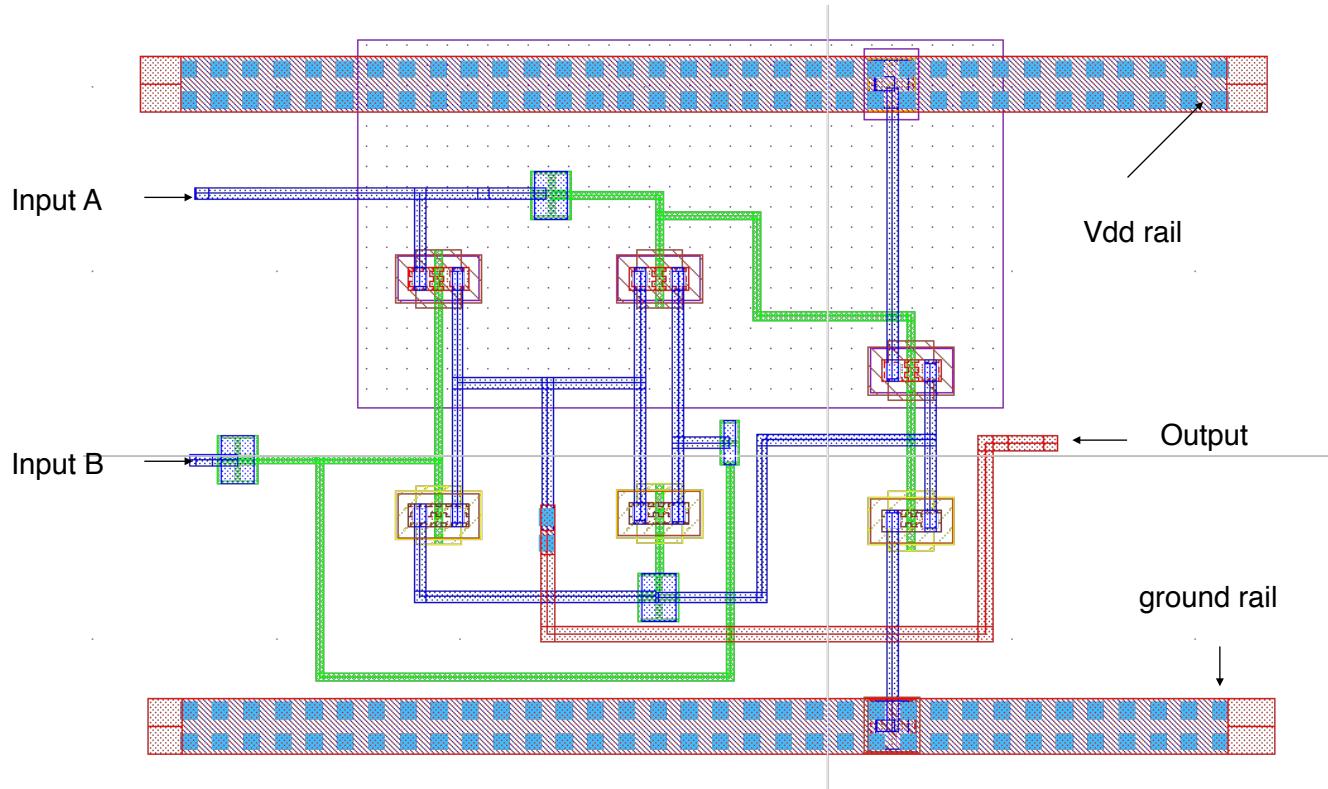
1. XOR GATE

- Schematic

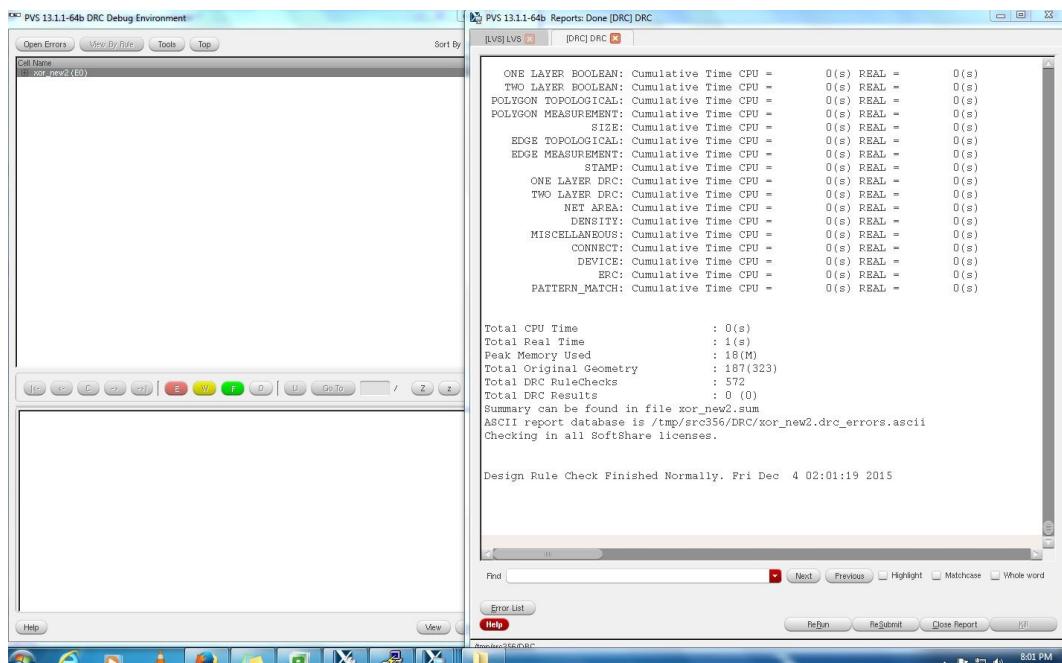
Previously XOR gate was implemented with NAND gates, the current XOR gate has been implemented with transmission gate logic.



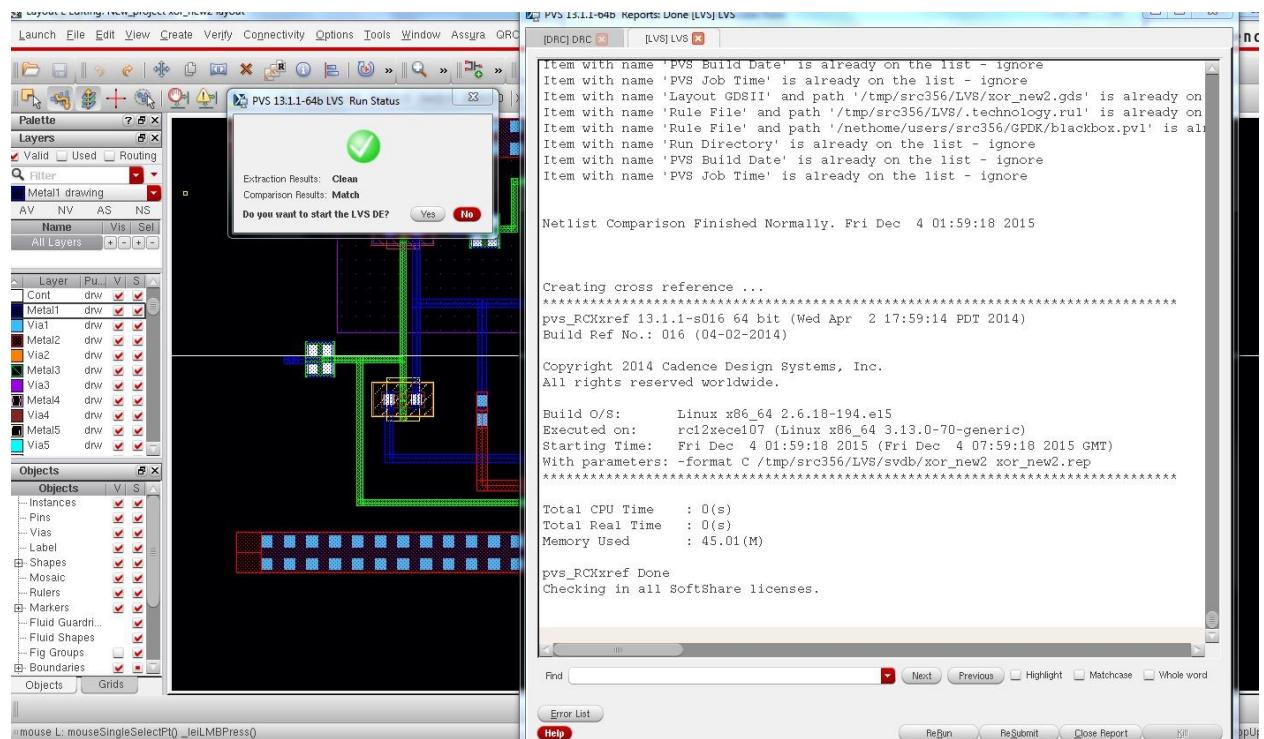
- Layout



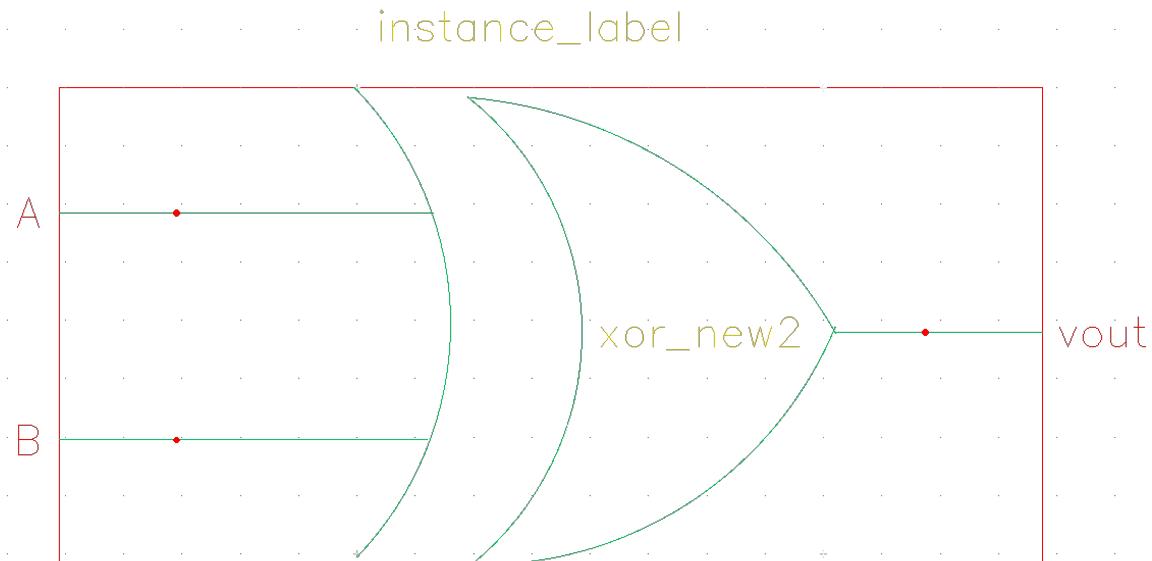
- DRC



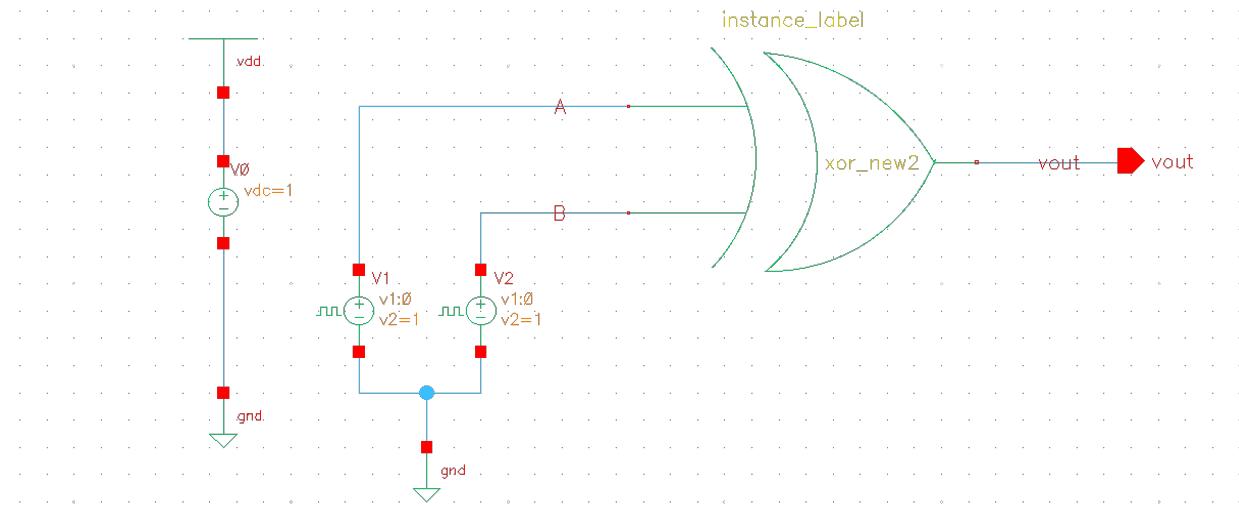
- LVS



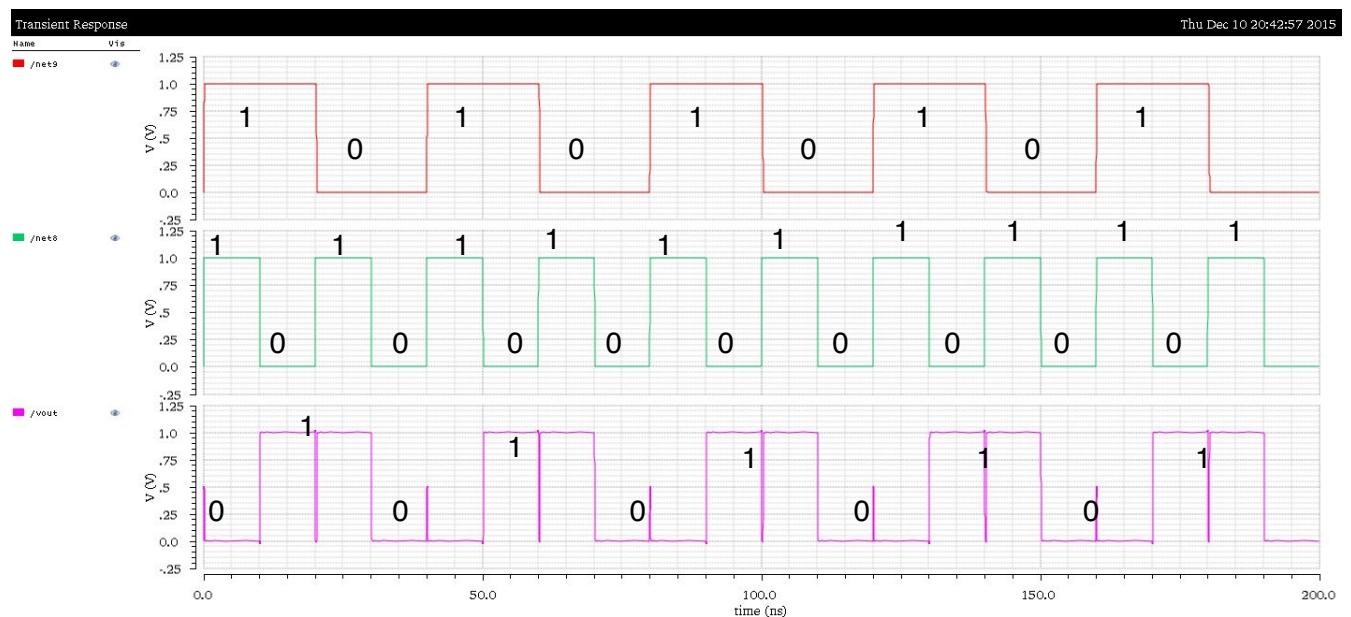
- Symbol



- Test bench Schematic



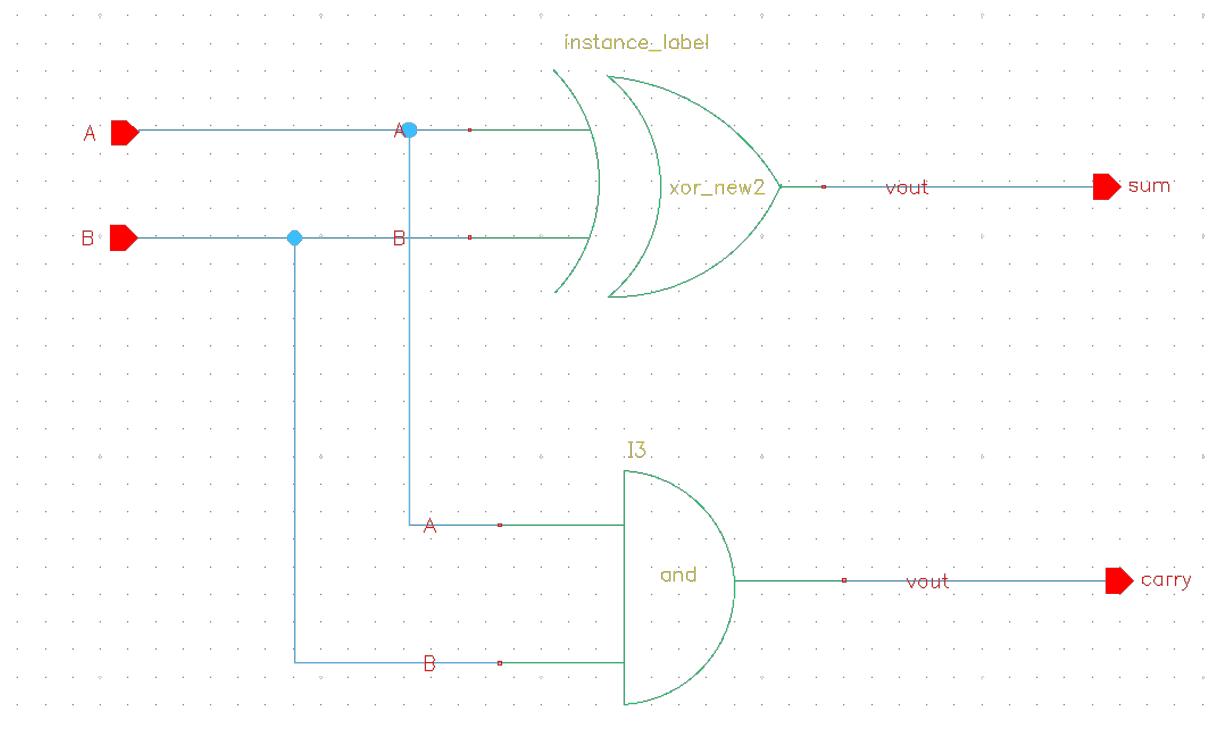
- Output Simulations



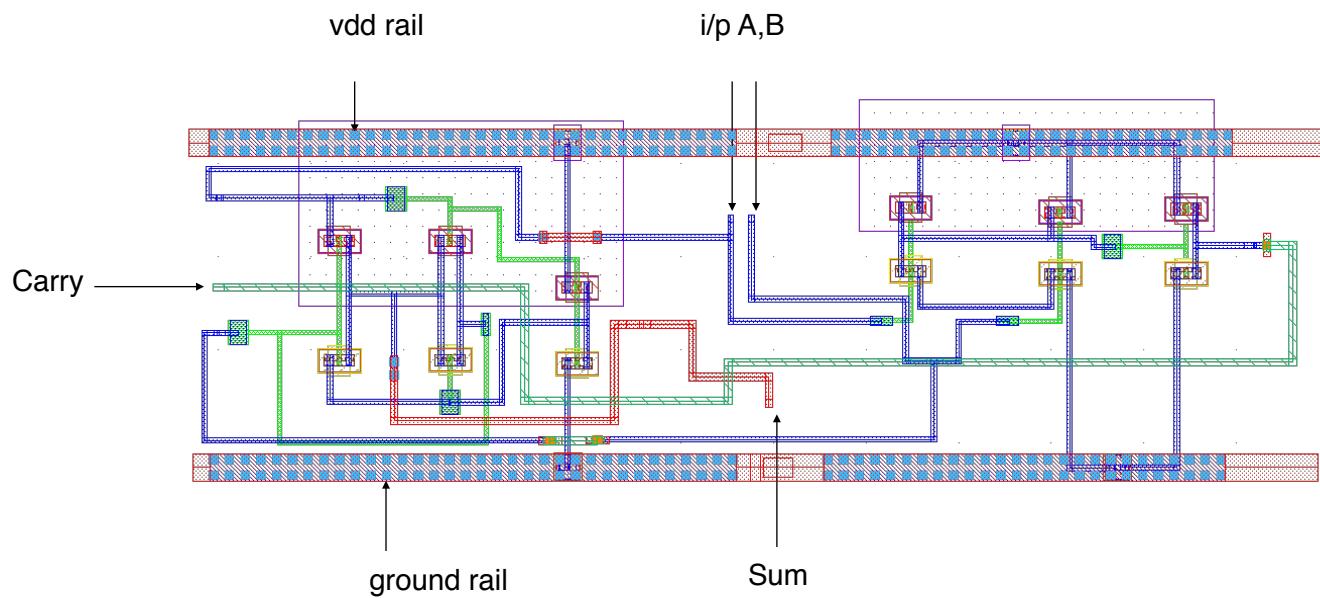
As observed from the graph the outputs follow the logic function of an XOR gate.

2. Half-adder

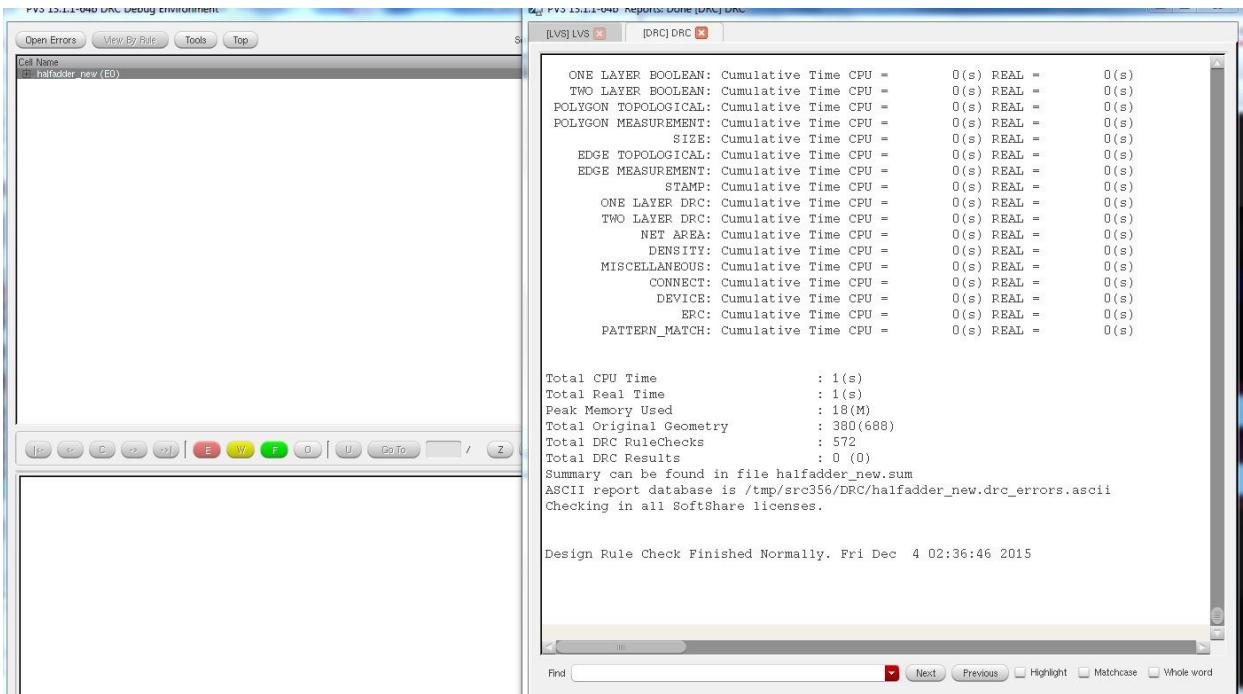
- Schematic



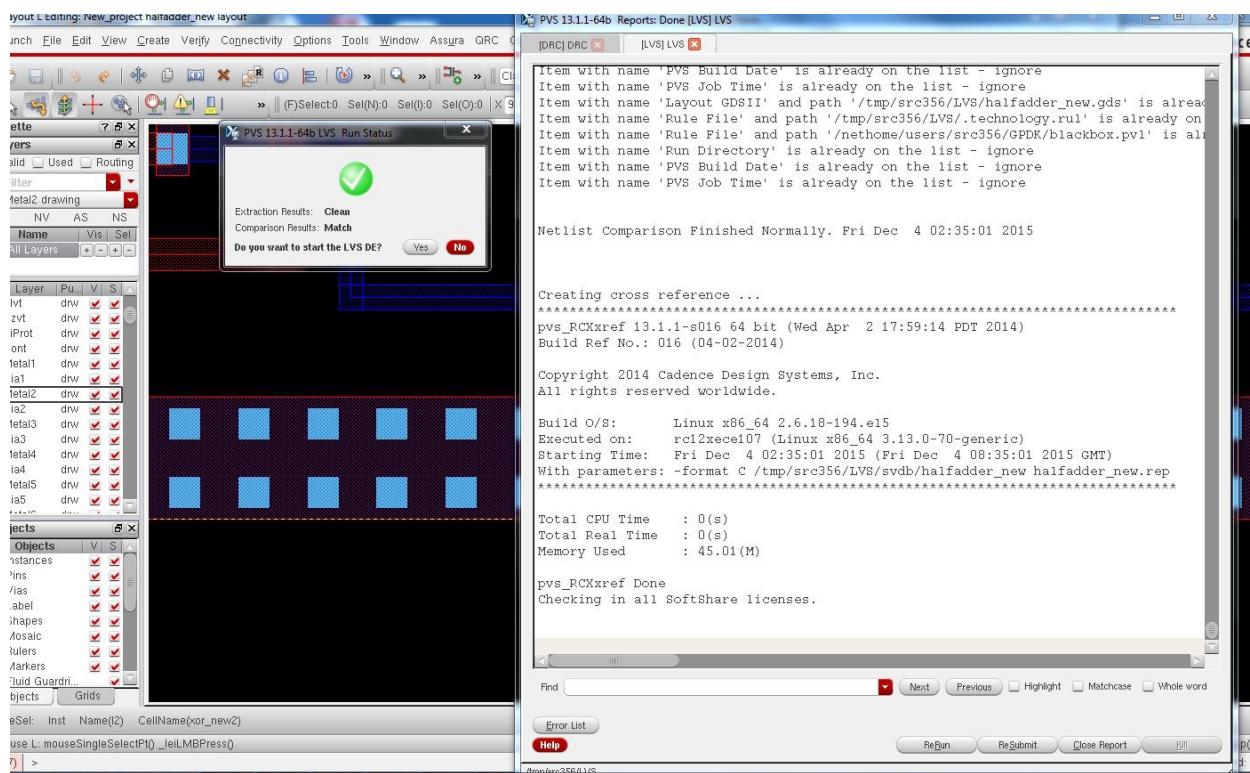
- Layout



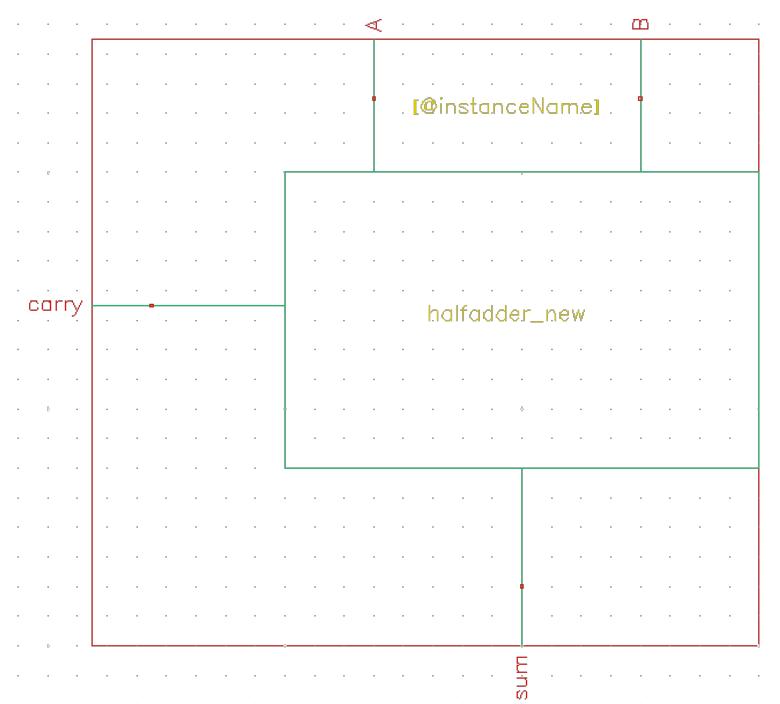
- DRC



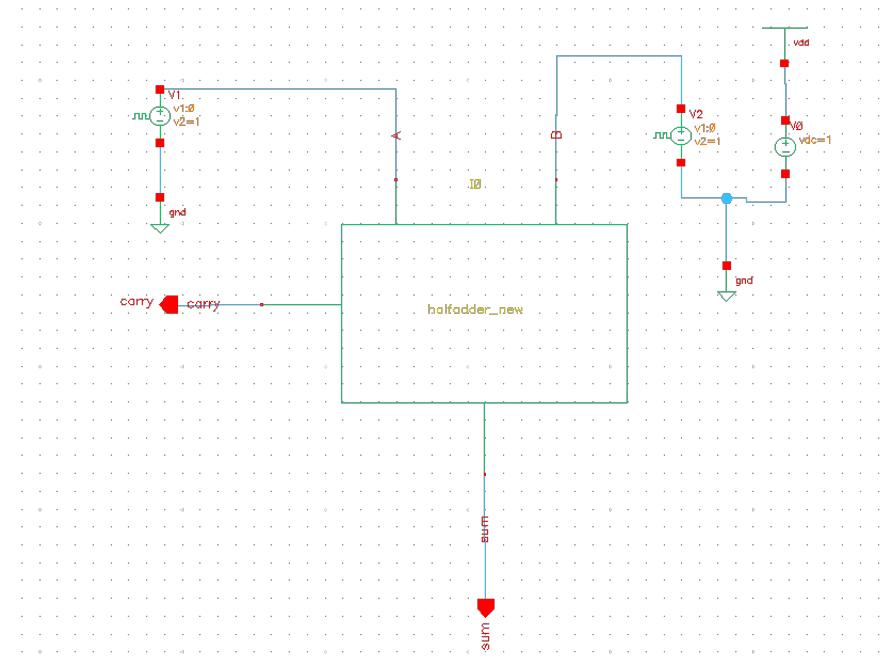
- LVS



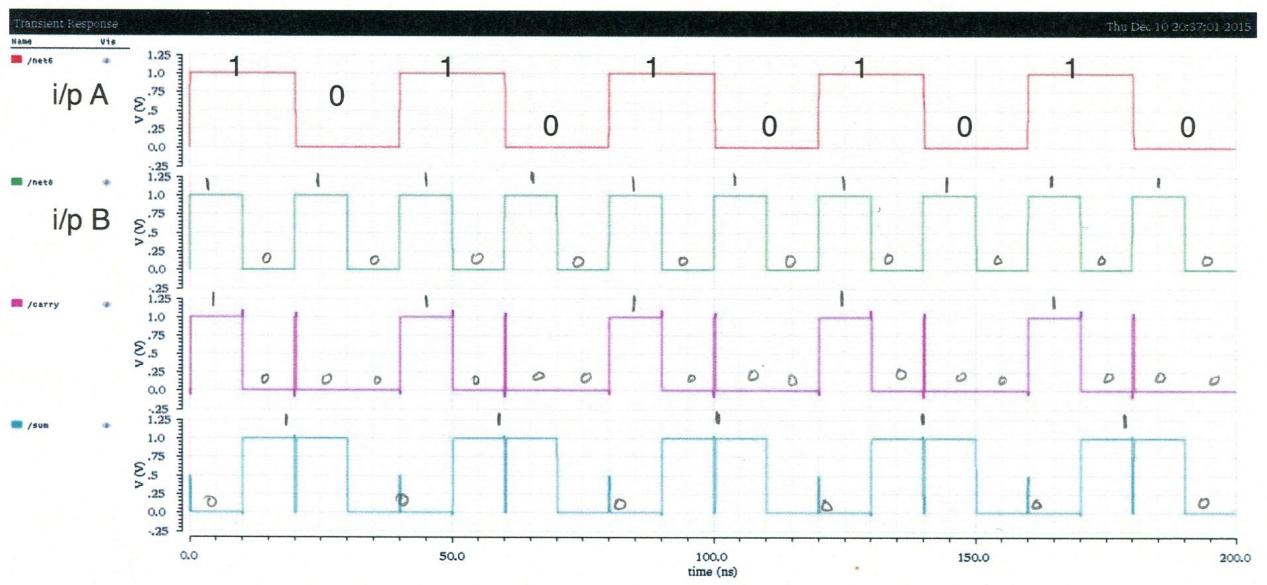
- Symbol



- Test bench schematic



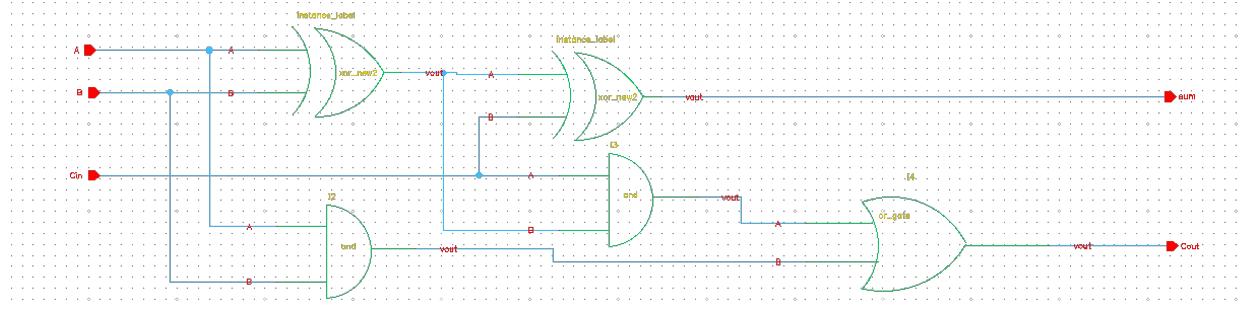
- Output Simulations



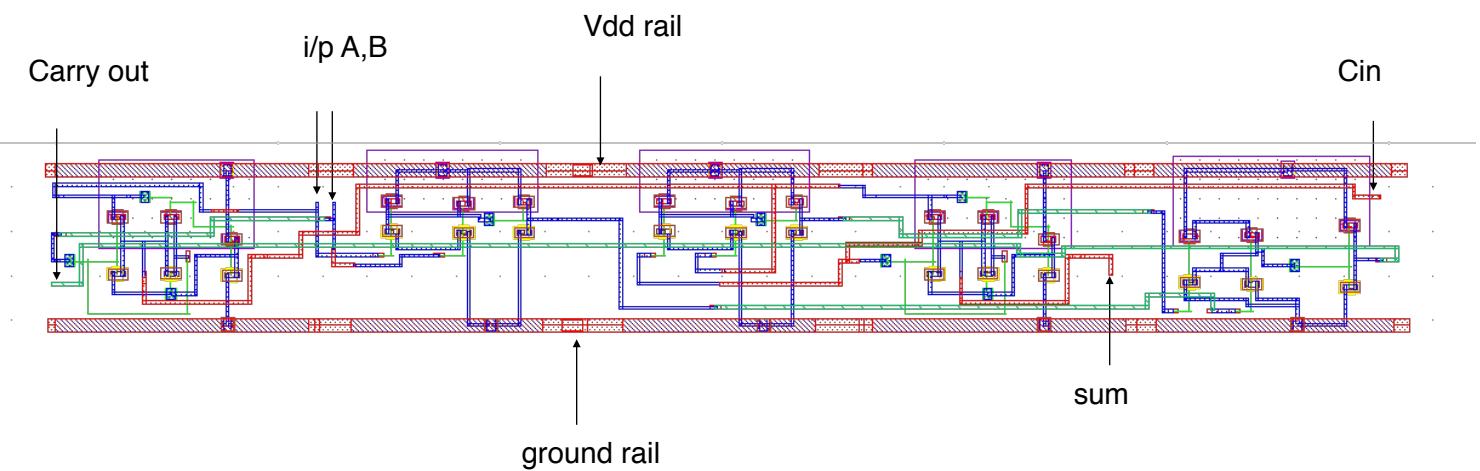
As observed from the graph the outputs 'sum' and 'carry' follow the logic function of a half-adder.

3. Full-adder

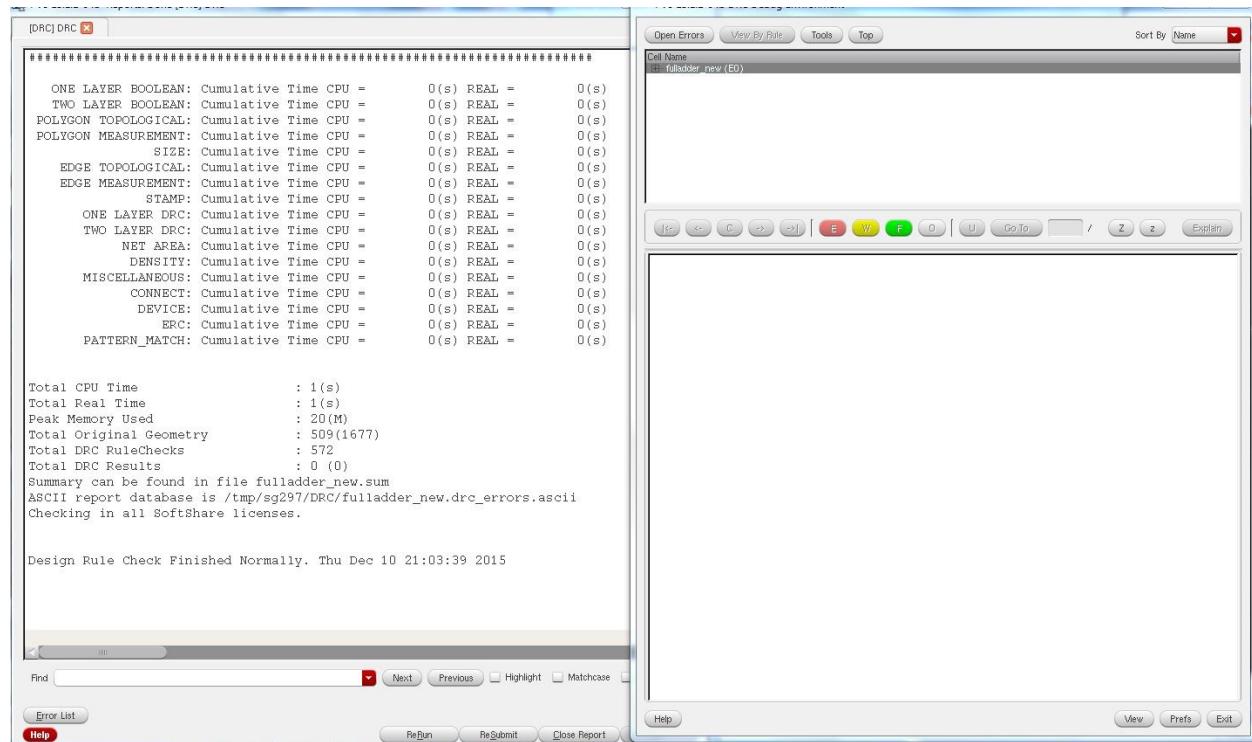
- Schematic



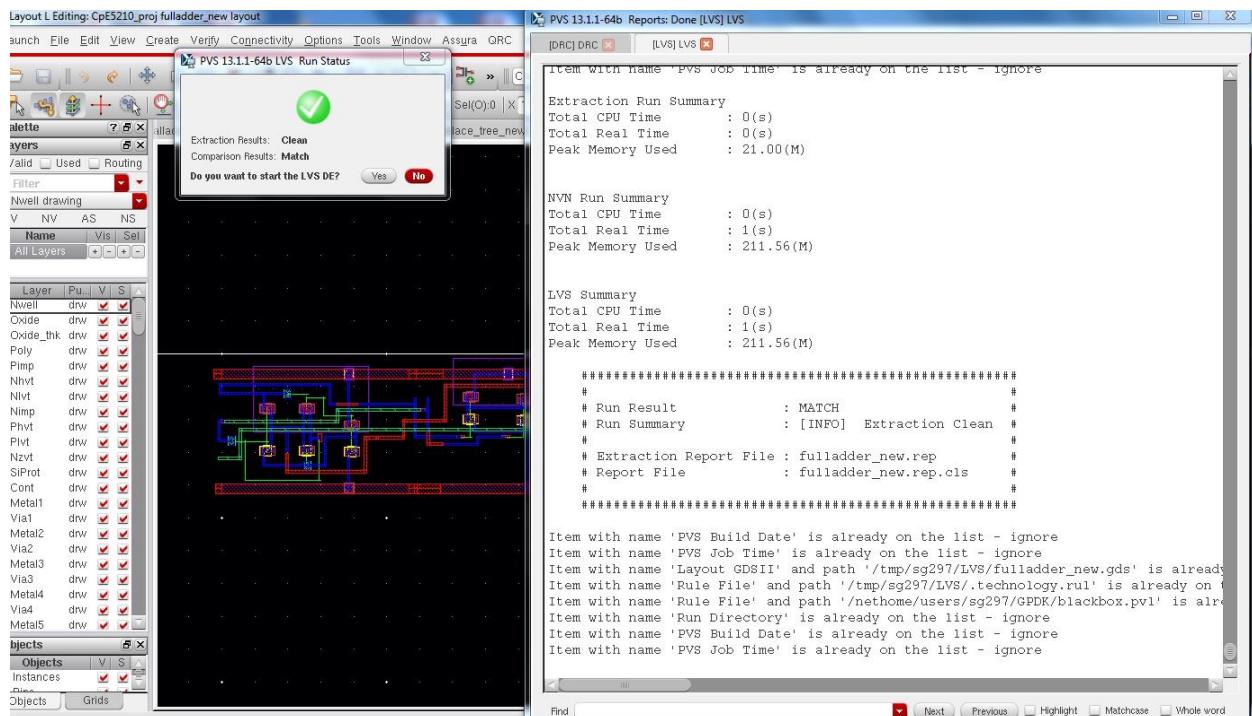
- Layout



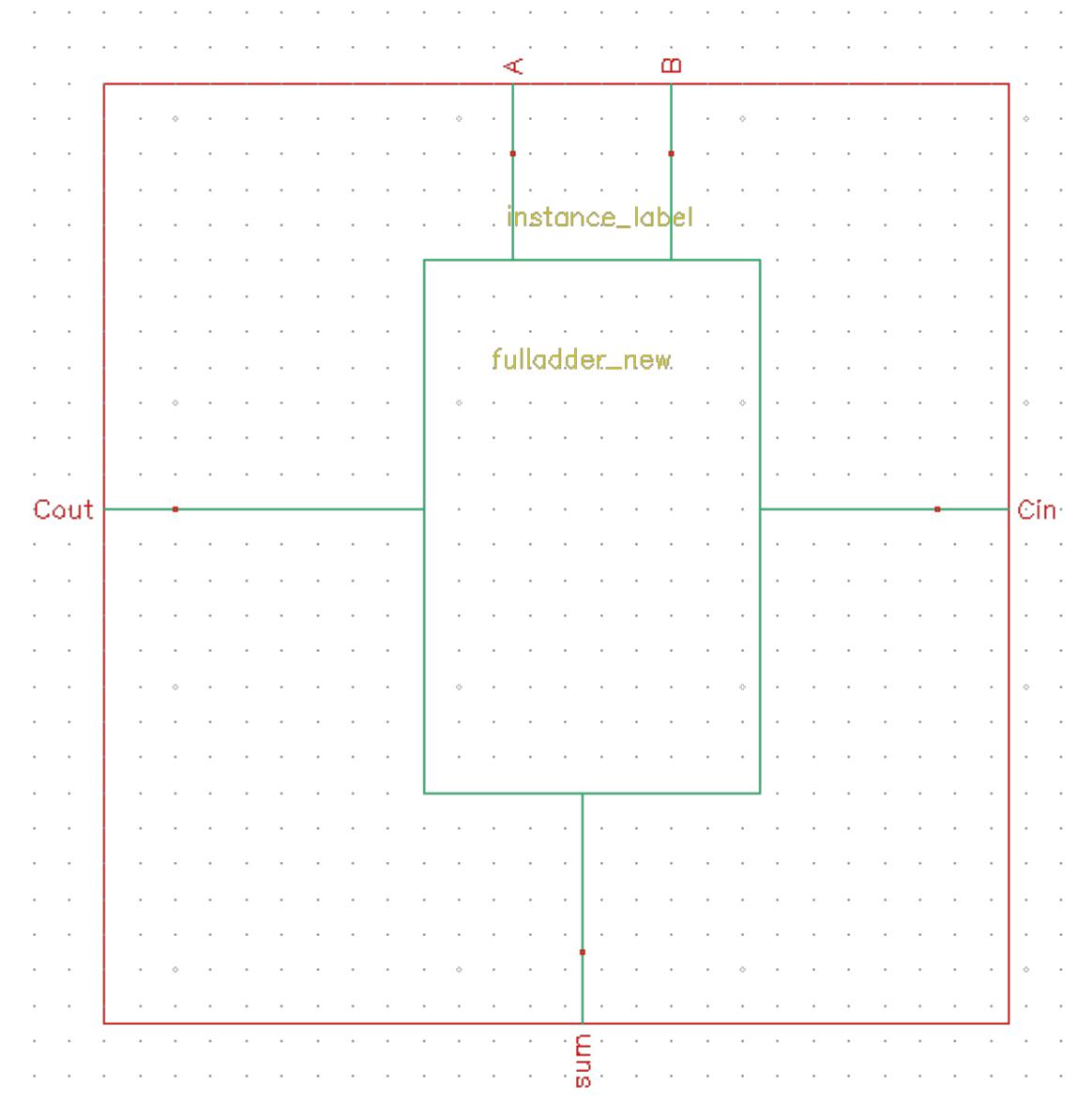
- DRC



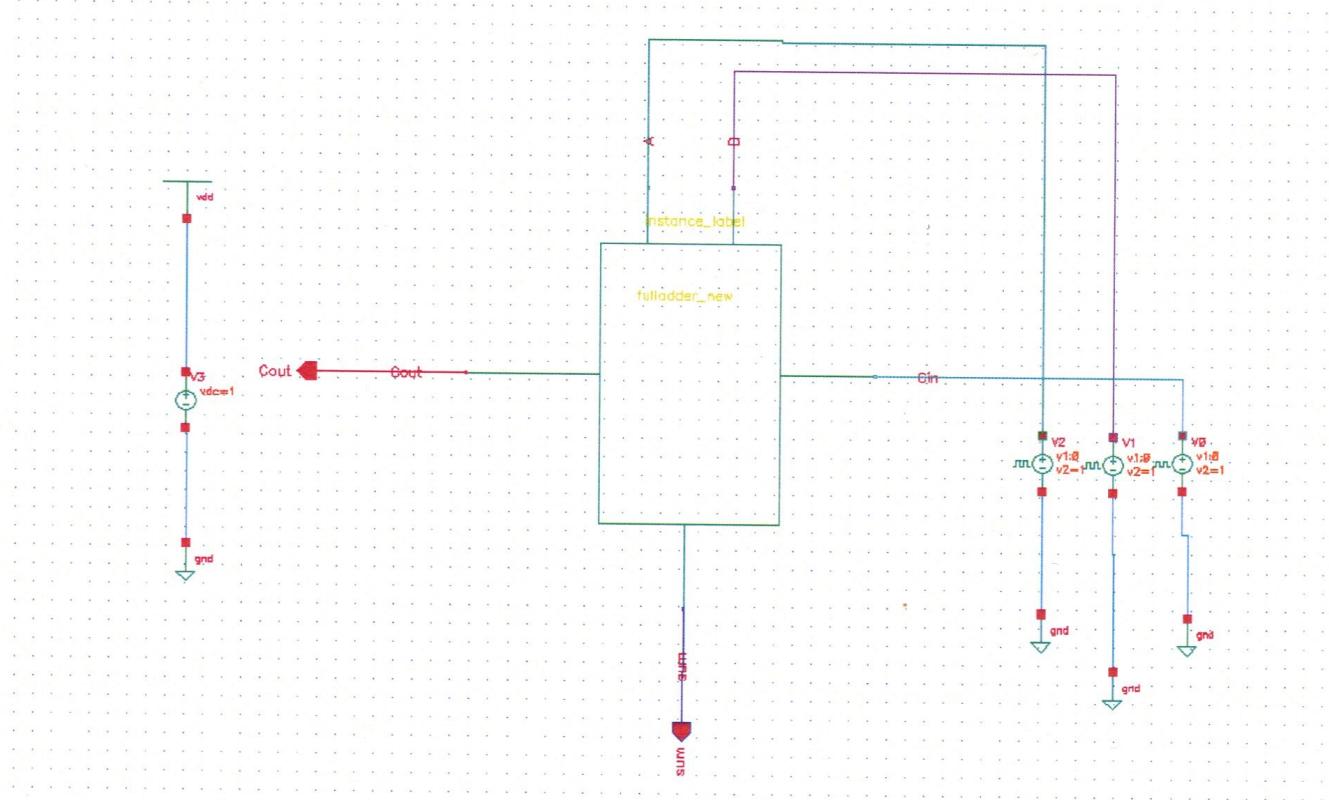
- LVS



- Symbol

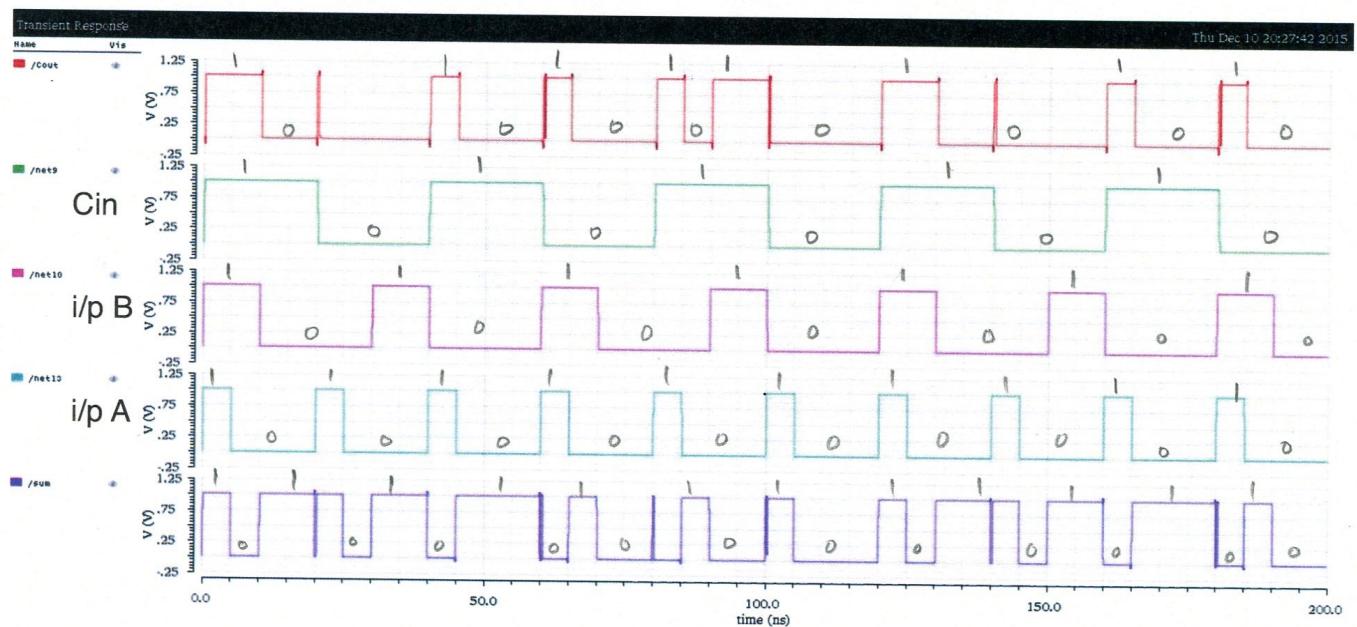


- Test bench Schematic

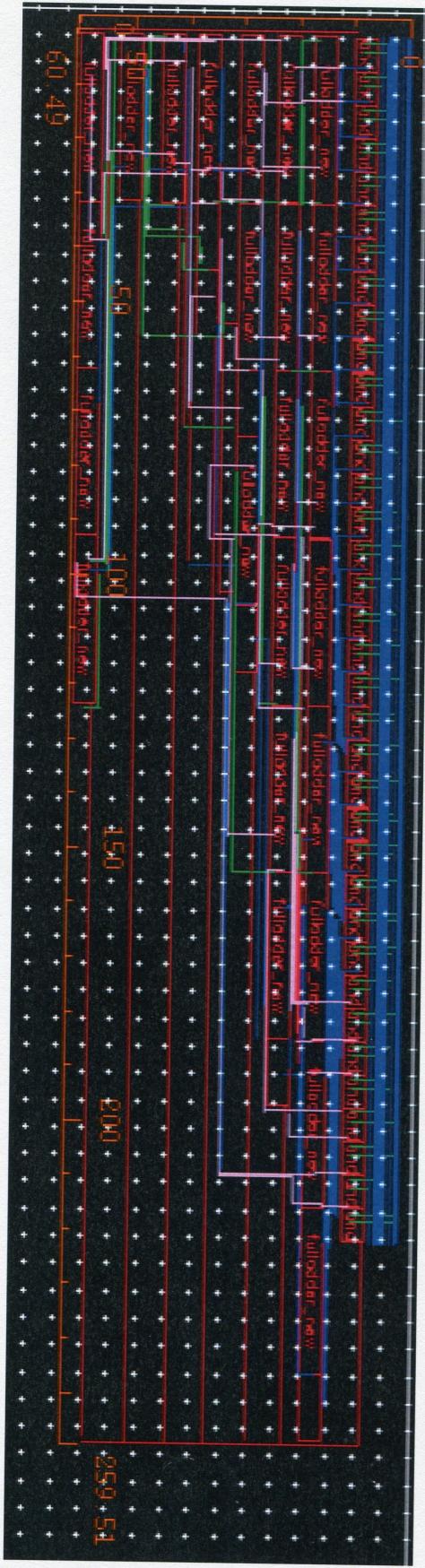


- Output Simulations

As observed from the graph outputs ‘sum’ and ‘carry’ follow the logic function of full-adder.



LAYOUT SHOWING AREA: $60.494 \text{ mm} \times 259.51 = 15723.7109 \text{ mm}^2 = 0.015723 \text{ mm}^2$



Inputs: $B_5 \ B_4 \ B_3 \ B_2 \ B_1 \ B_0 \ x$
 $A_5 \ A_4 \ A_3 \ A_2 \ A_1 \ A_0 = 0 \ 0 \ 0 \ 1 \ 1 \ 1$
 $P_n \ P_o \ P_g \ P_d \ P_e \ P_s \ P_t \ P_i \ P_o$

Binary '1' = 1.8V
 Binary '0' = 0V

