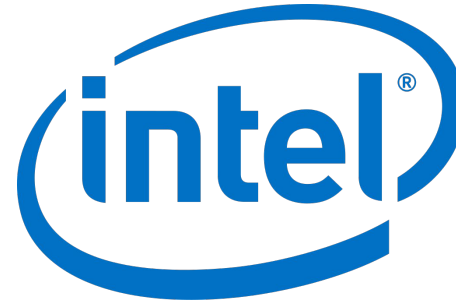


## Arquitecturas que se verán en la cátedra

---



x86

ISA	Pages	Words	Hours to read	Weeks to read
RISC-V	236	76,702	6	0.2
ARM-32	2736	895,032	79	1.9
x86-32	2198	2,186,259	182	4.5

**Figure 1.6: Number of pages and words of ISA manuals [Waterman and Asanović 2017a], [Waterman and Asanović 2017b], [Intel Corporation 2016], [ARM Ltd. 2014]. Hours and weeks to complete assumes reading at 200 words per minute for 40 hours a week. Based in part of Figure 1 of [Baumann 2017].**

# Combined Volume Set of Intel® 64 and IA-32 Architectures Software Developer's Manuals

Document	Description
<a href="#">Intel® 64 and IA-32 Architectures Software Developer's Manual Combined Volumes: 1, 2A, 2B, 2C, 2D, 3A, 3B, 3C, 3D, and 4</a>	<p>This document contains the following:</p> <p><b>Volume 1:</b> Describes the architecture and programming environment of processors supporting IA-32 and Intel® 64 architectures.</p> <p><b>Volume 2:</b> Includes the full instruction set reference, A-Z. Describes the format of the instruction and provides reference pages for instructions.</p> <p><b>Volume 3:</b> Includes the full system programming guide, parts 1, 2, 3, and 4. Describes the operating-system support environment of Intel® 64 and IA-32 architectures, including memory management, protection, task management, interrupt and exception handling, multi-processor support, thermal and power management features, debugging, performance monitoring, system management mode, virtual machine extensions (VMX) instructions, Intel® Virtualization Technology (Intel® VT), and Intel® Software Guard Extensions (Intel® SGX). NOTE: Performance monitoring events can be found here: <a href="https://perfmon-events.intel.com/">https://perfmon-events.intel.com/</a></p> <p><b>Volume 4:</b> Describes the model-specific registers of processors supporting IA-32 and Intel® 64 architectures.</p>
<a href="#">Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes</a>	<p>Describes bug fixes made to the Intel® 64 and IA-32 architectures software developer's manual between versions.</p> <p>NOTE: This change document applies to all Intel® 64 and IA-32 architectures software developer's manual sets (combined volume set, 4 volume set, and 10 volume set).</p>

<https://www.intel.com/content/www/us/en/developer/articles/technical/intel-sdm.html>

# INTEL 80386

## PROGRAMMER'S REFERENCE MANUAL

1986

Page 1 of 421

# Especificaciones RISC-V

<https://riscv.org/technical/specifications/>

## **The RISC-V Instruction Set Manual**

### **Volume I: Unprivileged ISA**

Document Version 20191213

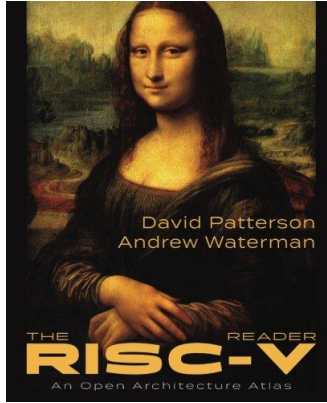
Editors: Andrew Waterman, Krste Asanović, SiFive Inc.,

## **The RISC-V Instruction Set Manual**

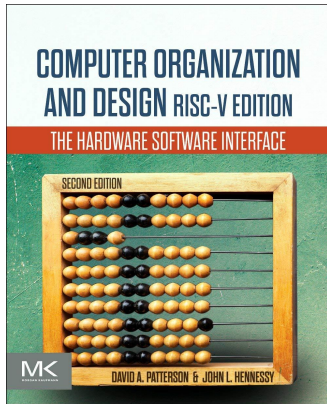
### **Volume II: Privileged Architecture**

Document Version 20211203

Editors: Andrew Waterman, Krste Asanović, John  
Hauser, SiFive Inc.,



The RISC-V Reader: An Open Architecture Atlas  
Paperback – November 7, 2017  
by [David Patterson](#), [Andrew Waterman](#)



Computer Organization and Design RISC-V Edition: The  
Hardware Software Interface - 2nd Edition  
by [David A. Patterson](#), [John L. Hennessy](#)

31	25	24	20	19	15	14	12	11	7	6	0		
imm[31:12]								rd	0110111			U lui	
imm[31:12]								rd	0010111			U auipc	
imm[20:10:1 11 19:12]								rd	1101111			J jal	
imm[11:0]				rs1	000			rd	1100111			I jalr	
imm[12:10:5]		rs2	rs1		000		imm[4:1 11]	1100011			B beq		
imm[12:10:5]		rs2	rs1		001		imm[4:1 11]	1100011			B bne		
imm[12:10:5]		rs2	rs1		100		imm[4:1 11]	1100011			B blt		
imm[12:10:5]		rs2	rs1		101		imm[4:1 11]	1100011			B bge		
imm[12:10:5]		rs2	rs1		110		imm[4:1 11]	1100011			B bltu		
imm[12:10:5]		rs2	rs1		111		imm[4:1 11]	1100011			B bgeu		
imm[11:0]				rs1		000		rd	0000011			I lb	
imm[11:0]				rs1		001		rd	0000011			I lh	
imm[11:0]				rs1		010		rd	0000011			I lw	
imm[11:0]				rs1		100		rd	0000011			I lbu	
imm[11:0]				rs1		101		rd	0000011			I lhu	
imm[11:5]		rs2	rs1		000		imm[4:0]	0100011			S sb		
imm[11:5]		rs2	rs1		001		imm[4:0]	0100011			S sh		
imm[11:5]		rs2	rs1		010		imm[4:0]	0100011			S sw		
imm[11:0]				rs1		000		rd	0010011			I addi	
imm[11:0]				rs1		010		rd	0010011			I slti	
imm[11:0]				rs1		011		rd	0010011			I sltiu	
imm[11:0]				rs1		100		rd	0010011			I xori	
imm[11:0]				rs1		110		rd	0010011			I ori	
imm[11:0]				rs1		111		rd	0010011			I andi	
0000000		shamt		rs1		001		rd	0010011			I slli	
0000000		shamt		rs1		101		rd	0010011			I srli	
0100000		shamt		rs1		101		rd	0010011			I srai	
0000000		rs2		rs1		000		rd	0110011			R add	
0100000		rs2		rs1		000		rd	0110011			R sub	
0000000		rs2		rs1		001		rd	0110011			R sll	
0000000		rs2		rs1		010		rd	0110011			R slt	
0000000		rs2		rs1		011		rd	0110011			R sltu	
0000000		rs2		rs1		100		rd	0110011			R xor	
0000000		rs2		rs1		101		rd	0110011			R srl	
0100000		rs2		rs1		101		rd	0110011			R sra	
0000000		rs2		rs1		110		rd	0110011			R or	
0000000		rs2		rs1		111		rd	0110011			R and	
0000		pred		succ		00000		000		00000		0001111	I fence
0000		0000		0000		00000		001		00000		0001111	I fence.i
000000000000						00000		000		00000		1110011	I ecall
000000000001						00000		000		00000		1110011	I ebreak
csr				rs1		001		rd		1110011			I csrsw
csr				rs1		010		rd		1110011			I csrrs
csr				rs1		011		rd		1110011			I csrrc
csr				zimm		101		rd		1110011			I csrrwi
csr				zimm		110		rd		1110011			I csrrsi
csr				zimm		111		rd		1110011			I csrrci

Figure 2.3: RV32I opcode map has instruction layout, opcodes, format type, and names. (Table 19.2 of [Waterman and Asanović 2017] is the basis of this figure.)

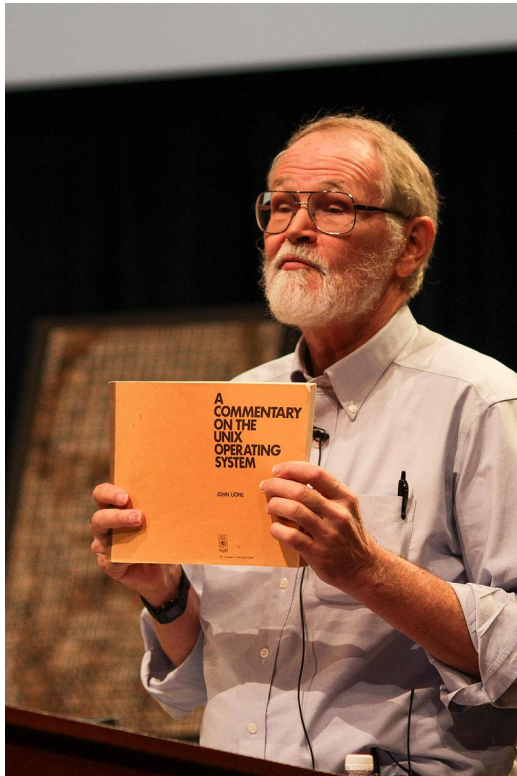
31	0
x0 / zero	Hardwired zero
x1 / ra	Return address
x2 / sp	Stack pointer
x3 / gp	Global pointer
x4 / tp	Thread pointer
x5 / t0	Temporary
x6 / t1	Temporary
x7 / t2	Temporary
x8 / s0 / fp	Saved register, frame pointer
x9 / s1	Saved register
x10 / a0	Function argument, return value
x11 / a1	Function argument, return value
x12 / a2	Function argument
x13 / a3	Function argument
x14 / a4	Function argument
x15 / a5	Function argument
x16 / a6	Function argument
x17 / a7	Function argument
x18 / s2	Saved register
x19 / s3	Saved register
x20 / s4	Saved register
x21 / s5	Saved register
x22 / s6	Saved register
x23 / s7	Saved register
x24 / s8	Saved register
x25 / s9	Saved register
x26 / s10	Saved register
x27 / s11	Saved register
x28 / t3	Temporary
x29 / t4	Temporary
x30 / t5	Temporary
x31 / t6	Temporary
32	
31	0
pc	
32	

**Figure 2.4:** The registers of RV32I. Chapter 3 explains the RISC-V calling convention, the rationale behind the various pointers (sp, gp, tp, fp), Saved registers (s0-s11), and Temporaries (t0-t6). (Figure 2.1 and Table 20.1 of [Waterman and Asanović 2017] is the basis of this figure.)

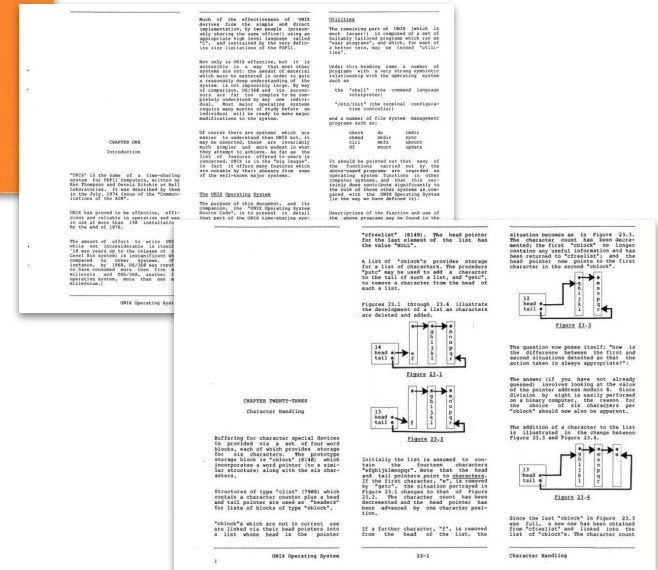
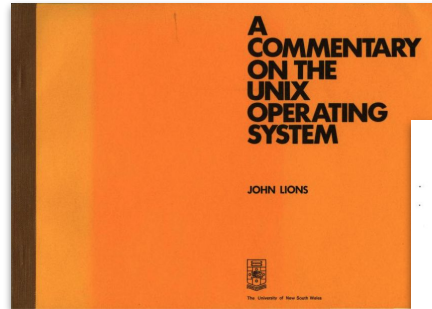


## **Caso de estudio: xv6**

# A Commentary on the UNIX Operating System



Brian Kernighan



[https://archive.org/details/bitsavers\\_attunix6thtaryontheUnixOperatingSystem197705\\_12314928](https://archive.org/details/bitsavers_attunix6thtaryontheUnixOperatingSystem197705_12314928)

<https://cs3210.cc.gatech.edu/r/unix6.pdf>



**xv6: a simple, Unix-like teaching operating system**

Russ Cox      Frans Kaashoek      Robert Morris

September 5, 2022

<https://pdos.csail.mit.edu/6.828/2023/xv6.html>

# Xv6, a simple Unix-like teaching operating system

## Introduction

---

Xv6 is a teaching operating system developed in the summer of 2006, which we ported xv6 to RISC-V for a new undergraduate class 6.1810.

## Xv6 sources and text

---

The latest xv6 source and text are available via

```
git clone https://github.com/mit-pdos/xv6-riscv.git
```

and

```
git clone https://github.com/mit-pdos/xv6-riscv-book.git
```

## Unix Version 6

---

xv6 is inspired by Unix V6 and by:

- *Lions' Commentary on UNIX' 6th Edition*, John Lions, Peer to Peer Communications; ISBN: 1-57398-013-7; 1st edition (June 14, 2000).
  - An on-line version of the [Lions commentary](#), and [the source code](#).
  - The v6 source code is also available [online](#) through [The Unix Heritage Society](#).

The following are useful to read the original code:

- *The PDP11/40 Processor Handbook*, Digital Equipment Corporation, 1972.
  - A [PDF](#) (made from scanned images, and not text-searchable)
  - A [web-based version](#) that is indexed by instruction name.

## **Repaso de la clase 1**

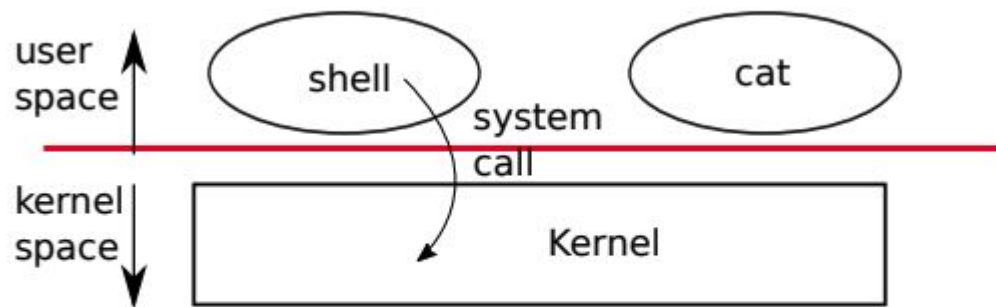


Figure 1.1: A kernel and two user processes.

System call	Description
<code>int fork()</code>	Create a process, return child's PID.
<code>int exit(int status)</code>	Terminate the current process; status reported to <code>wait()</code> . No return.
<code>int wait(int *status)</code>	Wait for a child to exit; exit status in <code>*status</code> ; returns child PID.
<code>int kill(int pid)</code>	Terminate process PID. Returns 0, or -1 for error.
<code>int getpid()</code>	Return the current process's PID.
<code>int sleep(int n)</code>	Pause for n clock ticks.
<code>int exec(char *file, char *argv[])</code>	Load a file and execute it with arguments; only returns if error.
<code>char *sbrk(int n)</code>	Grow process's memory by n bytes. Returns start of new memory.
<code>int open(char *file, int flags)</code>	Open a file; flags indicate read/write; returns an fd (file descriptor).
<code>int write(int fd, char *buf, int n)</code>	Write n bytes from buf to file descriptor fd; returns n.
<code>int read(int fd, char *buf, int n)</code>	Read n bytes into buf; returns number read; or 0 if end of file.
<code>int close(int fd)</code>	Release open file fd.
<code>int dup(int fd)</code>	Return a new file descriptor referring to the same file as fd.
<code>int pipe(int p[])</code>	Create a pipe, put read/write file descriptors in <code>p[0]</code> and <code>p[1]</code> .
<code>int chdir(char *dir)</code>	Change the current directory.
<code>int mkdir(char *dir)</code>	Create a new directory.
<code>int mknod(char *file, int, int)</code>	Create a device file.
<code>int fstat(int fd, struct stat *st)</code>	Place info about an open file into <code>*st</code> .
<code>int stat(char *file, struct stat *st)</code>	Place info about a named file into <code>*st</code> .
<code>int link(char *file1, char *file2)</code>	Create another name (file2) for the file file1.
<code>int unlink(char *file)</code>	Remove a file.

Figure 1.2: Xv6 system calls. If not otherwise stated, these calls return 0 for no error, and -1 if there's an error.



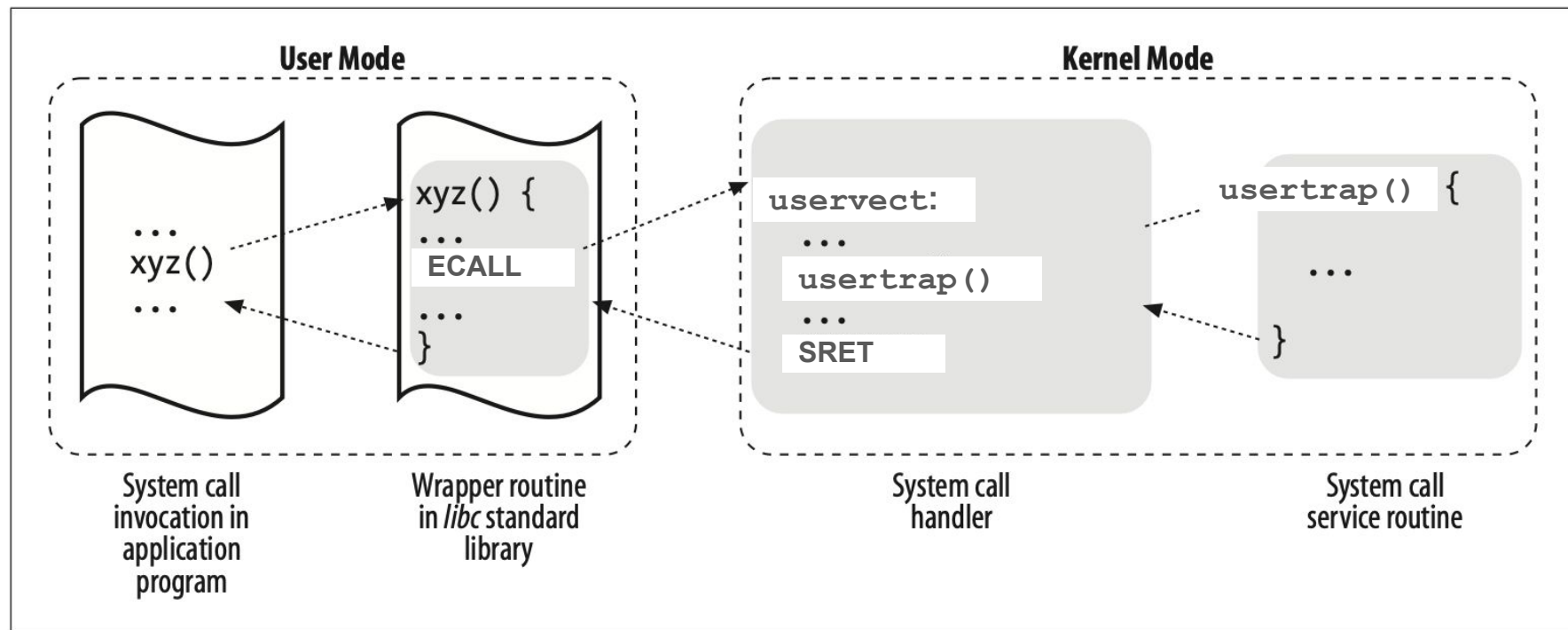
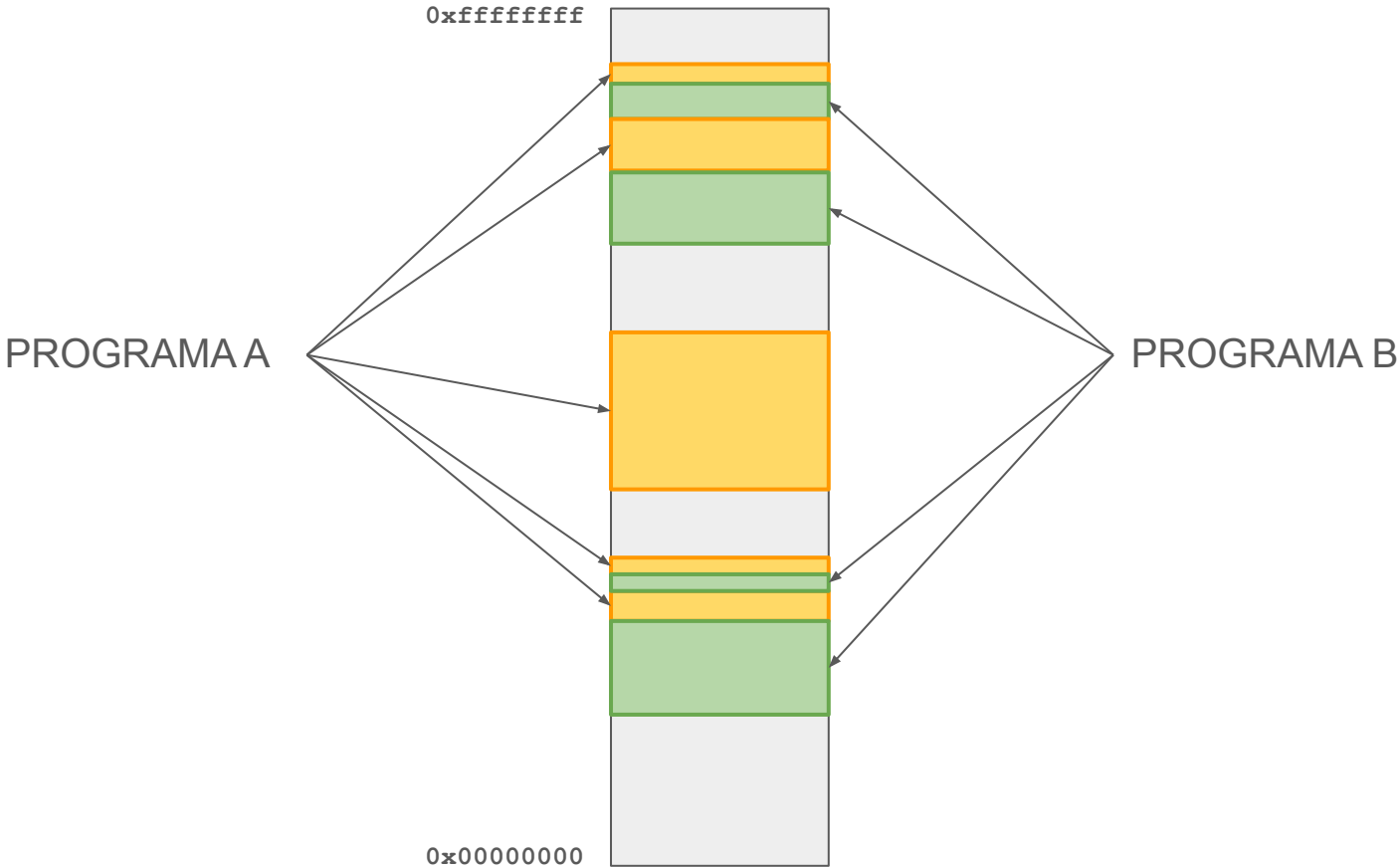
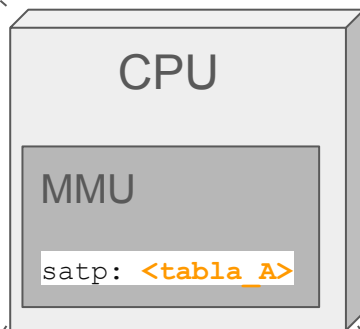
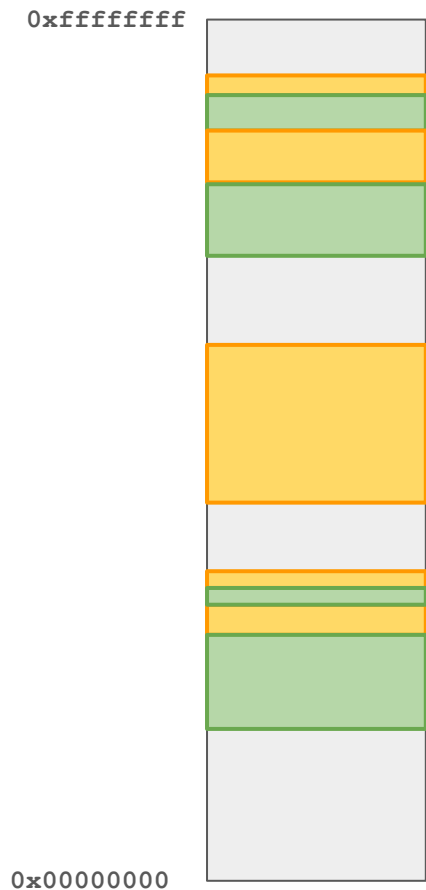


Figure 10-1. Invoking a system call

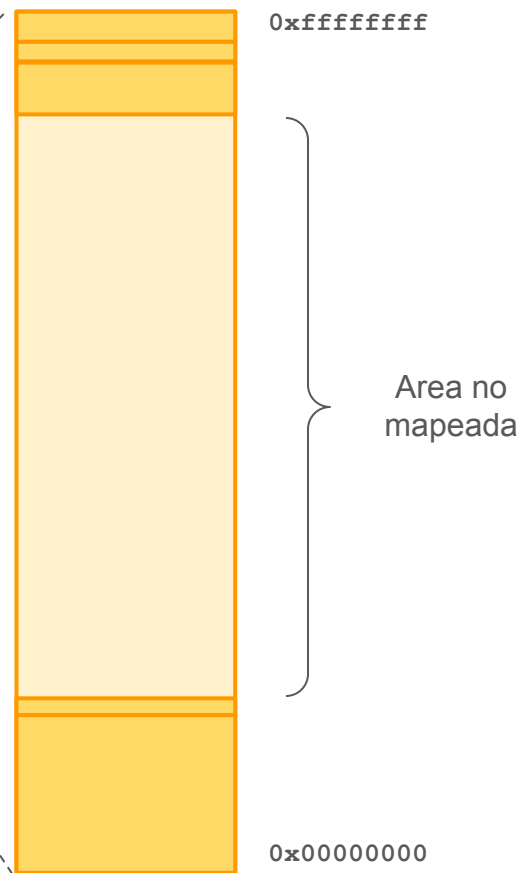
Memoria Fisica



## Memoria Fisica

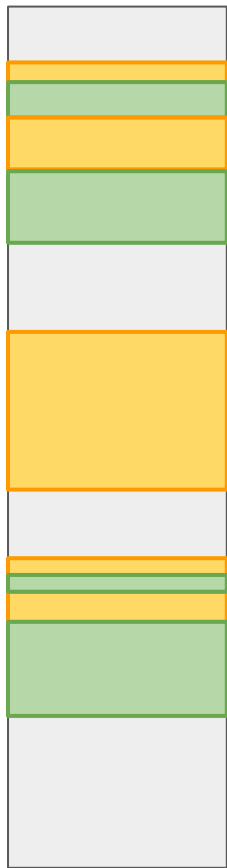


## Memoria Virtual



## Memoria Fisica

0xffffffff



0x00000000

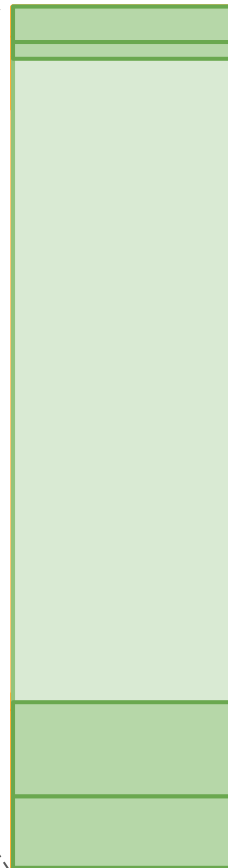
CPU

MMU

satp: <tabla\_B>

## Memoria Virtual

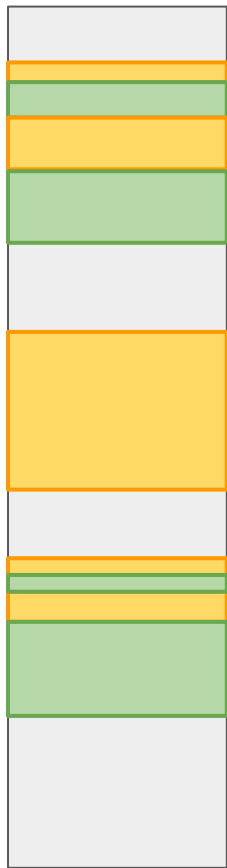
0xffffffff



0x00000000

## Memoria Fisica

0xffffffff



0x00000000

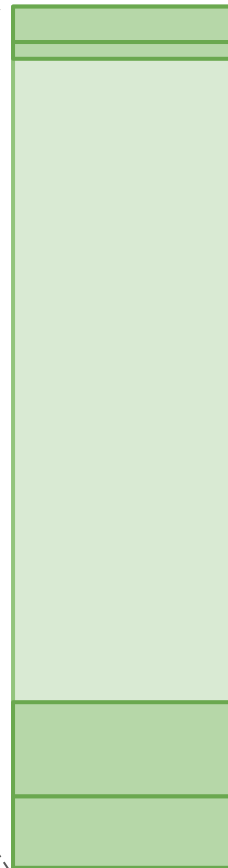
CPU

MMU

satp: <tabla\_B>

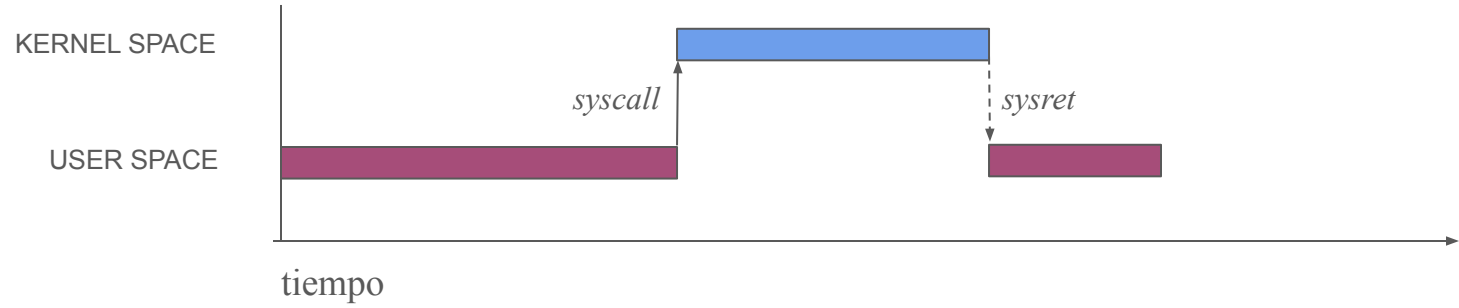
## Memoria Virtual

0xffffffff

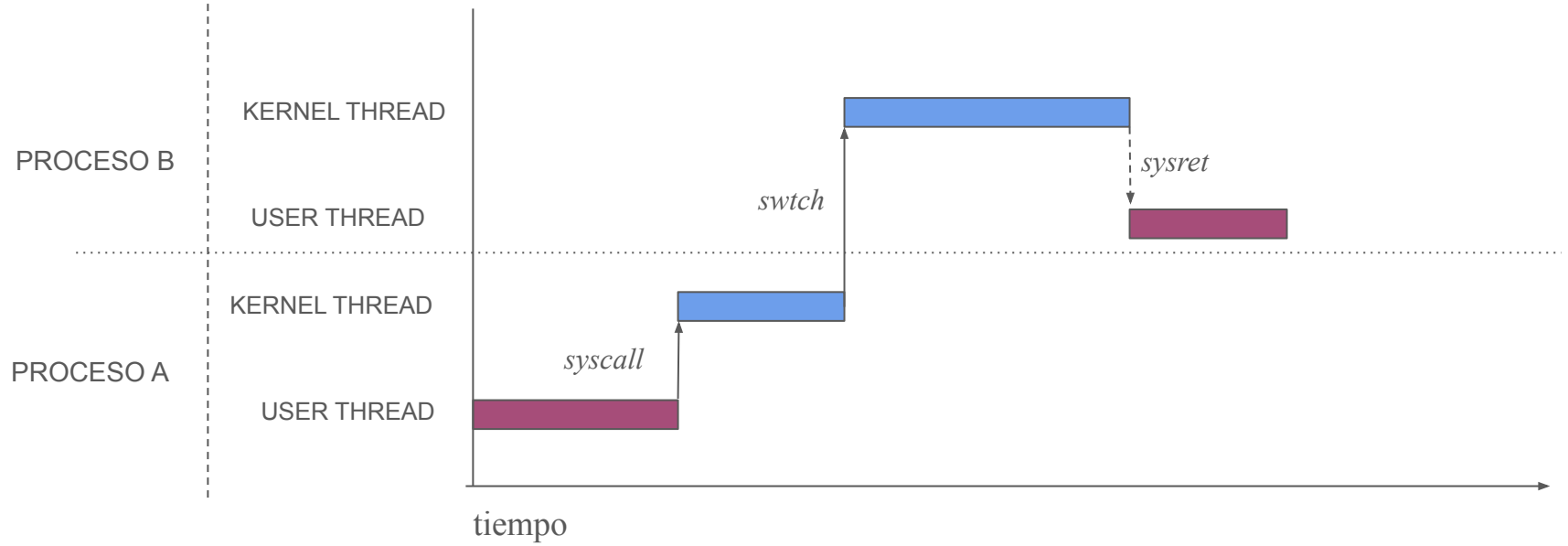


0x00000000

# Transición User-Kernel

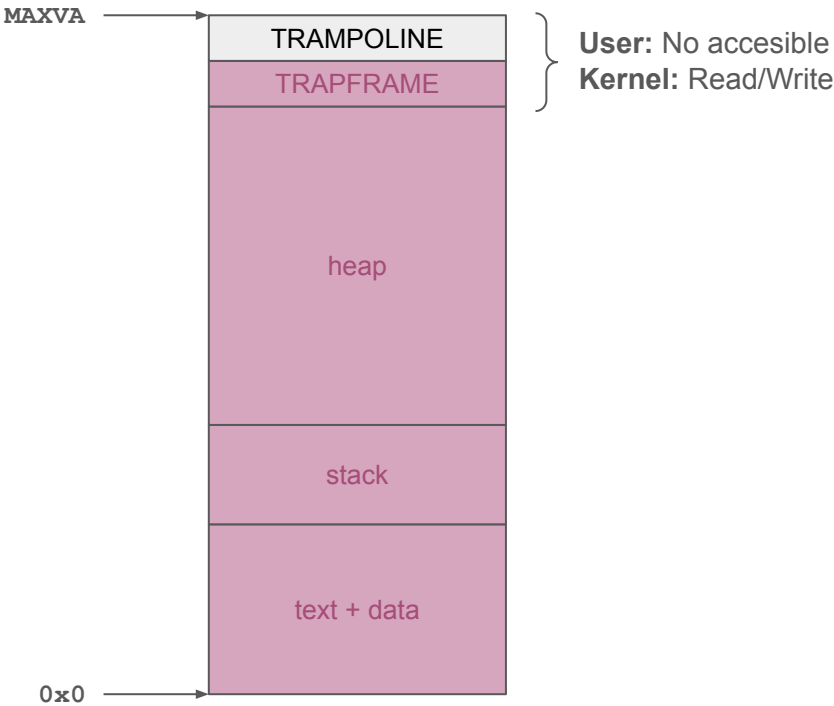


# Context Switch



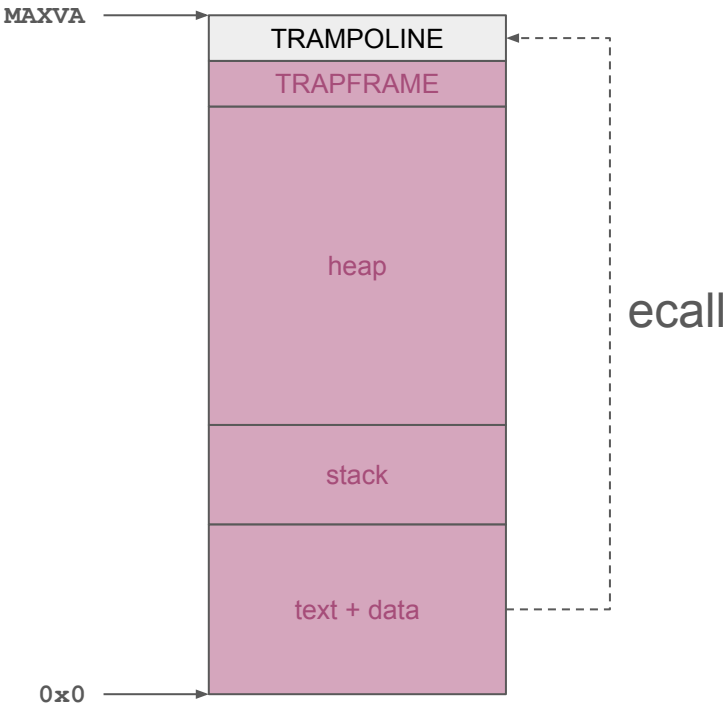
# Transición User-Kernel

Memoria virtual en user space



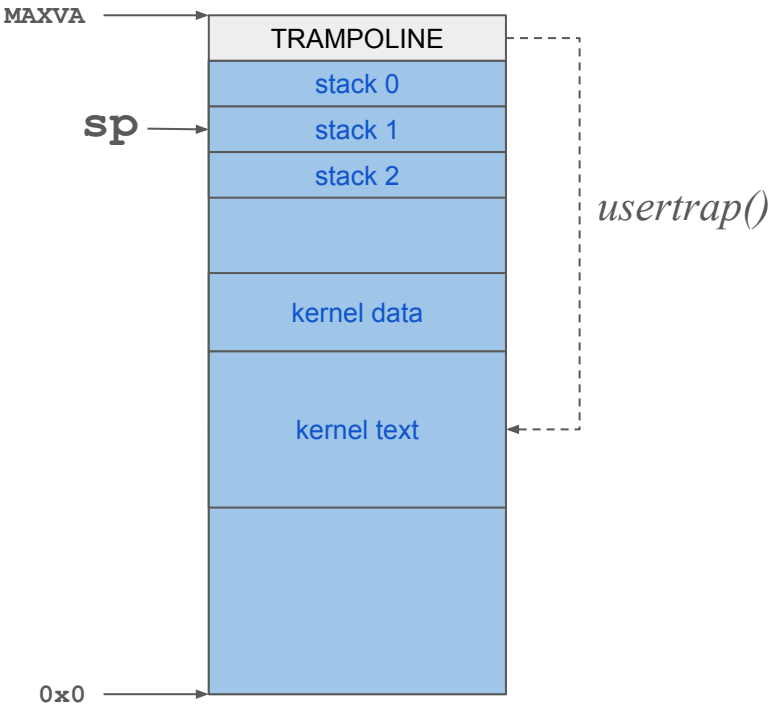


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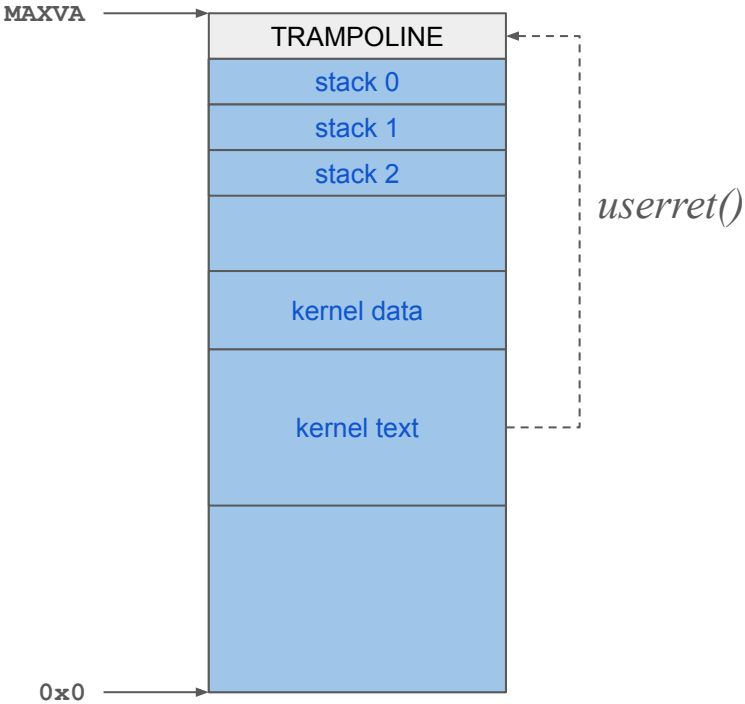


# Transición User-Kernel

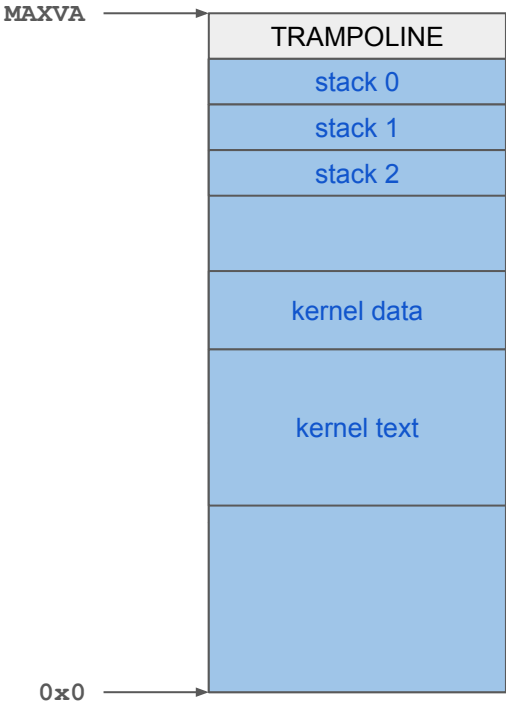
Memoria virtual en kernel space



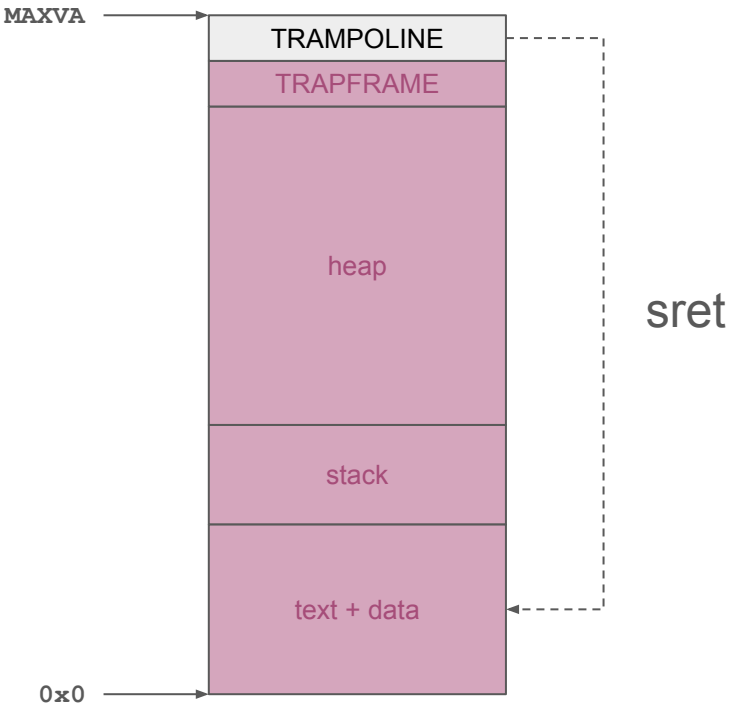
# Transición User-Kernel

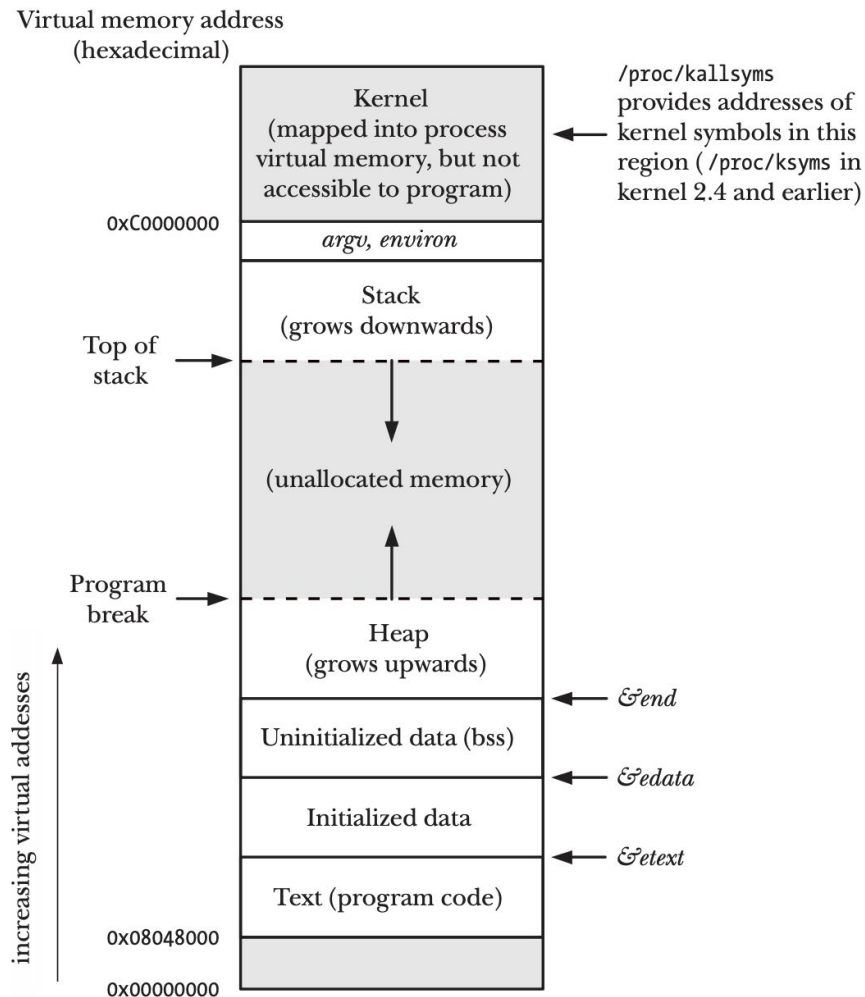


# Transición User-Kernel



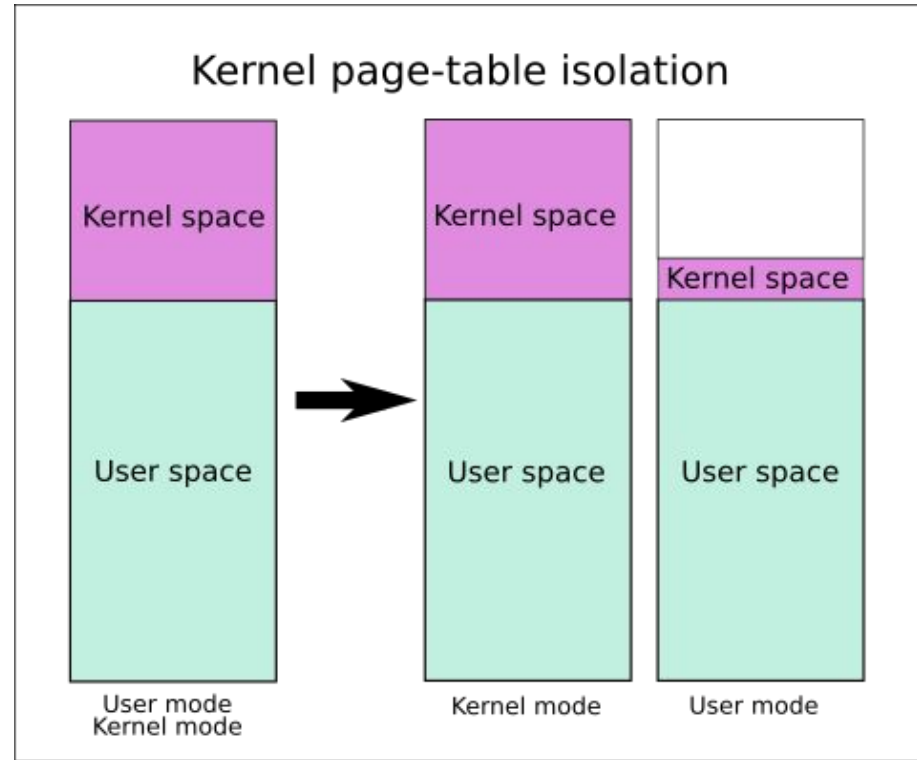
# Transición User-Kernel





**Figure 6-1:** Typical memory layout of a process on Linux/x86-32

# Vulnerabilidad Meltdown y su mitigación



Meltdown: <https://medium.com/@mattklein123/meltdown-spectre-explained-6bc8634cc0c2>

KPTS: [https://en.wikipedia.org/wiki/Kernel\\_page-table\\_isolation](https://en.wikipedia.org/wiki/Kernel_page-table_isolation)