Santiago **Mok**

Software Developer · FPGA Design Tool

San Jose, CA 95118

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Summary

FPGA Design Tool Software Developer currently at Intel. Over 14+ years of experience developing C++ software in FPGA design tools and EDA. Highly motivated and team collaborator in new software features development cycle. Track record of mentoring other software developers. Experienced in working with geographically distributed and cross functional teams.

Skills

Programming	Modern C++, Python, Tcl
Tool/Framework	Docker, Kubernetes, Rancher, boost C++, GNU utils, Flask, Django, Swig, Perforce, Git
Best-Practices	Peer code-reviews, unit-test, regression test, agile development
Foreign Languages	Spanish and Cantonese

Professional Experience

Intel Corp.

San Jose, CA

Sr. Staff Software Engineer

Apr. 2022 - Present

Supervisor and lead developer in Intel Quartus Prime software development. I lead multiple projects on productivity tools enhancement, Tcl scripting interfaces, web dashboard development, IP license flows, and backward compatibility. A mentor to other Quartus developer on FPGA design flows and internal C++ tool libraries.

- Key software developer in user design data model replacement in Quartus; a multi-year effort that require close collaboration with compiler engine.
- Engage with feature owner and field engineer to improve usability of new productivity tools.
- Supervise and mentor engineer in development of web dashboard (in containerized environment) to monitor progression of new feature productization.
- A consultant on many Quartus features support and enhancements in light of new developments.

Intel Corp.

San Jose, CA

Staff Software Engineer

Apr. 2017 - Mar. 2022

Lead developer in Quartus hierarchical design infrastructure development. In this role, I worked with system architects and other senior developers to design and implement C++ core libraries and data models to aid modernizing design netlist interfaces for large-scale FPGA devices.

- Design and implement an abstract interface database access layer to the underlying database for GUI applications and Tcl scripting interface.
- Implemented a notification system (in C++) to aid synchronizing design netlist states.
- Design a global state machine manager to better manage resources allocated through singleton design patterns in monolithic codebase, 20+ years legacy.
- Mentor other developers in Quartus advance hierarchical flows.

Supervisor lead on infrastructure project to validate developer code submission.

- Scope and design RESTful API in Django to verify perforce change submission
- Design for extensibility allowing DevOps to extend and configure validation specifications
- Mentor junior engineer on infrastructure implementation and test development Key developer in Quartus Hierarchical Design Database Infrastructure

FPGA-as-a-Service development on the Cloud

- Set-up single-host Kubernetes with FPGA device support to model data center service
- Create gRPC service for running image classification inference workload
- Joint work with Intel colleague presented on Spark+AI 2018 Conference link here: https://www.youtube.com/watch?v=AMXMfzgN0CY

Intel Corp. *San Jose, CA*

Sr. Software Engineer *Apr. 2015 - Mar. 2017*

Lead cross-functional project involving software database with advance HW designer flows.

- Scope design specifications for database compatibility across software version and align with advance designer flows
- Align test engineering with FPGA hardware modeling engineer
- Apply C++ boost serialization as persistent storage technique
- Implement tools to apply incremental changes from device software model updates Lead infrastructure project to validate developer code submission

Key developer in Quartus Hierarchical Design Database Infrastructure

- Design and implement flows to persist and validate encrypted IP licenses requirement
- Implement infrastructure to model partition-based design data and advance user flows
- Enhance and migrate database infrastructure
- Lead 3 other engineers on design and test development

Altera Corp. *San Jose, CA*

Software Engineer *Apr. 2011 - Mar. 2015*

Responsible for software data modeling of FPGA devices in Quartus II software

- Implemented C++ data structure to model hierarchical connectivity of FPGA blocks
- Implemented translation lookup of device model data with python extension
- Maintain and promote use of SWIG as interface generator to extend C++ to Python and Tcl
- Improved developer productivity by reducing software build time from 8 hours to 4 hours

NanoCAD Lab, UCLA (Prof. Puneet Gupta) *Los Angeles, CA*

Graduate Research Assistant *Sept. 2009 - Mar. 2011*

- VLSI CAD research on gate sizing algorithms to optimize for leakage power on post-layout designs.
- Published a comparative study of gate sizing techniques to reduce leakage power.
- Contributed incremental STA algorithm and wire delay calculator to open-source timing-analysis engine.

Publication

Santiago Mok, John Lee, Puneet Gupta, "Post-Layout Sizing for Leakage Power Optimization: A Comparative Study", in ACM Transaction on Design Automation of Electronic System, Jan. 2013

Education

University of California Los Angeles (UCLA) *Los Angeles, CA*

M.S. in Electrical Engineering *Sept. 2009 - Mar. 2011*

- Specialization in Digital Circuit Design Automation
- Research adviser: Dr. Puneet Gupta (NanoCAD Research Group)

University of California Los Angeles (UCLA) *Los Angeles, CA*

B.S. in Electrical and Computer Engineering *Sept. 2007 - June 2009*

- Undergraduate Research Fellow Program Scholarship
- CEED Research Scholar