# CURRENT FEEDBACK AMPLIFIERs

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*Abstract*-The need for high speed, wideband amplifiers is the driving force behind the development of the Current Feedback Amplifier (CFA). The CFA has significant advantages over conventional amplifiers in terms of slew rate performance and inherently wide bandwidth. This paper provides a review of the theory and design of current feedback amplifiers.

## I. INTRODUCTION

Analog design has historically been dominated by voltage mode signal processing [1]. This is apparent in the electronics industry where the Voltage Feedback Amplifier (VFA) has become ubiquitous. The lesser-known Current Feedback Amplifier (CFA) has a fundamentally different architecture and offers significant performance advantages over the traditional VFA. Although, the underlying circuit concepts have been around for many years, modern complementary bipolar processes were required for practical CFAs to be realized. The CFA was largely made popular in the mid 1980's by Comlinear Corporation. The early designs were hybrid amplifiers like the CLC205, which was representative of the typical performance attainable. The CLC205 offered a $-3dB$ bandwidth in excess of 200MHz at low gains (80MHz at $50V/V$) and $2400V/\mu s$ slew rate with $\pm 15V$ supply rails. The first monolithic device, the EL2020, was introduced in 1987 by Elantec Inc. The EL2020 achieved a 50MHZ $-3dB$ bandwidth at a gain of $1V/V$ (30MHz at $10V/V$) and $500V/\mu s$ slew rate [1, 2, 3].

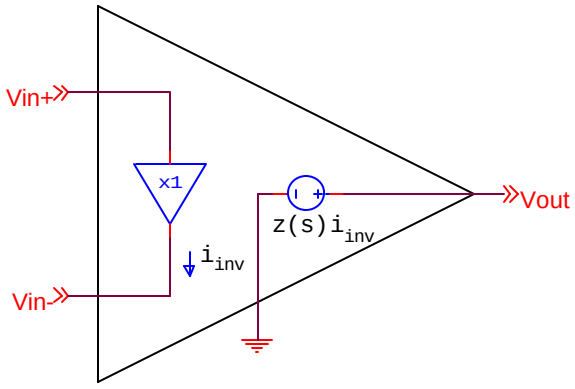
## II. CURRENT FEEDBACK AMPLIFIER FUNDAMENTALS

The operation of the CFA is best understood by considering the idealized model shown in Figure 1(a). A unity gain buffer is connected between the two input terminals such that $v_{in-}$ is forced to track $v_{in+}$. The inverting/non-inverting input terminal is

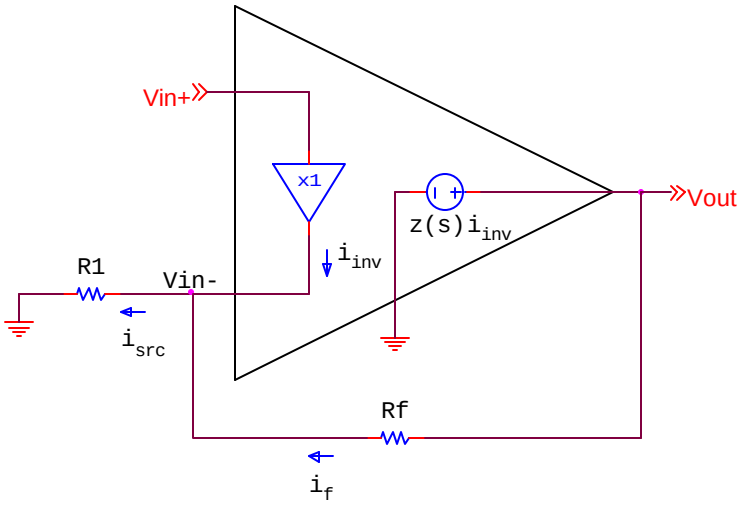
actually the output/input of the unity gain buffer, which ideally has zero output impedance and infinite input impedance. As a result, the inverting input impedance is zero whereas the non-inverting input impedance is infinite. The output is a linear, current-controlled voltage source with zero output impedance,

$$v_o = z(s) i_{inv} \qquad (1)$$

where z(s) is the transimpedance parameter (in ohms) and $i_{inv}$ is the current flowing out of the inverting input terminal.




(a)




(b)

**Figure 1: (a) Ideal CFA model; (b) Non-inverting configuration**

The basic non-inverting configuration of a CFA is shown in Figure 1(b). Analysis of this circuit reveals a unique relationship between the feedback resistor and the closed loop bandwidth. The output voltage is sensed and converted into current, which is fed back to the inverting input. Feedback acts to minimize the inverting input current. The unity gain buffer forces the voltage at the inverting terminal to $v_{in+}$. Combining the feedback current ($i_f$) and source current ($i_{src}$) at the inverting input terminal gives

$$i_{inv} = i_{src} - i_f = \frac{v_{in} - 0}{R_1} - \frac{v_o - v_{in}}{R_f} \qquad (2)$$

The overall closed loop voltage gain is then,

$$A_{VCL} \equiv \frac{v_o}{v_i} = \frac{1 + \frac{R_f}{R_1}}{1 + \frac{R_f}{z(s)}} \qquad (3)$$

As expected, the familiar closed loop voltage gain $1 + R_f / R_1$ is obtained as $z(s)$ approaches infinity. Assuming dominant pole compensation, the transimpedance can be approximated by,

$$z(s) = \frac{z_o}{1 + j(w/w_o)} \qquad (4)$$

where $w_o$ is the –3dB frequency and $z_o$ is the DC resistance. Substituting Eq. (4) into Eq. (3) and rearranging gives,

$$A_{VCL} = \frac{\left(1 + \frac{R_f}{R_1}\right)\left(\frac{z_o}{z_o + R_f}\right)}{1 + jw\left(\frac{R_f}{(z_o + R_f)w_o}\right)} \cong \frac{1 + \frac{R_f}{R_1}}{1 + j\left(\frac{w}{w_a}\right)} \qquad (5)$$

where the approximation for $A_{VCL}$ is valid for $z_o >> R_f$. The closed loop amplifier –3dB frequency ($\omega_a$) is given by,

$$\omega_a = \frac{(z_o + R_f)\omega_o}{R_f} \cong \frac{z_o \omega_o}{R_f} \qquad (6)$$

Thus, for a first order circuit only the feedback resistor determines the closed loop bandwidth. The closed loop gain can be set using resistor $R_1$. The relationship between the gain and frequency characteristics is shown in Figure 2(a) [4, 5].

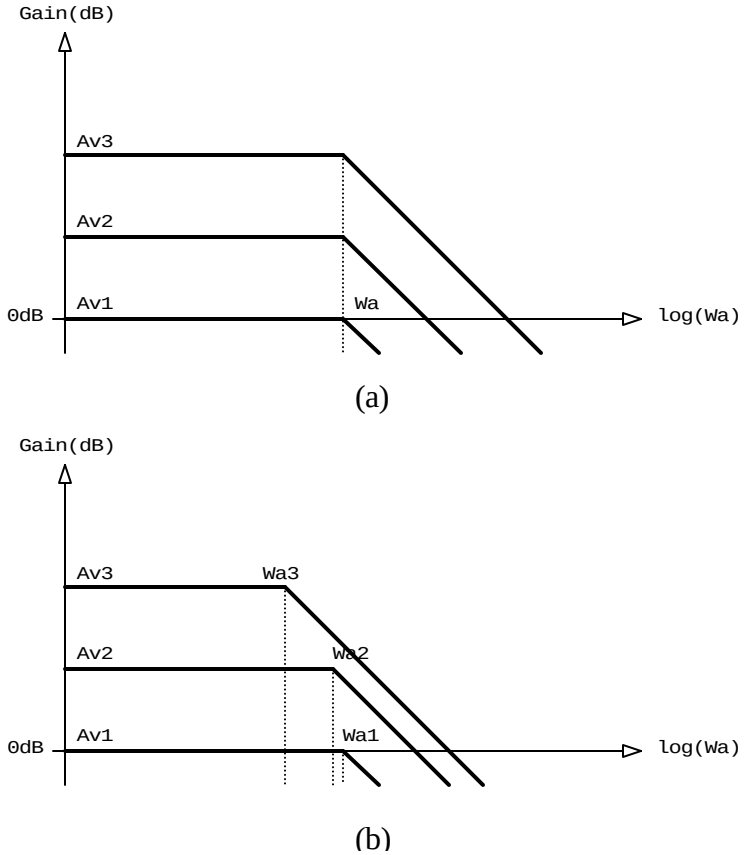



**Figure 2: (a) Frequency response $R_{o1,2} = 0$ ; (b) Frequency Response $R_{o1,2} \neq 0$**

The preceding analysis suggests that the closed loop gain does not affect the frequency response of the circuit once the feedback resistor has been set. However, in practice, the frequency response does vary with the closed loop gain due to the finite

output impedance ( $R_{o1}$ ) of the input unity gain buffer. The model of the CFA amplifier incorporating $R_{o1}$ is shown in Figure 3. The expression for the inverting input current can be derived from the following equations,

$$i_{inv} = i_{src} - i_f \qquad (7)$$

$$i_{inv} = \frac{v_{in+} - v_{in-}}{R_{o1}} \qquad (8)$$

$$i_{inv} = \frac{v_{in-}}{R_1} - \frac{v_o - v_{in-}}{R_f + R_{o2}} \qquad (9)$$

$$i_{inv}\left(1 + \frac{R_{o1}}{R_1} + \frac{R_{o1}}{R_f + R_{o2}}\right) = \frac{v_{in+}}{R_1} - \frac{v_o - v_{in+}}{R_f + R_{o2}} \qquad (10)$$

$$i_{inv} = \frac{v_{in+}}{R_1'} - \frac{v_o - v_{in+}}{R_f'} \qquad (11)$$

$$R_1' = R_1\left(1 + R_{o1}/R_1 + R_{o1}/\left(R_f + R_{o2}\right)\right) \qquad (12)$$

$$R_f' = \left(R_f + R_{o2}\right)\left(1 + R_{o1}/R_1 + R_{o1}/\left(R_f + R_{o2}\right)\right) \qquad (13)$$

The –3dB frequency is given by,

$$\omega_a \cong \frac{z_o \omega_o}{R_f'} = \frac{z_o \omega_o}{R_f + R_o\left(1 + R_f/R_1\right)} = \frac{z_o \omega_o}{R_f + R_o A_{VCL}} \qquad (14)$$

Consequently, the effect of $R_{o1}$ is to decrease the –3dB frequency for increasing closed loop gain. This decrease in bandwidth is not as drastic as that observed in the VFA.

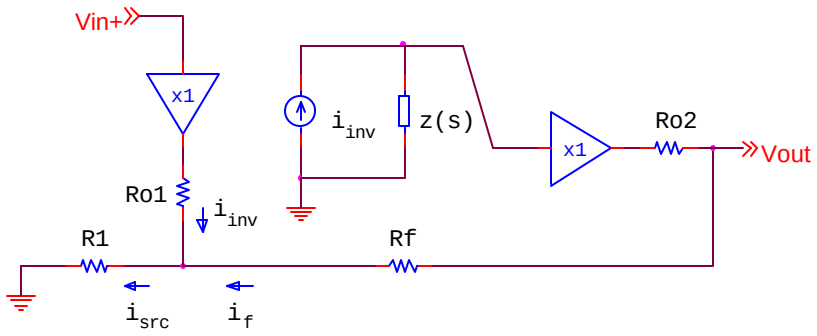



**Figure 3: CFA small signal model**

A modern single stage CFA is shown in Figure 4. The majority of commercial CFAs are a variation of this circuit. The input unity gain buffer consists of transistors Q1-Q4. Q3 and Q4 are configured as a complementary pair, push pull stage with low output impedance. The bias for this stage is generated by passing a constant current through Q1,2 such that Q3,4 are just on the edge of the active operating region. Q5 and Q6 sense the collector currents $i_{C3}$ and $i_{C4}$, which are mirrored to the high impedance node (Z) by Q7 and Q8 respectively. Thus, the effective current flowing into node Z $(i_{C7} - i_{C8})$ is a replica of $i_{inv}$. The output stage consisting of Q9-Q12 buffers the voltage at node Z to the output, thereby providing a low output impedance. Dominant pole compensation is realized by placing a capacitor between the high impedance node and ground.

The impedance at node Z is determined by using the equivalent small signal model and applying a test voltage at that node. The impedance is then defined as the ratio $v_X/i_X$ and is given by,

$$z(s) = \frac{v_x}{i_x} = r_{o7} \parallel r_{o8} \parallel r_{iob} \parallel (1/sC_c) = z_o \parallel (1/sC_c) \qquad (15)$$

where $r_{o7,8}$ represents the finite output impedance seen looking into the collector of Q7,8 and $r_{iob}$ is the output stage input impedance. Under worst-case conditions (i.e. with the

output connected to ground) the impedance seen looking into the bases of Q9 and Q10 can be determined by using the resistance reflection rule,

$$r_{iob} = \left[r_{p9} + (\beta_9 + 1) r_{p11}\right] \| \left[r_{p10} + (\beta_{10} + 1) r_{p12}\right] \qquad (16)$$

## III. STABILITY ANALYSIS

As the feedback resistance (or impedance) is reduced, the amplifier bandwidth increases. However, there is a corresponding loss of phase margin due to the higher order poles of z(s), which were ignored in Eq. (15). If the negative of the loop gain equals –1, or alternatively if the phase margin is zero and the amplifier gain is greater than 1, the CFA will become unstable. Even if the phase response fails to reach the crossover point, the CFA may still exhibit unacceptable peaking and ringing. Therefore, in order to guarantee stability a minimum feedback resistance ( $R_{\min}$ ) is required [6].

A more accurate representation of z(s) was presented in [7],

$$z(s) = \frac{z_o}{(1 + s\tau_1)(1 + s\tau_2)} \qquad (17)$$

where $1/\tau_1$ is the dominant pole frequency, $1/(z_o C_c)$, and $1/\tau_2$ models the higher frequency poles due to the current mirrors. For a maximally flat frequency response the feedback resistor should be chosen such that $R_f = 2\tau_2 / C_c$. The –3dB frequency is then given by,

$$\omega_a = \frac{0.707}{\tau_2} \qquad (18)$$

For an arbitrary phase margin $\phi_M$, the value of the feedback resistor can be determined from,

$$R_f' = \frac{2\tau_2}{C_c\sqrt{\left(\frac{2}{\tan^2 \omega_M}+1\right)^2-1}} \qquad (19)$$

and Eq. (13). A common misconception is that purely capacitive feedback will cause the CFA to oscillate. The reasoning is that the equivalent impedance of the feedback capacitor at higher frequencies is less than $R_{min}$. Nevertheless, a relatively stable circuit with capacitive feedback can be realized if the following condition is satisfied [7],

$$\frac{C_f}{C_c} >> \frac{\tan \omega_M}{2}\sqrt{\left(\frac{2}{\tan^2 \omega_M}+1\right)^2-1}$$

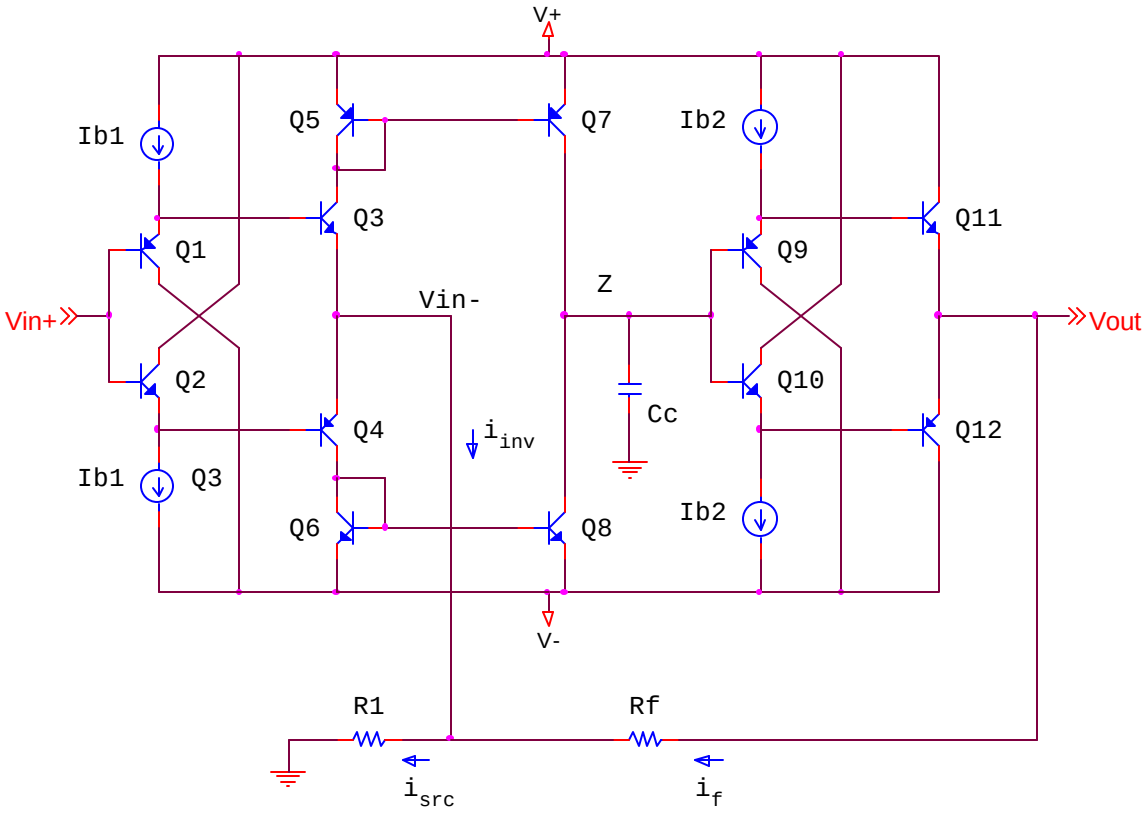



**Figure 4: A typical modern single stage CFA**

## IV. SLEW RATE

Consider a positive going voltage applied to the non-inverting input terminal for the circuit in Figure 4. The base voltage of Q1,2 increases by the same amount whereas the inverting input voltage increases by an amount almost equal in magnitude. Since the inverting input voltage is >0V, Q3 will source an error current into the external feedback resistor network, which is mirrored to the high impedance node. Thus, the voltage at the output is equal to the error current multiplied by the equivalent node impedance. The slew rate depends on the ability of Q7,8 to charge or discharge the compensation capacitor. Notice, that the input stage bias does not limit the available charging current. The error current that Q7/Q8 sources/sinks is dynamic. Therefore, to the first order, the slew rate is infinite. Ultimately, however, the slew rate is limited by the parasitic transistor capacitances and the finite base currents in the input and output buffer stages. Current boost circuitry can be used to reduce the effect of the parasitic capacitances and provide an order of magnitude increase in the slew rate. Figure 5(b) shows an improved slew rate buffer stage. For a positive input voltage step, as Q1 begins to slew due to Cjsp and Cjcn, Q2 sources more current to charge Cjsn and Cjsp. This extra current is re-circulated through Q7, which increase the bias current for Q1. Similarly, for a negative input voltage step, Q1 sinks more current to charge Cjsp and Cjsn, which is re-circulated through Q8 and increases the bias current for Q2 [8].

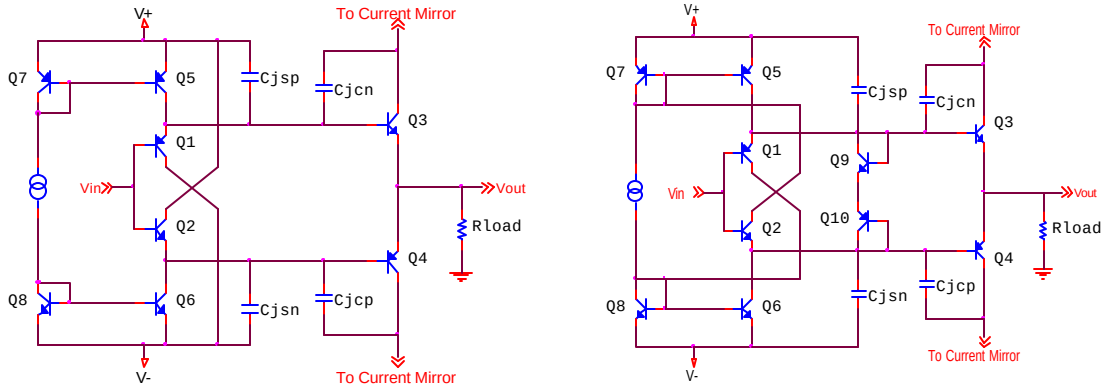



**Figure 5: (a) Simple CFA input stage; (b) CFA input stage with current boost circuitry**

## V. DC OFFSET ERROR

The asymmetrical circuit architecture of the CFA makes it very difficult at best to minimize the input offset voltage. The DC offset error from the input to the output can be expressed as,

$$V_{out}\,|_{Vin=0V} = V_{os-}A_{VCL} + I_{B-}R_f \qquad (20)$$

where $V_{os-}$ is the input unity gain buffer offset voltage and $I_{B-}$ is the inverting input bias current. The error due to $V_{os-}$ scales with the closed loop DC gain ($A_{VCL}$) but $I_{B-}$ adds a gain independent error. Generally, the $I_{B-}$ error dominates for low $A_{VCL}$ whereas the $V_{os-}$ error dominates for high $A_{VCL}$. A typical four-transistor CFA input stage buffer circuit is shown in Figure 5(a). Summing the voltage drops from the base of Q1 to the emitter of Q3 gives,

$$V_{os} = v_{in+} - v_{in-} = V_{BE3} - V_{BE1} \qquad (21)$$

Neglecting the finite base currents Eq. (21) can be re-written as,

$$V_{os} = V_T \ln\left(\frac{I_3/I_{Sn}}{I_1/I_{Sp}}\right) = V_T \ln\left(\frac{I_{Sp}}{I_{Sn}}\right) \qquad (22)$$

where $I_1 = I_3 = I_{b1}$ under quiescent conditions. As a result, the input offset voltage depends on how closely the base emitter voltages of the pnp transistors match those of the npn transistors. An alternative four-transistor unity gain buffer circuit with improved offset voltage is shown in Figure 6. This circuit uses diode-connected transistors of the correct type to bias the complementary pair output stage such that like transistors are matched with like transistors. One major drawback of this circuit however, is the relatively low input impedance [9].

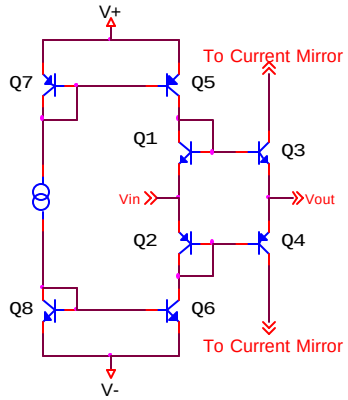



**Figure 6: Low offset voltage input buffer**

A number of factors are responsible for the inverting input bias current (refer to Figure 4); (1) mismatch between $I_{B11}$ and $I_{B12}$, (2) current mirror errors, (3) differences between $\alpha_3$ and $\alpha_4$. Higher gain current mirrors such as the Wilson mirror can be used to significantly reduce $I_{B-}$. However, these current mirrors exhibit local resonance, which decreases the overall amplifier bandwidth.

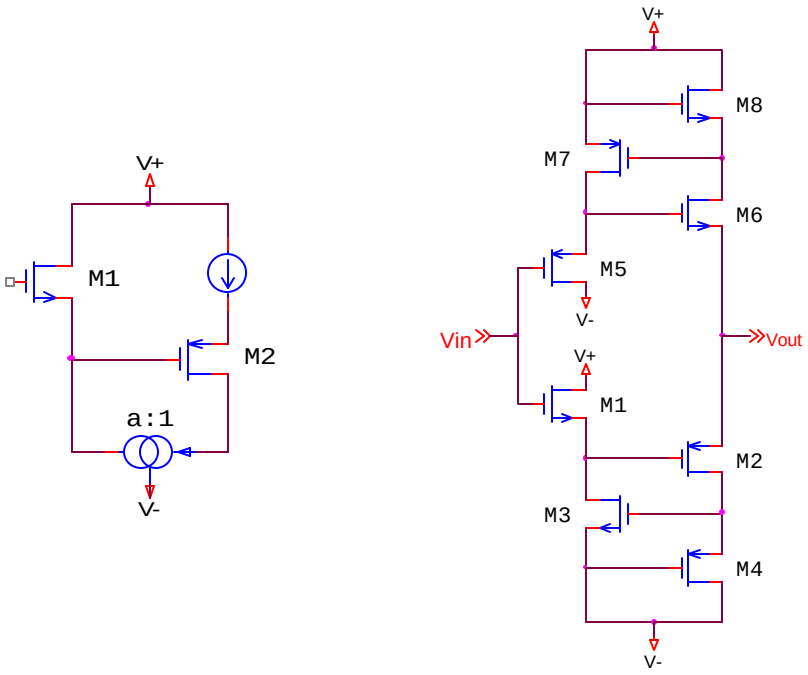
## VI. CMOS CFAs

The majority of modern commercial CFAs are based on bipolar transistor circuits. However, a novel CMOS realization of a CFA was recently reported in [10]. One of the

major disadvantages of MOS transistors compared to BJTs, is the reduced transconductance. The circuit in Figure 7(a) can be viewed as a compound MOS transistor with high transconductance . $G_{M1}$ is the compound gate and $S_{M2}$ is the compound source. The first order transconductance from $G_{M1}$ to $S_{M2}$ ignoring the output conductance of M1,2 is given by,

$$g_m = \frac{g_{m1} g_{m2}}{g_{m1} - \alpha g_{m2}}$$

where $\alpha = \frac{g_{m1}}{g_{m2}}$ is the current transfer ratio of the current mirror.




(a) (b)

**Figure 7: (a) Compound transistor; (b) CMOS voltage follower**

Figure 7(b) shows the CMOS implementation of a voltage follower circuit presented in [10]. M1-M4/M5-M8 forms a p-type/n-type compound transistor. Given that the gate of M3/M4 is tied to the source of M4/M3 the gate-source voltage of M3 and M4 are forced to be equal. Assuming all like transistors are the same size, the gate

source voltage of M1 and M2 are almost equal since $I_{d4}$ equals $I_{d2}$ and $I_{d3}$ equals $I_{d1}$. Therefore, the output voltage is forced to be equal to the input voltage. This voltage follower was subsequently used in the design of the CMOS CFA shown in Figure 8 [10, 11]. This circuit is very similar in principle to the amplifier in Figure 4. The input and output stage buffers are based on the architecture of Figure 7(b). M9-M12 and M13-M16 are regulated cascode current mirrors. A compensation capacitor is placed between the high impedance node (Z) and ground for stability. The circuit was fabricated using 0.6um digital CMOS technology.

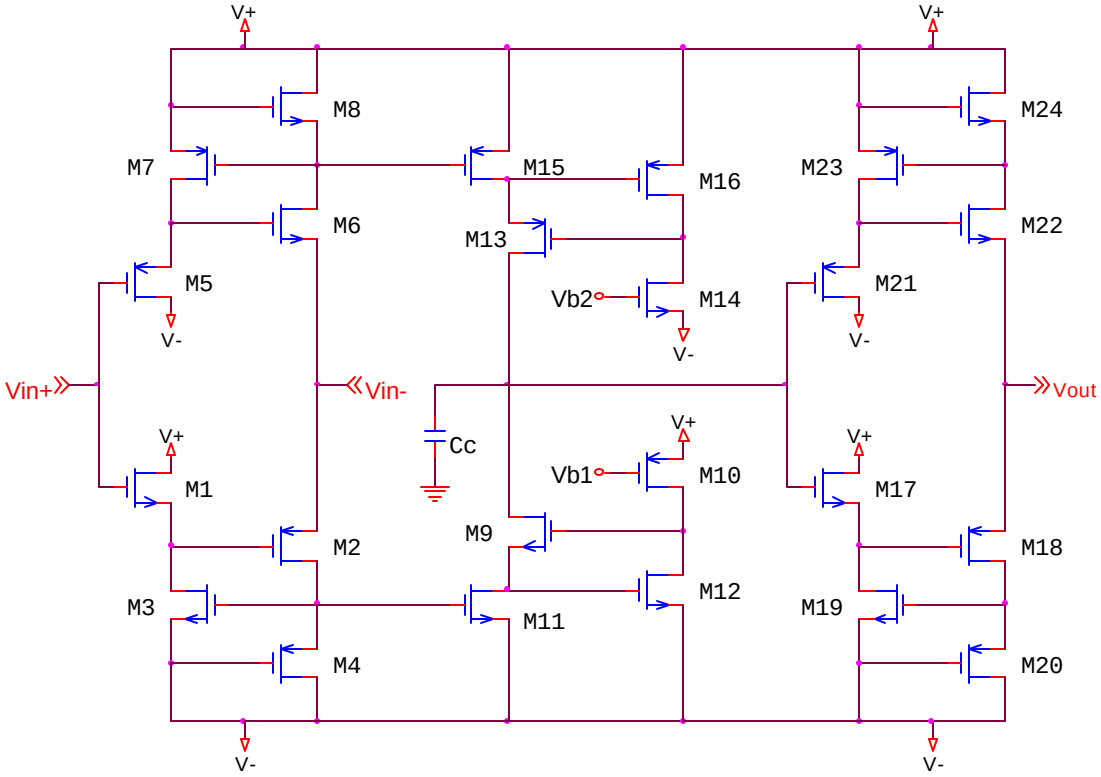



**Figure 8: CMOS current feedback amplifier**

## VII. CONCLUSION

The CFA is not a replacement for the VFA nor is it an "engineering curiosity". Until a specific application is considered, the CFA is not inherently better or worse than the VFA. The most significant advantage of the CFA over conventional amplifiers is the

high slew rate performance and wide bandwidth. It is interesting to note that some VFAs touted as high speed amplifiers are essentially a CFA with a voltage gain block connected between the inverting input terminal and the output of the input stage buffer [12].

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