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A current mode feedback operational amplifier design using complementary bipolar technology

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A CURRENT MODE FEEDBACK OPERATIONAL AMPLIFIER DESIGN USING COMPLEMENTARY BIPOLAR TECHNOLOGY

by

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Professor in Charge

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I dedicate this thesis to my wife, Doreen. Her love, support and patience during the past three years have afforded me the opportunity to obtain what would otherwise be unobtainable.

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ABSTRACT

A wideband current mode feedback operational amplifier has been designed using a complimentary bipolar integrated circuit technology. A novel input buffer has been used in the design that obtains an input dynamic range of +/- 3V, has reduced output impedance for superior speed performance, and has a low offset voltage. The op amp has a 3dB gain bandwidth of nearly 350Mhz and a slew rate of about 1500V/us. The nominal input offset voltage is about -1mv and output voltage swing is +/- 3V driving into a 50 ohm load.

CHAPTER 1

General Introduction

1.1 Introduction

An operational amplifier (op amp) is a device whose output is the multiplication of its internal gain times the differential voltage applied to its inputs. Its area of initial application was analog computation and instrumentation. It wasn't until the mid 1960's and the invention of the integrated circuit (IC) that the op amp's full versatility was realized. Until that point, op amp's were composed of discrete components, resistors and transistors, and were fairly expensive (in the tens of dollars range). The IC enabled manufacturers of op amps to produce a higher performance part, with superior quality, at an extremely low price (about a dime a piece). Today op amps can be found in circuits whose applications range from simple electronic timing circuits to sophisticated audio equipment.

Traditionally, an ideal op amp has been classified as a differential input, single ended output amplifier with infinite gain, infinite input resistance, and zero output resistance. Since the invention of the first IC, manufacturers of op amps have strived to approximate these

characteristics of an ideal op amp. They are always searching for ways to increase the input impedance, lower the output impedance, offset currents, offset voltages and noise. At the same time, they have been striving to push the bandwidths of the devices higher, and lower the settling-time characteristics. These particular characteristics are especially important in applications such as high speed digital to analog conversion (DAC) buffers, sample and hold (S/H) circuits, automatic test equipment (ATE) pin drivers, and video and IF drivers.

Being a voltage processing device, the traditional op amp has been subject to the speed limitations that arise primarily from stray capacitance of nodes in signal paths and the cutoff frequencies of transistors. In particular, because of stray capacitance at the inputs and outputs of high gain stages, voltage feedback (VFB) op amps suffer from the Miller effect which primarily sets the op amp's 3-dB point.

Current manipulation has always been known to be faster than voltage manipulation. Effects of stray inductance are much lower than stray capacitance and bipolar junction transistors (BJTs) can switch currents faster than voltages. For these reasons, a new mode of op amp design in IC form

has come to light in the past 5 to 10 years. It is know as current feedback (CFB) technology.

For current mode operation, all node voltages remain approximately the same, thus reducing the effect of stray capacitance. However, since the output signal must be in the form of a voltage, some type of current to voltage transfer must take place in the circuit. This is achieved mainly by using circuit stages that do not suffer from the Miller effect, such as common-collector and cascode configurations. To ensure symmetric operation, the PNP and NPN transistors must have comparable characteristics. Traditionally, PNP's have had poor AC characteristics, but with the emergence of complimentary bipolar integrated technology (CBIC), this handicap for the PNP has been nearly eliminated.

To better appreciate the differences between voltage and current feedback op amps, the two are compared side by side below.

1.2 Voltage Feedback Design

1.2.1 Closed Loop Frequency Response

A conceptional diagram of an ideal VFB op amp is shown in Figure 1.

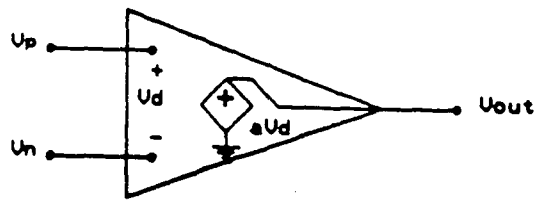


Figure 1
Ideal Voltage Feedback Op Amp

As mentioned previously, the output of the device is expressed as:

$$Vout = A(jf) \cdot Vd \qquad (1.1)$$

where A(jf), a complex function of frequency, is the open loop gain of the op amp, and Vd is the differential input voltage. If a resistive feedback connection is made as shown in Figure 2

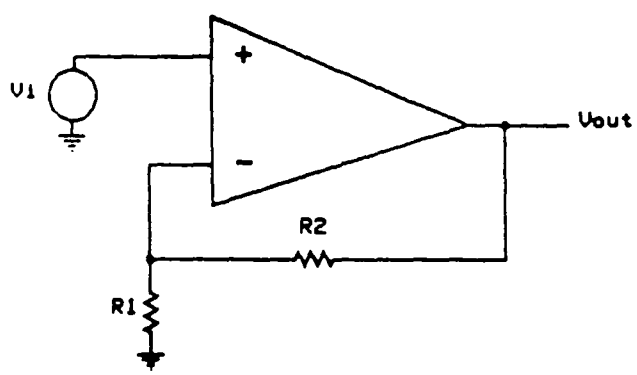


Figure 2
Voltage Feedback Op Amp in Non-Inverting Mode

the differential input voltage, Vd, can now be expressed as

$$Vd = Vin - \left[\frac{R1}{R1 + R2}\right] \cdot Vout \qquad (1.2)$$

If Vd from Eq. (1.2) is substituted for Vd in Eq. (1.1), the following results,

$$Vout = A(jf) \cdot \left[Vin - \left[\frac{R1}{R1 + R2}\right] \cdot Vout\right] \qquad (1.3)$$

After some algebra, an expression for the gain (Vout/Vin) can be realized:

$$\frac{Vout}{Vin} = \frac{1 + \frac{R2}{R1}}{1 + \frac{1}{T(jf)}} \qquad (1.4)$$

where T(jf), the loop gain of the circuit, can be expressed as

$$T(jf) = \frac{A(jf)}{1 + \frac{R2}{R1}} \qquad (1.5)$$

The loop gain originates from the fact that if the feedback loop is broken as shown in Figure 3, and a test signal, Vx, inserted, the gain of the circuit will be

$$Vout = Vx \cdot A(jf) \cdot \frac{R1}{R1 + R2} \tag{1.6}$$

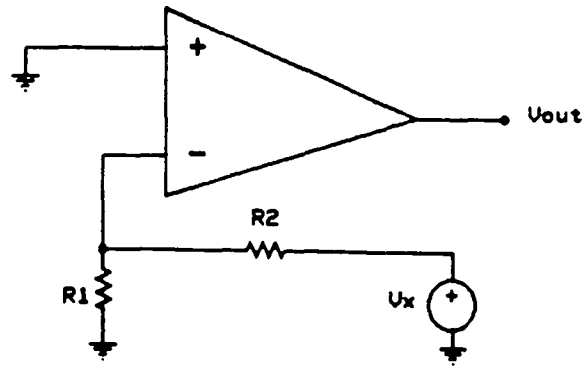


Figure 3
Loop Gain Calculation Circuit

Assuming the open loop gain has a single pole response, A(jf) can be expressed as

$$A(jf) = \frac{Ao}{1 + j\left[\frac{f}{f3dB}\right]} \tag{1.7}$$

where Ao is the dc open loop gain and f3dB is the frequency at which the gain begins to roll off.

Substituting the expression for A(jf) in Eq. (1.7) into Eq. (1.5), T(jf) now becomes

$$T(jf) = \frac{Ao}{\left[1 + j\left[\frac{f}{f3dB}\right] \cdot \left[1 + \frac{R2}{R1}\right]\right]} \qquad (1.8)$$

Now, substituting the expression for the loop gain in Eq. (1.8) into the expression for the overall gain in Eq. (1.4), doing more algebra, and assuming Ao is much greater than (1+R2/R1), a final expression for the gain can now be found

$$\frac{Vout}{Vin} = \frac{1 + \frac{R2}{R1}}{1 + \frac{j(R1 + R2)}{Ao \cdot R1} \cdot \frac{f}{f3dB}} \qquad (1.9)$$

The closed-loop frequency of this circuit can now be extracted from Eq. (1.9)

$$fcl = Ao \cdot \frac{f3dB}{1 + \frac{R2}{R1}} \qquad (1.10)$$

Eq. (1.10) shows the familiar trade-off that designers face when designing with VFB op amps. As the closed-loop gain, (1

+ R2/R1), increases, the frequency response of the device decreases. A graphical representation of Eq. (1.10) is shown in Figure 4.

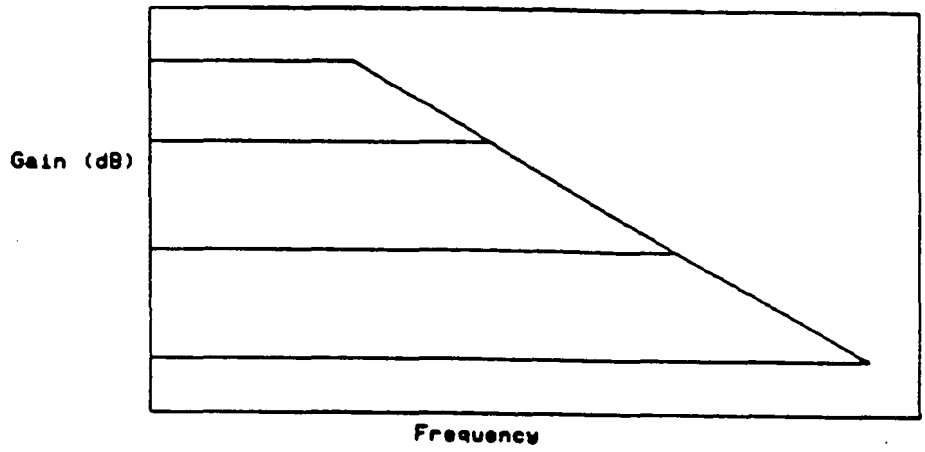


Figure 4
Frequency Response of Voltage Feedback Op Amp

From Figure 4 it is easy to see that as the gain (1 + R2/R1) is increased, the frequency response of the circuit begins to suffer at high frequencies.

1.2.2 Slew Rate

To obtain a better measure of an op amp's dynamic performance, the transient response needs to be characterized. This can be done by examining a phenomena known as slew rate limiting. If an op amp has a response in

the form of Eq. (1.7), it's output can be modeled as an RC network if the device is operated in a unity gain configuration. If a small input voltage, delta Vi, is applied, the output, Vo(t), will have the following response

$$Vo(t) = \delta Vin \cdot \left[1 - \exp\left[\frac{-t}{T}\right]\right] \qquad (1.11a)$$

with T being expressed as

$$T = \frac{1}{2 \cdot \pi \cdot ft} \qquad (1.11b)$$

where ft is the unity gain frequency of the op amp. The rate of change of the output will be greatest at the beginning of transition, at which time it will equal 1/T (this can be seen by taking the derivative of Eq. (1.11)). As the size of the input step increases, so will the rate of change. It will continue to increase until the rate begins to saturate. This is known as the slew rate limiting.

For a better illustration, refer to Figure 5 along with the following explanation.

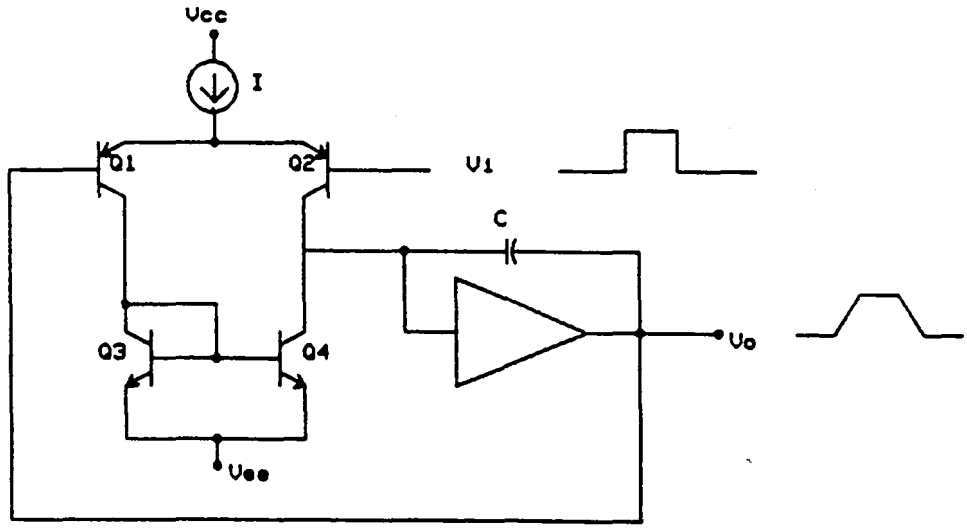


Figure 5
Simplified slew rate model of VFB op amp

This diagram is typical of VFB op amps. The input stage, a transconductance stage, consists of a differential pair, Q1 and Q2, along with a current mirror, Q3 and Q4. The remaining stages are lumped together and include an integrator block along with a compensation capacitor C. Slew rate limiting occurs when the input stage saturates and all the current available is used to charge or discharge C. If this current is called I, then the slew rate of a VFB op amp will be

$$SR = \frac{I}{C} \tag{1.12}$$

As long as the input voltage step is below the product of SR times T, the circuit will exhibit an exponential response. Otherwise the circuit will slew at a rate consistent with Eq. (1.12). An op amp having an input stage current of 20uA and a compensation capacitor of 10pF will have a slew rate in the single volts per microsecond and settling time in the hundreds of nanoseconds.

1.3 Current Feedback Design

1.3.1 Closed Loop Response

A conceptual diagram of an ideal current feedback op amp is shown in Figure 6.

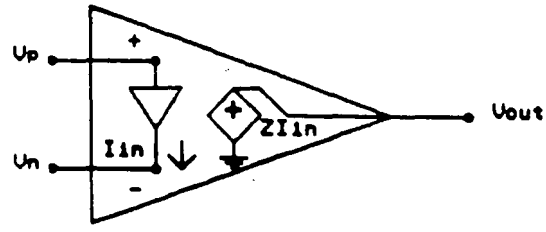


Figure 6
Ideal Current Feedback Op Amp

The VFB op amp has a high resistance seen at both input terminals and has a voltage open-loop gain. Two obvious differences of the CFB op amp topology are the low inverting

input resistance and that the gain is in ohms (transimpedance). The output of the device is expressed as

$$Vout = Z(jf) \cdot Iin \qquad (1.13)$$

Where Z(jf) is the open loop transimpedance gain of the circuit , a complex function of frequency, and Iin is the output current from the input buffer. Figure 7 shows the ideal CFB op amp surrounded by a resistive feedback similar to that shown of the VFB op amp.

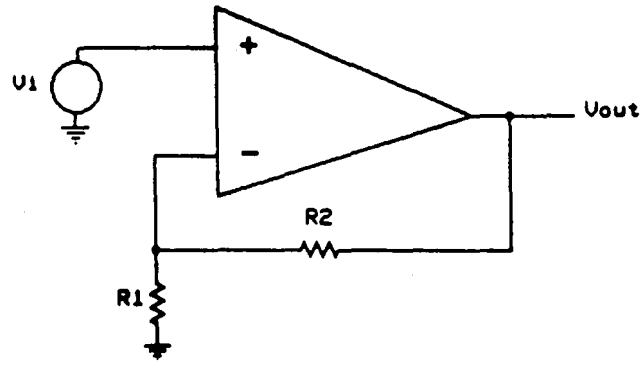


Figure 7
Current Feedback Op Amp in Non-Inverting Mode

At the node labeled Vn, an expression for Iin can be found

$$Iin = \frac{Vin}{R1} + \frac{Vin - Vout}{R2} \qquad (1.13a)$$

Placing the expression for Iin in Eq. (1.13a) into Eq. (1.13) and doing some algebra, an expression for the voltage gain, Vout/Vin, can be found.

$$\frac{Vout}{Vin} = \frac{1 + \frac{R2}{R1}}{1 + \frac{1}{T(jf)}} \tag{1.14}$$

Where the loop gain, T(jf) is expressed as

$$T(jf) = \frac{Z(jf)}{R2} \tag{1.15}$$

Once again, the loop gain, is a measure of how ideal the op amp is. The higher the loop gain, the better the op amp. Now, assuming that the open loop transimpedance gain of the op amp has a single pole response, Z(jf) can be expressed as

$$Z(jf) = \frac{Zo}{1 + \frac{jf}{f3dB}} \tag{1.16}$$

Where Zo is the dc transimpedance and f3dB is the frequency at which the gain begins to roll off. Substituting the

expression for Z(jf) in Eq (1.16) into the loop gain of Eq. (1.15), the loop gain is now expressed as:

$$T(jf) = \frac{Zo}{R2 \cdot \left[1 + j\left[\frac{f}{f3dB}\right]\right]} \tag{1.17}$$

Substitution of the loop gain expression of Eq. (1.17) into the gain expression of Eq. (1.14), doing some algebra, and assuming that Zo >> R2 the final gain can be expressed as

$$\frac{Vout}{Vin} = \frac{1 + \frac{R2}{R1}}{1 + j\left[\frac{R2}{Zo} \cdot \frac{f}{f3dB}\right]} \tag{1.18}$$

From Eq. (1.18), the expression for the closed loop gain can be acquired.

$$fcl = Zo \cdot \frac{f3dB}{R2} \tag{1.19}$$

It is obvious from Eq. (1.19) that once the closed loop frequency is set by R2, the gain of the circuit can be set by R1 without altering the frequency response. This is a major advantage that CFB has over VFB. A graphical

representation of this characteristic can be found in Figure 8.

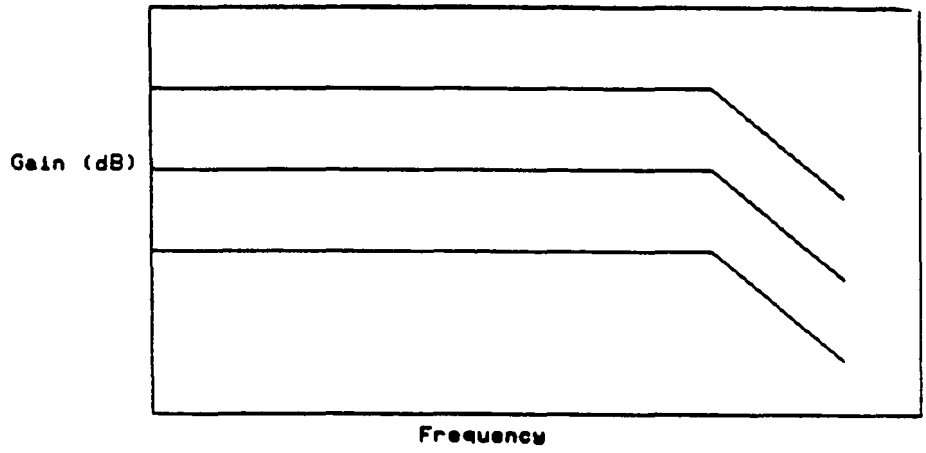


Figure 8
Frequency Response of Current Feedback Op Amp

However, later it will shown that second order effects do effect the closed loop frequency response.

1.3.2 Slew Rate

In addition to not having the closed loop frequency response dependent to gain, CFB op amps also have higher slew rates than their voltage feedback counterparts. This arises from the fact that the current available to charge the capacitor, during a delta Vin step, is proportional to the step voltage. This can be seen by rearrangement of Eq. (1.13). The equation is repeated below for convenience

$$Iin = \frac{Vin}{R1} - \frac{Vin - Vout}{R2} \tag{1.20}$$

If like terms of Vin and Vout are combined, Eq. (1.20) can be expressed as the following

$$Iin = Vin \cdot \frac{R1 + R2}{R1 \cdot R2} - \frac{Vout}{R2} \tag{1.21}$$

From Eq. (1.21), it is easy to see that the feedback signal is in the form of a current. If the slew rate is defined as the ratio of input current to the capacitance, the following analysis can be made. A step voltage delta Vin will generate an increase in current of

$$\delta Iin = \delta Vin \cdot \frac{R1 + R2}{R1 \cdot R2} \tag{1.22}$$

This will be the current available to charge the compensation capacitor Cc. The slew rate can now be defined as

$$SR = \frac{\delta Iin}{Cc} \tag{1.23}$$

$$SR = \delta Vin \cdot \frac{R1 + R2}{R1 \cdot R2 \cdot Cc} \tag{1.24}$$

With a little rearrangement of Eq. (1.24), the following definition for slew rate can be realized

$$SR = \frac{Vout}{R2 \cdot Cc} \tag{1.25}$$

It was mentioned earlier that Vout is an exponential function having a time constant of

$$T = R2 \cdot Cc \tag{1.26}$$

A CFB op amp having a capacitance similar to that of the VFB op amp mentioned above, 10pF, and a feedback resistance of 500 ohms will have a slew rate in the hundreds or even thousands of volts per microsecond and have a settling time in the single digit nanoseconds.

It is obvious from the above analysis that the slew rate for a CFB amplifier is not solely dependent on the amount of current being supplied to the input stage as it is for a VFB op amp. This absence of slew rate limiting allows for not only faster settling times, but also eliminates slew rate nonlinearities. This makes CFB op amps ideal for such applications as video amplifiers and IF/RF signal processing.

If a designer were using an op amp for an application that required a gain of say 10, needed a flat response out

to 300Mhz and a settling time of less than 10ns, it would seem logical that the designer would need a CFB op amp to fit his or her particular application.

CHAPTER 2

Input Buffer Considerations

2.1 Introduction

Before a CFB op amp design is presented, there are three topics that Chapter two will cover. These are: basic operation of a CFB opamp in block level form, the effect that the output resistance of the input buffer has on frequency response, and input offset characteristics of different input buffer designs.

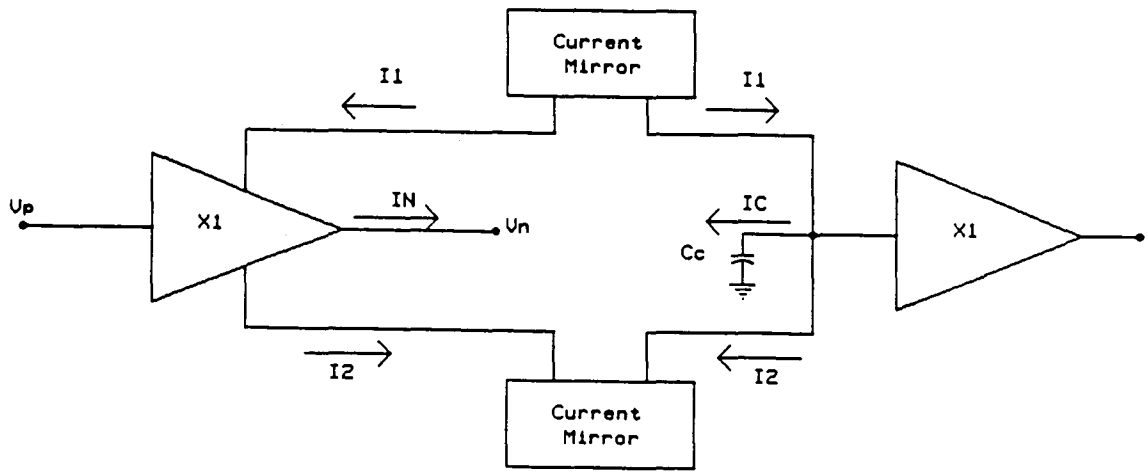


Figure 9
Block Level Schematic of CFB Op Amp

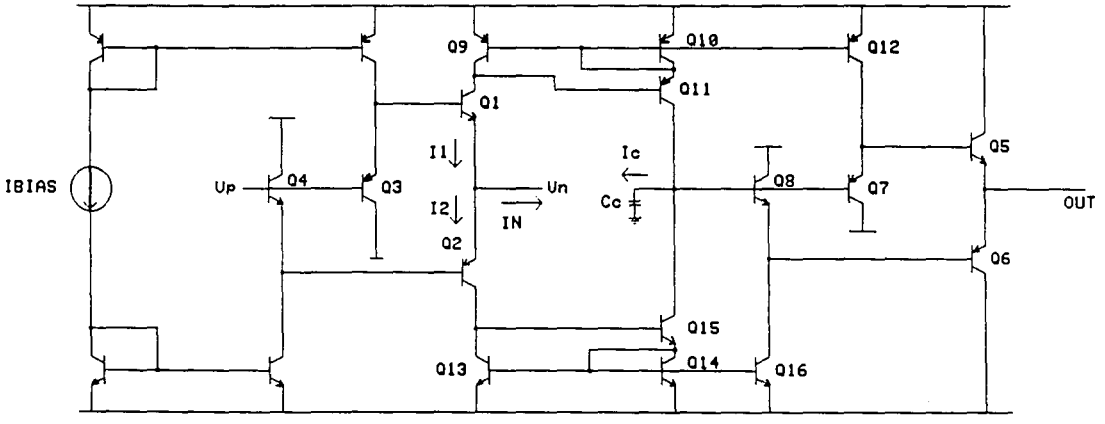


Figure 10
Simplified Circuit Schematic of CFB Op Amp

Figure 9 presents a block diagram of a CFB op amp, while Figure 10 displays a simplified circuit schematic of the op amp. Transistors Q1 through Q4 represent the input buffer with transistors Q1 and Q2 representing its low output impedance. Looking at node Vn, currents can be summed to yield I1 - I2 = In. The current mirror, Q9 through Q11, and its NPN counterpart, Q13 through Q15, mirror this current to the node CC. Node CC is commonly called the gain node. This difference current charges C and

is sent to the output via the output buffer, transistors Q5 through Q8. When the loop is closed, ie a feedback resistor from the output to node Vn and a resistor from Vn to ground, and an external signal is presented to the input creating an inbalance, the input buffer begins to sink or source current in an attempt to balance the inputs. This imbalance is conveyed to the mirrors, charging C, forcing Vout to swing positive or negative. This carries on until the imbalance is nulled through the feedback loop.

Based on the results from models presented in Figures 6 and 7, the closed loop frequency was calculated as

$$fcl = Zo \cdot \frac{f3dB}{R2} \qquad (2.1)$$

This result is based on the fact that the input buffer of the CFB op amp has zero output resistance. Of course this is not the case and the buffer does have a non-zero output resistance. A new CFB op amp model, including the output resistance of the input buffer, is shown in Figure 11.

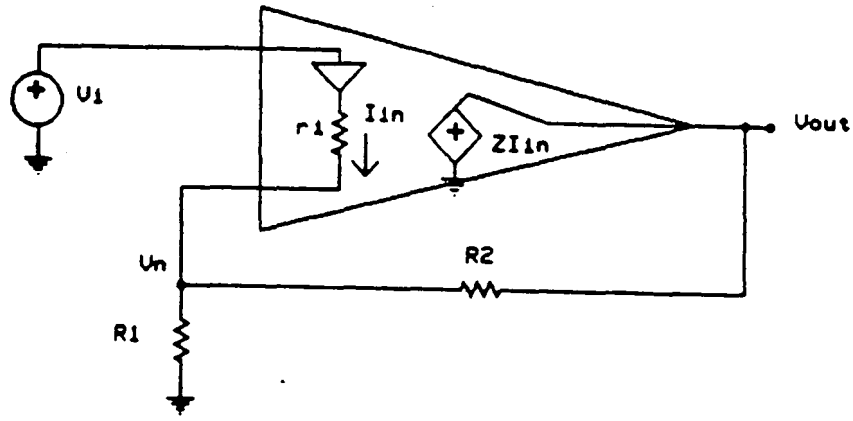


Figure 11
CFB Op Amp With Non-ideal Input Buffer

As was presented earlier, the output voltage, Vout can be expressed as

$$Vout = Z(jf) \cdot Iin \tag{2.2}$$

also from Figure 11, Iin is expressed as

$$Iin = \frac{Vn}{R1} + \frac{Vn - Vout}{R2} \tag{2.3}$$

A third equation for Vin can be written from Figure 11

$$Vn + Iin \cdot ri = Vin \tag{2.4}$$

or

$$Vn = Vin - Iin \cdot ri \tag{2.5}$$

Substitution of Eq. (2.5) into Eq. (2.3) for Vn gives the following

$$Iin = \frac{Vin - Iin \cdot ri}{R1} + \frac{Vin - Iin \cdot ri - Vout}{R2} \tag{2.6}$$

After completing some algebra on Eq. (2.6), Iin can be found.

$$Iin = \frac{Vin \cdot (R1 + R2) - R1 \cdot Vout}{R1 \cdot R2 + R2 \cdot ri + R1 \cdot ri} \tag{2.7}$$

Substitution of Eq. (2.7) into Eq. (2.1) yields

$$Vout = Zo \cdot \frac{Vin \cdot (R1 + R2) - R1 \cdot Vout}{R1 \cdot R2 + R2 \cdot ri + R1 \cdot ri} \tag{2.8}$$

After doing some algebra on Eq. (2.8), an expression for the gain, Vout/Vin can be obtained

$$\frac{Vout}{Vin} = \frac{1 + \frac{R2}{R1}}{1 + \frac{1}{T(jf)}} \tag{2.9}$$

where T(jf) is

$$T(jf) = \frac{Z(jf)}{R2 + ri \cdot \left[1 + \frac{R2}{R1}\right]} \tag{2.10}$$

Now assuming a single pole response, the transimpedance, Z(jf), can be expressed as

$$Z(jf) = \frac{Zo}{1 + j\left[\frac{f}{f3dB}\right]} \tag{2.11}$$

Substitution of Eq. (2.11) into Eq. (2.10) gives the following expression for the loop gain

$$T(jf) = \frac{Zo}{\left[1 + j\left[\frac{f}{f3dB}\right] \cdot \left[R2 + ri \cdot \left[1 + \frac{R2}{R1}\right]\right]\right]} \tag{2.12}$$

Substitution of Eq. (2.12) into Eq. (2.9), doing some algebra, and assuming the quantity

$$\frac{R2 + Ri\left[1 + \frac{R2}{R1}\right]}{Zo} \tag{2.13}$$

is small, a final expression for the voltage gain can be obtained

$$\frac{Vout}{Vin} = \frac{1 + \frac{R2}{R1}}{1 + \frac{\left[R2 + ri \cdot \left[1 + \frac{R2}{R1}\right]\right] \cdot \left[1 + \frac{jf}{f3dB}\right]}{Zo}} \qquad (2.14)$$

From Eq. (2.14) the closed loop frequency, fcl, is

$$fcl = \frac{Zo \cdot f3dB}{R2 + ri \cdot \left[1 + \frac{R2}{R1}\right]} \qquad (2.15)$$

A graphical representation of the closed loop frequency is shown in Figure 12.

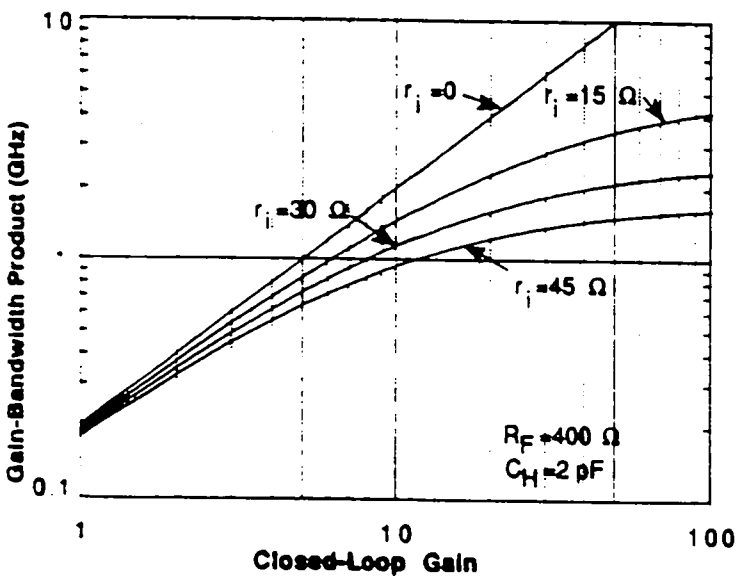


Figure 12
Closed Loop Frequency Response vs. Closed Loop Gain

From both Eq. (2.15) and Figure 12, the effect that the output resistance from the input buffer has on the frequency

response is evident. When designing an input buffer to be used for a CFB op amp, the designer must take this output resistance into account because as the closed loop gain gets higher, say to about 10, this output resistance starts to affect the circuit's AC performance. In addition to the output resistance, it is desirable that the input buffer have a low input offset voltage, Vio. Of course, the lower Vio the better.

2.2 Input Buffer Design #1

The basic input buffer is shown in Figure 13

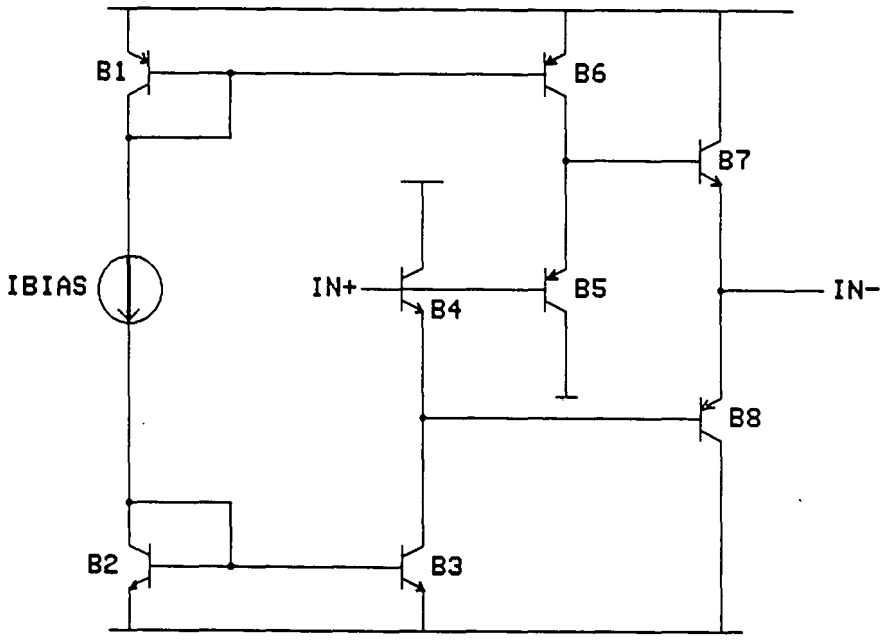


Figure 13
Input Buffer Diagram #1

The Vos calculation for the buffer in Figure 13 is as follows

$$Vos - Vbe4 + Vbe8 = 0 \tag{2.16}$$

$$Vos + Vbe5 - Vbe7 = 0 \tag{2.17}$$

noting that Eq. (2.16) and Eq. (2.17) sum to zero, the following can be obtained

$$Vos = \frac{1}{2} \cdot Vt \cdot \left[\ln\left[\frac{In}{Is4}\right] + \ln\left[\frac{Ic7}{Is7}\right] + \ln\left[\frac{Ip}{Is5}\right] + \ln\left[\frac{Ic8}{Is8}\right] \right] \tag{2.18}$$

letting Isx=Js*Ax Eq. (2.18) can be expressed as

$$Vos = \frac{1}{2} \cdot Vt \cdot \left[\ln\left[\frac{In}{Jsn \cdot A4}\right] + \ln\left[\frac{Ic7}{Jsn \cdot A7}\right] + \ln\left[\frac{Ip}{Jsp \cdot A5}\right] + \ln\left[\frac{Ic8}{Jsp \cdot A8}\right] \right] \tag{2.19}$$

combining terms in Eq. (2.19) gives the follow expression for offset voltage

$$Vos = \frac{1}{2} \cdot Vt \cdot \ln\left[\frac{In}{Ip}\right] + Vt \cdot \ln\left[\frac{jsp}{jsn}\right] + \frac{1}{2} \cdot \ln\left[\frac{A5 \cdot A8}{A4 \cdot A7}\right] \tag{2.20}$$

From the above analysis, the offset voltage for the configuration in Figure 13 is dependant upon mismatches between NPN and PNP Vbes. Clearly from Eq. (2.20) the main contributor of offset is from the second term. Based on the

technology being used for this design, the offset can vary by as much as +/- 20mv.

2.3 Input Buffer Design #2

To help reduce the offset from the circuit in Figure 13, the circuit in Figure 14 is sometimes used. This circuit places diodes in series with all emitter followers in order to combat the offset problem.

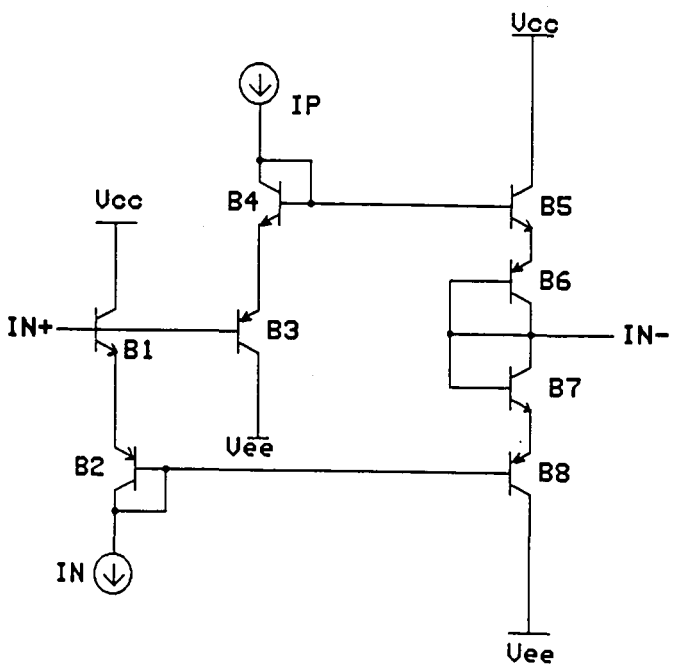


Figure 14
Input Buffer Diagram #2

Following similar analysis from the previous example, two equations can be written

$$Vos - Vbe1 - Vbe2 + Vbe8 + Vbe7 = 0 \qquad (2.21)$$

$$Vos + Vbe8 + Vbe4 - Vbe5 - Vbe6 = 0 \qquad (2.22)$$

After some algebra and collection of terms, the following offset equation is obtained

$$Vos = Vt \cdot \ln\left[\frac{In}{Ip}\right] + \frac{Vt}{2} \cdot \ln\left[\frac{A3 \cdot A4 \cdot A7 \cdot A8}{A1 \cdot A2 \cdot A5 \cdot A6}\right] \qquad (2.23)$$

Comparing Eq. (2.20) to Eq. (2.23), the former is missing the main contributor to offset voltage that exists in the latter. Therefore, by insertion of the diodes, offset is greatly reduced. One problem with the circuit of Figure 14 is that the input voltage swing has been limited by an extra Vbe on each side of the supply. If operation of the op amp is on a +/- 5V supply, this will probably not be a factor, but, operation on a single 5V supply would be difficult. Additionally, the circuit of Figure 14 has double the output resistance of the circuit in Figure 13. Assuming that the areas of the input transistors, A1 through A8, are matched, the main offset contributor is now with the mismatch in currents In and Ip.

2.4 Input Buffer Design #3

One method of attacking both the current mismatch and the input voltage swing limitation is presented in Figure 15.

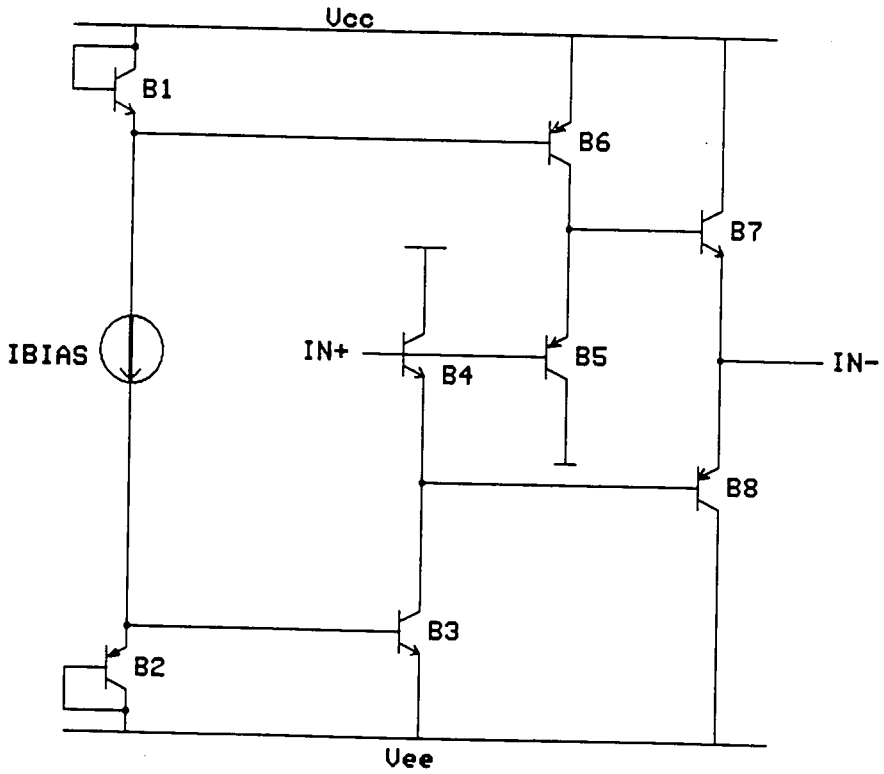


Figure 15
Input Buffer Diagram #3

Writing two equations around the buffer yields the following

$$Vos - Vbe4 + Vbe8 = 0 \tag{2.24}$$

$$Vos + Vbe5 - Vbe7 = 0 \tag{2.25}$$

Going through the analysis, collecting terms, and assuming Ic7 = Ic8, the following offset voltage equation is obtained

$$Vos = \frac{1}{2} \cdot Vt \cdot \ln\left[\frac{Ic4}{Ic5}\right] + Vt \cdot \ln\left[\frac{jsp}{jsn}\right] + \frac{1}{2} \cdot Vt \cdot \ln\left[\frac{A5 \cdot A8}{A4 \cdot A7}\right] \tag{2.26}$$

At first glance, Eq. (2.26) looks no better than Eq. (2.20). But one characteristic distinguishing the circuit in Figure 15 to the one in Figure 13, is that the currents, Ic4 and Ic5, in Figure 15, are derived in such a way so that the offset is dependant upon only area matching. The calculation of the currents Ic4 and Ic5 is as follows

$$Vbe1 = Vbe6 \tag{2.27}$$

or

$$Vt \cdot \ln\left[\frac{Ic1}{jsn \cdot A1}\right] = Vt \cdot \ln\left[\frac{Ic6}{jsp \cdot A6}\right] \tag{2.28}$$

solving Eq. (2.28) for Ic6 yields

$$Ic6 = Ibias \cdot \left[\frac{jsp \cdot A6}{jsn \cdot A1}\right] \tag{2.29}$$

Eq. (2.29) is presented with the assumption that Ibias is approximately equivalent to Ic1. Now that Ic6 is known, Ic5 is known assuming that the base current into B7 is negligible.

$$Ic5 = Ibias \cdot \left[\frac{jsp \cdot A6}{jsn \cdot A1}\right] \tag{2.30}$$

A similar analysis can be done to solve for Ic4 yielding

$$Ic4 = Ibias \cdot \left[\frac{jsn \cdot A3}{jsp \cdot A2}\right] \tag{2.31}$$

Placing the expressions for Ic5 and Ic4 from Eqs. (2.30 and 2.31) into the expression for offset voltage of Eq. (2.26) yields the following result

$$Vos = \frac{1}{2} \cdot Vt \cdot \ln\left[\frac{A1 \cdot A3 \cdot A5 \cdot A8}{A2 \cdot A4 \cdot A6 \cdot A7}\right] \tag{2.32}$$

Clearly from Eq. (2.32), the offset can be set to zero by matching areas A1 through A8. The main consequence of this design is that higher currents must be run through the input stage to ensure that proper operation occurs for all process variations.

2.5 Input Buffer Design #4

The previous three input buffers have shown that by matching PNP transistors against NPN transistors on a one to one basis, the offset voltage can be nulled to an acceptable level, excluding any beta or early voltage effects. The fourth and final buffer to be presented below, Figure 16, does something a little different.

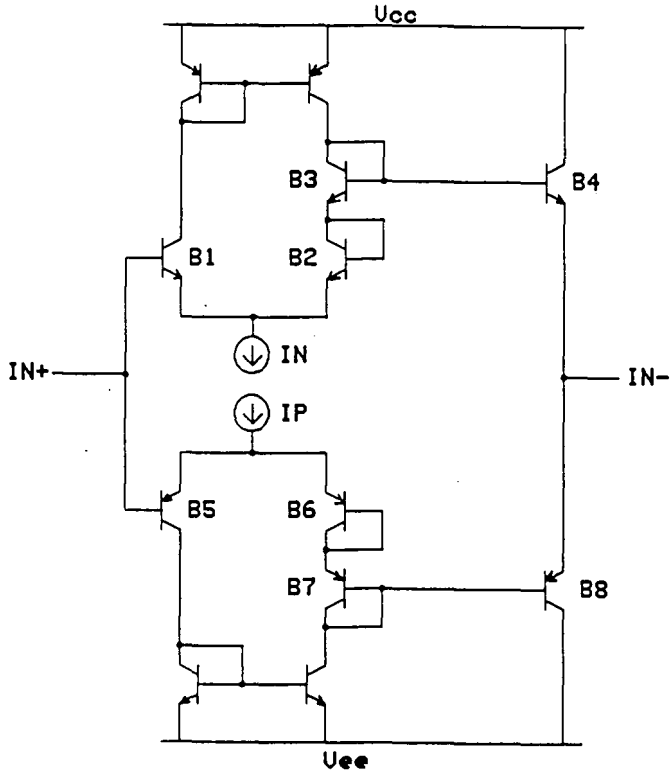


Figure 16
Input Buffer Diagram #4

The circuit of Figure 16 matches four NPN Vbes against one another while the signal is going in one direction, and does

the same for PNP's while the signal traverses through the other path. The offset voltage can be calculated as follows

$$Vos - Vbe1 + Vbe2 + Vbe3 - Vbe4 = 0 \tag{2.33}$$

$$Vos + Vbe5 - Vbe6 - Vbe7 + Vbe8 = 0 \tag{2.34}$$

Noting that Eq. (2.33) and Eq. (2.34) sum to zero and the definition of a Vbe, the above two equations can be condensed to the following one

$$Vos = \frac{1}{2} \cdot Vt \cdot \left[\ln\left[\frac{in}{2 \cdot Is1}\right] - \ln\left[\frac{In}{2 \cdot Is2}\right] - \ln\left[\frac{In}{(2 \cdot Is3)}\right] + \ln\left[\frac{Ic4}{2 \cdot Is4}\right] \right.$$

$$\left. - \ln\left[\frac{Ip}{2 \cdot Is5}\right] + \ln\left[\frac{Ip}{2 \cdot Is6}\right] + \ln\left[\frac{Ip}{2 \cdot Is7}\right] - \ln\left[\frac{Ic8}{2 \cdot Is8}\right] \right] \tag{2.35}$$

making the following substitution

$$Isx = Jsx \cdot Ax \tag{2.36}$$

and combining terms yields the following offset term

$$Vos = \frac{1}{2} \cdot Vt \cdot \ln\left[\frac{Ic4 \cdot Ip \cdot A2 \cdot A3 \cdot A5 \cdot A8}{Ic8 \cdot In \cdot A1 \cdot A4 \cdot A6 \cdot A7}\right] \tag{2.37}$$

With Ic4=Ic8 and designing the op amp such that all transistor areas involved, A1 through A8, are equal, and In=Ip, the offset voltage can be set to zero.

Looking back at the previous four circuits, with the exception of the first one, Figure 13, each has it's own unique tradeoffs. However, since the middle two, Figure 14 and Figure 15, are the most commonly used, the final one, Figure 16, will be the topology used in designing the input buffer for the CFB op amp.

CHAPTER 3

Circuit Design

3.1 Introduction

Chapter two described the operation of a CFB op amp and touched on several architectures for an input buffer design used in a CFB op amp. This chapter presents a CFB op amp design and covers the dc and ac analysis of the amplifier.

The op amp design is shown in Figure 17. Marked out are four sections. Section one is the bias circuitry, section two, the input buffer, section three, the transimpedance gain section, and section four, the output buffer.

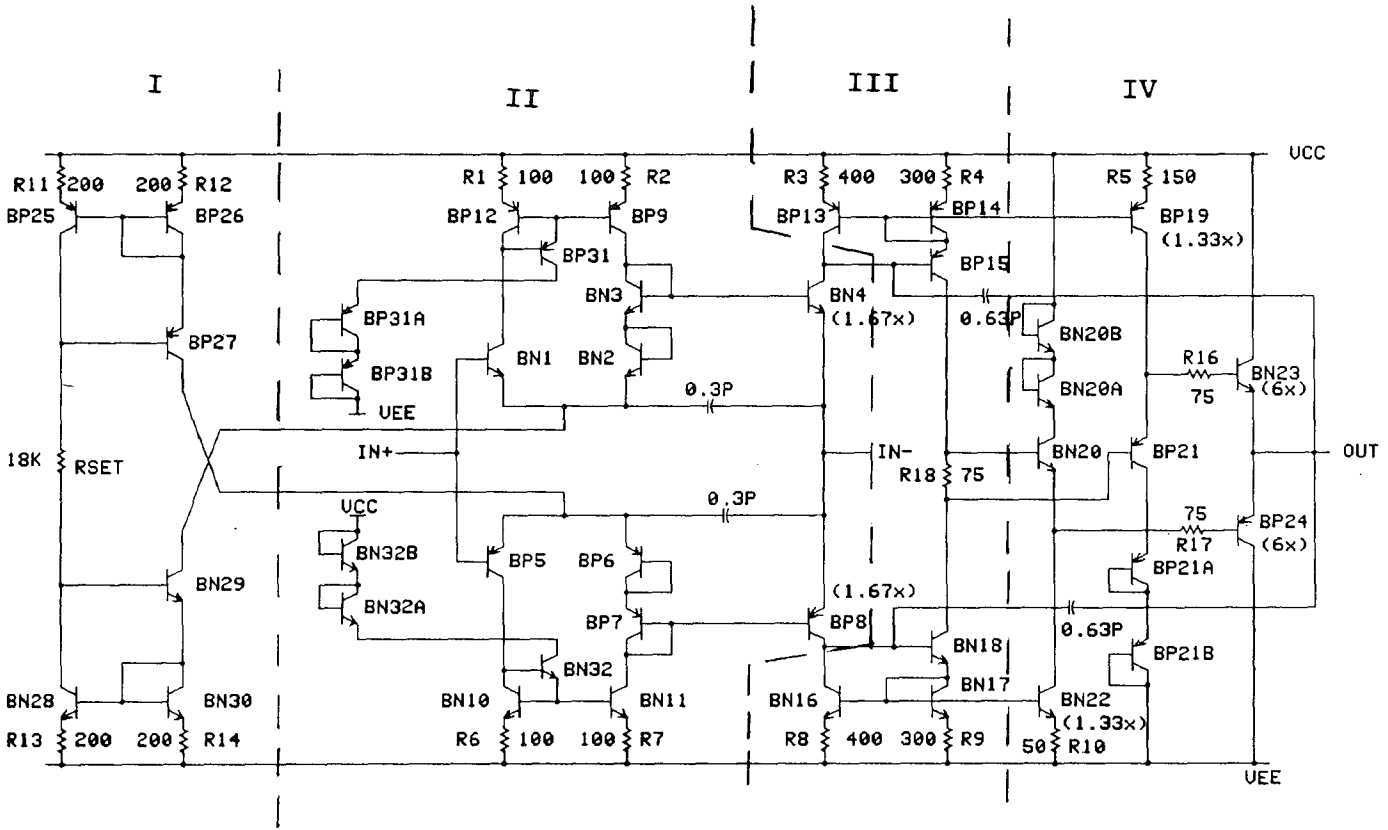


Figure 17
CFB Op Amp Design

3.2 DC ANALYSIS

3.2.1 BIAS CIRCUITRY

During the process of arriving at a bias stage, there are several questions that were raised. These were:

1) How stable must the current be with process variations?
2) How should the current vary over temperature?
3) How high must the output resistance be?
4) What are the power restraints of the circuit?
5) How stable must the current be with power supply variations?

In trying to answer these questions, there were several types of bias stages that were considered. The best answer for questions 1, 2 and 5 was a current derived from a bandgap reference circuit. The bandgap reference would generate a very stable current over both temperature and power supply variations. However, the bandgap reference does generate more power dissipation, and, for this reason, this type of circuitry was not used.

After eliminating the bandgap reference circuitry, the choices narrowed down to some type of basic current mirror with a beta helper, Figure 18, or a modified Wilson current mirror, Figure 19.

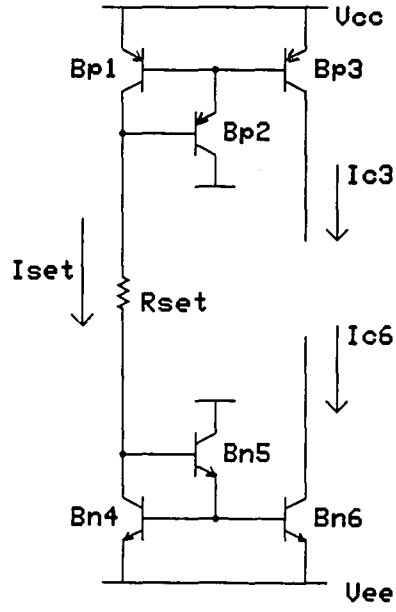


Figure 18
Current Mirror with Beta Helper

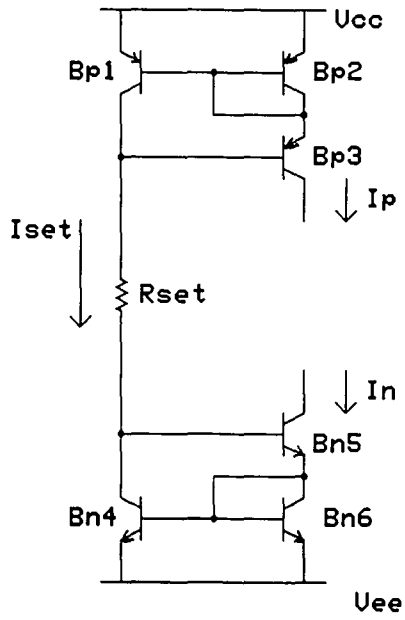


Figure 19
Modified Wilson Current Mirror

Looking at Figure 18, the goal is to calculate the currents, Ic3 and Ic6. Both depend upon Iset which is calculated as follows:

$$Iset = \frac{Vcc - Vee - Vbe1 - Vbe2 - Vbe4 - Vbe5}{Rset} \qquad (3.1)$$

Knowing Iset, currents Ic3 and Ic6 can now be calculated. The current in the emitter of transistor Q2 is

$$Ie2 = Ib1 + Ib3 \qquad (3.2)$$

Noting that Ib = Ic/B,

$$Ie2 = \frac{Ic1}{B1} + \frac{Ic3}{B3} = \frac{Ic3 \cdot 2}{B} \qquad (3.3)$$

Eqn. (3.3) is arrived at assuming the NPN betas of Q1 and Q3 are equal and noting that Ic1 = Ic3 since their Vbe's are equivalent. With Ie2 known, Ib2 can now be calculated.

$$Ib2 = \frac{Ie2}{B + 1} = \frac{Ic3 \cdot 2}{B \cdot (B + 1)} \qquad (3.4)$$

Now, an equation equating Iset to Ic1 and Ib2 can be written

$$Iset = Ib2 + Ic1 \qquad (3.5)$$

$$Iset = \left[Ic3 \cdot \frac{2}{B \cdot (B + 1)} + Ic3 \right] \tag{3.6}$$

After completing some algebra, Ic3(Iset) can be found

$$Ic3 = Iset \cdot \frac{Bn^2 + Bn}{Bn^2 + Bn + 2} \tag{3.7}$$

where Bn is the NPN beta.

The equation for the current Ic6 is identical to Eqn. (3.7) except that Bn is switched with Bp, the PNP beta. For comparison, to the Wilson mirror later on, a NPN beta of 100 and a PNP beta of 40, currents Ic3 and Ic6 are as follows:

$$Ic6 = 0.9998 * Iset \tag{3.8}$$

$$Ic3 = 0.998 * Iset \tag{3.9}$$

To calculate the output resistance of the mirror, the small signal hybrid pi model of transistor Q3 is shown in Figure 20.

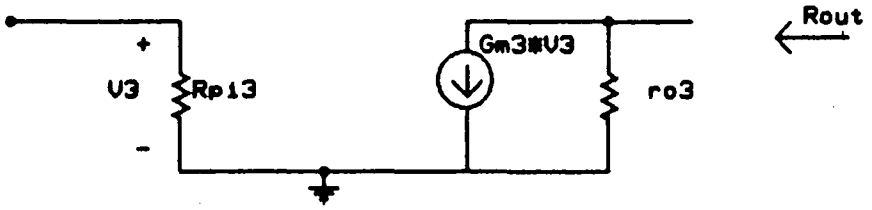


Figure 20
Small Signal Hybrid Pi Model of Q3

It is obvious that from Figure 20, the output resistance of the mirror is ro.

Another important characteristic of the mirror is the percentage change in current with change in a power supply. If vcc changes by 10%, how does Iset change? This can be found by replacing Vcc in Eqn. (3.1) with 1.1*Vcc. The result is a 7% change in the Iset current.

Looking at Figure 19, the currents In and Ip are found in a similar way as Ic3 and Ic6 in the simple mirror. These currents are:

$$In = Iset \cdot \frac{Bn^2 + 2 \cdot Bn}{Bn^2 + 2 \cdot Bn + 2} \qquad (3.10)$$

$$Ip = Iset \cdot \frac{Bp^2 + 2 \cdot Bp}{Bp^2 + 2 \cdot Bp + 2} \qquad (3.11)$$

The equations for In and Ip are very similar to those calculated for I1 and I2 in the simple mirror. Each is accurate to better than 1% of Iset. Each has a 7% change in value for a 10% change in a supply. The difference is that the output resistance of the Wilson is about a factor of B/2 greater than the simple mirror. This can be arrived at by looking at the small signal model of the Wilson in Figure 21.

Figure 21a shows the full model. Figure 21b shows the simplified model noting that the resistance 1/gm2 is much smaller than rp1. Figure 21c shows the final model used to calculate the output resistance.

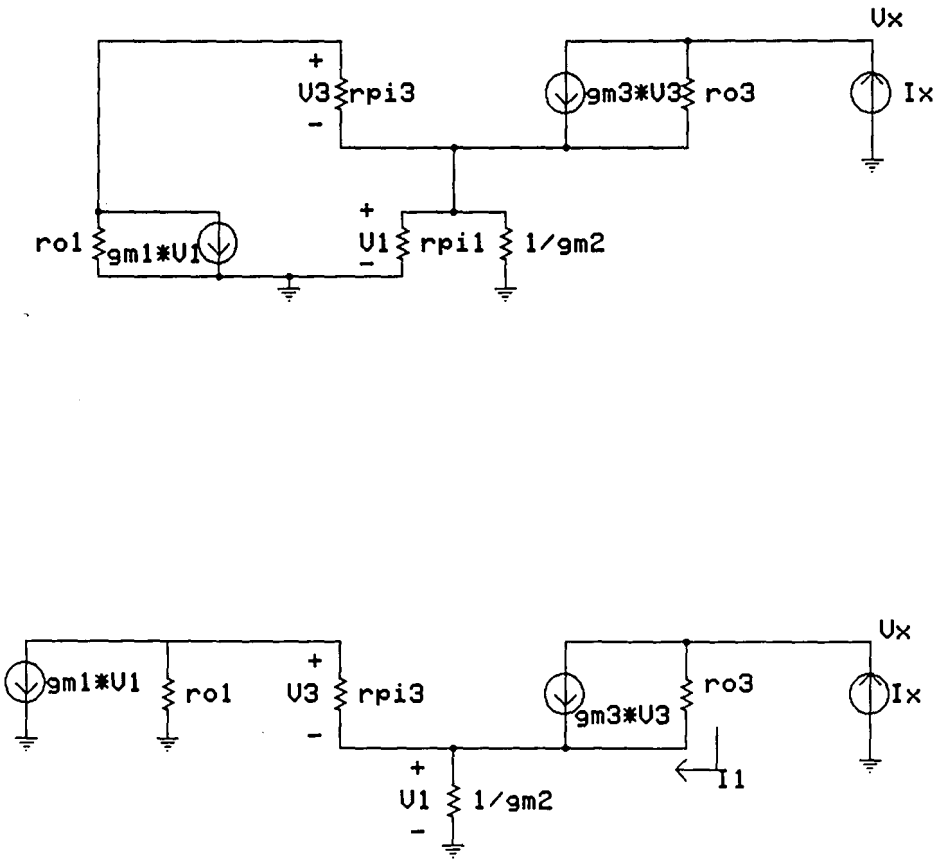


Figure 21
Small Signal Model of Wilson Source

From Figure 21c, two independent equations can be written:

$$Ix = Va \cdot gm2 + \frac{Va - Vb}{rp3} \tag{3.12}$$

$$0 = \frac{Vb - Va}{rp3} + \frac{Vb}{ro1} + gm1 \cdot Va \tag{3.13}$$

rearrangement of Eqn. (3.12) and (3.13) yields

$$Va \cdot (rp3 \cdot gm2 + 1) - Vb = rp3 \cdot Ix \tag{3.14}$$

$$Va \cdot (gm1 \cdot ro1 \cdot rp3 - ro1) + Vb \cdot (ro1 + rp3) = 0 \tag{3.15}$$

Eqn. (3.14) and Eqn. (3.15) can be solved for Va and Vb. Once Va and Vb are known, Figure 21b can be used to find the final output resistance. From Figure 21b, the test voltage measured, Vx, is

$$Vx = Va + I1 \cdot ro3 \tag{3.17}$$

where

$$I1 = Ix - gm3 \cdot (Vb - Va) \tag{3.18}$$

making all the proper substitutions in Eqn. (3.17) for Va, Vb, and I1, the output resistance, Rout, is found to be

$$Rout = \frac{ro3 \cdot gm3 \cdot gm1 \cdot rp3 \cdot ro1 + ro3 \cdot gm3 \cdot rp3}{gm2 \cdot ro1 + gm2 \cdot rp3 + gm1 \cdot ro1 + 1} \qquad (3.19)$$

where

ro - output resistance of an individual transistor = Va/Ic

gm - transconductance of an individual transistor = Ic/vt

rp - the resistance Rpi of an individual transistor = B*vt/Ic

If it is assumed that all of the Ic's are equal, Eqn. (3.19) reduces to

$$Rout = \frac{\left[gm^2 \cdot rp \cdot ro + gm \cdot rp\right] \cdot ro}{gm \cdot (2 \cdot ro + ro)} \qquad (3.20)$$

some further simplification of Eqn. (3.20) yields the familiar result

$$Rout = \frac{B \cdot ro}{2} \qquad (3.21)$$

With everything else being equal, the main difference between the two mirrors, is that the Wilson has a much larger output resistance than the basic mirror. It is for this reason that the Wilson was chosen as a bias for the CFB amplifier. The final bias circuitry, with emitter

degeneration, is shown in Figure 22. The resistors in the emitters tend to limit the variation of current on changes of Vbe. A computer simulation of the bias circuitry is presented in Chapter four.

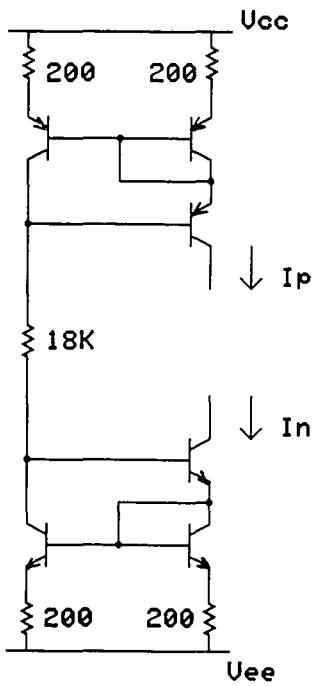


Figure 22
Final Bias Circuitry

3.2.2 INPUT BUFFER

Figure 23 breaks out the input buffer for analysis purposes.

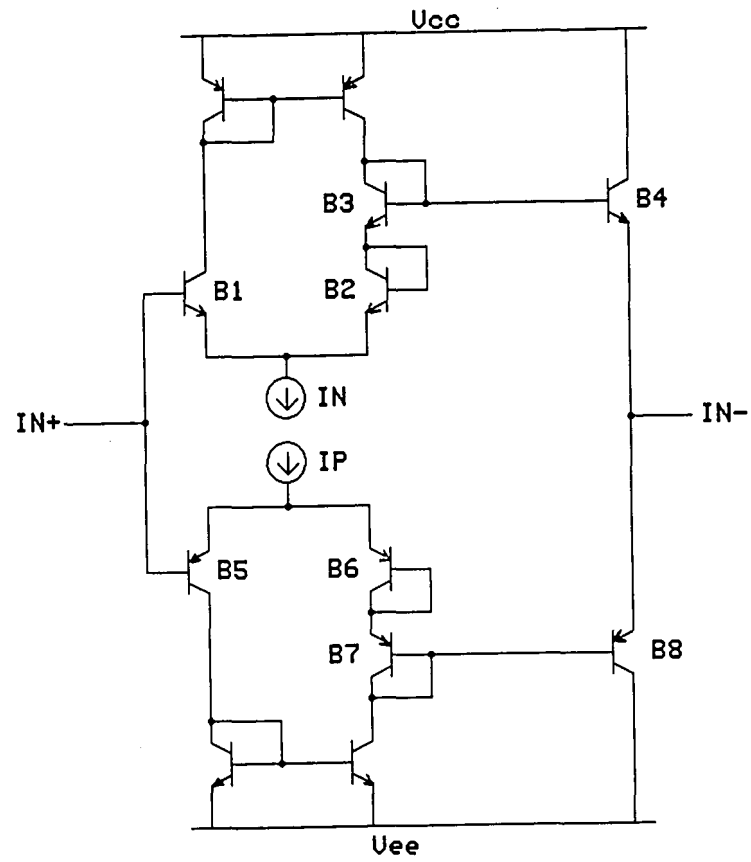


Figure 23
Input Buffer

Eqn. (2.37) from Chapter 2 established the offset voltage for this buffer as

$$Vos = \frac{1}{2} \cdot Vt \cdot \ln\left[\frac{Ic4 \cdot Ip \cdot A2 \cdot A3 \cdot A5 \cdot A8}{Ic8 \cdot In \cdot A1 \cdot A4 \cdot A6 \cdot A7}\right] \qquad (3.22)$$

The statement was made that the nominal offset voltage could be set to zero if the areas, A1 through A8, were equal, Ic4 was equal to Ic8, and In = Ip. The first two assumptions

will be fairly accurate if all transistors are located in close proximity. However, because of the fact that a PNP transistor has a lower beta than a NPN transistor, the currents In and Ip are not equal. This will have some affect on the offset voltage of the buffer. Also in the previous offset calculation, it was assumed that In and Ip split equally between both sides of the diff pairs, this too, is not entirely accurate. Due to finite beta's, the currents In and Ip will split unequally.

Following a similar analysis as in Chapter 2, Vos can be expressed as

$$Vos = \frac{1}{2} \cdot (Vbe1 - Vbe2 - Vbe3 + Vbe4 - Vbe5 + Vbe6 + Vbe7 - Vbe8) \qquad (3.23)$$

Breaking this down further yields

$$Vos = \frac{1}{2} \cdot Vt \cdot \left[\ln\left[\frac{Ic1}{Is1}\right] - \ln\left[\frac{Ic2}{Is2}\right] - \ln\left[\frac{Ic3}{Is3}\right] + \ln\left[\frac{Ic4}{Is4}\right] - \ln\left[\frac{Ic5}{Is5}\right] + \ln\left[\frac{Ic6}{Is6}\right] + \ln\left[\frac{Ic7}{Is7}\right] - \ln\left[\frac{Ic8}{Is8}\right] \right] \qquad (3.24)$$

Now, instead of assuming that currents In/2 and Ip/2 flow through both sides, the following can be said:

$$Ic9 = \frac{Ic1}{1 + \left[\frac{2}{Bp^2 + Bp}\right]} \tag{3.25}$$

Eqn. (3.25) is obtained from an analysis of the Qa/Qb mirror in a similar manner as was done in analyzing the bias circuitry. Looking back at Figure 23, the following can be written:

$$Ic3 = Ic9 - Ib3 - Ib4 \tag{3.26}$$

noting that Ib3=Ic3/Bn, Eqn. (3.26) can be solved for Ic3

$$Ic3 = \left[\frac{Ic1}{1 + \frac{2}{Bp^2 + Bp} - Ib4} \cdot \frac{Bn}{Bn + 1}\right] \tag{3.27}$$

also

$$Ie3 = Ic3 \cdot \frac{Bn + 1}{Bn} \tag{3.28}$$

$$Ic2 = Ie3 - Ib2 = Ie3 - \frac{Ic2}{Bn} \tag{3.29}$$

After solving Eqn. (3.29) for Ic2 it is seen that Ic2 = Ic3. Further analyzing Figure 23 shows:

$$In = Ie1 + Ie2 \tag{3.30}$$

$$Ie1 = \frac{Bn + 1}{Bn} \cdot Ic1 \tag{3.31}$$

$$Ie2 = \frac{Bn + 1}{Bn} \cdot Ic2 \tag{3.32}$$

$$Ie2 = \frac{Ic1}{1 + \dfrac{2}{Bp^2 + Bp}} - Ib4 \tag{3.33}$$

Ignoring Ib4 from Eqn. (3.33) and substituting Eqn. (3.33) and Eqn. (3.31) into Eqn. (3.30), Ic1(In) can now be accurately found:

$$Ic1 = \frac{In}{\dfrac{Bn + 1}{Bn} + \dfrac{Bp^2 + Bp}{Bp^2 + Bp + 2}} \tag{3.34}$$

A similar analysis can be completed on the bottom half of the buffer to find Ic5. Once Ic5 and Ic1 are found in terms of Ip and In, the rest of the currents can be found. With a Bn of 121 and Bp of 40 (nominal for the process used) Ic1, Ic2, Ic3, Ic5, Ic6, Ic7 are as follows

$$In = 0.3786 \text{ mA}$$

$$Ip = 0.3782 \text{ mA}$$

$$Ic1 = 0.1886 \text{ mA}$$

$$Ic2 = Ic3 = 0.1868 \text{ mA}$$

$$Ic5 = 0.1867 \text{ mA}$$

$$Ic6 = Ic7 = 0.18219 \text{ mA}$$

The currents Ic4 and Ic8, which can be assumed equivalent, can be found by writing the following equation

$$Vbe4 + Vbe8 = Vbe2 + Vbe3 + Vbe6 + Vbe7 - Vbe1 - Vbe5 \tag{3.35}$$

Eqn. (3.35) can be expanded to

$$\ln\left[\frac{Ic4 \cdot Ic8}{A4 \cdot A8}\right] = \ln\left[\frac{Ic2 \cdot Ic3 \cdot Ic6 \cdot Ic7 \cdot A1 \cdot A5}{Ic1 \cdot Ic5 \cdot A2 \cdot A3 \cdot A6 \cdot A7}\right] \tag{3.36}$$

When Eqn. (3.36) is solved for I=Ic4=Ic8, the result is

$$Ic4 = Ic8 = 0.30288 \text{ mA}$$

Now if the above current values are placed into Eqn. (3.22) an offset can be calculated, but it is still not entirely correct. The effect of early voltage has still not been considered. With matching areas, Eqn. (3.22) can be written as follows:

$$Vos = \frac{1}{2} \cdot Vt \cdot \ln\left[\frac{Ic1 \cdot Ic4 \cdot Ic6 \cdot Ic7}{Ic2 \cdot Ic3 \cdot Ic5 \cdot Ic8}\right] \qquad (3.37)$$

To take early voltage into account, the following substitution will be made in Eqn. (3.37)

$$Icx = Icxo \cdot \left[1 + \frac{Vcex}{Va}\right] \qquad (3.38)$$

where Icx stands for the current in question and Icxo is the current not taking into account early voltage.
Th following Vce's can be approximated from the circuit in Figure 17 with no input voltage applied:

Vce1 = 4.3 V
Vce4 = 3.6 V
Vce6 = Vce7 = 0.75 V
Vce5 = 4.3 V
Vce8 = 3.6 V
Vce2 = Vce3 = 0.75 V

Placing these Vce values into Eqn. (3.38) and placing those values into Eqn. (3.37) a more accurate offset voltage can be calculated.

Vos = -1.32 mV

Please note that this value does not take into account the area mismatch between adjacent transistors and a detailed

statistical analysis must be done to further quantify the offset voltage. Once again, with the transistors placed in close proximity of one another, the area mismatch can be made minimized. Therefore, extreme care must be taken when laying out the input buffer of the CFB op amp.

Eqns. (3.37 & 3.38) can be used to calculate the power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) of the amplifier. A 10% increase in Vcc changes the offset voltage to -2.64 mV. With this change, the PSRR can be calculated as

$$PSRR = 20 \cdot \log\left[\frac{\delta Vcc}{\delta Vio}\right] \tag{3.39}$$

The PSRR of the amplifier comes to 51.6 dB. In a similar fashion, the CMRR calculates to 50.4 dB.

The next step in analyzing the input buffer is to calculate its input and output resistance along with its input bias current. A small signal model of the buffer can be found in Figure 24

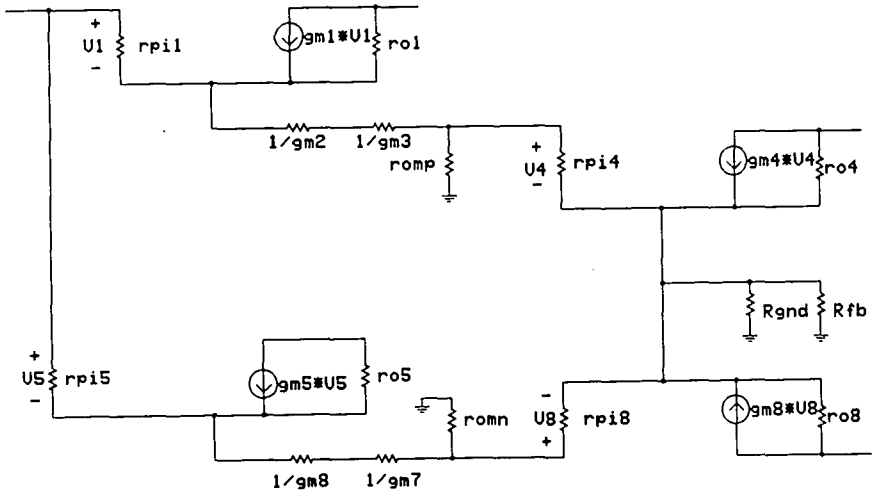


Figure 24
Small Signal Model of the Input Buffer

Only the critical areas needed to make the calculation are drawn. For simplicity in calculating the resistance, superposition will be used on the top section and similar analysis followed through on the bottom section. The top section only is shown in Figure 25.

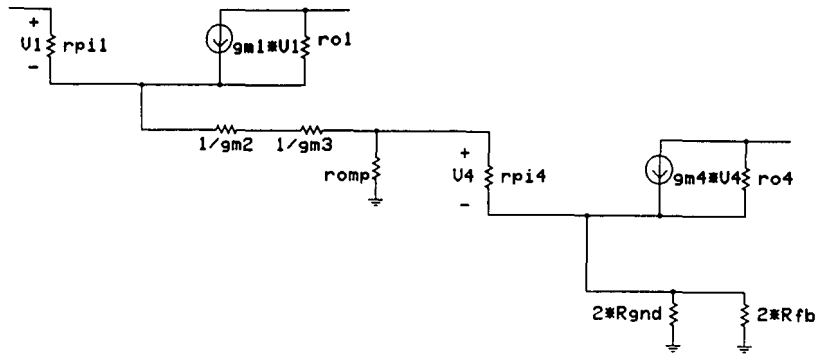


Figure 25
Small Signal Model of Top half of Buffer

By inspection, the input resistance of the top half of the input buffer is

$$Rintop = rp1 + (Bn + 1)*(2/gm + (romp//(rp4 + (Bn + 1)*(2*Rgnd//2*Rfb))) \quad (3.40a)$$

$$Rinbot = rp5 + (Bp + 1)*(2/gm + (romn//(rp8 + (Bp + 1)*(2*Rgnd//2*Rfb))) \quad (3.40b)$$

Please note that the 2/gm term models the resistance of the diodes Q2 and Q3 and since it was shown earlier that their currents were equal, the two were combined to get 2/gm. From earlier analysis the following was obtained,

$$Ic1 = 0.1886 \text{ mA}$$

$$Ic2 = Ic3 = 0.1868 \text{ mA}$$

Noting that Bn=120 for the process and Vt, the thermal voltage, is 25.4 mV at room temperature, rp1 and rp2 can be calculated

$$rpx = Bx \cdot \frac{Vt}{Icx} \tag{3.41}$$

rp1 and rp2 can be calculated as 16,161 ohms and 16,317 ohms respectfully. Also, gm, the transistor transconductance, is defined as

$$Gm = \frac{Ic}{Vt} \tag{3.42}$$

From the above, gm is 0.00735 mhos.
Placing all the correct values in their proper places in Eqn. (3.41) yields the following

$$Rintop = 4.230 \text{ Mohms}$$

A similar analysis on the bottom section of the buffer yields

$$Rinbot = 406{,}782 \text{ ohms}$$

The input resistance of the buffer will be the parallel combination of Rintop and Rinbot. When this is done, the total input resistance of the input buffer is

$$Rintotal = 370{,}964 \text{ ohms}$$

Referring back to Figure 24, the output resistance of the buffer can be calculated by superposition. By inspection, the output resistance of the top half of the output buffer is

$$Routtop = \frac{\frac{Rp1}{Bn + 1} + \frac{2}{gm} + Rp4}{Bn + 1} \tag{3.43a}$$

$$Routbot = \frac{\frac{Rp5}{Bp + 1} + \frac{2}{gm} + Rp8}{Bp + 1} \tag{3.43b}$$

Completing the analysis yields the total output resistance as

$$Routtotal = 27.43 \text{ ohms}$$

for one of the sample buffers, it is easy to see how the output resistance would double.

Figure 26 shows the circuit used to calculate the non-inverting input bias current of the op amp.

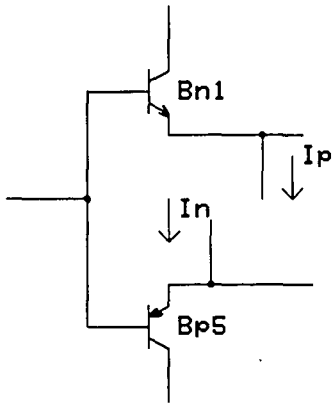


Figure 26
Circuit for Non-Inv Bias Current

Noting the directions of the currents, the following equation can be written

$$Ini = Ibn - Ibp \tag{3.44}$$

From an earlier analysis, Ibn = Ic1 = 0.1886 mA and Ibp = Ic5 = 0.1867 mA. Completing the equation yields

$$Ini = -3.09 \text{ uA}$$

the negative sign means that the current is flowing out of the node into the signal source. Although the inverting bias current can be calculated in the same manner, it is difficult to put a number on this value. As was mentioned in Chapter two, the inverting node is always getting the feedback current and because of this, the current varies.

3.2.3 Transimpedance Gain Stage

The transimpedance gain stage can be found in Figure 27.

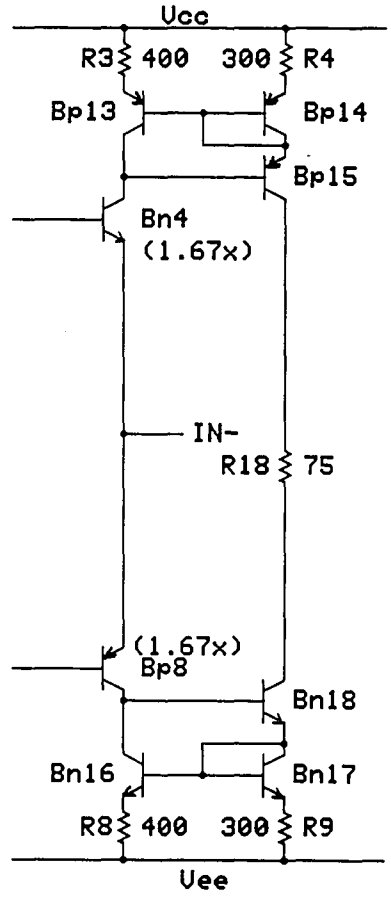


Figure 27
Transimpedance Gain Stage

Although the stage is relatively simple, two Wilson current mirrors, it is the most important section of the amplifier. Its function is to mirror the difference current at the inverting node of the amplifier to the input of the output buffer as quickly as possible. The fewer transistors the current has to travel through, the faster the amplifier.

There are only two necessary DC calculations that need to be made in order to fully understand this section, the currents in transistors Bp14 and Bn17, and the output resistance of the two mirrors. Ic14 can be found by writing the following loop equation

$$Vb13 + I13 \cdot R3 = I14 \cdot R4 + Vbe14 \tag{3.45}$$

rearranging yields

$$Vt \cdot \ln\left[\frac{I13 \cdot A14}{I14 \cdot A13}\right] + I13 \cdot R3 - I14 \cdot R4 = 0 \tag{3.46}$$

the current I14 solves out to

$$I14 = 0.384 \text{ mA}$$

similarly, the current I17 solves out to

$$I17 = 0.384 \text{ mA}$$

The output resistance of both mirrors, as was shown earlier is

$$Rout = \frac{B \cdot ro}{2} \tag{3.47}$$

The NPN output resistance is 4.2 Mohm while the PNP is 573 Kohm. These two numbers will become more important later when the DC transimpdance gain is calculated.

The equivalent resistance of the gain node is simply the parallel combination of both the NPN (Bn16, Bn17 & Bn18) and PNP (Bp13, Bp14 & Bp15) current mirrors, and the resistance looking into the bases of Bn20 and Bp21. The first two resistances are already known:

NPN mirror R = 4.2 Mohm

PNP mirror R = 573 Kohm

The resistance looking into the output stage will be approximated by the resistance seen going in any one particular direction. The output stage input resistance is calculated below.

3.2.4 Output Stage

The currents in transistors Bn23 and Bp24 can be calculated by looking at the circuit of Figure 28.

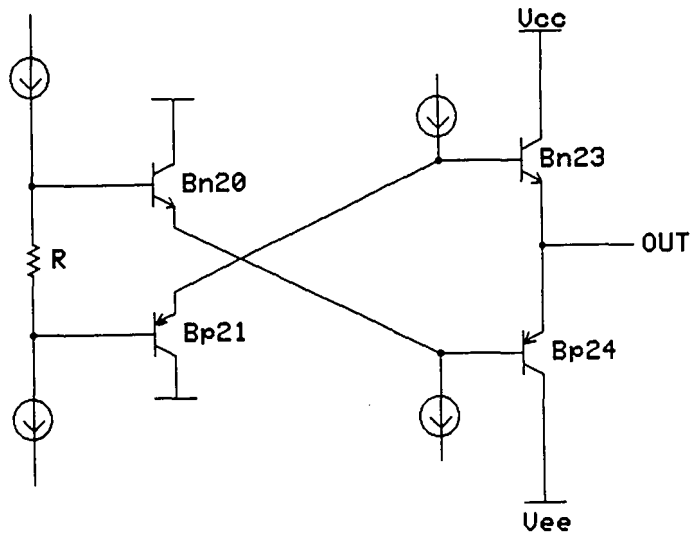


Figure 28
Output Stage

A loop equation can be written as follows

$$Vbe23 + Vbe24 = IR + Vbe21 + Vbe20 \qquad (3.48)$$

As was done previously, the currents Ic23 and Ic24 are equivalent and can be calculated from Eqn. (3.48)

$$Ic23 = Ic24 = 4.93 \text{ mA}$$

The output voltage swing for this circuit is limited by the BVCEx of the transistors. CBICV has a BVCEx of 8V minimum and as a result, the output voltage swing is limited to +/- 3V when the circuit is operated at +/- 5V supplies.

The input resistance of the output stage is important for calculating the transimpedance 3-dB point. This resistance is in parallel with the output resistances of Bp15 and Bn18. A small signal model of one side of the output stage is shown in Figure 29. Only one side is used for the calculation since only one side will be conducting during a signal swing.

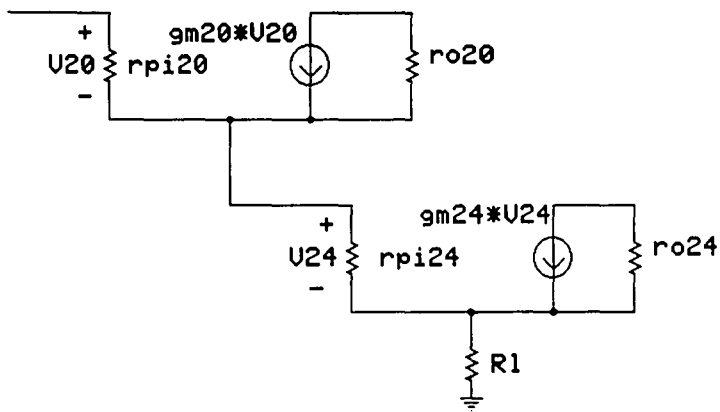


Figure 29
Bn20 Small Signal Model

By inspection, this resistance is

$$Rin = Rp20 + (Bn + 1)\cdot((Bp + 1)\cdot Rl + Rp24) \qquad (3.49)$$

Noting that Ic23=Ic24=4.93mA, Bn=120 and Bp=43, the input resistance of the output stages is

$$Rinout = 520.3 \text{ Kohm}$$

The effective resistance as seen by the gain node is the parallel resistance of Rinout, Rout15 and Rout18 is

$$Rgain = 268.3 \text{ Kohm}$$

This number will be used in the AC calculation section for the transimpedance 3-dB calculation.

3.3 AC Analysis

3.3.1 Gain Bandwidth

To calculate the gain bandwidth, or 3-dB point, of the amplifier, the effective capacitance of the gain node needs to be calculated. Once this is known, the transimpedance 3-dB point is defined as

$$f3dB = \frac{1}{2 \cdot \pi \cdot Cg \cdot Rg} \qquad (3.50)$$

where Rg and Cg are the effective resistance and capacitance of the gain node.

With Rg already known, the tricky part is to now calculated the equivalent capacitance of the gain node by looking back at the circuit of Figure 27. The effective capacitance of the gain node is as follows

$$Cg = C\mu 15 + Ccs15 + C\mu 18 + Ccs18 + C\mu 20 + C\mu 21 + 2 \cdot C \quad (3.51)$$

The values of these capacitors with no bias applied can be found in Appendix II, but some additional calculations need to be completed to obtain proper values. The general capacitance calculation is as follows

$$C = \frac{Co}{\left[1 + \frac{Vj}{a}\right]^{b}} \quad (3.52)$$

where Vj is the voltage across the junction and a and b are coefficients found in Appendix II.

Each capacitance is as follows:

$$\begin{aligned} Cu15 &= 0.540 \text{ pF} \\ Ccs15 &= 0.202 \text{ pF} \\ Cu18 &= 0.035 \text{ pF} \\ Ccs18 &= 0.370 \text{ pF} \\ Cu20 &= 0.030 \text{ pF} \\ Cu21 &= 0.046 \text{ pF} \\ C &= 0.630 \text{ pF} \end{aligned}$$

The total capacitance of the gain node is

$$Cg = 1.664 \text{ pF}$$

With this value in hand, the transimpedance 3-dB point can now be calculated and is

$$F3dB = 356,517 \text{ Hz}$$

In Chapter 4, the simulated transimpedance 3-dB point was found to be

$$F3dbsim = 365,438 \text{ Hz}$$

3.3.2 Slew Rate

The most important part of the input buffer is its slew rate limiting characteristics. In actuality, there are two slew rate calculations, one for positive pulse waveforms and one for negative pulse waveforms. Looking back at the circuit of Figure 17, the slew rate can be described as the ratio of the amount of current available to charge the Bp9:Bn3 node to the effective capacitance of the gain node calculated earlier. The current, Itot, is broken into two pieces. The first, Ibias, is simply the DC bias current of the buffer and is

$$Ibias = 0.378 \text{ mA}$$

The second current, Iac, is the C dv/dt current generated during the time the incoming signal is changing. The design of the buffer has taken advantage of this current by incorporating capacitors from the output of the buffer to the emitters of Bn1 and Bp5. The current capacitance is

$$Cc = C\mu 1 + Ccs12 + Ccs9 + Ccs3 + 2 \cdot C\mu 9 + Ccs2 + 2 \cdot C\mu 29 + Ccs29 + C \qquad (3.53)$$

Using the general capacitance formula in Eqn. (3.52) and the coefficients of Appendix II, the capacitances are as follows

$$\begin{aligned} Cu1 &= 0.032 \text{ pF} \\ Ccs12 &= 0.163 \text{ pF} \\ Ccs9 &= 0.190 \text{ pF} \\ Ccs3 &= 0.034 \text{ pF} \\ Cu9 &= 0.053 \text{ pF} \\ Ccs2 &= 0.036 \text{ pF} \\ Cu29 &= 0.038 \text{ pF} \\ Ccs29 &= 0.039 \text{ pF} \\ C &= 0.300 \text{ pF} \end{aligned}$$

The total capacitance is 0.976 pF.

To calculate the current, dv/dt must be known. For simulation purposes, a 4000v/us waveform was introduced at the input. However, parasitics were added to model the package, an 8-pin plastic dip, and the waveform reaching the part was actually about 1650V/us. Using 1650V/us, the current I2, calculates to

$$I2 = 1.59 \text{ mA}$$

The total charging current is now

$$Itot = 1.973 \text{ ma}$$

The slew rate is defined as

$$SR = \frac{Itot}{Cg} \tag{3.54}$$

Placing in the appropriate numbers, the positive slew calculates to

$$+SR = 1185 \text{ V/us}$$

Simulation results showed a positive slew rate of 1450 V/us.

In a similar manner the negative slew rate can be calculated, this time focusing on the Bp5, Bp6, Bp7, and Bp8 buffer. Calculations from this buffer determine the negative slew rate as

$$-SR = 1622 \text{ V/us}$$

Simulation results showed a negative slew rate of 1650 V/us.

Looking at the results of the slew rate calculation, two questions arise:

1) Why are the simulation results different?
2) Why is positive slew rate lower than negative slew rate?

The answer to the first question arises from the fact that only one side of the buffer was considered. To obtain a more accurate number, the AC currents through both buffers need to be considered.

The answer to the second question also comes from a closer look at the AC currents. Each buffer has a different amount of NPN and PNP transistors. For the lower buffer the PNP dominates with a larger parasitic capacitance. This capacitance multiplied by the dv/dt generates a larger AC current.

CHAPTER 4

Simulation Results

Chapter 3 presented the CFB op amp design and derived many of the DC and some of the important AC characteristics. In arriving at many, if not all, of the values, there were many approximations made to simplify the calculations. To fully characterize the amplifiers response, a detailed computer simulation must be completed. With a computer simulation, items such as base currents, early voltages, stray capacitances or even layout parasitics are now taken into consideration. Even case by case simulations taking into account manufacturing variations are made to ensure manufacturability of a particular design.

With all of the above in mind, Chapter 4 presents simply a nominal case simulation so that the reader can check the calculated values of Chapter 3 to the computer model. Chapter 4 also presents a nominal case simulation of CFB op amps encompassing the first two input buffer designs of Chapter 2. This will allow the reader to see how the input buffer used not only obtains a better offset voltage, but is also superior in several other aspects. Finally, this chapter presents a side by side comparison of the CFB op amp designed and Comlinear's CLC409.

For the reader's convenience, the full circuit design is repeated in Figure 30. Following Figure 30 is a printout of the nodal analysis and the transistor operating points. Afterwards is the detailed ADVICE file listing including package parasitics. Since the circuit has not been layed out, layout parasistics are not included. Figure 31 shows both the gain and phase response of the amplifier. From Figure 31, the 3-dB point of the circuit is nearly 350Mhz with a phase margin of about 45 degrees. The slew rate curve is presented in Figure 32 and calculates out to about 1500 V/uS. The main DC characteristic, output voltage swing, is shown in Figure 33, and output current drive in Figure 34. From Figure 34, with a 50 ohm output load, the circuit can drive nearly 70mA nominally. From the DC operating point data, the op amp has a 0.3 mV offset and dissipates 130 mW of power. Figures 35 and 36 present the transimpedance gain and phase of the amplifier. From the graph, the 3-dB point of the transimpedance gain is nearly 330 Khz.

Figures 37 and 38 present the gain and slew rate of a CFB amplifier identical to the design with the exception that the input buffer of Figure 13 used. The 3-dB point of the voltage gain curve is 195 Mhz, slew rate 1100 V/us, offset 10 mV, and power dissipation 110 mW.

Figures 39 and 40 present the gain and slew rate of a CFB amplifier identical to the design with the exception that the input buffer of Figure 14 was used. The 3-dB point of the voltage gain curve is 140 Mhz, slew rate 700 V/us, offset -3.6 mV, and power dissipation 110 mW.

It seems that while the input buffer chosen was strictly for offset voltage reduction, many other performance parameters are improved.

Finally Figure 41 presents a comparison of the CLC409 to the designed op amp.

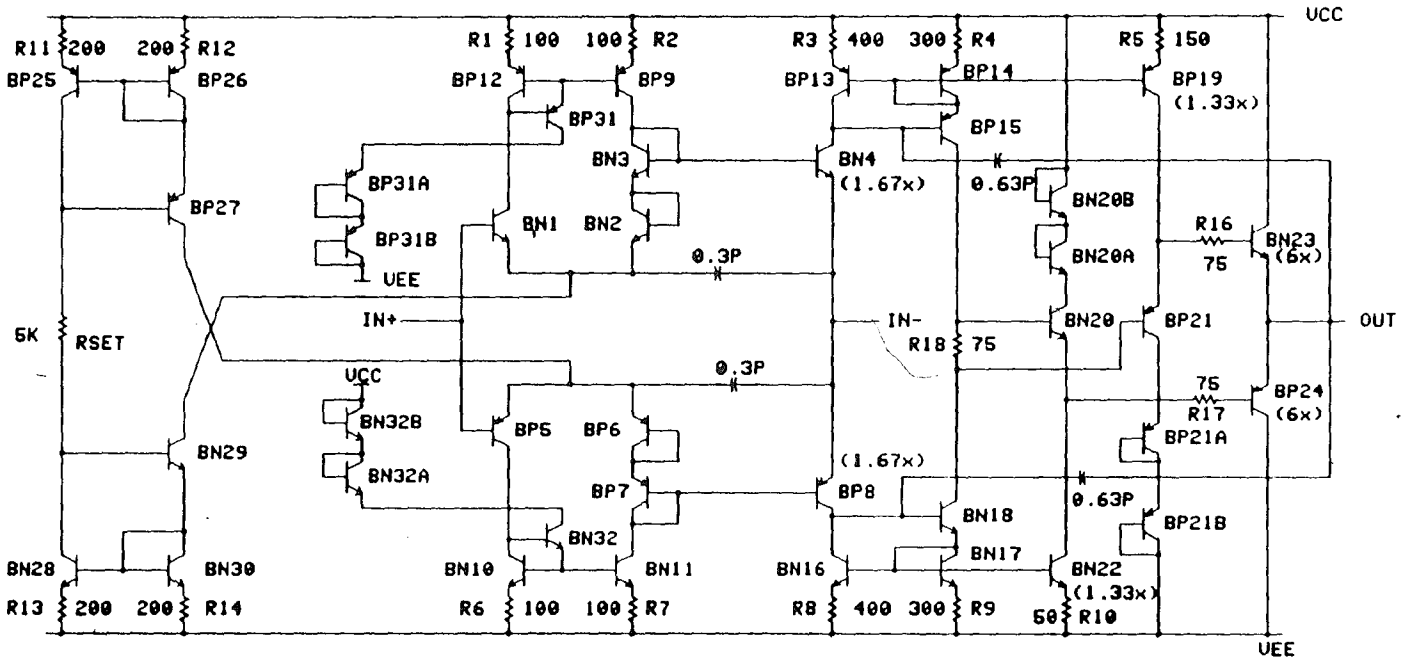


Figure 30
CFB op amp Design

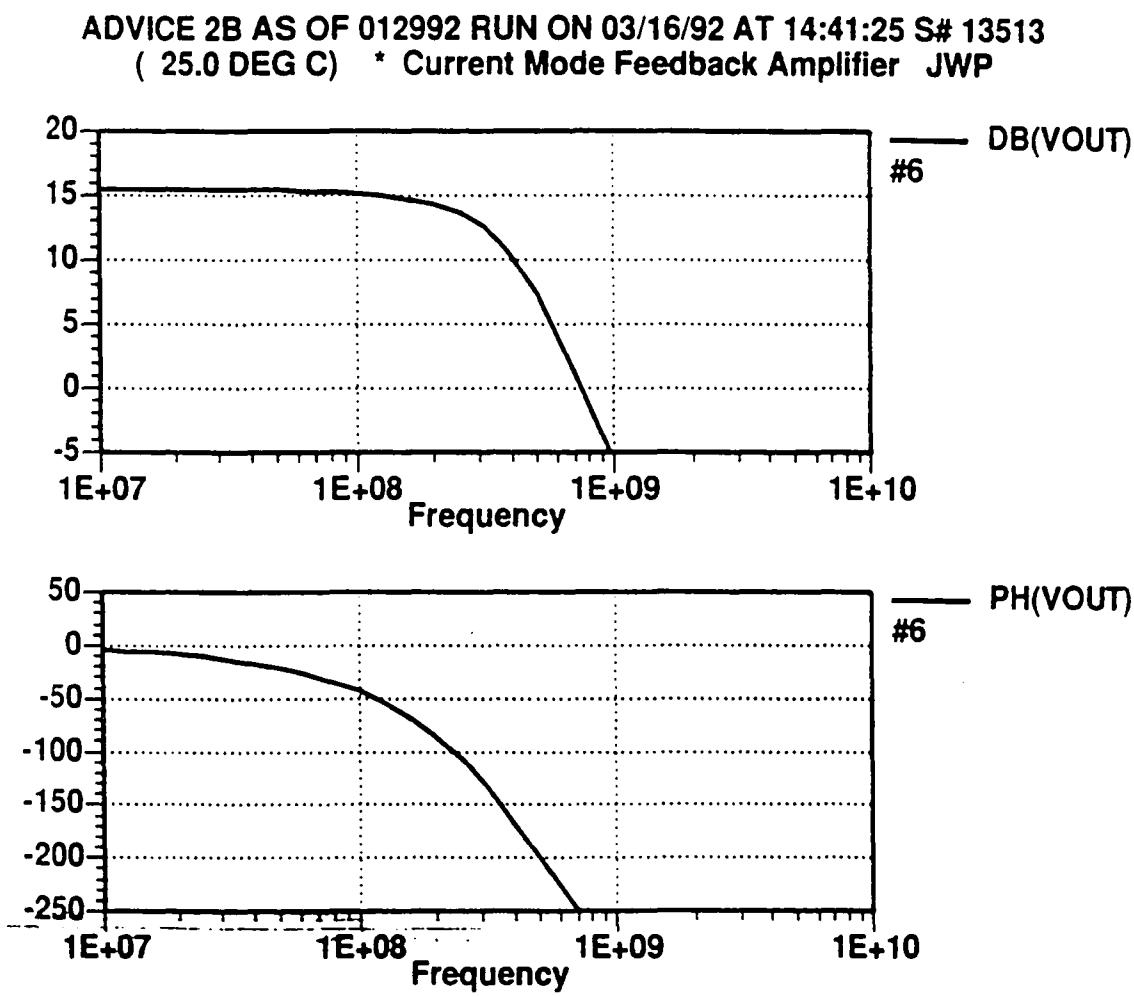


Figure 31
CFB Op Amp Gain and Phase Response

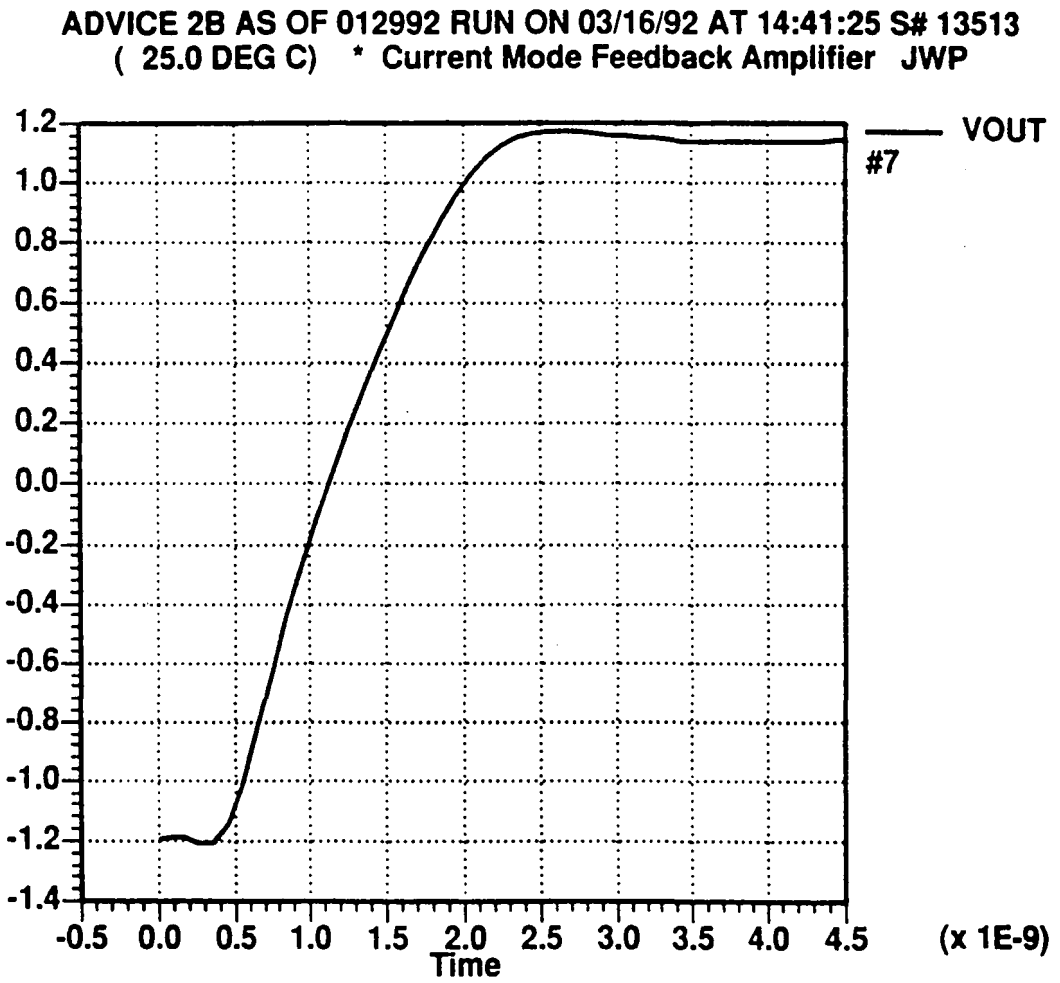


Figure 32
CFB Op Amp Pulse Response

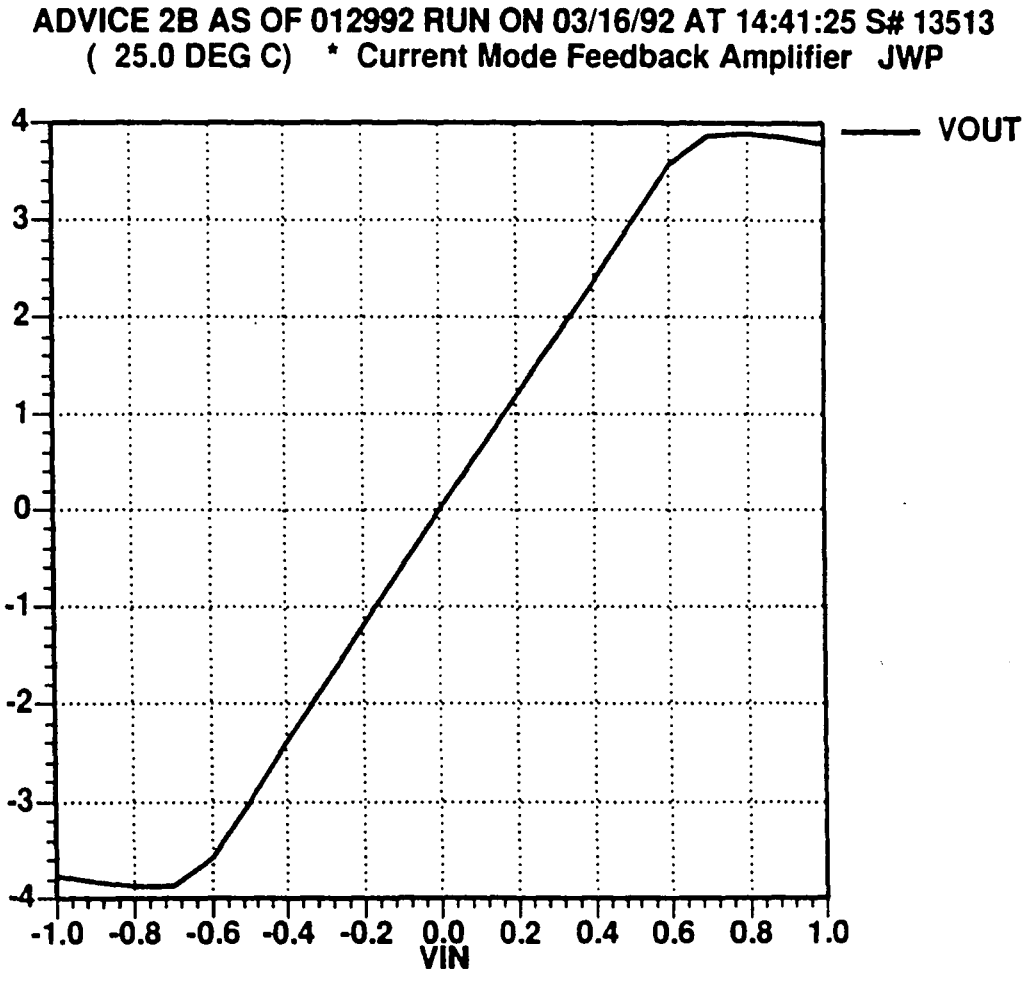


Figure 33
CFB Op Amp Output Voltage Swing

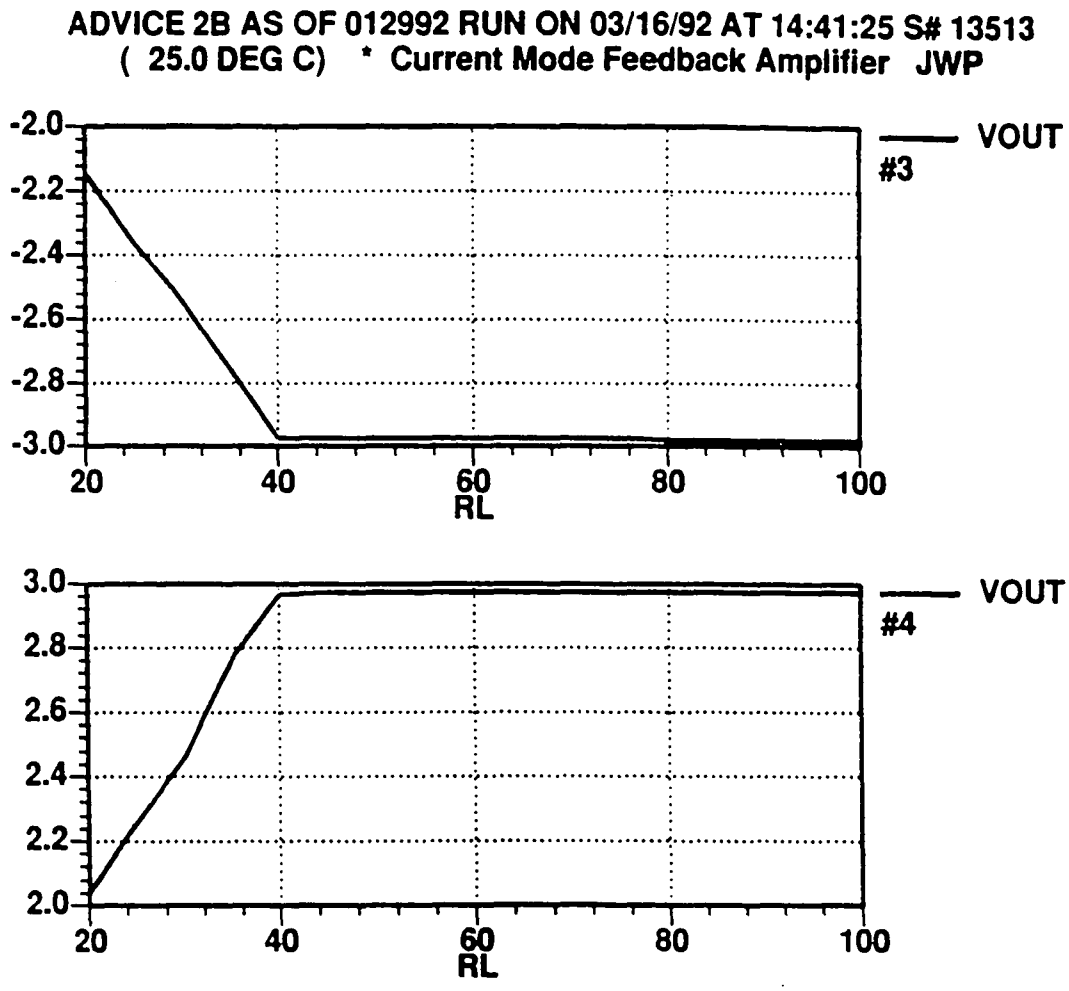


Figure 34
CFB Output Current Drive

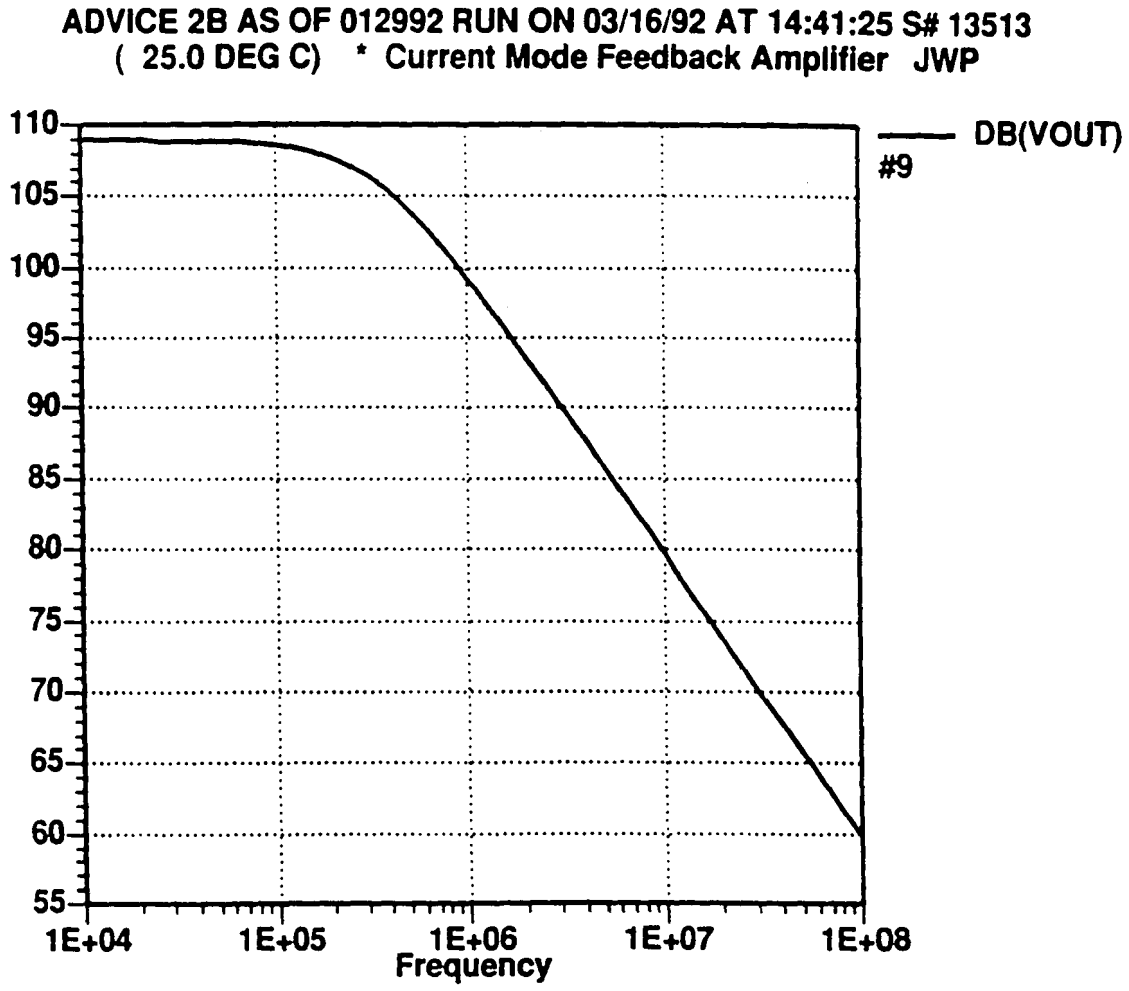


Figure 35
CFB Op Amp Transimpedance Gain

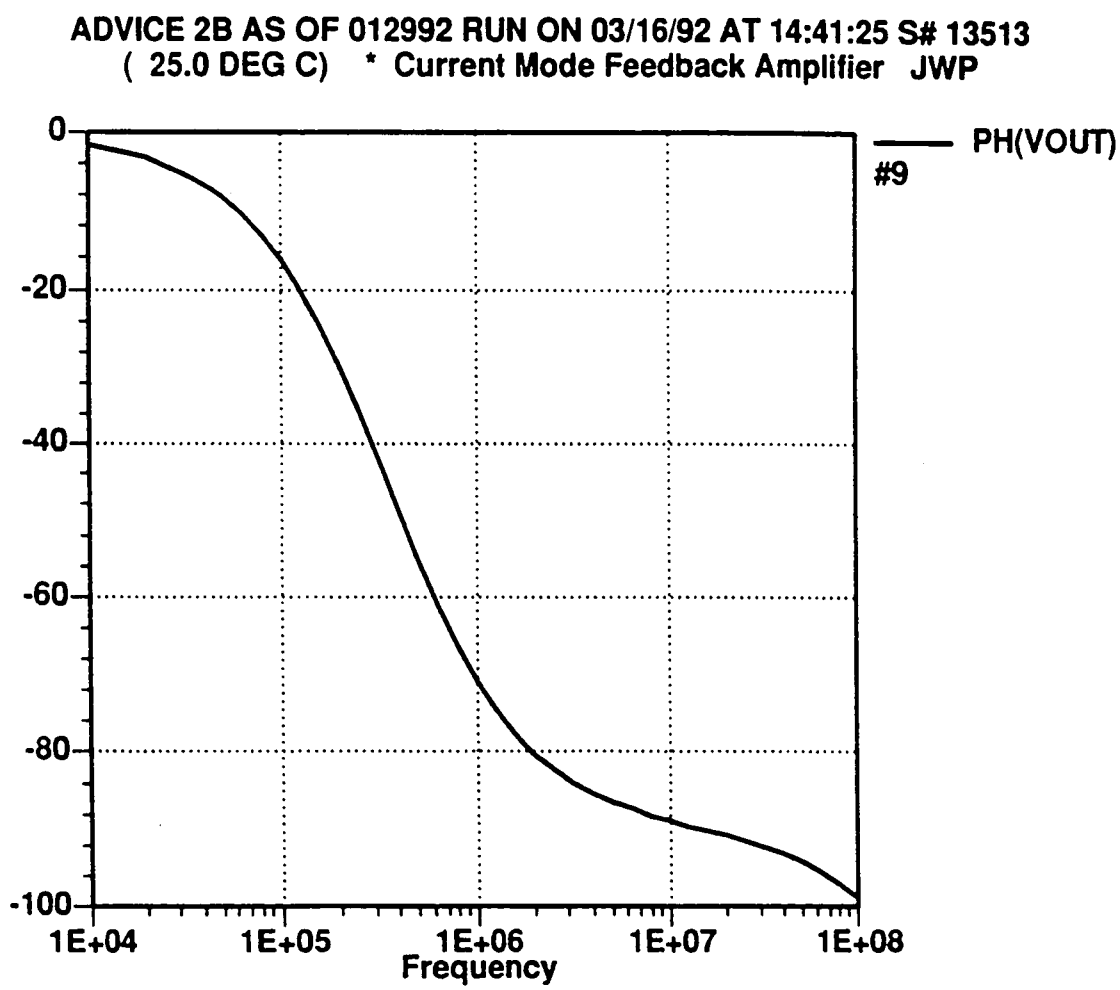


Figure 36
CFB Op Amp Transimpedance Phase

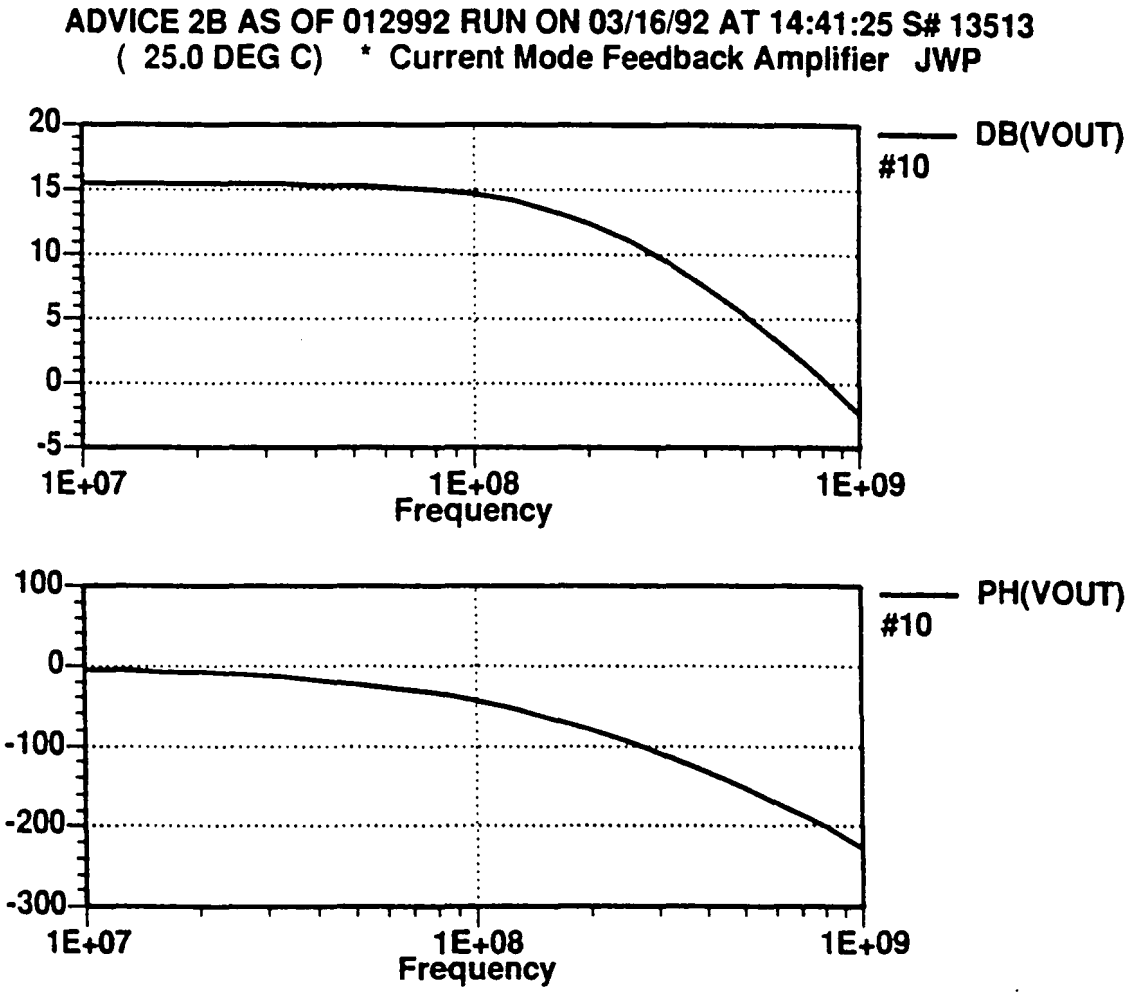


Figure 37
CFB Op Amp with Input Buffer #1 Frequency Response

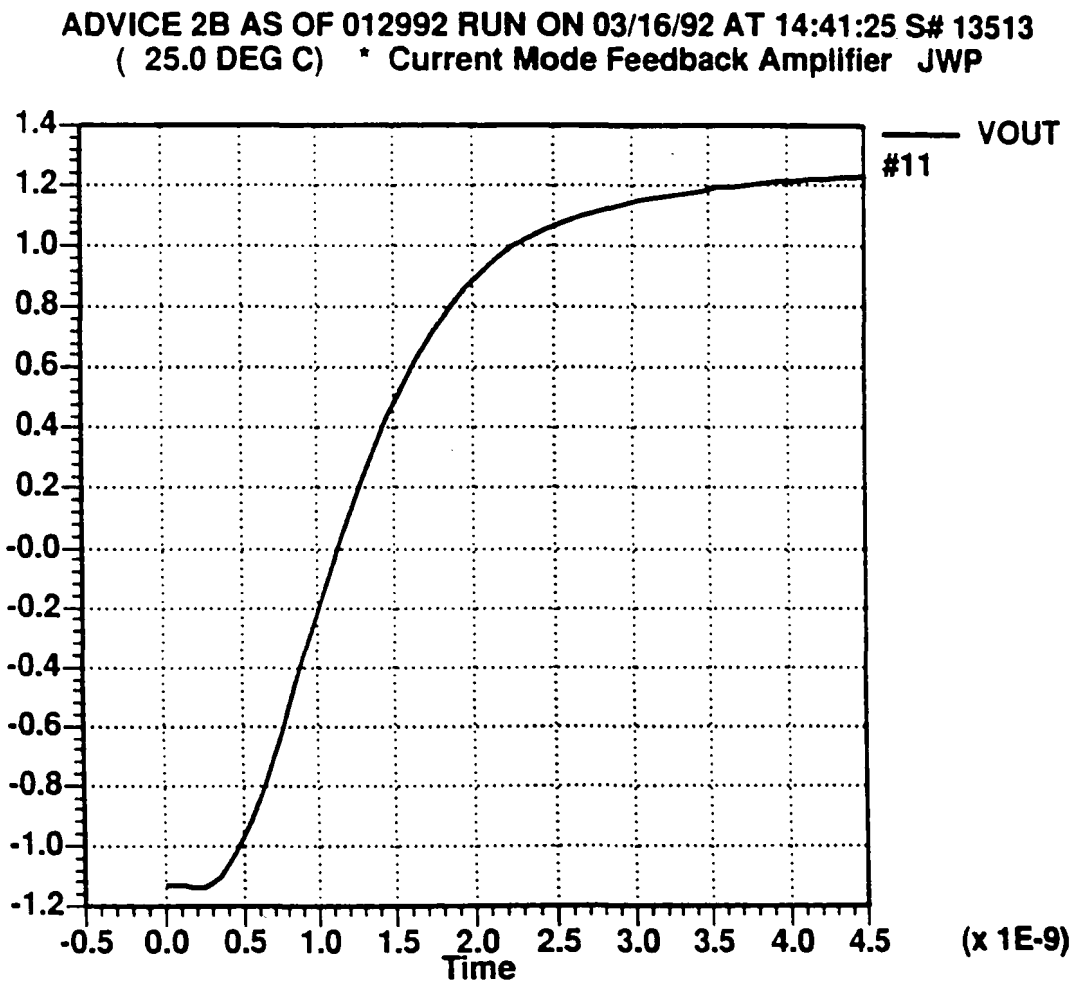


Figure 38
CFB Op Amp with Input Buffer #1 Pulse Response

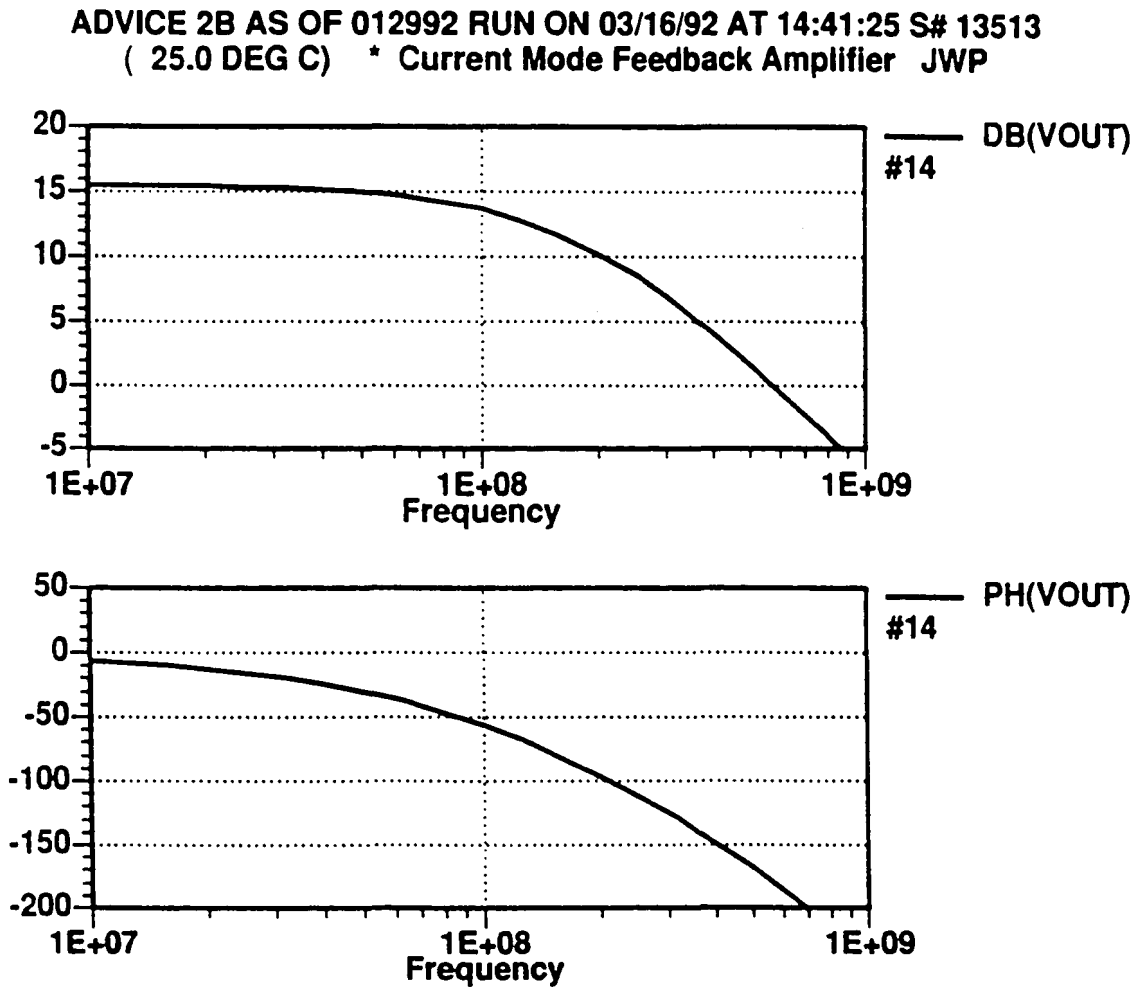


Figure 39
CFB Op Amp with Input Buffer #2 Frequency Response

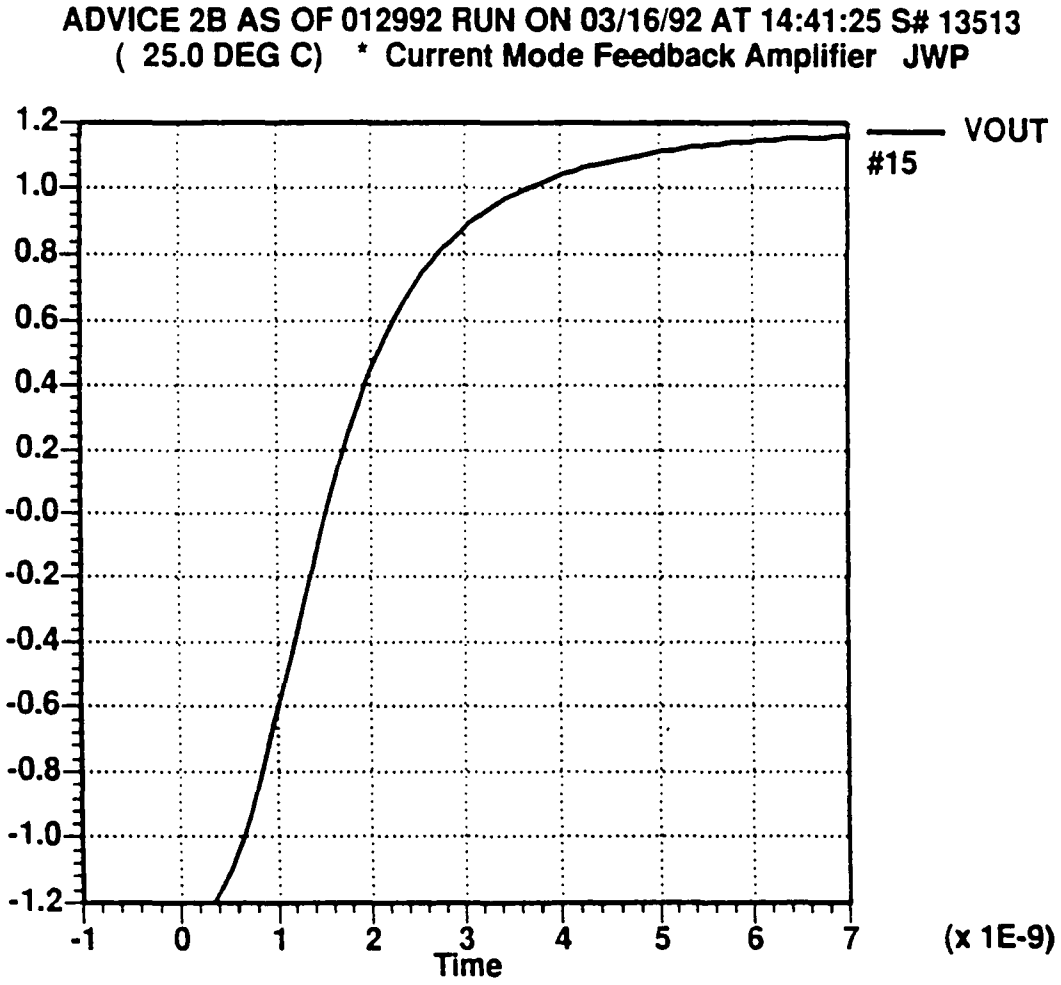


Figure 40
CFB Op Amp with Input Buffer #2 Pulse Response

Rfb=500, Rload=100 Av = +6	CFB DESIGN	CLC409
-3dB Bandwidth	350Mhz	350Mhz
Slew Rate	1500V/us	1200V/us
Settling Time 0.1%	7ns	8ns
Overshoot 2V step	< 1%	5%
Harmonic Distortion		
2nd @ 20Mhz	-61dB	-65dB
2nd @ 60Mhz	-51dB	-49dB
3rd @ 20Mhz	-73dB	-72dB
3rd @ 60Mhz	-66dB	-59dB
Input Offset Voltage	-1.3mV	0.5mV
PSRR	52dB	50dB
CMRR	51dB	50dB
Output Voltage Range	+/- 3V	+/- 3.5V
Input Dynamic Range	+/- 3V	+/- 2.2V
Ivcc	13.6mA	13.5mA
Output Current	70mA	70mA

Figure 41
CFB Op Amp Market Comparison

CONCLUSION

In this paper, the concept of current-feedback has been discussed and a current-feedback amplifier design was presented.

Chapter 1 compared voltage-feedback topology to current-feedback topology. Voltage-feedback was found to have a closed-loop frequency response dependant upon the closed-loop gain, and a suppressed slew rate due to the Miller effect. Current-feedback was found not to exhibit a frequency response solely dependant upon closed-loop gain and had a slew rate capability that was orders of magnitude above voltage-feedback.

Chapter 2 presented 4 different input buffer designs for use in a CFB op amp. Buffer 1 was found to have a high offset voltage due to the mismatch in current density in NPN and PNP transistors. Buffer 2 added emitter follower diodes after each transistor to eliminate the deficiency of buffer 1. However, this design now suffered a decreased input dynamic range and poorer frequency response due to the diodes. Buffer 3 presented a means of eliminate the deficiencies of buffer 1 without the repercussions of buffer 2. However, this design suffered from the fact that

increased currents were needed to permit the buffer to function properly in all worst case scenarios. Finally, buffer 4 was presented and was found to not exhibit the deficiencies of the previous three buffers. Buffer 4 was used in the final design of the CFB op amp.

Chapter 3 presented a detailed analysis of the amplifier for the nominal case. Several different biasing schemes were discussed and it was decided to use a dual Wilson mirror because of it's high output impedance. Buffer 4 was analyzed in more detail and it was found that the offset, PSRR, and CMRR were dependant upon the early voltage of the devices. Bias currents were calculated for all transistors along with the op amp's 3-dB point and slew rate.

Chapter 4 presented nominal case simulation results using AT&T's ADVICE simulator. Results from the hand analysis were compared to the simulator and were found to be within an acceptable error range.

APPENDIX I: DC Operating Point

```
*  Current Mode Feedback Amplifier   JWP
*  Written  1/21/91  J.W. Pierdomenico
*  Diodes added to output stage for breakdown
*  3/5/92
*  150fF added for ESD diodes  3/9/92
*
Bn1     4    in+     1       8     NV231A01
Bn2     2    2       1       8     NV231A01
Bn3     3    3       2       8     NV231A01
Bn4    14    3     in-       8     NV231A01 1.67
Bp5     6   in+      5       7     PV231A01
Bp6    10   10       5       7     PV231A01
Bp7     9    9      10       7     PV231A01
Bp8    15    9     in-       7     PV231A01 1.67
Bp9     3   4a      12       7     PV231A01
Bn10    6   6a      16       8     NV231A01
Bn11    9   6a      17       8     NV231A01
Bp12    4   4a      11       7     PV231A01
Bp13   14   21      13       7     PV231A01
Bp14   21   21      22       7     PV231A01
Bp15   CCa  14      21       7     PV231A01
Bn16   15   19      18       8     NV231A01
Bn17   19   19      20       8     NV231A01
Bn18   CCb  15      19       8     NV231A01
Bp19   24   21      23       7     PV231A01 1.33
Bn20   25a  CCa     25       8     NV231A01
Bn20a  25b  25b     25a      8     NV231A01
Bn20b   7    7      25b      8     NV231A01
Bp21   24a  CCb     24       7     PV231A01
Bp21a  24b  24b     24a      7     PV231A01
Bp21b   8    8      24b      7     PV231A01
Bn22   25   19      26       8     NV231A01 1.33
Bn23    7   24c     OUT      8     NV663A01 2
Bp24    8   25c     OUT      7     PV693A01 1.33
Bp31   8a    4      4a       7     PV231A01
Bp31a  8b   8b      8a       7     PV231A01
Bp31b   8    8      8b       7     PV231A01
Bn32   7a    6      6a       8     NV231A01
Bn32a  7b   7b      7a       8     NV231A01
Bn32b   7    7      7b       8     NV231A01
*
*   Currents In and Ip
*
*
Bp25      29   34   28   7     PV231A01
Bp26      34   34   27   7     PV231A01
Bp27       5   29   34   7     PV231A01
Bn28      30   31   32   8     NV231A01
Bn29       1   30   31   8     NV231A01
Bn30      31   31   33   8     NV231A01
XRset       29    30   7    RVH   (R=18000)
XR11        28     7   7    RVL   (R=200)
XR12        27     7   7    RVL   (R=200)
XR13        32     8   7    RVL   (R=200)
XR14        33     8   7    RVL   (R=200)
*
*
XC2       OUT    14    8    CVC   (C=0.63p)
XC3       OUT    15    8    CVC   (C=0.63p)
XC4       IN-    1     8    CVC   (C=0.3p)
XC5       IN-    5     8    CVC   (C=0.3p)
*
XR1     11     7     7    RVL   (R=85)
XR2     12     7     7    RVL   (R=100)
XR3     13     7     7    RVL   (R=400)
XR4     22     7     7    RVL   (R=300)
```

```
XR5     23      -       -     RVL   (R=150)
XR6     16      8       -     RVL   (R=100)
XR7     17      8       -     RVL   (R=125)
XR8     18      8       -     RVL   (R=400)
XR9     20      8       -     RVL   (R=300)
XR10    26      8       -     RVL   (R=50)
*XR15   25      8       -     RVL   (R=10K)
XR16    25    25c       -     RVL   (R=75)
XR17    24    24c       -     RVL   (R=75)
XR18   CCA   CCB       -     RVL   (R=75)
*
*  Package Parasitics
*
L1  inc+  inb+  2.3n
L2  inb+  ina+  1.9n
L3  ina+  in+   1.4n
C1  inb+   0  0.32p
C2  ina+   0  0.32p
C2a in+    0  0.15p
*
L4  inc-  inb-  2.3n
L5  inb-  ina-  1.9n
L6  ina-  in-   1.4n
C3  inb-   0  0.32p
C4  ina-   0  0.32p
C4a in-    0  0.15p
*
L7  outc   outb   2.3n
L8  outb   outa   1.9n
L9  outa   out    1.4n
C5  outb    0  0.32p
C6  outa    0  0.32p
C6a out     0  0.15p
*
L10  vccc   vccb   2.3n
L11  vccb   vcca   1.9n
L12  vcca   7      1.4n
C7  vccb    0  0.32p
C8  vcca    0  0.32p
C8a  7      0  0.15p
*
L13  veec   veeb   2.3n
L14  veeb   veea   1.9n
L15  veea   8      1.4n
C9  veeb    0  0.32p
C10  veea    0  0.32p
C10a  8     0   0.15p
*
Rin      IND+    INC+  100
VCC      vccc     0     +5V
VEE      veec     0     -5V
*Iin      IND+     0      10u
*Iout      OUTC     0      10u
Vin      IND+     0      0V   AC   1
*VIN      IND+     0       PULSE(-0.2  0.2  0 0.1n 0.1n 100n 110n)
*VIN      IND+     0       SIN(0  0.333  20Meg 0 0 0)
Rg       INC-     0     100
Rfb      OUTC   INC-    500
R1       OUTC    0     100
*
*.tran 1n 200n
.out vin- in- 0;
.out vout out 0;
.out vin in+ 0;
*
.AC  DEC 10  10M   10G
```

***** independent voltage source operating points

name	current	voltage	power
VCC	-1.364E-02	5.000	-6.820E-02
VEE	1.366E-02	-5.000	-6.830E-02
VIN	2.321E-06	0.000	0.000E+00

***** node voltages

Node	Voltage	Node	Voltage	Node	Voltage
(0)	0.00000E+00	(1)	-7.29712E-01	(10)	-5.88376E-03
(11)	4.98430E+00	(12)	4.97994E+00	(13)	4.81938E+00
(14)	3.27339E+00	(15)	-3.29997E+00	(16)	-4.98061E+00
(17)	-4.97656E+00	(18)	-4.82170E+00	(19)	-4.06370E+00
(2)	6.11871E-03	(20)	-4.82974E+00	(21)	4.04792E+00
(22)	4.82845E+00	(23)	4.83226E+00	(24)	7.68770E-01
(24A)	-3.40482E+00	(24B)	-4.20241E+00	(24C)	7.64274E-01
(25)	-7.88758E-01	(25A)	3.37444E+00	(25B)	4.18722E+00
(25C)	-7.77940E-01	(26)	-4.86570E+00	(27)	4.92567E+00
(28)	4.92403E+00	(29)	3.39518E+00	(3)	7.41949E-01
(30)	-3.41960E+00	(31)	-4.17083E+00	(32)	-4.92423E+00
(33)	-4.92504E+00	(34)	4.15747E+00	(4)	3.59529E+00
(4A)	4.23767E+00	(5)	7.41567E-01	(6)	-3.62995E+00
(6A)	-4.24566E+00	(7)	5.00000E+00	(7A)	3.75203E+00
(7B)	4.37601E+00	(8)	-5.00000E+00	(8A)	-3.67388E+00

(8B) -4.33694E+00 (9 -7.33334E-01 (CCA) 2.09617E-02

(CCB) -2.17742E-02 (IN+) 2.32092E-04 (IN-) -3.05027E-04

(INA+) 2.32092E-04 (INA-) -3.05027E-04 (INB+) 2.32092E-04

(INB-) -3.05027E-04 (INC+) 2.32092E-04 (INC-) -3.05027E-04

(IND+) 0.00000E+00 (OUT) -2.02287E-03 (OUTA) -2.02287E-03

(OUTB) -2.02287E-03 (OUTC) -2.02287E-03 (VCCA) 5.00000E+00

(VCCB) 5.00000E+00 (VCCC) 5.00000E+00 (VEEA) -5.00000E+00

(VEEB) -5.00000E+00 (VEEC) -5.00000E+00 (XC2 .4) 3.27339E+00

(XC3 .4) -3.29997E+00 (XC4 .4) -7.29712E-01 (XC5 .4) 7.41567E-01

(XR1 .D) 4.99215E+00 (XR10 .D) -4.93285E+00 (XR11 .D) 4.96201E+00

(XR12 .D) 4.96283E+00 (XR13 .D) -4.96212E+00 (XR14 .D) -4.96252E+00

(XR16 .D) -7.83349E-01 (XR17 .D) 7.66522E-01 (XR18 .D) -4.06286E-04

(XR2 .D) 4.98997E+00 (XR3 .D) 4.90969E+00 (XR4 .D) 4.91423E+00

(XR5 .D) 4.91613E+00 (XR6 .D) -4.99031E+00 (XR7 .D) -4.98828E+00

(XR8 .D) -4.91085E+00 (XR9 .D) -4.91487E+00 (XRSET .D) -1.22073E-02

***** User-Defined Model NEB1 operating point

name	ib	ic is	vbe vsc	vbc rci-mod	vce	beta	power
BN1	1.319E-06	1.804E-04 -9.214E-18	0.730 -8.595	-3.595 1.009	4.325	136.8	7.812E-04
BN2	1.646E-06	1.917E-04 -1.064E-17	0.736 -5.006	0.000 1.009	0.736	116.5	1.422E-04
BN3	1.646E-06	1.917E-04 -1.065E-17	0.736 -5.742	0.000 1.009	0.736	116.5	1.422E-04

BN4	3.485E-06	4.527E-04	0.742	-3.531	3.274	129.9	1.485E-03
		-1.538E-17	-8.273	1.013			
BN10	1.592E-06	1.923E-04	0.735	-0.616	1.351	120.8	2.609E-04
		-9.088E-18	-1.370	1.009			
BN11	1.867E-06	1.961E-04	0.731	-3.492	4.223	136.2	7.971E-04
		-9.134E-18	-4.247	1.009			
BN16	3.745E-06	4.420E-04	0.758	-1.764	1.522	118.0	6.755E-04
		-9.094E-18	-1.700	1.022			
BN17	5.038E-06	5.625E-04	0.766	1.000	0.766	111.7	4.348E-04
		-1.105E-17	-0.936	1.028			
BN18	4.603E-06	5.902E-04	0.764	-3.278	4.042	128.2	2.389E-03
		-9.148E-18	-4.978	1.030			
BN20	2.272E-05	2.495E-03	0.810	-3.353	4.163	109.8	1.041E-02
		-9.209E-18	-8.374	1.139			
BN20A	2.551E-05	2.470E-03	0.813	0.000	0.813	96.8	2.028E-03
		-1.753E-17	-9.187	1.137			
BN20B	2.551E-05	2.470E-03	0.813	0.000	0.813	96.8	2.028E-03
		-1.755E-17	-10.000	1.137			
BN22	2.348E-05	2.662E-03	0.802	-3.275	4.077	113.4	1.087E-02
		-1.215E-17	-4.211	1.108			
BN23	5.994E-05	7.863E-03	0.766	-4.236	5.002	131.2	3.938E-02
		-8.950E-17	-10.000	1.033			
BN32	2.299E-08	2.936E-06	0.616	-7.382	7.998	127.7	2.349E-05
		-9.208E-18	-8.752	1.000			
BN32A	3.005E-08	2.906E-06	0.624	0.000	0.624	96.7	1.832E-06
		-1.052E-17	-9.376	1.000			
BN32B	3.005E-08	2.906E-06	0.624	0.000	0.624	96.7	1.832E-06
		-1.053E-17	-10.000	1.000			
BN28	3.160E-06	3.757E-04	0.753	-0.751	1.505	118.9	5.677E-04
		-9.092E-18	-1.580	1.019			
BN29	2.910E-06	3.750E-04	0.751	-2.690	3.441	128.9	1.293E-03
		-9.136E-18	-4.270	1.019			
BN30	3.260E-06	3.715E-04	0.754	0.000	0.754	114.0	2.827E-04
		-1.078E-17	-0.829	1.019			

***** User-Defined Model PEB1 operating point

name	ib	ic is	vbe vsc	vbc rci-mod	vce	beta	power
BP5	-3.640E-06	-1.923E-04	-0.741	3.630	-4.372	52.8	8.434E-04
		5.080E-17	8.630	1.012			
BP6	-4.523E-06	-1.724E-04	-0.747	0.000	-0.747	38.1	1.323E-04
		6.435E-17	5.006	1.011			
BP7	-4.523E-06	-1.724E-04	-0.747	0.000	-0.747	38.1	1.323E-04
		6.443E-17	5.753	1.011			
BP8	-9.169E-06	-4.466E-04	-0.753	2.547	-3.300	48.7	1.481E-03
		8.481E-17	8.300	1.016			
BP9	-3.762E-06	-1.968E-04	-0.742	3.496	-4.238	52.3	8.368E-04
		5.036E-17	4.258	1.012			
BP12	-4.393E-06	-1.803E-04	-0.747	0.642	-1.389	41.0	2.537E-04
		5.011E-17	1.405	1.011			
BP13	-1.053E-05	-4.410E-04	-0.771	0.775	-1.546	41.9	6.899E-04
		5.014E-17	1.727	1.027			
BP14	-1.450E-05	-5.573E-04	-0.781	0.000	-0.781	38.4	4.463E-04
		1.044E-16	0.952	1.035			
BP15	-1.167E-05	-5.925E-04	-0.775	3.252	-4.027	50.8	2.395E-03
		5.043E-17	4.979	1.037			
BP19	-2.184E-05	-1.096E-03	-0.784	3.279	-4.063	50.2	4.472E-03
		6.697E-17	4.231	1.053			
BP21	-2.034E-05	-1.016E-03	-0.791	3.383	-4.174	50.0	4.257E-03
		5.078E-17	8.405	1.066			
BP21A	-2.623E-05	-9.899E-04	-0.798	0.000	-0.798	37.7	8.105E-04

		3.033E-16	9.202	1.064			
BP21B	-2.623E-05	-9.899E-04	-0.798	0.000	-0.798	37.7	8.108E-04
		3.034E-16	10.000	1.064			
BP24	-1.442E-04	-7.802E-03	-0.776	4.222	-4.998	54.1	3.911E-02
		4.693E-16	10.000	1.042			
BP31	-1.303E-07	-8.025E-06	-1.642	7.269	-7.911	61.6	6.357E-05
		5.076E-17	8.674	1.000			
BP31A	-2.544E-07	-7.771E-06	-0.663	0.000	-0.663	30.5	5.321E-06
		5.865E-17	9.337	1.000			
BP31B	-2.544E-07	-7.771E-06	-0.663	0.000	-0.663	30.5	5.321E-06
		5.872E-17	10.000	1.000			
BP25	-8.859E-06	-3.710E-04	-0.767	0.762	-1.529	41.9	5.740E-04
		5.013E-17	1.605	1.023			
BP26	-9.397E-06	-3.623E-04	-0.768	0.000	-0.768	38.6	2.855E-04
		7.727E-17	0.843	1.022			
BP27	-7.601E-06	-3.729E-04	-0.762	3.654	-3.416	49.1	1.280E-03
		5.037E-17	4.258	1.023			

APPENDIX II

Complementary Bipolar Technology

CBIC, Complimentary Bipolar Integrated Circuit, has several key advantages over an conventional all NPN process. It performs voltage level shifting, provides high output load drive capability while maintaining frequency operation, allows for large input and output voltage swings and can operate at lower power supply voltages. With CBIC technology, circuits can be optimized with reduced amount of time and experience on the designers behalf. The one main disadvantage of CBIC technology is its higher than nominal costs. This arises because there are many more steps, as high as 25 or more, in making a wafer containing CBIC technology than there is for an all NPN technology.

The arrival of linear arrays in the mid 1980's has allowed for circuits to be manufactured at lower costs. A linear array is basically a circuit with no metallization. NPN and PNP transistors are layed out in a way such that all a designer needs to do is connect them with metal. This allows for lower costing devices and faster time to market, about 6 to 8 weeks. One main disadvantage is that, being layed out on an array, area is larger than needs to be, and as a result, layout parasitics are higher. Still, the array

allows the designer to evaluate his or her design quickly and cost effectly to see if a custom layout is necessary.

This circuit is designed for AT&T's ALA110 linear array. This array utilizes AT&T's CBIC-V technology which features a NPN ft of 11.2 Ghz and PNP ft of 5.6 Ghz. There are 51 NPN and 41 PNP transistors ranging from 6X to 54X. Also provided are 80 and 2000 ohm/square resistors, programmable MOS capacitors, ESD diodes, and 16 bonding pads. The array's footprint is 2.1 mm X 1.4 mm.

Cross sections of CBIC NPN and PNP transistors are shown in Figure 42. The transistors are isolated by reversed biased junctions as opposed to a dielectric isolated process. As a result, parasitic capacitances are slightly higher. Both transistors are true vertical devices.

The n-type epitaxial layer is grown on top of a p-type substrate after buried layers are implanted. These buried layers are of low resistivity so parasitic collector resistance is reduced. The n-type epitaxial layer also forms the collector for the NPN device. The collector of the PNP is a p-type implantation and diffusion into the epitaxial layer. The n-epi acts as the substrate for the PNP device and must be connected to the most positive supply and the p-substrate for the NPN must be connected to the

most negative supply to ensure proper operation of the devices.

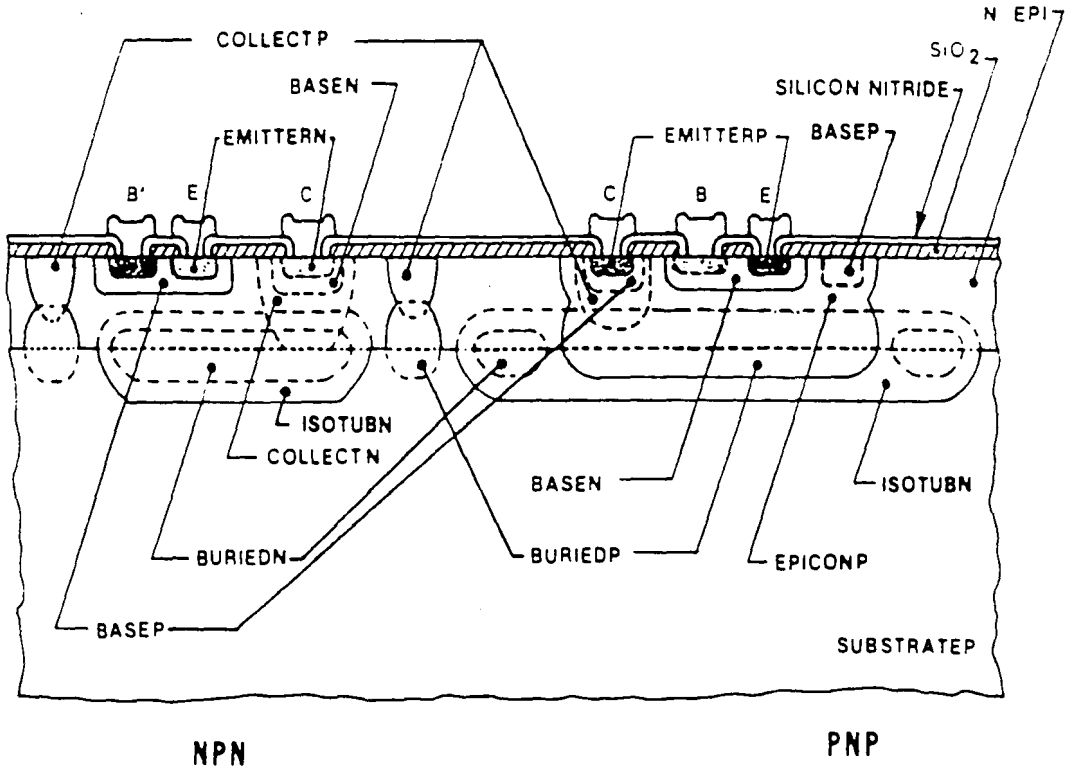


Figure 42
CBIC Transistor Cross Section

The critical step in the process is the emitter implantation and diffusion. So critical is this step that many lots are done in a wafer to wafer manner to ensure proper thickness. The length of each emitter stripe is 1.5 um so the base width can be made narrow while keeping a low parasitic resistance.

The smallest device for a transistor is what AT&T calls an NV111A01. This is a 5 um emitter device. The smallest device available on the ALA110 is the NV231A01, a 30 um device. AT&T distinguishes between transistors in the following manner:

N	-	type of device (N-NPN P-PNP)
V	-	technology (CBIC-V)
2	-	number of emitter stripes
3	-	length of each emitter stripe divided by 5 um
1	-	number of collector contacts
A	-	version A
0	-	layout style
1	-	number of devices within same isolation

Figure 43 provides a table of electrical characteristics for both the NV231A01 and PV231A01 transistors.

NPN (NV231A01) Characteristics (TA = 25°C)

Parameter	Measurement Condition	Limits			Units
		Min	Typ	Max	
HFE	IC = 1 mA, VCB = 2 V	50	118	–	–
fT	IC = 4 mA, VCE = 3 V	8	10.2	–	GHz
VA	IC = 1 mA, VCE = 2, 4 V	12	27	–	V
VCE(sat)	IC = 1 mA, IB = 100 µA	–	86	180	mV
VBE	IE = –1 mA, VCB = 2 V	740	780	810	mV
BVCEX	IC = 100 µA, IB = 0.1 µA	6	11.5	–	V
BVCBO	IC = 1 µA	6	19	–	V
BVCIO	IC = 1 µA	25	45	–	V
BVEBO	IE = 10 µA	2	–	–	V
BVEBS	IE = 1 µA	0.2 *	–	–	V

PNP (PV231A01) Characteristics (TA = 25°C)

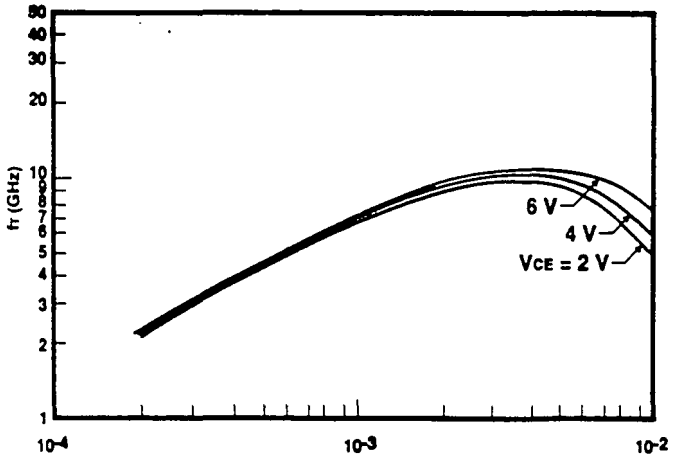
Parameter	Measurement Condition	Limits			Units
		Min	Typ	Max	
HFE	IC = –1 mA, VCB = –2 V	25	45	–	–
fT	IC = –3 mA, VCE = –3 V	3	4.3	–	GHz
VA	IC = –1 mA, VCE = –2, –4 V	6	11	–	V
VCE(sat)	IC = –1 mA, IB = –100 µA	–	–188	–360	mV
VBE	IE = 1 mA, VCB = –2 V	–750	–792	–830	mV
BVCEX	IC = –100 µA, IB = –0.1 µA	6	15	–	V
BVCBO	IC = –1 µA	8	22	–	V
BVCIO	IC = –1 µA	11	17	–	V
BVEBO	IE = –10 µA	–3.5	–	–	V
BVEBS	IE = –1 µA	0.1 *	–	–	V

Figure 43
Transistor electrical characteristics

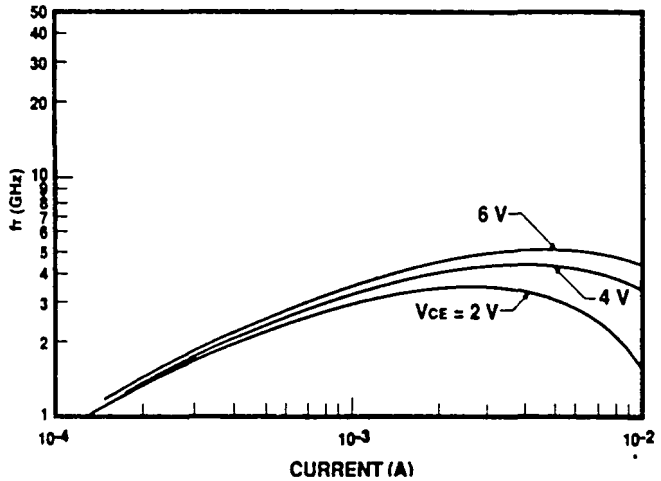
One of the more limiting characteristics of the CBIC-V technology is it's breakdown voltage. This breakdown limited the output voltage swing of the CFB op amp to +/- 3V. The breakdown is different for NPN and PNP devices. For the NPN, the BVCEx is the result of the avalanche breakdown of collector to base junction. For the PNP, the BVCEx is primarily a base punchthrough effect. The

basewidth becomes depleted and the collector is effectively shorted to the emitter.

Figures 44 through 49 presents the rest of the transistor curves utilized while design the CFB op amp.

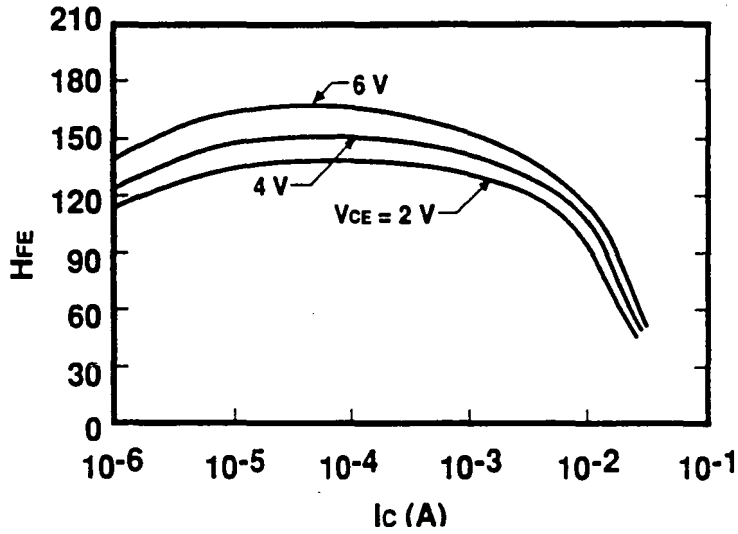


Typical Unity Gain Frequency Response (NV231A01)

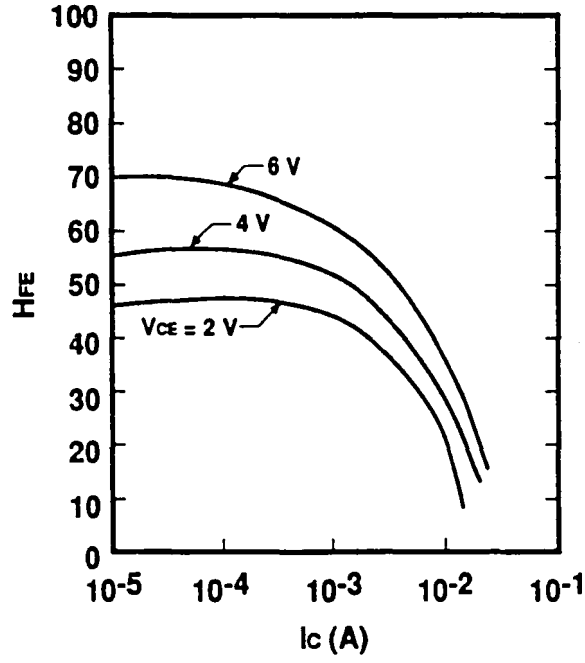


Typical Unity Gain Frequency Response (PV231A01)

Figure 44
Typical Unity Gain Frequency Response

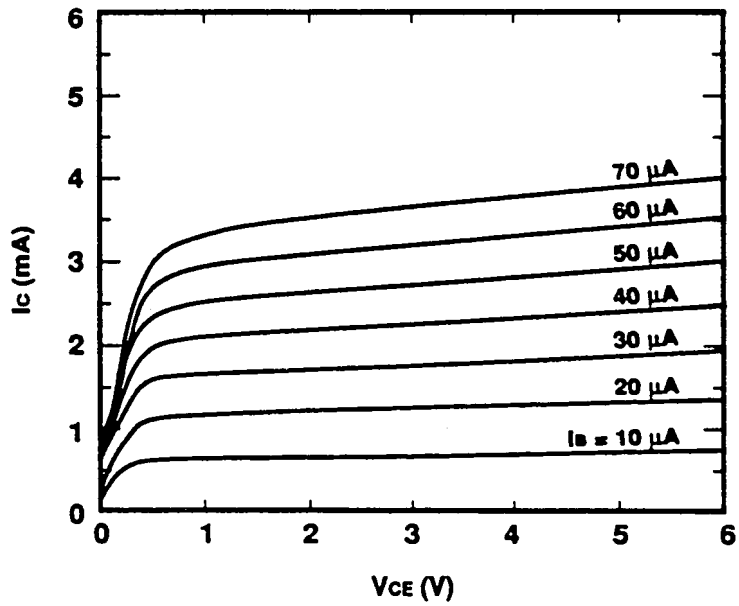


Typical Current Gain Characteristics (NV231A01)

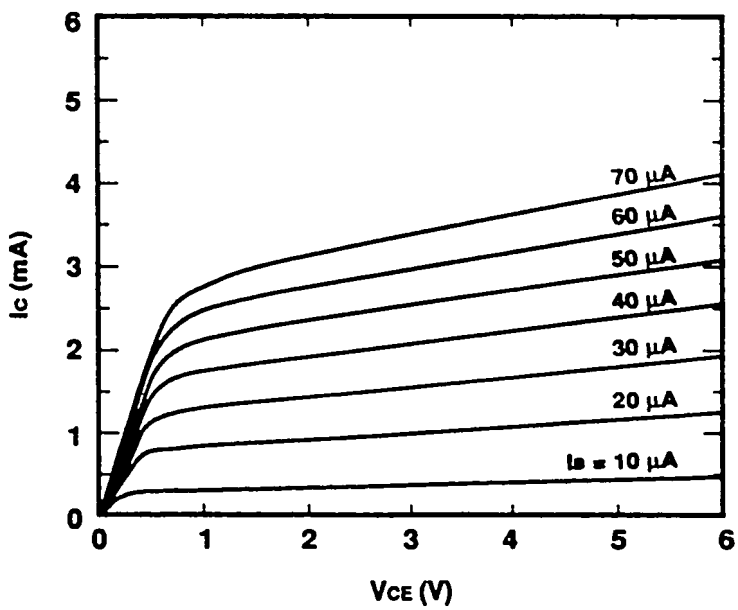


Typical Current Gain Characteristics (PV231A01)

Figure 45
Typical Current Gain Characteristics

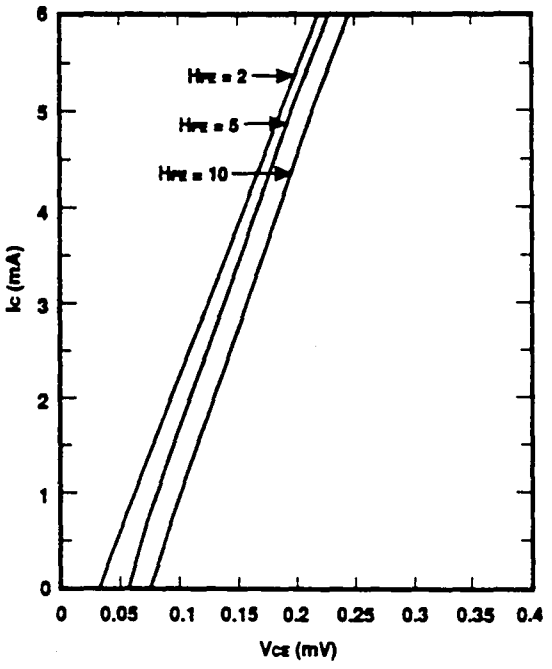


Typical Output Voltage Characteristics (NV231A01)

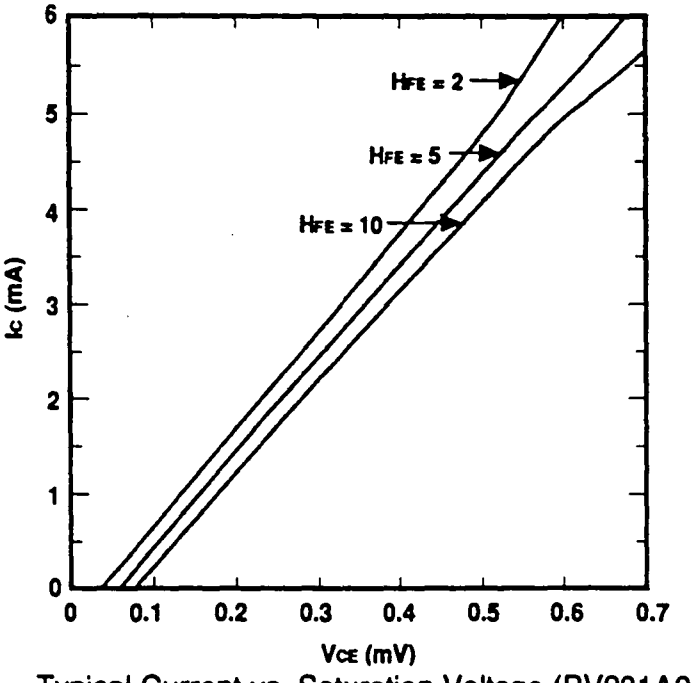


Typical Output Voltage Characteristics (PV231A01)

Figure 46
Typical Output Voltage Characteristics

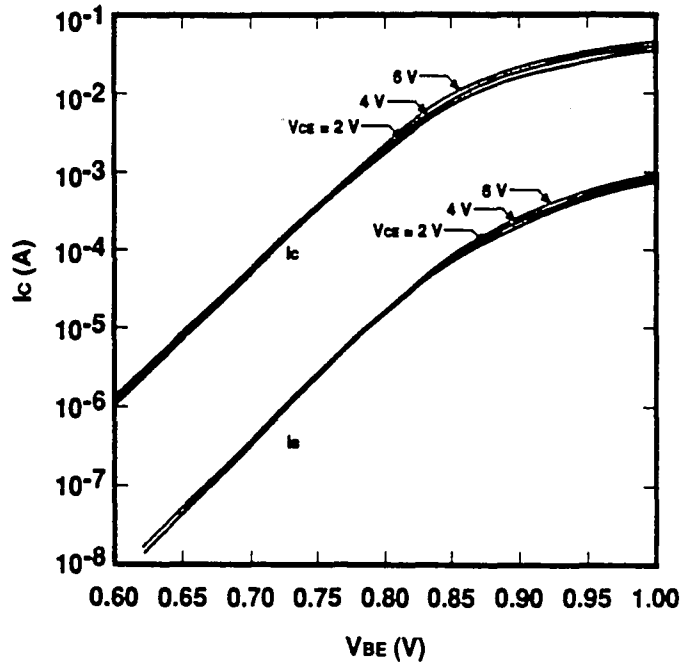


Typical Current vs. Saturation Voltage (NV231A01)

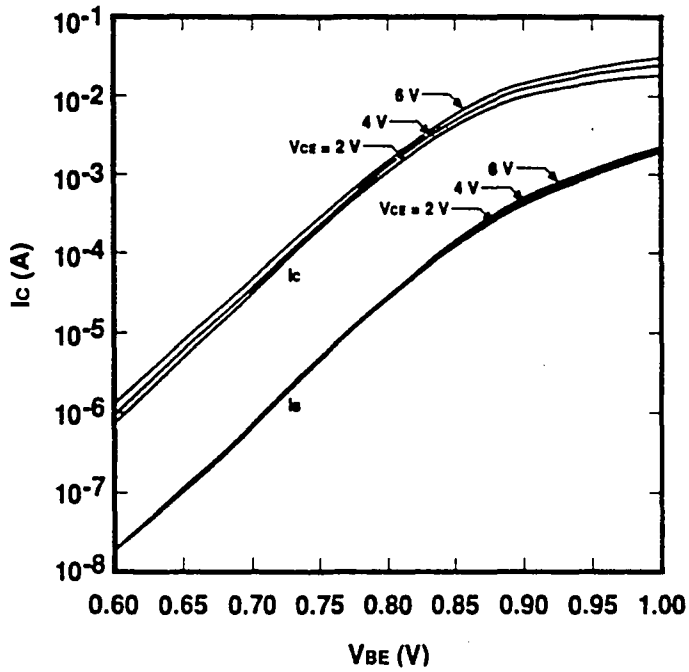


Typical Current vs. Saturation Voltage (PV231A01)

Figure 47
Typical Current vs. Saturation Voltage

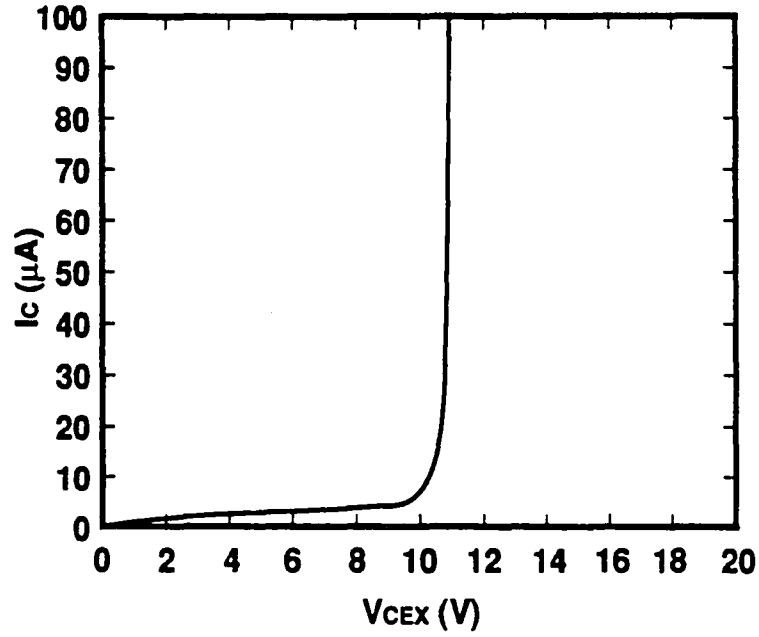


Typical Current vs. Voltage Characteristics (NV231A01)

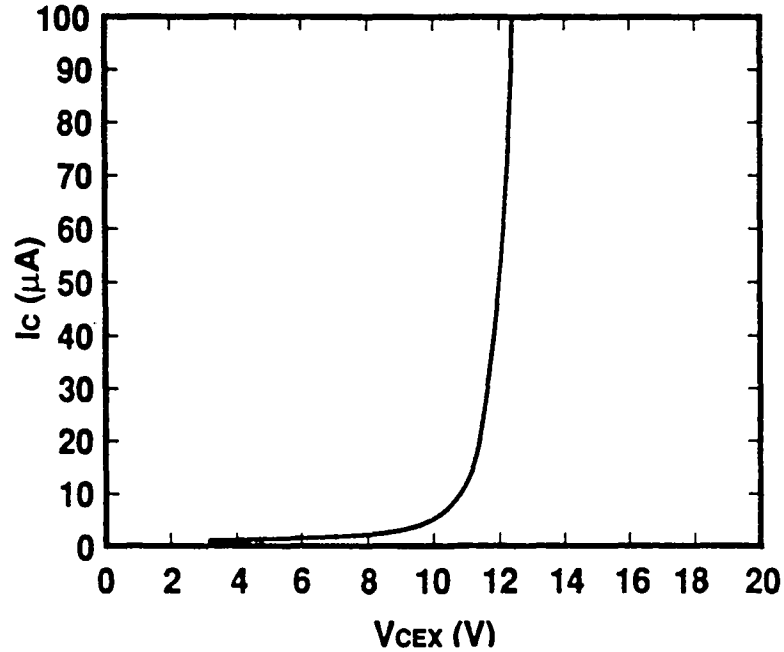


Typical Current vs. Voltage Characteristics (PV231A01)

Figure 48
Typical Current vs. Voltage Characteristics



Typical Collector Breakdown Characteristics (NV231A01)



Typical Collector Breakdown Characteristics (PV231A01)

Figure 49
Typical Collector Breakdown Characteristics

```
* TWO 1.5 BY 15 MICRON STRIPES - NOM
**                                                    JDJ/RDP 11/11/91
**
.MODEL NV231A01 USRMOD=NEB1 ; NPN NOM  MODEL
 + RBX = 2.500E+01  RBI = 2.783E+01  RCX = 1.967E+01  RCI = 4.427E+01
 + RE  = 1.945E+00  IS  = 1.420E-16  I1  = 5.800E-19  I2  = 5.108E-14
 + NE  = 2.000E+00  IK  = 9.714E-03  VBO = 1.320E+00  TFO = 3.900E-12
 + CJE = 1.200E-13  PE  = 8.000E-01  ME  = 4.950E-01  BE  = 1.000E-01
 + I3  = 1.502E-16  I4  = 6.444E-21  NC  = 1.847E+00  IKR = 8.172E-02
 + VAO = 7.901E+00  TRO = 4.000E-11  CJC = 6.670E-15  PC  = 6.701E-01
 + MC  = 4.509E-01  BC  = 1.000E-01  EA  = 1.184E+00  DEA = 6.825E-02
 + TO  = 2.500E+01  KFN = 0.000E+00  AFN = 1.000E+00  BFN = 1.000E+00
 + BVBC= 0.000E+00  ALC1= 2.000E+00  ALC2= 0.000E+00  ALTC= 7.500E-01
 + BVBE= 0.000E+00  ALE1= 2.000E+00  ALE2= 0.000E+00  ALTE= 7.500E-01
 + NID = 8.197E-12  QCO = 1.744E-14  VJCO= 9.055E-01  TRCI= 2.000E+00
 + TVCO= 1.680E+00  RBIP= 8.042E+01  I1P = 7.500E-20  I2P = 1.000E-14
 + NEP = 1.313E+00  IKP = 3.000E-03  CJEP= 7.183E-14  ISP = 1.285E-18
 + I3P = 9.069E-18  CJCP= 1.016E-13  PS  = 5.335E-01  MS  = 4.389E-01
 + BS  = 1.000E-01  MTQB= 1.103E+00  DEA2= 5.615E-02  XTIS= 2.000E+00
 + XTI1= 3.000E+00  XTI2= 2.500E+00  QCOX= 8.722E-14  NR  = 1.020E+00
 + NF  = 1.002E+00  NCR = 1.090E+00  NCRP= 1.000E+00  MVC1= 1.000E-01

 **
 **
* FOUR 1.5 BY 15 MICRON STRIPES - NOM
**                                                    JDJ/RDP 11/11/91
**
.MODEL NV431A01 USRMOD=NEB1 ; NPN NOM  MODEL
 + RBX = 1.250E+01  RBI = 1.391E+01  RCX = 3.002E+01  RCI = 2.213E+01
 + RE  = 9.725E-01  IS  = 2.840E-16  I1  = 1.160E-18  I2  = 1.022E-13
 + NE  = 2.000E+00  IK  = 1.943E-02  VBO = 1.320E+00  TFO = 3.900E-12
 + CJE = 2.400E-13  PE  = 8.000E-01  ME  = 4.950E-01  BE  = 1.000E-01
 + I3  = 3.004E-16  I4  = 1.289E-20  NC  = 1.847E+00  IKR = 1.634E-01
 + VAO = 7.901E+00  TRO = 4.000E-11  CJC = 1.334E-14  PC  = 6.701E-01
 + MC  = 4.509E-01  BC  = 1.000E-01  EA  = 1.184E+00  DEA = 6.825E-02
 + TO  = 2.500E+01  KFN = 0.000E+00  AFN = 1.000E+00  BFN = 1.000E+00
 + BVBC= 0.000E+00  ALC1= 2.000E+00  ALC2= 0.000E+00  ALTC= 7.500E-01
 + BVBE= 0.000E+00  ALE1= 2.000E+00  ALE2= 0.000E+00  ALTE= 7.500E-01
 + NID = 8.197E-12  QCO = 2.442E-14  VJCO= 9.055E-01  TRCI= 2.000E+00
 + TVCO= 1.680E+00  RBIP= 4.650E+01  I1P = 1.320E-19  I2P = 1.760E-14
 + NEP = 1.313E+00  IKP = 5.280E-03  CJEP= 1.242E-13  ISP = 2.019E-18
 + I3P = 1.596E-17  CJCP= 1.491E-13  PS  = 5.335E-01  MS  = 4.389E-01
 + BS  = 1.000E-01  MTQB= 1.103E+00  DEA2= 5.615E-02  XTIS= 2.000E+00
 + XTI1= 3.000E+00  XTI2= 2.500E+00  QCOX= 1.221E-13  NR  = 1.020E+00
 + NF  = 1.002E+00  NCR = 1.090E+00  NCRP= 1.000E+00  MVC1= 1.000E-01

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```
* SIX 1.5 BY 30 MICRON STRIPES - NOM
**                                                    JDJ/RDP 11/11/91
**
.MODEL NV663A01 USRMOD=NEB1 % NPN NOM  MODEL
 + RBX = 4.212E+00  RBI = 4.689E+00  RCX = 2.869E+00  RCI = 7.458E+00
 + RE  = 3.277E-01  IS  = 8.429E-16  I1  = 3.443E-18  I2  = 3.032E-13
 + NE  = 2.000E+00  IK  = 5.766E-02  VBO = 1.320E+00  TFO = 3.900E-12
 + CJE = 7.123E-13  PE  = 8.000E-01  ME  = 4.950E-01  BE  = 1.000E-01
 + I3  = 8.916E-16  I4  = 3.825E-20  NC  = 1.847E+00  IKR = 4.851E-01
 + VAO = 7.901E+00  TRO = 4.000E-11  CJC = 3.959E-14  PC  = 6.701E-01
 + MC  = 4.509E-01  BC  = 1.000E-01  EA  = 1.184E+00  DEA = 6.825E-02
 + TO  = 2.500E+01  KFN = 0.000E+00  AFN = 1.000E+00  BFN = 1.000E+00
 + BVBC= 0.000E+00  ALC1= 2.000E+00  ALC2= 0.000E+00  ALTC= 7.500E-01
 + BVBE= 0.000E+00  ALE1= 2.000E+00  ALE2= 0.000E+00  ALTE= 7.500E-01
 + NID = 8.197E-12  QCO = 4.709E-14  VJCO= 9.055E-01  TRCI= 2.000E+00
 + TVCO= 1.680E+00  RBIP= 1.708E+01  I1P = 3.636E-19  I2P = 4.848E-14
 + NEP = 1.313E+00  IKP = 1.454E-02  CJEP= 3.383E-13  ISP = 2.607E-18
 + I3P = 4.397E-17  CJCP= 3.879E-13  PS  = 5.335E-01  MS  = 4.389E-01
 + BS  = 1.000E-01  MTQB= 1.103E+00  DEA2= 5.615E-02  XTIS= 2.000E+00
 + XTI1= 3.000E+00  XTI2= 2.500E+00  QCOX= 2.355E-13  NR  = 1.020E+00
 + NF  = 1.002E+00  NCR = 1.090E+00  NCRP= 1.000E+00  MVC1= 1.000E-01

 **
 **
 **
* TWO 1.5 BY 15 MICRON STRIPES - NOM
**                                                    JDJ/RDP 11/19/91
**
.MODEL PV231A01 USRMOD=PEB1 % PNP NOM  MODEL
 + RBX = 1.447E+01  RBI = 1.933E+01  RCX = 9.156E+01  RCI = 9.067E+01
 + RE  = 1.276E+00  IS  = 1.051E-16  I1  = 7.800E-19  I2  = 2.676E-15
 + NE  = 1.459E+00  IK  = 8.847E-03  VBO = 8.500E-01  TFO = 4.500E-12
 + CJE = 1.200E-13  PE  = 7.351E-01  ME  = 4.930E-01  BE  = 8.922E-02
 + I3  = 1.700E-18  I4  = 7.541E-16  NC  = 1.700E+00  IKR = 1.000E-01
 + VAO = 2.958E+00  TRO = 1.500E-10  CJC = 1.068E-14  PC  = 7.771E-01
 + MC  = 5.000E-01  BC  = 1.000E-01  EA  = 1.184E+00  DEA = 6.825E-02
 + TO  = 2.500E+01  KFN = 0.000E+00  AFN = 1.000E+00  BFN = 1.000E+00
 + BVBC= 0.000E+00  ALC1= 2.000E+00  ALC2= 0.000E+00  ALTC= 7.500E-01
 + BVBE= 0.000E+00  ALE1= 2.000E+00  ALE2= 0.000E+00  ALTE= 7.500E-01
 + NID = 2.932E-12  QCO = 3.000E-14  VJCO= 1.498E+00  TRCI= 2.000E+00
 + TVCO= 1.680E+00  RBIP= 5.000E+01  I1P = 5.575E-18  I2P = 1.475E-15
 + NEP = 1.722E+00  IKP = 1.154E-02  CJEP= 1.149E-13  ISP = 7.525E-18
 + I3P = 5.000E-17  CJCP= 5.080E-13  PS  = 9.082E-01  MS  = 4.931E-01
 + BS  = 1.000E-01  MTQB= 1.050E+00  DEA2= 1.778E-01  XTIS= 2.000E+00
 + XTI1= 3.000E+00  XTI2= 2.200E+00  QCOX= 1.500E-13  NFP = 1.000E+00
 + NF  = 1.000E+00  NCR = 1.000E+00  NCRP= 1.000E+00  NR  = 1.000E+00

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* FOUR 1.5 BY 15 MICRON STRIPES - NOM
**                                                    JDJ/RDP 11/19/91
**
.MODEL PV432A01 USRMOD=PEB1 % PNP NOM  MODEL
 + RBX = 7.235E+00  RBI = 9.665E+00  RCX = 5.180E+01  RCI = 4.533E+01
 + RE  = 6.380E-01  IS  = 2.102E-16  I1  = 1.560E-18  I2  = 5.352E-15
 + NE  = 1.459E+00  IK  = 1.769E-02  VBO = 8.500E-01  TFO = 4.500E-12
 + CJE = 2.400E-13  PE  = 7.351E-01  ME  = 4.930E-01  BE  = 8.922E-02
 + I3  = 3.400E-18  I4  = 1.508E-15  NC  = 1.700E+00  IKR = 2.000E-01
 + VAO = 2.958E+00  TRO = 1.500E-10  CJC = 2.136E-14  PC  = 7.771E-01
 + MC  = 5.000E-01  BC  = 1.000E-01  EA  = 1.184E+00  DEA = 6.825E-02
 + TO  = 2.500E+01  KFN = 0.000E+00  AFN = 1.000E+00  BFN = 1.000E+00
 + BVBC= 0.000E+00  ALC1= 2.000E+00  ALC2= 0.000E+00  ALTC= 7.500E-01
 + BVBE= 0.000E+00  ALE1= 2.000E+00  ALE2= 0.000E+00  ALTE= 7.500E-01
 + NID = 2.932E-12  QCO = 3.923E-14  VJCO= 1.498E+00  TRCI= 2.000E+00
 + TVCO= 1.680E+00  RBIP= 2.891E+01  I1P = 9.812E-18  I2P = 2.596E-15
 + NEP = 1.722E+00  IKP = 2.031E-02  CJEP= 1.987E-13  ISP = 9.782E-18
 + I3P = 8.800E-17  CJCP= 8.300E-13  PS  = 9.082E-01  MS  = 4.931E-01
 + BS  = 1.000E-01  MTQB= 1.050E+00  DEA2= 1.778E-01  XTIS= 2.000E+00
 + XTI1= 3.000E+00  XTI2= 2.200E+00  QCOX= 1.962E-13  NFP = 1.000E+00
 + NF  = 1.000E+00  NCR = 1.000E+00  NCRP= 1.000E+00  NR  = 1.000E+00

 **
 **
* SIX 1.5 BY 45 MICRON STRIPES - NOM
**                                                    JDJ/RDP 11/19/91
**
.MODEL PV693A01 USRMOD=PEB1 % PNP NOM  MODEL
 + RBX = 1.631E+00  RBI = 2.179E+00  RCX = 1.095E+01  RCI = 1.022E+01
 + RE  = 1.438E-01  IS  = 9.324E-16  I1  = 6.920E-18  I2  = 2.374E-14
 + NE  = 1.459E+00  IK  = 7.849E-02  VBO = 8.500E-01  TFO = 4.500E-12
 + CJE = 1.065E-12  PE  = 7.351E-01  ME  = 4.930E-01  BE  = 8.922E-02
 + I3  = 1.508E-17  I4  = 6.690E-15  NC  = 1.700E+00  IKR = 8.872E-01
 + VAO = 2.958E+00  TRO = 1.500E-10  CJC = 9.475E-14  PC  = 7.771E-01
 + MC  = 5.000E-01  BC  = 1.000E-01  EA  = 1.184E+00  DEA = 6.825E-02
 + TO  = 2.500E+01  KFN = 0.000E+00  AFN = 1.000E+00  BFN = 1.000E+00
 + BVBC= 0.000E+00  ALC1= 2.000E+00  ALC2= 0.000E+00  ALTC= 7.500E-01
 + BVBE= 0.000E+00  ALE1= 2.000E+00  ALE2= 0.000E+00  ALTE= 7.500E-01
 + NID = 2.932E-12  QCO = 7.615E-14  VJCO= 1.498E+00  TRCI= 2.000E+00
 + TVCO= 1.680E+00  RBIP= 7.474E+00  I1P = 3.867E-17  I2P = 1.023E-14
 + NEP = 1.722E+00  IKP = 8.004E-02  CJEP= 7.687E-13  ISP = 1.526E-17
 + I3P = 3.468E-16  CJCP= 2.530E-12  PS  = 9.082E-01  MS  = 4.931E-01
 + BS  = 1.000E-01  MTQB= 1.050E+00  DEA2= 1.778E-01  XTIS= 2.000E+00
 + XTI1= 3.000E+00  XTI2= 2.200E+00  QCOX= 3.808E-13  NFP = 1.000E+00
 + NF  = 1.000E+00  NCR = 1.000E+00  NCRP= 1.000E+00  NR  = 1.000E+00

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VITA

John William Pierdomenico was born August 3, 1965 to E. Vincent and N. Louise (Thompson) Pierdomenico in Chester Pennsylvania. He attended Sun Valley High School and Pennsylvania State University where he received his B.S. in Electrical Engineering in 1988. He attended Lehigh University where he received his M.S. in Electrical Engineering in 1992. He currently works for AT&T Microelectronics in Reading, PA where he is an Analog Circuit Designer. Previously he was a Testing Engineer for AT&T.

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