Name proyect: Proyecto0

Autor: Santiago Rodriguez

Email: santiagtms@gmail.com

Date reales: 7 ene. 2025

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4	USB, USB-TO-AURT converter
5	Flash Memory
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BOARD DESCRIPTION

Based on ARTIX 7 FPGA.

Supplied via USB or a dedicated port.

FPGA Programmed via USB.

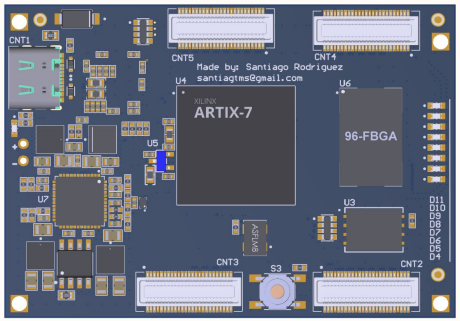
4 ports for external connectios.

Button for reset and 8 leds for user interface.

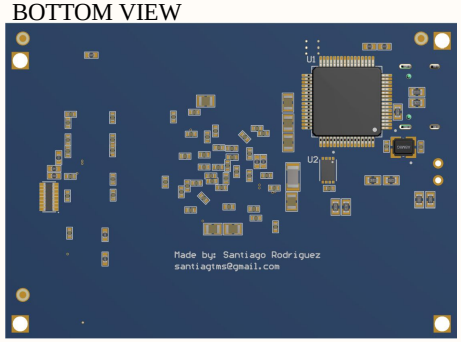
256Mx16bit (4 Gb) DDR3L Synchronous DRAM (SDRAM).

100 MHz clock (FPGA can synthetize new frequencies)

TOP VIEW



BOTTOM VIEW



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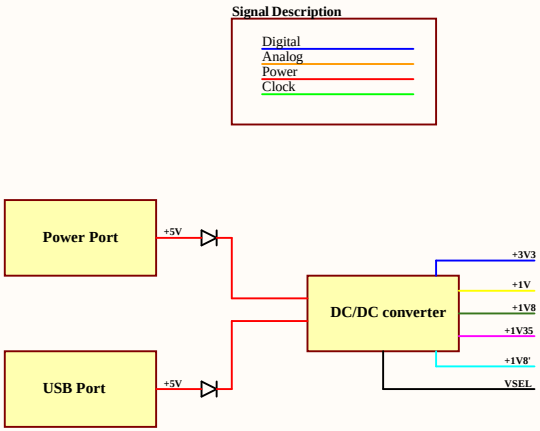
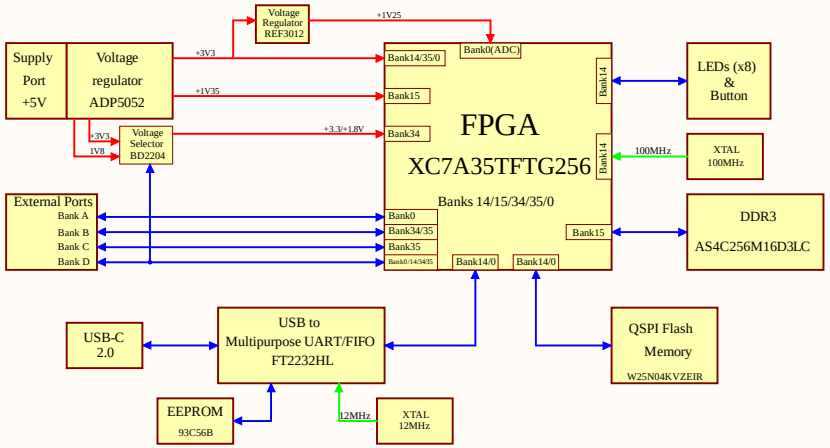
BLOCK DIAGRAM





U_TOP_Sheet
TOP_Sheet.SchDoc

Fiducial Marks

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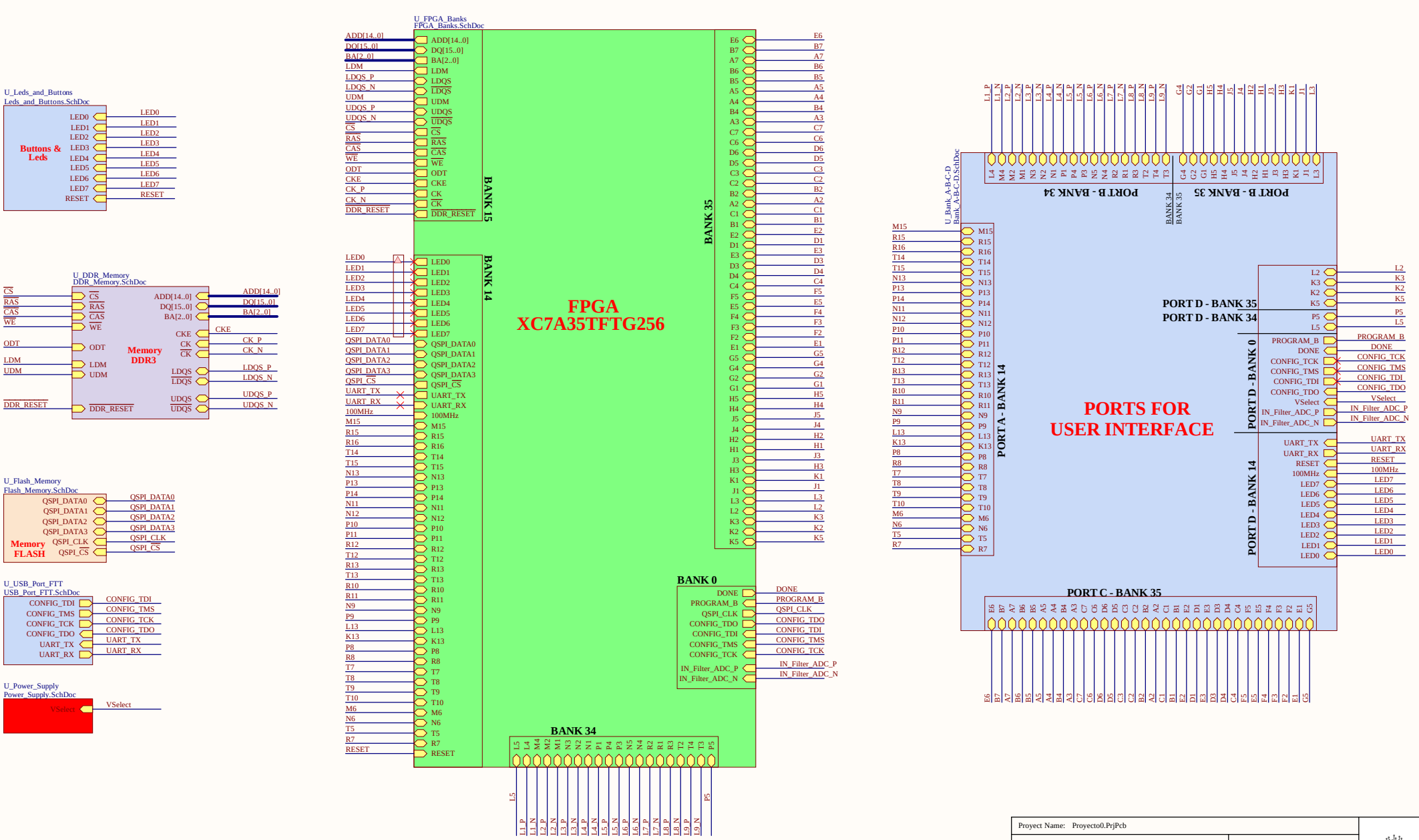

Proyect Name:	Proyecto0.PrjPcb		
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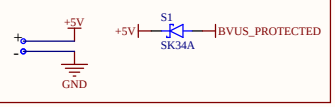
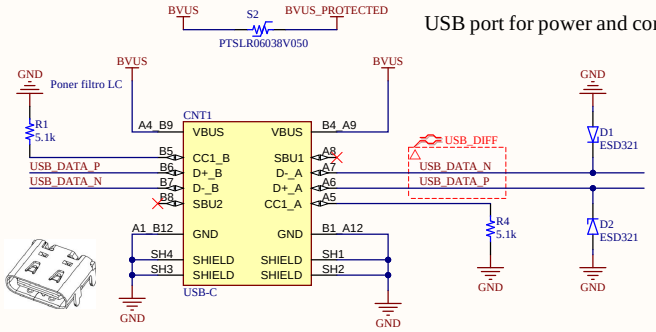
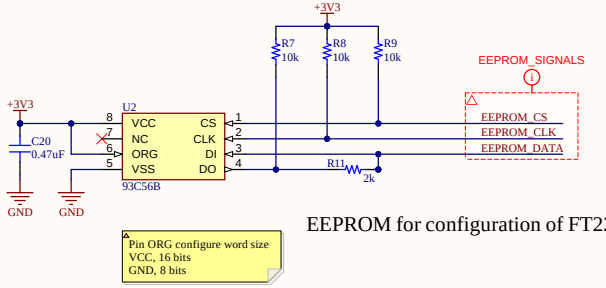
USB PORT

Holes on PCB for +5V external power supply





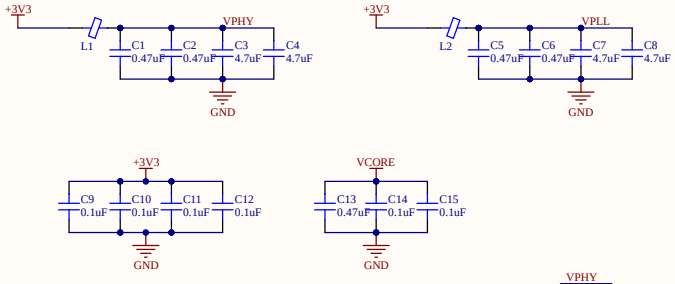
USB port for power and configuration

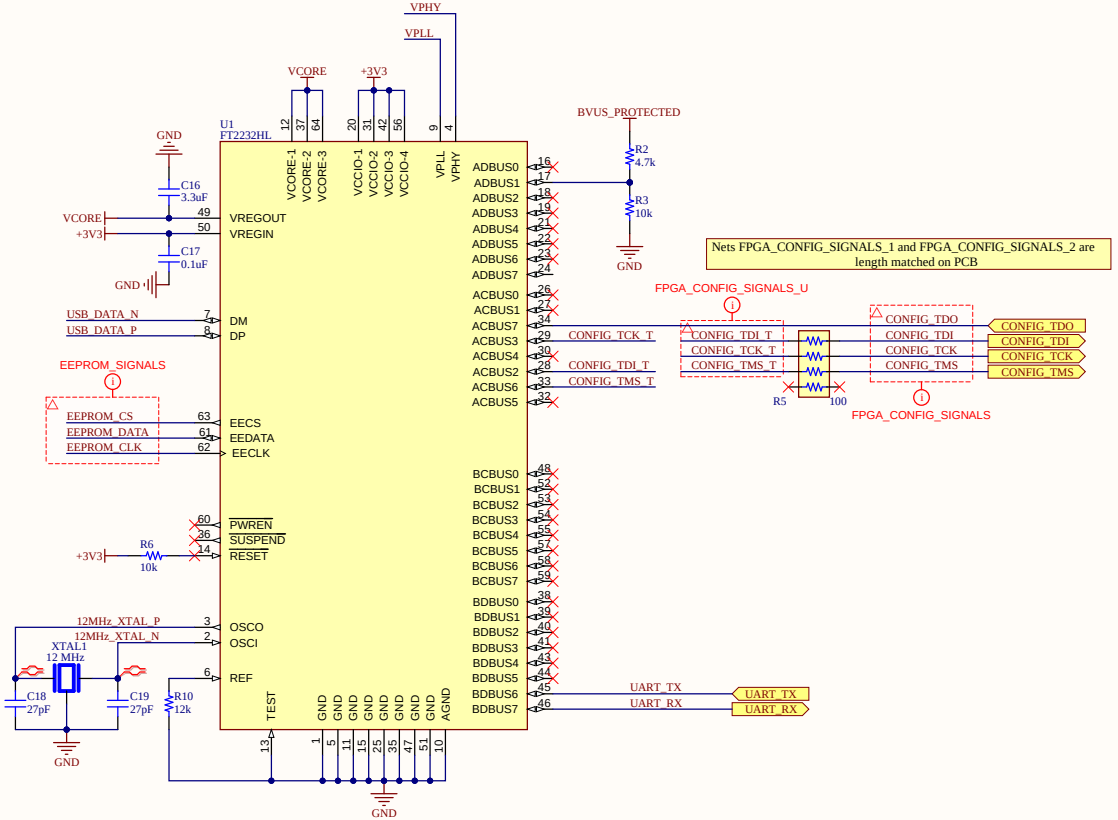


EEPROM for configuration of FT2232HL

Pin ORG configure word size
VCC, 16 bits
GND, 8 bits

USB TO MULTIPURPOSE UART/FIFO





Nets FPGA_CONFIG_SIGNALS_1 and FPGA_CONFIG_SIGNALS_2 are length matched on PCB

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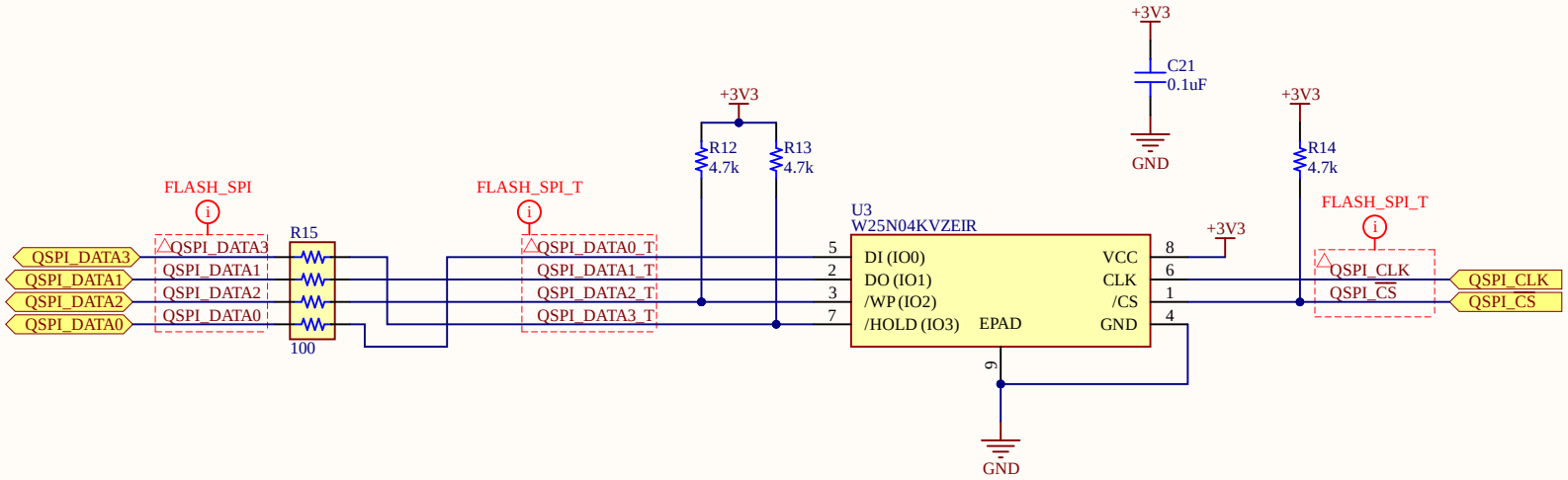
FLASH MEMORY



Proyect Name:	Proyecto0.PrjPcb		
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FPGA BANKS

BANK_0 (Configuration)

BANK_0 (ADC)

BANK_35

Used for DIF GPIO

BANK_14

Used for config. and GPIO

BANK_34

Used for GPIO

3.3V Supply, switched to 1.8V for LVDS

BANK_15

Used for DDR memory

Nets FLASH_SPI_T and FLASH_SPI are length matched on PCB, not by rules.

A 0.47uF decoupling capacitor (C20) is removed for PCB space reasons.

A 0.47uF (C45) and 4.7uF (C49) decoupling capacitor are removed for PCB space reasons.

Temperature sensor not used

Ferrite for ADC supply filtering

Ferrite for ADC_ground isolation from GND

LDO for ADC supply

Antia-alias ADC filter calculation

External Clock: 100 MHz (Max 250 MHz).
ADC_clock: 25 MHz (Max 26 MHz) [Prescaler: 4].
Tiempo de adquisición y conversión: 26 ciclos de ADC_clock.
Tiempo de Adquisición: 16 a 22 ciclos, se configura para 22 ciclos ADC_clock.
Conversión: 22 ciclos ADC_clock

T_adc_clock = 1 / 25 MHz = 40 nS
T_adquisicion = 40 nS * 22 = 880 nS

Para lograr un error menora 1/16 LSB, el total de constantes de tiempo necesaria tiene que ser menor a 880 nS

Error: 1/16 LSB ADC: 12 bits
880 nS = 11.10 * R * C
[C = 1 nF]
R = 80 ohms.
[R must be < 80 ohms]

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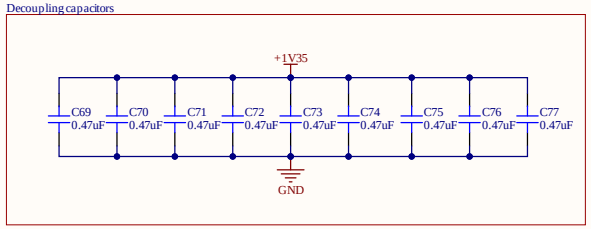
DDR3 MEMORY



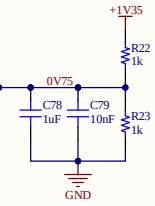


Table 1. DDR Signal Groupings for Routing Purposes

Group	Signal Name	Description	Section
Clocks	MCK[0:5]	DDR differential clock outputs	See Section 7.1, "Clock Signal Group MCK[0:5] and MCK[0:5]"
	$\overline{MCK}$[0:5]	DDR differential clock outputs (complement)	
Data	MDQ[0:63]	64-bit data bus	See Section 7.2, "Data—MDQ[0:63], MDQS[0:8], MDM[0:8], MECC[0:7]"
	MECC[0:7]	ECC pins	
	MDM[0:8]	Data mask pins	
	MDQS[0:8]	Data strobe pins	
Address/Command	MA[0:14]	Address bus	See Section 7.3, "Address and Command Signal Group"
	MBA[0:1]	Bank address	
	$\overline{MRAS}$	Row address strobe	
	$\overline{MCAS}$	Column address strobe	
	$\overline{MWE}$	Write enable	
Control	MCKE[0:1]	Clock enable	See Section 7.4, "Control Signal Group"
	$\overline{MCS}$[0:3]	Chip selects	
Feedback	MSYNC_OUT	DRAM DLL synchronization output	See Section 7.5, "Feedback Signal Group"
	MSYNC_IN	DRAM DLL synchronization input	
Power	V_{REF}	Voltage reference for differential receivers	See Section 7.6, "DDR Power Delivery"
	V_{TT}	Termination voltage	

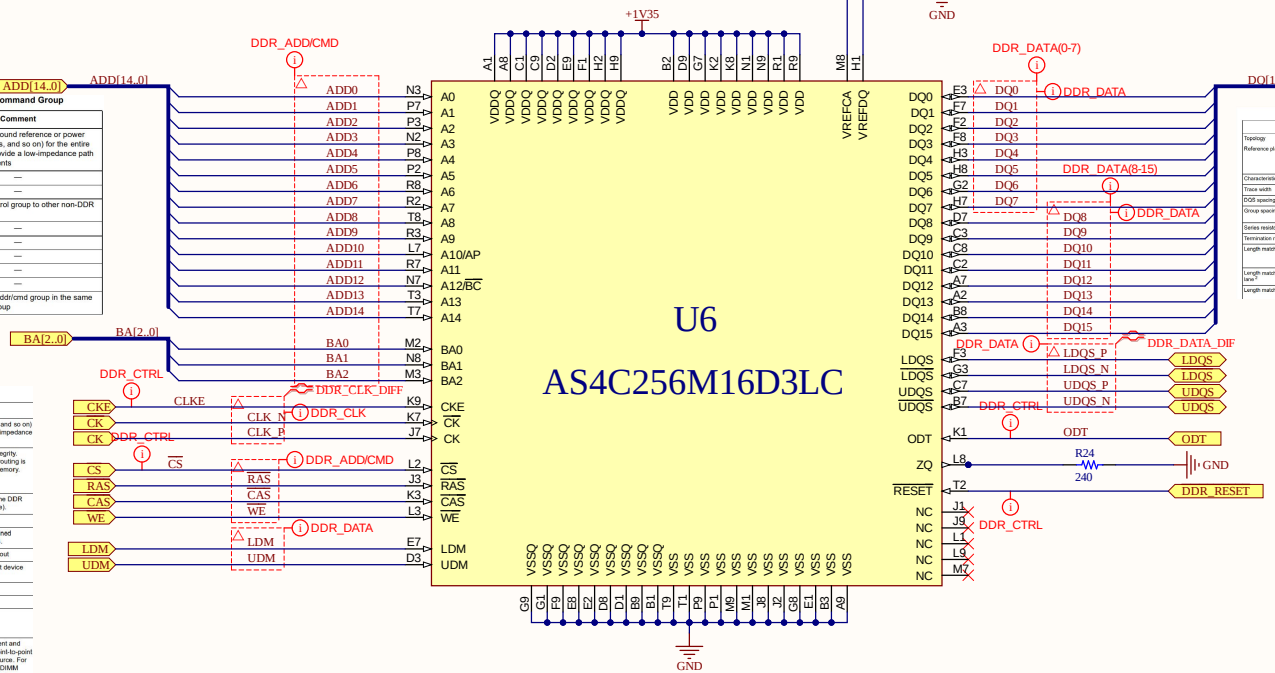


Table 6. General Routing Recommendations for the DDR Address and Command Group

Item	Recommendation	Comment
Reference plane	Ground-referenced or power-referenced	Maintain a solid ground reference or power reference (no splits, and so on) for the entire signal group to provide a low-impedance path for the return currents
Characteristic impedance [1]	= 50 – 60 Ω	—
Trace width	Implementation-specific	—
Group spacing	20 mils	Isolation from control group to other non-DDR signals
Length matching (with respect to clock)	Min <= Addr/Cmd Group <= Max	—
Minimum Addr/Cmd group length [2]	Max clock length – 'Y'	—
Maximum Addr/Cmd group length [2]	Minimum clock length – 'Y' inches	—
Series resistor [1]	0–33 Ω ± 5%	—
Termination resistor [1]	25–57 Ω ± 5%	—
Resistor packs	Use as needed	Do not place the addr/cmd group in the same RN as the data group

Table 3. General Layout Recommendations for the DDR Clock Group

Item	Recommendation	Comment
Reference plane	Ground-referenced	Maintain a solid ground reference (no splits and so on) for all routed clocks, thereby providing a low-impedance path for the return currents.
Same layer routing	Route all clock pairs on the same critical layer. Avoid switching between layers except where required. See Figure 5 and Figure 6.	Ensures all clocks have the same signal integrity. Swap clock pairs as needed so that signal routing is optimized between the controller and the memory.
Characteristic impedance	= 50–60 Ω single-ended = 100–120 Ω differential	All pairs must be routed differentially from the DDR controller to the end point (DIMM or discrete).
Trace width	Implementation-specific	—
Differential spacing	Implementation-specific	Correct differential spacing must be maintained throughout entire signal route. See Figure 4.
Pair-to-pair spacing	20 mils	Exceptions may be needed at device breakout
Group spacing (clocks to all other signals)	20 mils to any other signal	See Figure 4. Exceptions may be needed at device breakout.
Serpentine isolation spacing	Maintain at least 20 mils	See Figure 4
MCK to $\overline{MCK}$ trace matching	Matched to within 20 mils	—
Clock pair-to-clock pair matching	All clock pairs to a given memory bank (DIMM or discrete) matched to within 20 mils	—
Series damping resistor value	Range 15–33	Optimal value and location system dependent and should be determined by simulations. For point-to-point connections, placement is optimal at the source. For point-to-multipoint, placement at the loads (DIMM connector or discrete bank) may prove optimal.
Optional–parallel termination to V_{TT} [1]	25–57 Ω ± 1%	Considered to be an optional item based on internal simulation runs and application notes published by Micron (see Section 14, "Useful References").
Use of resistor networks for damping resistor	Not recommended	—

Table 5. General Routing Recommendations for the DDR Data Signal Group

Item	Recommendation	Comment
Topology	Daisy chain	
Reference plane	Ground-referenced	Maintain a solid ground reference (no splits and so on) for all routed clocks, thereby providing a low-impedance path for the return currents
Characteristic impedance [1]	50–60 Ω	—
Trace width	Implementation-specific	—
DQS spacing	4 W minimum	—
Group spacing	20 mils of isolation from other non-DDR related signals	—
Series resistor [1]	0–33 Ω ± 5%	—
Termination resistor [1]	25–57 Ω ± 5%	—
Length matching within the byte lane	±25 mils from the data strobe	Allows max interface speeds. See Section 7.2.2, "Data Group Matching Requirements"
Length matching byte lane to byte lane [2]	No more than 1 inch delta between all groups	See also Section 10.3.1, "Meeting the 75%–125% Write Data JEDEC Window"
Length matching DQS to clock	See Section 10.3.1, "Meeting the 75%–125% Write Data JEDEC Window"	See Section 10.3.1, "Meeting the 75%–125% Write Data JEDEC Window"

Table 7. General Routing Recommendations for the DDR Control Group

Item	Recommendation	Comment
Reference plane	Ground-referenced or power-referenced	Maintain a solid ground reference or power reference (no splits and so on.) for the entire signal group thereby providing a low-impedance path for the return currents
Characteristic impedance [1]	= 50–60 Ω	—
Trace width	Implementation-specific	—
Group spacing	20 mils	Isolation from control group to other non-DDR signals
Length matching (with respect to clock)	Min <= control group <= Max	—
Minimum control group length [2]	Max clock length—'Z'	—
Maximum control group length [2]	Minimum clock length—'Z' inches	—
Series resistor [1]	0–33 Ω ± 5%	—
Termination resistor [1]	25–57 Ω ± 5%	—
Resistor packs	Use as needed	Do not place the control signals in the same RN as the data group

1. Power (V_{TT} island with termination resistors, V_{REF})
2. Pin swapping within resistor networks
3. Route data
4. Route address/command
5. Route control
6. Route clocks
7. Route feedback

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DC/DC CONVERTER

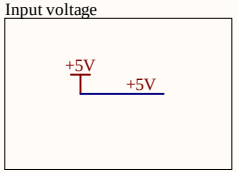
Vin = 5 V

Vou1 (CH1, BUCK) = +3V3 / 4A(max)
Vou2 (CH2, BUCK) = +1V / 2.63A(max)
Vou3 (CH3, BUCK) = +1V8 / 1A2(max)
Vou4 (CH4, BUCK) = +1V35 / 1A2(max)
Vou5 (CH5, LDO) = +1V8 / 200mA(max)

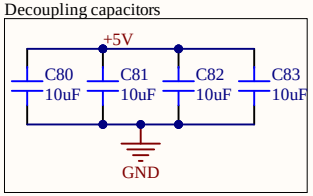
Secuencia de encendido:
CH2 (+1V) -> CH3 (+1V8) -> CH4 (+1V35) -> CH5 (+1V8') y CH1 (+3V3)

Configuration of ADP5052:
-CH1, Iout limited to 4.4 A
-CH2, Iout limited to 2.62A
-Switching Frequeny 600 KHz
-Operation Mode: forced PWM (FPWM) mode
-Soft Start CH1/2: 8 mS
-Soft Start CH3/4: 2 mS

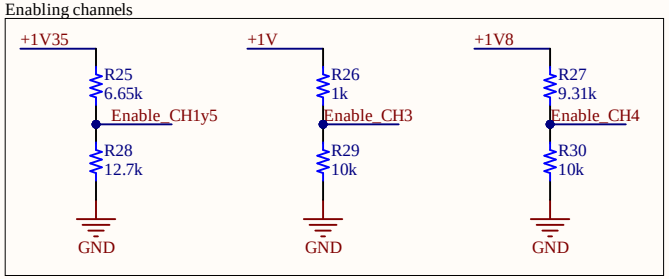
Input voltage



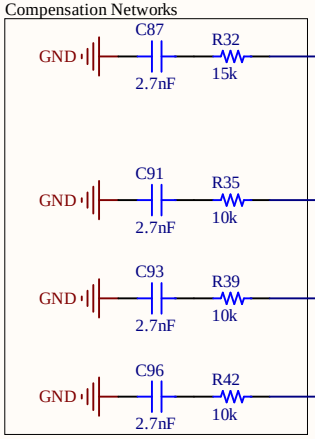
Decoupling capacitors



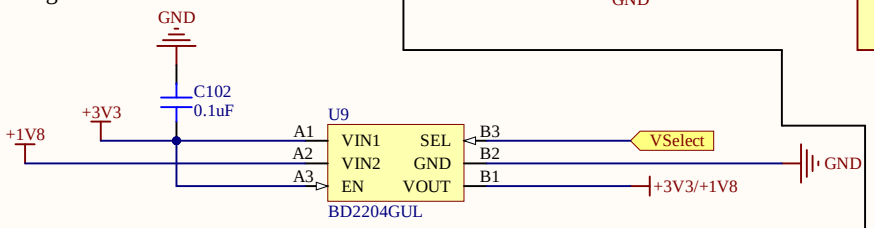
Enabling channels



Compensation Networks



Voltage selector



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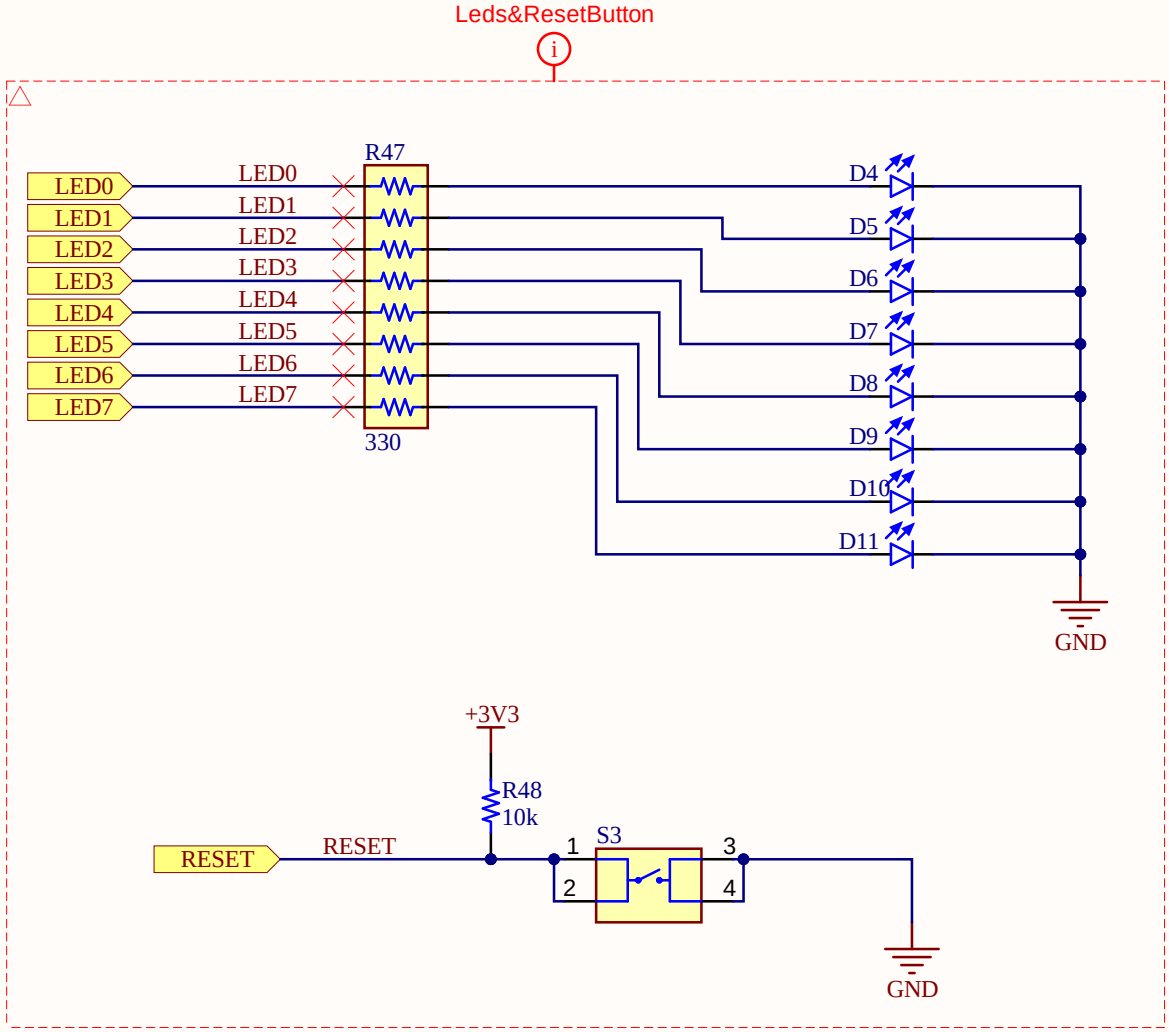
LEDS & BUTTON



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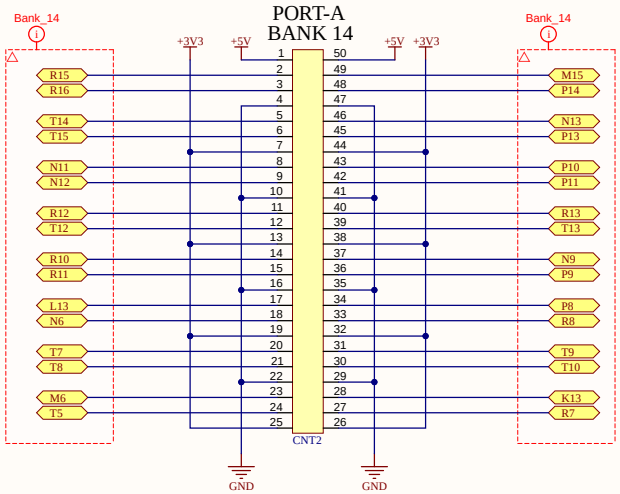
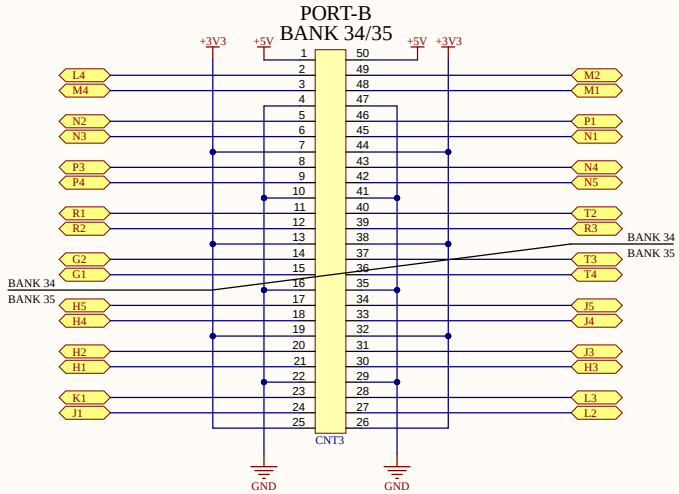
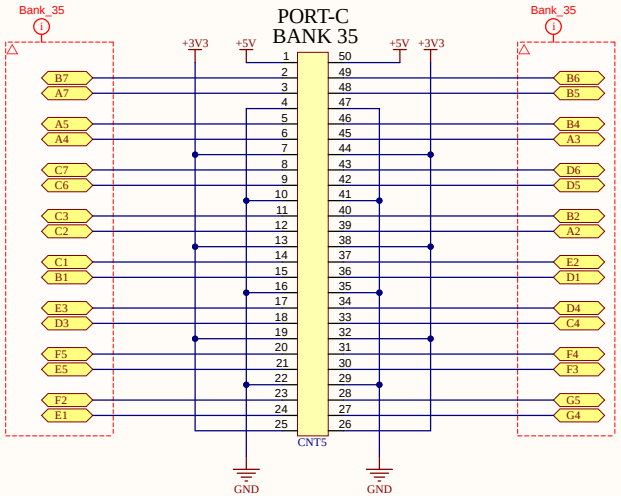
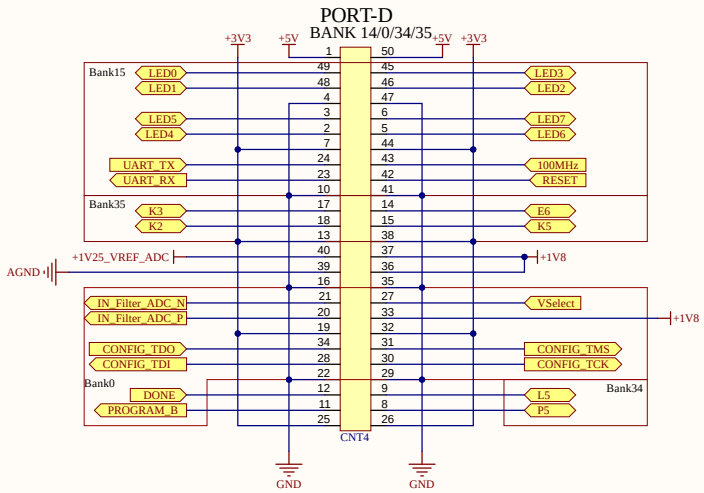
EXTERNAL PORTS









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