Recent Advancements in Thyristor Developments for HVDC Applications

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Recent Advancements in Thyristor Developments for HVDC Applications

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Abstract

This paper presents recent advancements made in large-area high-voltage bipolar thyristor technology, particularly with respect to improvements in device performance and reliability for high voltage direct current (HVDC) power transmission applications.

In order to meet global market trends for more efficient transmission of power, at ever increasing line voltages, much attention has been focused in the literature on ultra-high voltage series connected asymmetric thyristors (ASCRs) and diodes as a possible more 'cost-effective' solution[1] than the use of symmetric phase controlled thyristors (PCTs). Details are discussed on the design, process development and fabrication of 12-14 kV ASCRs/diodes in preparation for a full performance evaluation and comparison with PCT technology under HVDC operating conditions.

Also presented is the development and realisation of a PCT fabrication technology fully optimised for use in HVDC applications. In future it is anticipated this device will demonstrate 'best-in-class' electrical and reliability performance, with low temperature bonding being the key 'enabling' technology to deliver the enhanced performance expectations.

1. Introduction

Industrial thyristors are commercially available at voltage ratings up to 8.5 kV, and diameters of 125 mm. However, the highest voltage and power switching devices are reserved for HVDC power transmission where they are series connected to form converter/inverter switches operating at the desired transmitting voltage (e.g. ± 800 kV). Interestingly, the silicon bipolar PCT still remains the device of first-choice for this application, exhibiting lowest energy losses, an ability to withstand a number of critical associated electrical fault conditions, a history of proven reliability, and a competitive product selling price.

At present, long distance HVDC is a rapidly expanding area of business in growing economic regions. Leading global markets in China and India are demanding increases in power transmission and efficiency, together with system life expectations of 40 years. The manufacturers of PCTs are therefore presented with great financial incentive to deliver improved device performance and/or technologies to provide the system supplier with an advantage in the transmission market place.

Given this background, a fully optimised HVDC PCT has been designed and fabricated at Dynex Semiconductor. The details of this 125 mm, 8.5 kV thyristor technology demonstrators are presented in this paper.

For a given transmission line voltage, reducing the number of devices connected in series is another possibility to reduce system capital and/or operating costs. This approach obviously

requires devices with voltage ratings as high as possible. Unfortunately, it is well known that as PCT voltage increases their dynamic performance decreases as a consequence of silicon thickness. Indeed, much above 8.5 kV, energy losses and inrush current performance become unacceptable for HVDC.

To solve this problem, the use of ultra-high voltage asymmetric thyristors (ASCRs) and series connected diodes has been proposed in the literature[2]. ASCRs are significantly thinner than equivalent voltage rated PCTs and would therefore be expected to exhibit improved dynamic characteristics (the diodes would provide reverse blocking capability). For example a 14 kV ASCR would have approximately the same thickness as an 8.5 kV PCT.

This paper provides details of the device design and fabrication processes that have been developed in order to manufacture ASCRs and diodes at a target voltage rating of 12-14 kV, prior to a full evaluation of the technique under HVDC conditions. The need to choose gas doped float zone (FZ) material rather than neutron transmutation doped (NTD) silicon is also discussed.

2. Realisation of a Fully Optimised PCT HVDC Thyristor

For any power semiconductor device, a key parameter in design optimisation design is the choice of junction edge termination profile. Fig 1 shows the use of a double-positive bevel geometry not only reduces off-state surface electric fields, but also forces the avalanche breakdown voltage to occur uniformly across the semiconductor bulk.

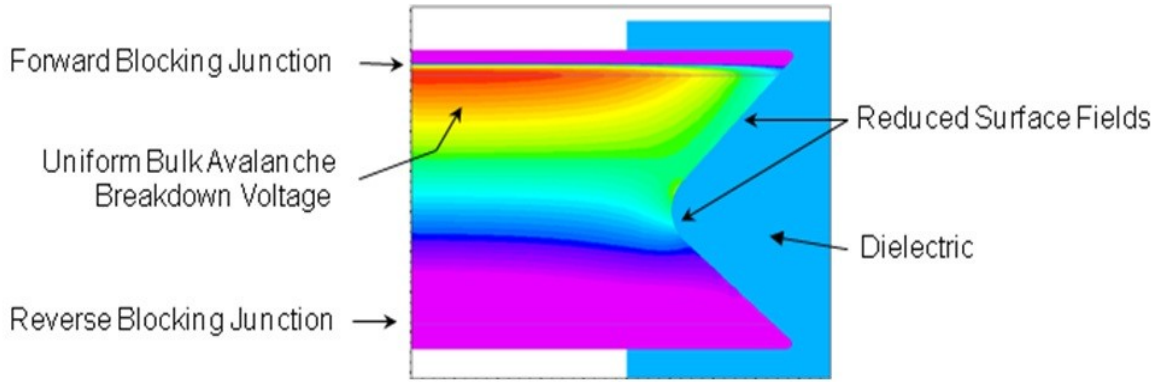

Fig 1 – Pressure contact double-positive bevel during 8.5 kV off-state blocking voltage

When this bevel is combined with the so called *i²* implant diffusion technology [3] the full performance capability of the silicon is achieved. For a given line voltage, minimum silicon resistivity and thickness can be specified, enabling device dynamic operating energy losses to be optimised - most important when considering financial savings for giga-watt HVDC transmission systems operating over 40 years.

Fig 2(a) is an exploded view of a 125 mm, 8.5 kV pressure contact PCT assembly, where the silicon chip is seen with its distinctive cathode gating pattern. Molybdenum or tungsten discs/washers are placed adjacent to the silicon to act as protective strain buffers during operational thermal cycling. Without this physical protection, the brittle silicon becomes prone to early failure due to its mis-match in thermal expansion coefficient with the different materials present, primarily copper.

Although pressure contact devices are ultimately clamped with substantial force to make electrical and thermal contact with external circuitry and heatsinks (e.g. 135 kN for a 125 mm

diameter PCT), the internal assembly components are not in perfect contact. Microscopically, the surfaces only make intimate contact at localised points and/or in small areas.

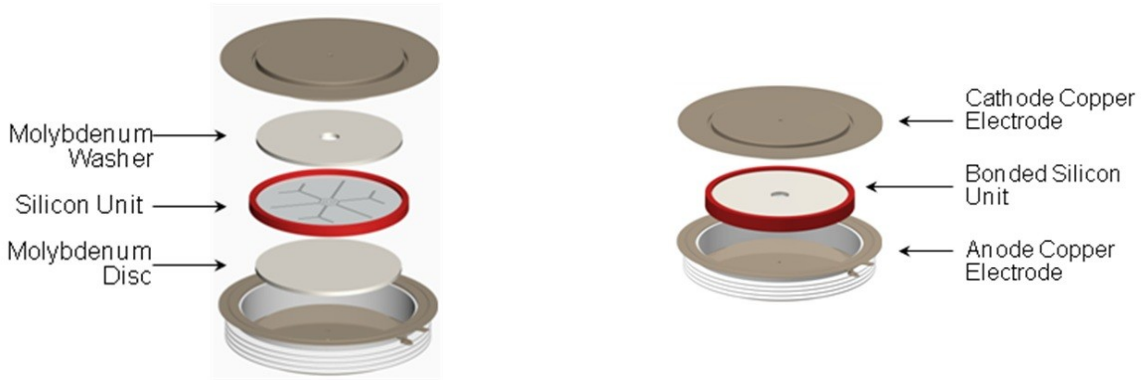

Fig 2 – 125mm, 8.5 kV PCT assembly for (a) pressure contact (b) bonded silicon technology

In contrast, Fig 2(b) is a concept assembly for the same PCT, but now the silicon unit has been bonded in 'perfect fashion' to both strain buffers, thus removing the immediate thermally resistive interfaces. As we shall see, these strain buffers actually extend radially to include the bevel region. The effect this bonding configuration has on HVDC operation is most significant, and has been quantified by 3D finite element simulation.

First though, it is important to understand that in an HVDC system, the PCT must demonstrate it can survive a number of worse case defined multi-cycle surge current fault conditions. Destruction is usually the consequence of joule heating over-temperature, hence the interest in improving non-perfect thermally resistive interfaces.

For the 125 mm, 8.5 kV PCT demonstrator simulations, thermal resistance measurements were made on a variety of pressure contact devices, from which the silicon to molybdenum interface heat transfer coefficient was estimated to be 150 kW/^{o}C-m^{2}. At this stage, a perfect join was assumed for the bonded interface.

Fig 3 compares the simulated thermal response for the two contact technologies during a typical 60 ms, 3-cycle 40 kA HVDC current surge. As can be seen, the silicon bulk and bevel regions run considerably cooler for the bonded case. This advantage can be utilised in differing ways. Either the device surge current rating can be increased (by an estimated 15% for this PCT) which can have a positive influence on the cost of expensive circuit transformers. Or, if surge levels remain constant, there is increased life survival expectancy due to the greater safety margins present.

There is a further advantage gained by bonding the double-positive bevel. In Fig 4(a) equipotential contours are plotted for the 125 mm PCT under an 8.3 kV forward voltage blocking condition. The potential lines wrap themselves around the bevel shoulder in the passivation layer creating a locally high dielectric field. However, once bonded these potentials follow the molybdenum surface as shown in Fig 4(b) which reduces this local field by an estimated 50%, as presented in Fig 4(c). Although the double-positive bevel has an excellent reliability record in the field, the impact of this design is seen as one of producing ultra-reliability.

At this stage we have seen how the concept PCT has enabled optimised electrical and thermal performance to be attained, essential to HVDC applications. The practical realisation of a double-side bonded device is now described.

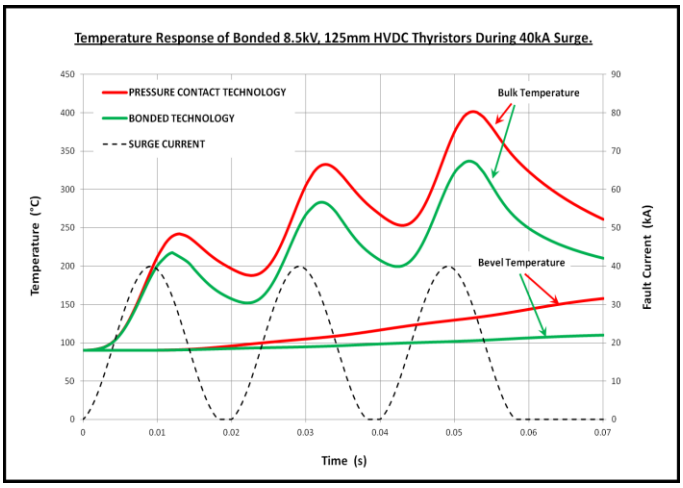

Fig 3 - Thermal advantages of double-side bonding for a 60 ms, 40 kA multi-cycle fault current condition.

For device diameters of 10-15 mm or larger, double-side bonding using traditional high temperature alloying (>570°C) causes destructive cleaving of the silicon due to the high tensile stresses created by the mis-match of material expansion coefficients during cooling from the freeze state. Hence, the need for a considerably lower temperature bonding technology, namely nano-silver sintering.

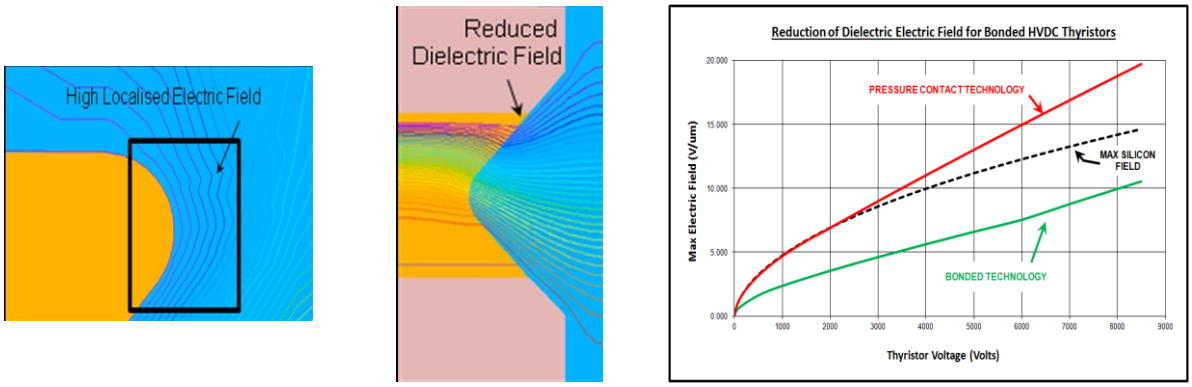

Fig 4 - (a) Potentials at bevel shoulder, (b) modified potentials at bonded bevel shoulder, (c) graph showing 50% reduction in dielectric electric field for bonded case

Fig 5(a) shows a successfully bonded 125 mm, 8.5 kV PCT, where nano-silver sintering technology has been used for bonding performed at compressive pressures between 4-8 MPa and temperatures less than 250°C. Specific to double-side bonding is the need to define the nano-silver layer on the thyristor cathode surface in order to avoid bonding the gating pattern. Indeed, Fig 5(b) shows successful definition of the nano-silver around the gate pattern prior to bonding.

After the bonding has been completed, high precision edge grinding equipment developed specifically for this purpose is used to form the double positive bevel profile with slight chamfering of the molybdenum as previously seen. A typical profile and ground finish is shown in Fig 6, though it still remains to optimise the process for future production purposes.

Finally, the thickness of the molybdenum components have been minimised by calculating a value which only just absorbs the full heat energy generated in the silicon during the worse

case 60 ms surge condition. High energy electron irradiation easily penetrates this thickness of molybdenum and is used to fine control final device energy loss characteristics.

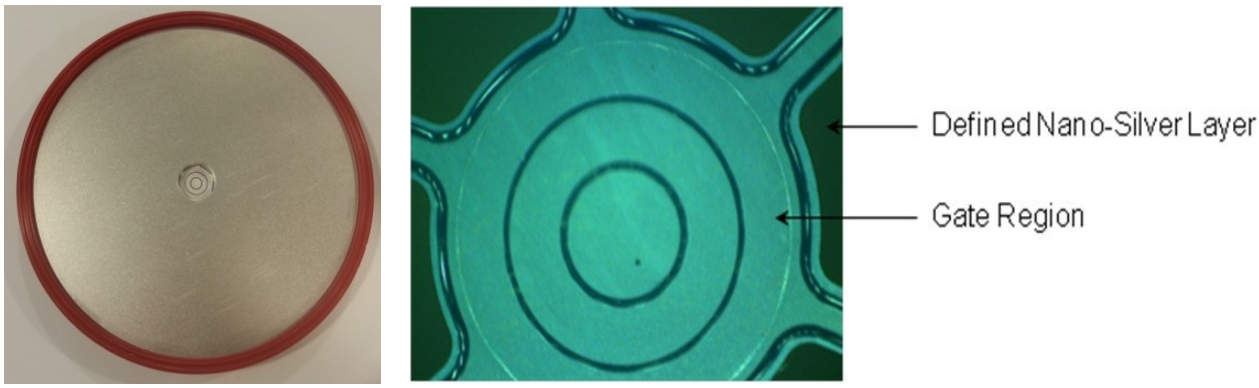

Fig 5 – (a) Double-side bonded 125 mm, 8.5 kV PCT, (b) defined nano-silver layer on the cathode

Having achieved the goal of realising an optimised PCT design and fabrication process for HVDC applications, full operating characteristics will be presented at a later date in a future paper.

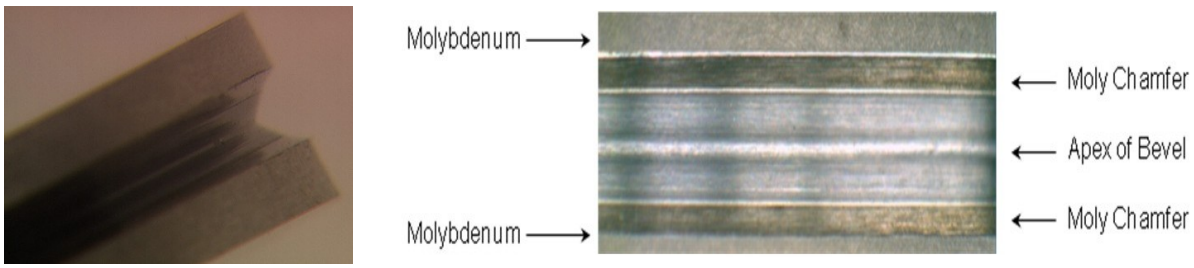

Fig 6 – Typical bonded double-positive bevel profile and surface finish after edge grinding

3. Development of 12-14 kV Series Connected ASCR and Diodes.

As previously discussed, it is essential that semiconductor devices are optimised for overall energy losses in HVDC systems. In a conventional PCT, this is achieved by designing the n-base width to be as narrow as possible through tight control of the starting silicon resistivity, With this in mind, neutron transmutation doped silicon material (NTD) is usually chosen by the power device manufacturer as it possesses the lowest available resistivity tolerance levels.

Above 8.5 kV voltage rating, PCT dynamic characteristics and switching losses become unacceptable for HVDC due to the required n-base width. An alternative solution is the use an asymmetric silicon controlled rectifier (ASCR) which incorporates an n-buffer diffusion profile on the anode side to limit depletion spread, and considerably reduce the effective n-base width.

Fig 7 schematically compares the vertical structure of an ASCR with that of a PCT and illustrates the modulation of the electric field during forward off-state conditions. Unfortunately, the asymmetric device lacks significant voltage blocking capability in the reverse direction and hence for HVDC applications a series connected diode of similar voltage rating is required to provide AC functionality.

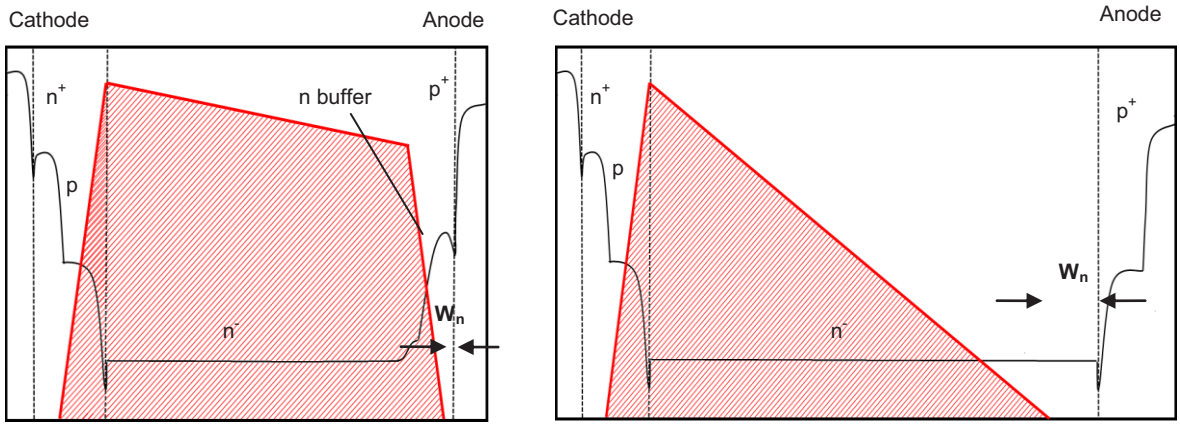

Fig 7 – Field distribution in (a) asymmetric and (b) symmetric PCT structures

Once the depletion region reaches the buffer diffusion, the effective un-depleted n-region (Wn) is much narrower than a conventional PCT, giving rise to a relatively high anode transistor gain (α_{pnp}). This can degrade higher temperature performance unless mitigating steps are taken. One solution is to use electron or proton irradiation to reduce carrier lifetimes. Another technique is to incorporate anode shorting combined with electron irradiation for the final fine tuning of dynamic characteristics. Obviously, both approaches increase on-state forward volt drop, and energy losses of the device. In order to study the effect and suitability of anode shorting 3D simulation is essential. As an example, a 3D device model and mesh to investigate the positional effects of anode shorting with respect to blocking voltage and trigger currents within the ASCR amplifying gate region is shown in Fig 8.

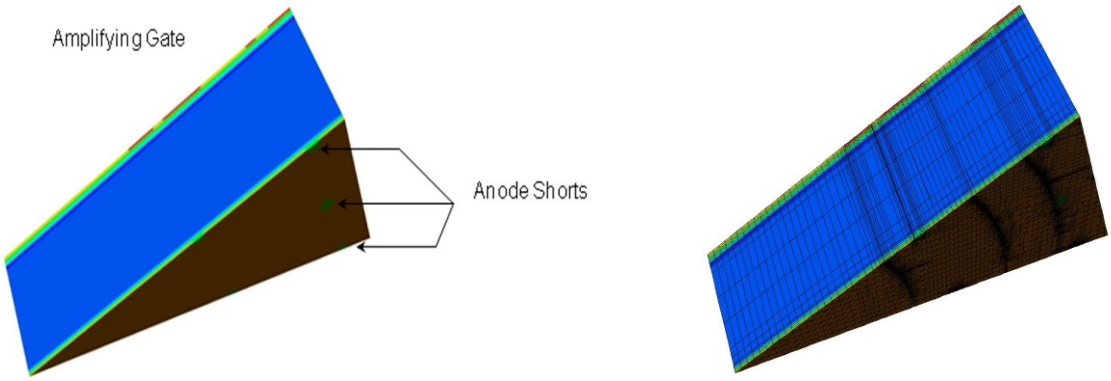

Fig 8 – 3D ASCR device amplifying gate model and resulting finite element mesh

The comparison of ASCR blocking with and without anode shorts is shown in Fig 9a. Here anode voltage was gradually increased until avalanche breakdown occurred. Without anode shorts, the reduction in 90°C blocking voltage is more than 50%. Placement of anode shorts directly underneath cathode shorting has been found to be a satisfactory design rule to provide full blocking capability whilst minimising increases in forward voltage drop.

Fig 9b compares the relative switching speed of ASCRs without anode shorts and with anode shorts located at two differing locations. Best switching occurs when no anode shorts are present. As above though, acceptable switching is achieved when the anode and cathode shorts are vertically aligned.

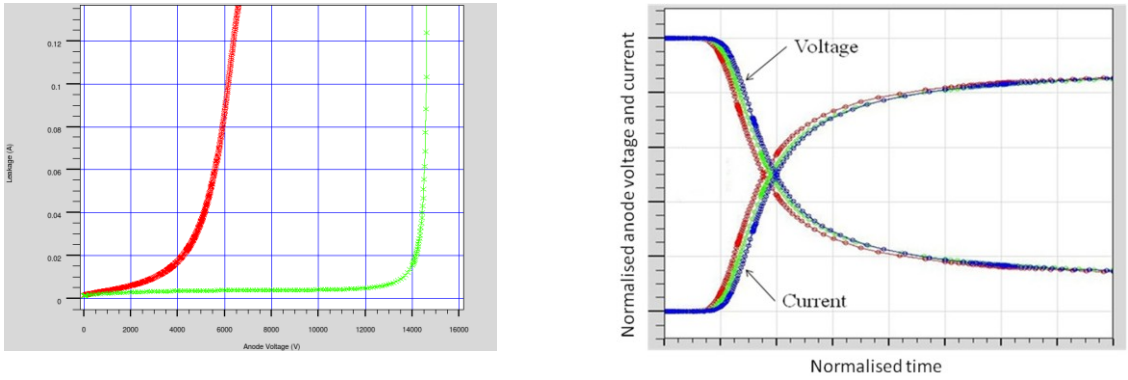

Fig 9 – (a) ASCR avalanche breakdown voltage comparison, (b) ASCR device switching comparison. In both cases, the red curve represents no anode shorting, whilst the blue and green curves represent anode shorts at different locations. Both graphs refer to a 90°C condition.

As previously stated, the junction edge termination geometry is critical when designing to optimise blocking voltage, energy losses and long term reliability. In this particular case, it was appropriate to design the ASCRs and diodes with wider tolerance FZ resistivity silicon material rather than very expensive high resistivity NTD.

In order to determine the best bevel profile for a 12-14 kV ASCR (and diode), experimentally measured diffusion profiles were used in the device simulator and blocking performance assessed for numerous surface geometries which could be achieved using production techniques. Fig 10 compares the performance of the optimised novel bevel profile with the standard Dynex Semiconductor double-positive bevel at avalanche breakdown. Although exhibiting no improvement in breakdown voltage (bulk breakdown), the novel bevel profile shows a significant improvement in surface electric field characteristics.

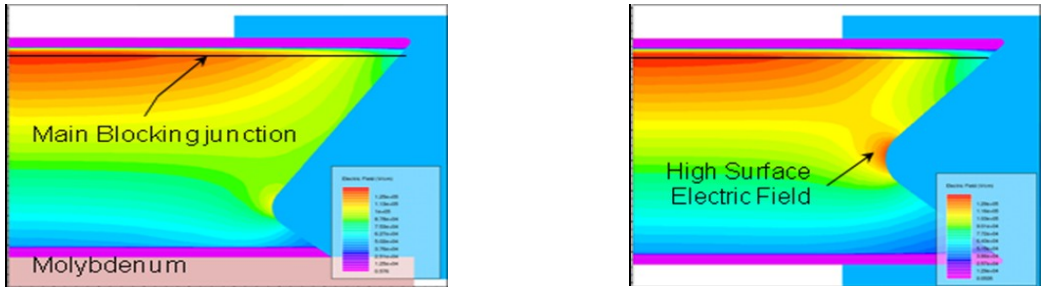

Fig 10 – Electric field distribution for a 12-14 kV ASCR at avalanche breakdown (a) novel bevel profile low temperature bonded to molybdenum (b) standard pressure contact bevel

At present, 12-14 kV ASCRs and diodes have now been successfully fabricated using high resistivity (>800 ohm-cm) gas doped FZ material. A modified, high lifetime i^2 implant based diffusion process has been developed for each device type, with a deep n-type implant forming the buffer layer. An implanted buffer is the preferred option since this has been found to provide greater control over the p-emitter rollover, a key process parameter for the ASCR.

Anode shorting was realised using an oxide masked phosphorus diffusion and is shown in Fig 11. Here, silicon from an ASCR has been acid etched to highlight regions of high concentration diffusants, and the location of junctions.

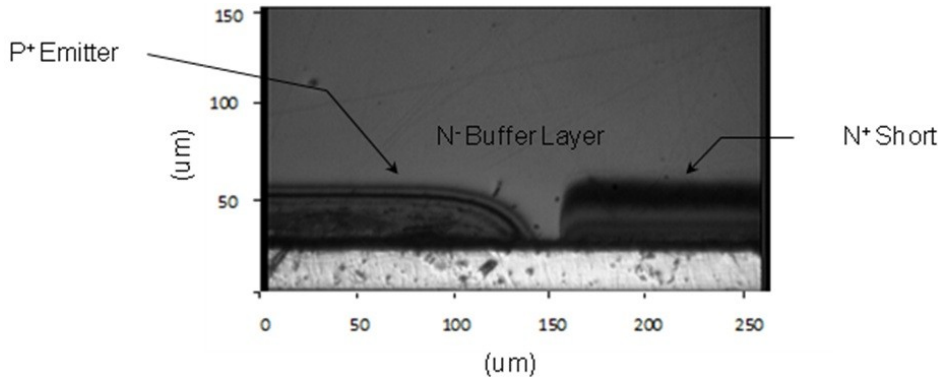

Fig 11 – Acid staining showing anode shorting

Having completed the initial objective of generating functional samples of 12-14kV ASCRs and diodes, the next phase is to perform a full evaluation of the series connected technology.

On state conduction, turn-on and recovery energy loss measurements are now being made with devices electron irradiated to produce a range of carrier lifetimes (forward volt drop) which will be compared with PCT technology at 8.5kV and 6.5kV. A conclusion on the validity of the tandem approach for HVDC will be forthcoming.

4. Conclusion

The design and fabrication of an optimised PCT for HVDC applications has been presented, using a 125 mm, 8.5 kV low temperature double-side bonded device as demonstrator. It is expected this technology will lead to 'best-in-class' performing PCT products for HVDC, in terms of both performance and reliability.

The design and fabrication of 12-14 kV ultra-high voltage ASCRs and diodes has also been discussed and presented. Extensive dynamic testing is now in progress to gain a full understanding of the series connected behaviour and suitability for use in future HVDC applications.

5. Literature

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