Dr. Durgesh Nandan
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Career Summary

A result-oriented leader with more than 7 years of teaching experience with effective communicator, exceptional presentation skills & abilities in leading cross-cultural teams & establishing relationship.

Previously working as a role of **faculty under SMDP-C2SD project at ECE Department in National Institutes of Technology, Patna (Bihar)**.

Currently working as a role of **Research Mentor in CL educate ltd.**

Education

Examination	School /college / Board / University	Duration	Percentage /CGPA
PhD	Jaypee University of Engineering & Technology, Guna	2014- 2018 (08-10-2018)	8 (C.W.)
PGDIPR	IGNOU	2018	Enroll
M.TECH (MEVD)	Technocrats Institutes of Technology, Bhopal (R.G.P.V)	2010 - 2013	79.4 % (First with Distinction.)
B.E.(EC)	Bansal College of Engineering, Mandideep (R.G.P.V.)	2005 - 2009	70.34% (First)
High Secondary (10+2)	A.N.D.C, Shahpur Patory (Bihar Board)	2001	76.3% (First with Distinction.)
High School (10th)	G.B.H.S, Shahpur Patory (Bihar Board)	1999	61.2% (First)

Employment Details

Research:

- Currently worked as a role of the **Research Mentor in CL educate Ltd** from 21th September 2018 to till date.
- Worked as a full-time research scholar on the research topic of "**Design and analysis of an efficient architecture of logarithmic multiplier and its applications"** in **Jaypee University of Engineering and Technology**, Guna (MP) from 07th August 2014 to 21 April 2018.

Teaching:

- Worked as a **faculty under SMDP-C2SD project at ECE Department in National Institutes of Technology, Patna (Bihar)** from 25th April 2018 to 20th September 2018.

- Worked as an **Asst. professor** in IASSCOM fortune institutes of technology, Bhopal (M.P) from 5th April 2013 to 31st July 2014.
- Worked as a **Lecturer** in IASSCOM fortune institutes of technology, Bhopal (M.P) from 2nd July 2009 to 17th Sept. 2010.

Other work:

- Worked as a **Head of department** (E.C) in IASSCOM fortune institutes of technology, Bhopal (M.P) from 5th April 2013 to 31st July 2014.
- Worked as an **Asst. Exam controller** in IASSCOM fortune institutes of technology, Bhopal (M.P) From December 2013 to June 2014.
- Worked as Quantitative aptitude trainer in Engineering College for preparing campus interview.

Area of Research Interest

- Image Processing
- VLSI Systems Design for Signal Processing Algorithms
- Hardwar security and Cryptography
- Reversible Logic for Signal Processing & Quantum computing
- Artificial intelligence
- VLSI Systems Design for Speech Processing Algorithms

Area of Subject Interest

- Basic of electronics
- Digital signal processing
- Electronic devices
- Computer arithmetic
- CMOS and ASIC VLSI design
- Digital electronics

Research Publication

Journal Paper:

1. **Durgesh Nandan**, Jitendra Kanungo and Anurag Mahajan, **"An Efficient VLSI architecture design for logarithmic multiplication by using the improved operand decomposition,"** Elsevier, VLSI the integration journal, Vol. 58, pp. 134-141, June 2017, DOI:10.1016/j.vlsi.2017.02.003 (**SCI**).
2. **Durgesh Nandan,** Jitendra Kanungo and Anurag Mahajan, **"An errorless Gaussian filter for image processing by using expanded operand decomposition logarithm multiplication,"** *Springer, Journal of ambient intelligence and humanized computing***,** DOI:10.1007/s12652-018-0933-x, 2018 **(SCI,** In Press**).**
3. **Durgesh Nandan,** Jitendra Kanungo and Anurag Mahajan, **"An efficient VLSI architecture design of Leading One Detector,"** International journal of pure and applied mathematics, Vol.118 (14), pp. 267-272, 2018 (**Scopus**).
4. **Durgesh Nandan,** Jitendra Kanungo and Anurag Mahajan, **"65 years journey of logarithm multiplier,"** International journal of pure and applied mathematics, Vol.118 (14), pp. 261-266, 2018 (**Scopus**).

5. **Durgesh Nandan**, Mahajan, A. and Kanungo, J. (2018), **"An efficient architecture of Iterative Logarithmic Multiplier,"** *International journal of engineering & technology (UAE)*. Vol.7 (2.16), pp. 24-28, 2018 (**Scopus**).
6. **Durgesh Nandan**, Anurag Mahajan and Jitendra Kanungo**, "Implementation of Leading One Detector based on reversible logic for logarithmic arithmetic,"** International Journal of Computer Applications, Vol.173 (8), pp. 40-45, Sep. 2017.
7. Parvin Akhter, Sachin Bandewar, **Durgesh Nandan, "Logarithmic Multiplier: An Analytical Review**" International Journal of Engineering Research, Vol.5 (8), pp: 721-723, August 2016.

International Conference paper:

8. **Durgesh Nandan**, Anurag Mahajan and Jitendra Kanungo, "**An Efficient antilogarithmic converter by using 11-regions error correction scheme,**" IEEE 4th International Conference on Signal Processing, Computing and Control (ISPCC 2017), JUIT, Waknaghat, pp. 118-121, 21-23 Sep.2017 (**Scopus**).
9. **Durgesh Nandan**, Jitendra Kanungo and Anurag Mahajan, "**An efficient VLSI architecture for Iterative Logarithmic Multiplier,**" IEEE 4th International conference on signal processing and integrated networks (SPIN), Noida, pp.419-423, Feb.2017 (**Scopus**).
10. **Durgesh Nandan**, Jitendra Kanungo and Anurag Mahajan, "**An Efficient VLSI architecture design for antilogarithmic converter by using the error correction scheme**," IET International conference on signal processing (ICSP), SATI, vidisha, 11-13 Nov. 2016, DOI: 10.1049/cp.2016.1445.
11. Sachet Jamliya, Anurag Mahajan, Abhishek Choubey and **Durgesh Nandan**, "**An efficient VLSI architecture of multiplier-less 1-D DWT using CSD technique**," IET International conference on signal processing (ICSP), SATI, vidisha, 11-13 Nov. 2016.
12. Khushboo Patel, Vibha Tiwari, and **Durgesh Nandan**, **"Crosstalk mitigation of network on chip: an analytical review"** IEEE International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, pp. 378-383, 3-5 March 2016, DOI: 10.1109/ICEEOT.2016.7755393 (**Scopus**).
13. **Durgesh Nandan** and Shivendra Singh, **"The comparative result of symmetric encryption techniques,"** Springer indexed ICICIC Global, Chennai, Dec. 2012.
14. **Durgesh Nandan** and Shivendra Singh, **"Key Reconfiguration Scheme for DES Algorithm,"** Springer indexed ICICIC Global, Chennai, Dec. 2012.

Professional Trainings Attended

- Attended a one-week GIAN course on "Logic design under paradigm of rebooting computing" from 25-29 Dec.2017 at IIT Roorkee.
- Attended a one-week course on "Hands on session on VLSI design tools" from 18 -22 Dec. 2017 at NIT Delhi.
- Attended UGC funded a one-week workshop on "VLSI design & sensors in systems" from March 20-25, 2017 at School of physics, University of Hyderabad, Hyderabad.
- Attended a two days National workshop on "MATLAB application in science & engineering" from February 11-12, 2017 at JUET, Guna.
- Attended a two-week GIAN course on "VLSI Architectures for Signal Processing and machine learning" from 19-30 December 2016 at IIT Kharagpur.
- Attended in National workshop on "High-performance VLSI Architectures for Digital Signal Processing Applications: Design and Implementations" from 9-11 September 2016 at JUET, Guna (MP).

- Attended in faculty recharge program on "VLSI Design" from 14-16 July 2015 at JUET, Guna (MP).
- Attended a two days National workshop on "Low Voltage and Low Power VLSI Design" from 22-23 August 2014 at JIIT, Noida.
- Attended a two- week ISTE workshop on "SIGNAL & SYSTEM" under the national mission on education through ICT which is organized by IIT, Kharagpur from 02-12 January 2012.
- Attended a two- week ISTE workshop on "ANALOG ELECTRONICS" under the national mission on education through ICT which is organized by IIT, Kharagpur.

Research Mentor activities

Reviewer of SCI Journal:

- Journal of Circuits, Systems and Computers, World Scientific.
- Circuit, systems and signal processing, Springer

Reviewer of Scopus Journal:

- Biomedical research, Allied Academies Journals.
- International journal of engineering and technology innovation.
- The Institution of Engineers (India) Series B.

Reviewer of International conference: (1) ICSPT'2013, (2) ICMASCTS'2014, (3) ICSIN'2014, (4) ICSPIE'2014, (5) ICTMASCS'2014, (6) ICSPCT 2014, (7) IJ--IS, (8) WSCNIS'2015, (9) WCI-2015, (10) ADMMET'2015, (11) ICCTIS'2015, (12) GAMEPEC 2015, (13) ICCEA'2015, (14) ISySM'2015, (15) PIAMSE'2015, (16) ICED 2016, (17) AVAREIT'2016, (18) AREITIC'2016, (19) ARECAS'2016, (20) ARONCAS'2016, (21) APPEMSE'2016, (22) AR2BIO-ICEMIT-RAIEIC'2016, (23) ICCCSIT-2016, (24) ICCITR'2016, (25) WCCAIS'16, (26) COMSIT'2016, (27) ENVICET'2016, (28) SCIEMATHIC'2016, (29) SYMINTECH'2016, (30) PROCSIT'2016, (31) WICOIS'2016, (32) I2BM'2017, (33) APPEMSE'2017, (34) ICACCI-2017, (35) ICOBSS'2017, (36) ICOCOE'2017, (37) SYMINTECH'2017, (38) CICN 2016, (39) ICCDMTA 2017, (40) PIAMSE'2017, (41) RENCES'2017, (42) I4CT'2015, (43) I4CT'2016, (44) SIRS-2015, (45) SIRS-2017, (46) SIRS-2018, (47) WCITCA'2015, (48) WCITCA'2016, (49) ISTA-2018.

TPC Member: (1) ICITA'2014, (2) GSCIT' 2015, (3) ENCINS' 2015, (4) ICCAAD' 2015, (5) ICCVIA' 2015, (6) IBMSGS' 2015, (7) GSCIT 2016, (8) ISTA-2017, (9) WSMEAP' 2015, (10) WSMEAP 2016, (11) WSCAR' 2015, (12) WSCAR 2016, (13) WSCAR 2017

Computer skills

Languages	**: c, c^{++}, MATLAB, VERILOG & VHDL.**
Operating Systems	**: Windows 2000/XP/2007.**
Software used	**: MATLAB, Xilinx ISE, Vivado, Mentor graphics, Cadence & Synopsys.**

Awards and Achievements

- JSS Research Fellowship for PhD in 2014.
- Selected for PhD in 1) J.P university, Guna; 2) KIIT, Odhisa.
- GATE 2014 qualify with GATE score 357.
- "Best of best" award in 2013 at I.F.I.T, Bhopal.
- Score 98.7 percentile in MAT 2009.
- Selected software companies like Infosensys Pvt. Ltd & Ilnathan technology Pvt. Ltd.

Personal Vitae

Date of Birth	:	28. Feb.1984
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References

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