CURRICULUM VITAE

Durgesh Nandan
prof.durgeshnandan@gmail.com
durgeshnandano51@gmail.com
Contact No.: +91- 9329483287 (M)

H.No-131, Chhawni
Mangalwara road,
Bhopal-462001
Madhya Pradesh

CAREER OBJECTIVE:

To transfer the knowledge to next generation, create best technocrats and work in an atmosphere where my talent and knowledge are best utilized.

EDUCATIONAL QUALIFICATIONS:

Examination	School /college / Board / University	Duration	Percentage /CGPA
Ph.D*	**Jaypee University of Engineering & Technology, Guna**	**On going**	**8** (During course-work subject)
M.TECH (MEVD)	**Technocrats Institutes of Technology, Bhopal (R.G.P.V)**	**2010 - 2013**	**79.4 %** (First with Distinction.)
B.E.(EC)	**Bansal College of Engineering, Mandideep (R.G.P.V.)**	**2005 - 2009**	**70.34%** (First)
High Secondary (10+2)	**A.N.D.C, Shahpur Patory (Bihar Board)**	**2001**	**76.3%** (First with Distinction.)
High School (10th)	**G.B.H.S, Shahpur Patory (Bihar Board)**	**1999**	**61.2%** (First)

EXPERIENCE:

Research:

- Working as a full time research scholar with Teaching Assistantship or Fellowship (Rs 18000/- pm) on the research topic of **"Low power VLSI design for digital filters and analysis"** in **Jaypee University of Engineering and Technology**, Guna (MP) from 07th August 2014 to till date.

Teaching:

- Worked as a **Asst. professor** in IASSCOM fortune institutes of technology , Bhopal (M.P) from 5th April 2013 to 31st July 2014.
- Worked as a **Lecturer** in Sri Satya Sai College of engineering (RKDF University), Bhopal (M.P) from 6 Sept, 2009 to 09 Sept. 2011.

Other work:

- Worked as a **Head of department** (E.C) in IASSCOM fortune institutes of technology **,**Bhopal (M.P) From 5th April 2013 to 31st July 2014;
- Worked as a **Asst. Exam controller** in IASSCOM fortune institutes of technology **,**Bhopal (M.P) From December 2013 to June 2014;
- Worked as Quantitative aptitude trainer in Engineering College for preparing campus interview.

AREA OF INTEREST:

1) Basic of electronics
2) Digital signal processing
3) Electronic device
4) Electronic circuit
5) Electronic device & circuit
6) CMOS VLSI design
7) Digital electronics

RESEARCH PUBLICATION:

Journal Paper:

1. Parvin Akhter, Sachin Bandewar, **Durgesh Nandan, "Logarithmic Multiplier: An Analytical Review**" International Journal of Engineering Research, Volume No.5, Issue No.8, pp: 721-723, August 2016.
2. **Durgesh Nandan**, Jitendra Kanungo and Anurag Mahajan **"An Efficient VLSI architecture design for logarithmic multiplication by using the improved operand decomposition,"** VLSI the integration journal, Elsevier, (*revision submitted*).
3. **Durgesh Nandan,** Jitendra Kanungo and Anurag Mahajan, **"An errorless 2 D convolution based Gaussian smoothing filter using expanded operand decomposition logarithm multiplication,"** Journal of Circuits, Systems and Computers, World Scientific, **(under review).**

Conference paper:

1. **Durgesh Nandan**, Jitendra Kanungo and Anurag Mahajan, "**An efficient VLSI architecture for Iterative Logarithmic Multiplier,**" IEEE 4th International conference on signal processing and integrated networks (SPIN), Amity University, Noida, 2-3 Feb.2017.
2. **Durgesh Nandan**, Jitendra Kanungo and Anurag Mahajan, "**An Efficient VLSI architecture design for antilogarithmic converter by using the error correction scheme**," IETE International conference on signal processing (ICSP), SATI, vidisha, 11-13 Nov. 2016.
3. Sachet Jamliya, Anurag Mahajan, Abhishek Choubey and **Durgesh Nandan**, "**An efficient VLSI architecture of multiplier-less 1-D DWT using CSD technique**," IETE International conference on signal processing (ICSP), SATI, vidisha, 11-13 Nov. 2016.
4. Khushboo Patel, Vibha Tiwari, and **Durgesh Nandan**, **"Crosstalk mitigation of network on chip: an analytical review"** IEEE International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, pp: 378-383, 3-5 March 2016, DOI: 10.1109/ICEEOT.2016.7755393.
5. **Durgesh Nandan** and Shivendra Singh, **"The comparative result of symmetric encryption techniques,"** ICICIC Global, Springer indexed, Chennai, Dec. 2012.
6. **Durgesh Nandan** and Shivendra Singh, **"Key Reconfiguration Scheme for DES Algorithm,"** ICICIC Global, Springer indexed, Chennai, Dec. 2012.

Workshop:-

- Attended a two- week GIAN course on "VLSI Architectures for Signal Processing and machine learning" from 19-30 December 2016 at IIT Kharagpur.
- Attended in National workshop on "High-performance VLSI Architectures for Digital Signal Processing Applications: Design and Implementations" from 9-11 September 2016 at JUET, Guna (MP).
- Attended in faculty recharge program on "VLSI Design" from 14-16 July 2015 at JUET, Guna (MP).
- Attended in National workshop on "Low Voltage and Low Power VLSI Design" from 22-23 August 2014 at JUET, Guna (MP).
- Attended a two- week ISTE workshop on "SIGNAL & SYSTEM" under the national mission on education through ICT which is organized by IIT, Kharagpur from 02-12 January 2012.
- Attended a two days national workshop on "Mixed signal VLSI design" from 20 & 21 July 2012 which is organized by SSSIST, Bhopal (M.P).
- Attended a two- week ISTE workshop on "ANALOG ELECTRONICS" under the national mission on education through ICT which is organized by IIT, Kharagpur.

TECHNICAL SOCIETY ACTIVITIES:

Reviews: (1) ICSPT'2013, (2) ICMASCTS'2014, (3) ICSIN'2014, (4) ICSPIE'2014, (5) ICTMASCS'2014, (6) ICSPCT 2014, (7) IJ--IS, (8) WSCNIS'2015, (9) WCI-2015, (10) ADMMET'2015, (11) ICCTIS'2015, (12) GAMEPEC 2015, (13) ICCEA'2015, (14) ISySM'2015, (15) PIAMSE'2015, (16) ICED 2016, (17) AVAREIT'2016, (18) AREITIC'2016, (19) ARECAS'2016, (20) ARONCAS'2016, (21) APPEMSE'2016, (22) AR2BIO-ICEMIT-RAIEIC'2016, (23) ICCCSIT-2016, (24) ICCITR'2016, (25) WCCAIS'16, (26) COMSIT'2016, (27) ENVICET'2016, (28) SCIEMATHIC'2016, (29) SYMINTECH'2016, (30) PROCSIT'2016, (31) WICOIS'2016, (32) I2BM'2017, (33) APPEMSE'2017, (34) ICACCI-2017, (35) ICOBSS'2017, (36) ICOCOE'2017, (37) SYMINTECH'2017, (38) CICN 2016, (39) ICCDMTA 2017, (40) PIAMSE'2017, (41) RENCES'2017, (42) I4CT'2015, (43) I4CT'2016, (44) SIRS-2015, (45) SIRS-2017, (46) WCITCA'2015, (47) WCITCA'2016.

TPC Member: (1) ICITA'2014, (2) GSCIT' 2015, (3) ENCINS' 2015, (4) ICCAAD' 2015, (5) ICCVIA' 2015, (6) IBMSGS' 2015, (7) GSCIT 2016, (8) ISTA-2017, (9) WSMEAP' 2015, (10) WSMEAP 2016, (11) WSCAR' 2015, (12) WSCAR 2016, (13) WSCAR 2017

MEMBERSHIP:

IEEE Member (Membership No. 94154884).

COMPUTER SKILLS:

Languages **: c, c^{++}, MATLAB & VHDL.**

Operating Systems **: Windows 2000/XP/2007.**

Software used **: PCB maker, MATLAB, Xilinx & Synopsys.**

AWARDS/ACHIEVEMENTS:

- **Selected for PhD in 1) J.P university, Guna; 2) KIIT, Odhisa.**
- **GATE 2014 qualify with GATE score 357.**
- "Best of best" award in 2013 at I.F.I.T, Bhopal.
- Score 98.7 percentile in MAT 2009.
- Selected software companies like **Infosensys Pvt. Ltd** & **Ilnathan technology Pvt. Ltd**.

PERSONAL PROFILE:

Name	:	Durgesh Nandan
Father's Name	:	Mr. R. S. Chaudhary
Mother's Name	:	Mrs. Vibha Kumari
Date of Birth	:	28. Feb.1984

DECLARATION:

I hereby declare that the above-mentioned information is correct up to my knowledge and I bear the responsibility for the correctness of the above-mentioned particulars.

Place: Bhopal **(DURGESH NANDAN)**