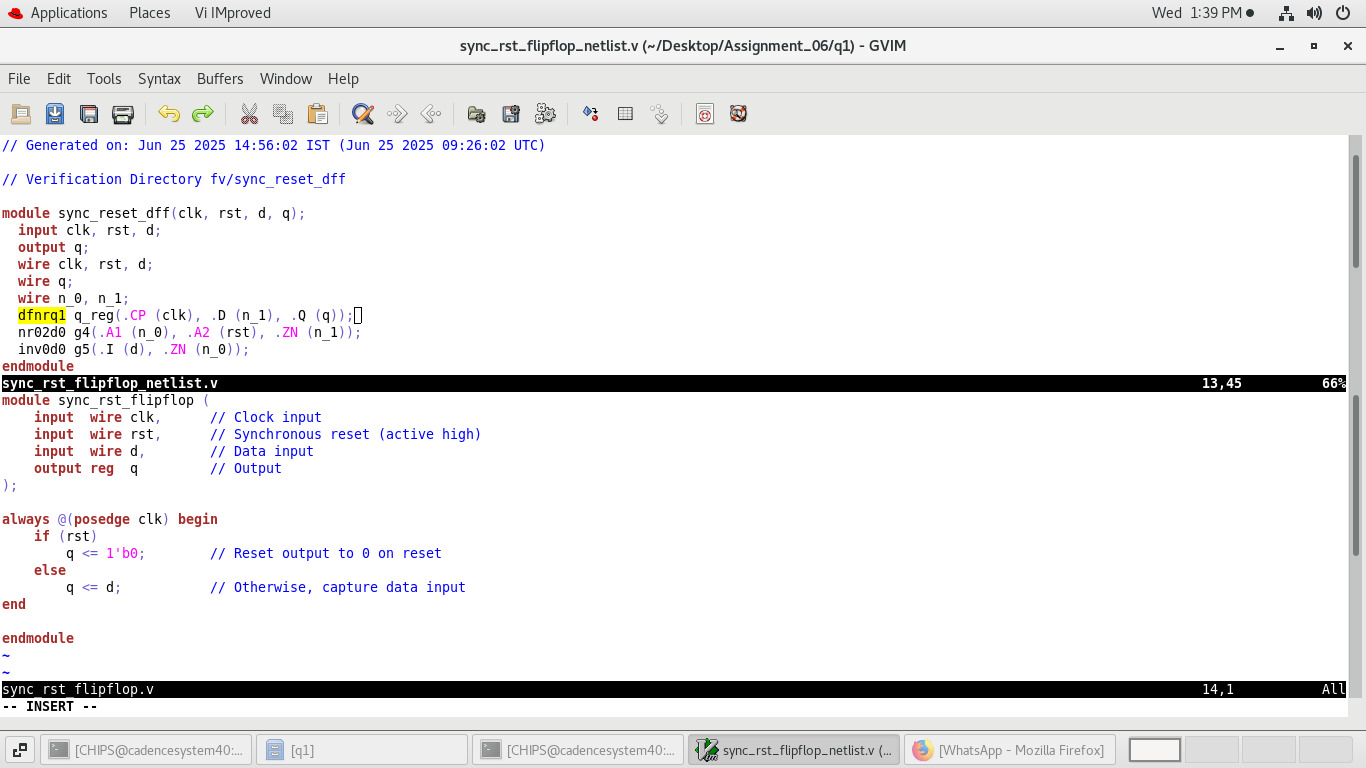
Synthesis

***1) sync\_reset\_dff***

**Verilog code**

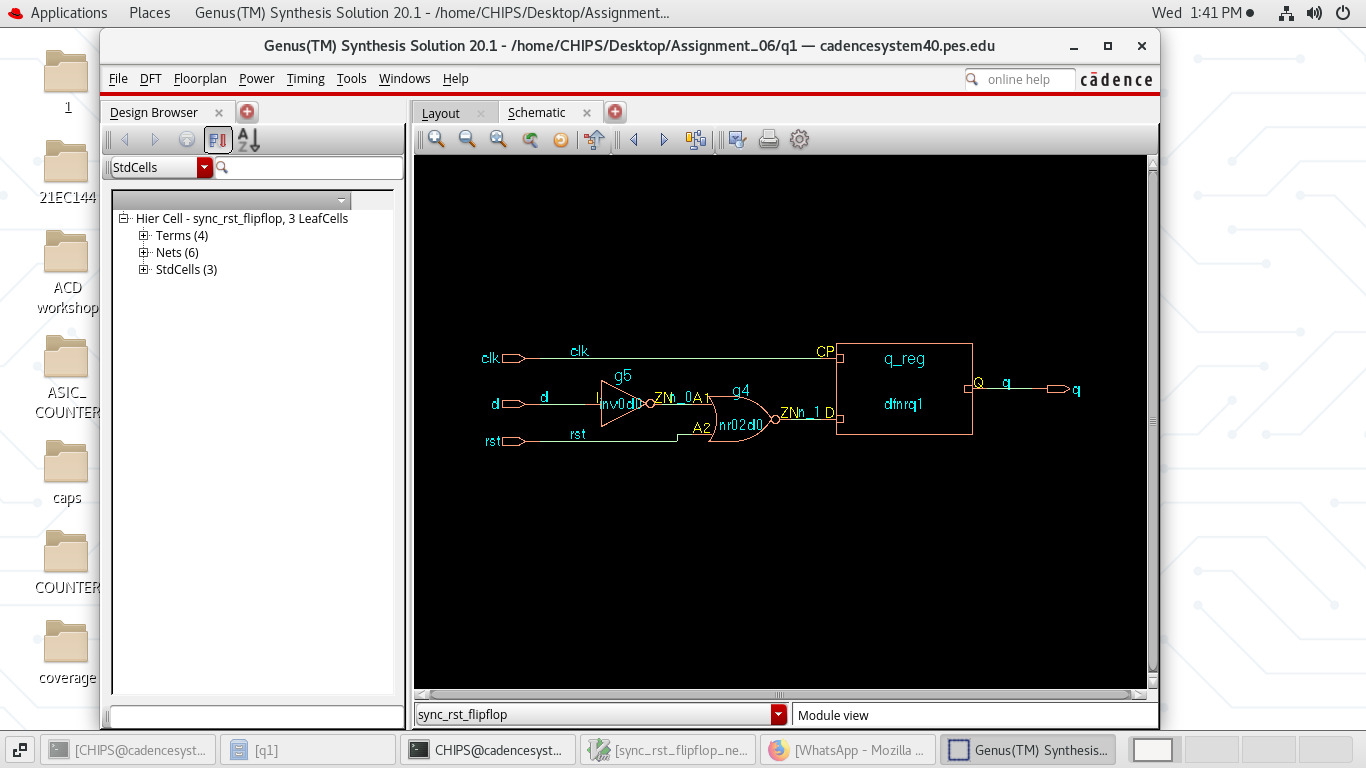
**Mark lib cell /instance /pins/nets**

Trace nets in netlist

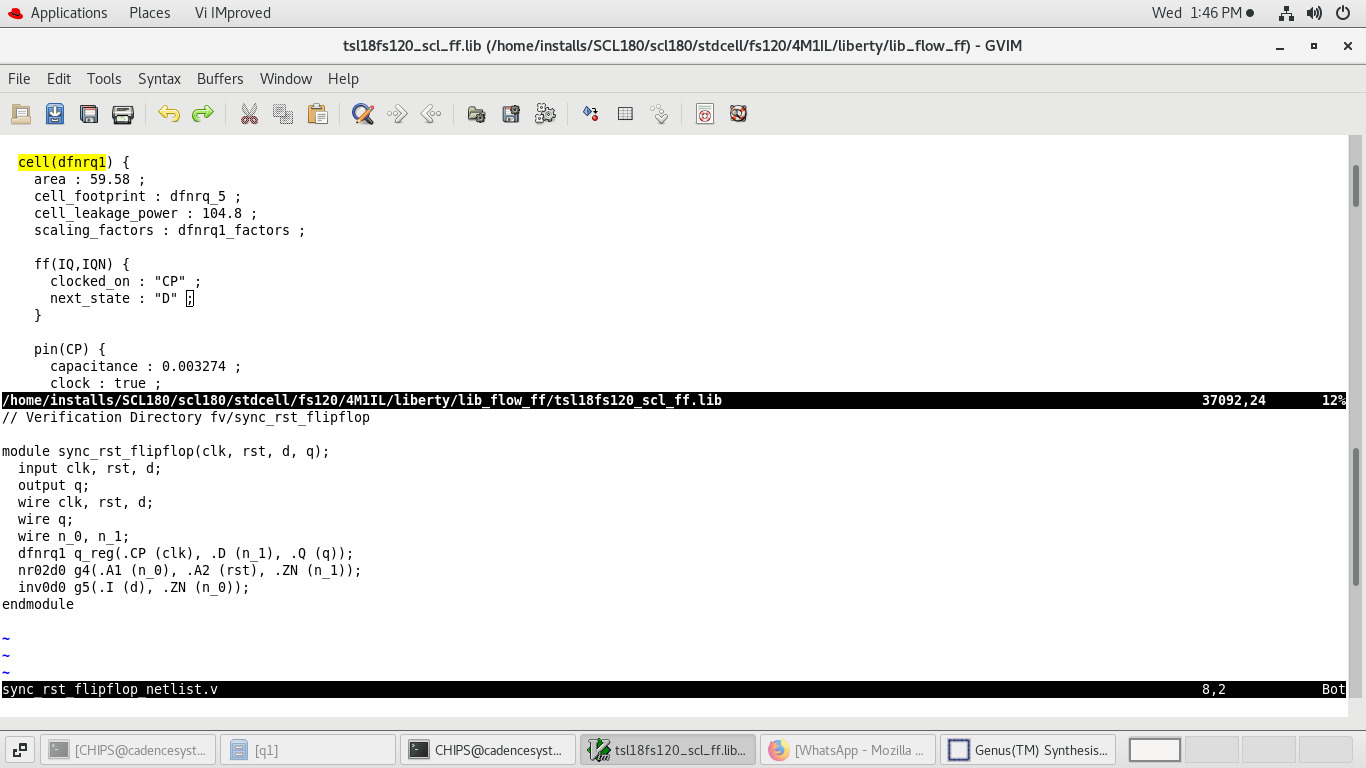
1)n\_1 is traced it is driven by g4/ZN and its load pin is q\_reg/D

2)n\_0 is driven by g5/ZN and its load pin is g4/A1

**Genus schematic: example**



***Lib mapping:***



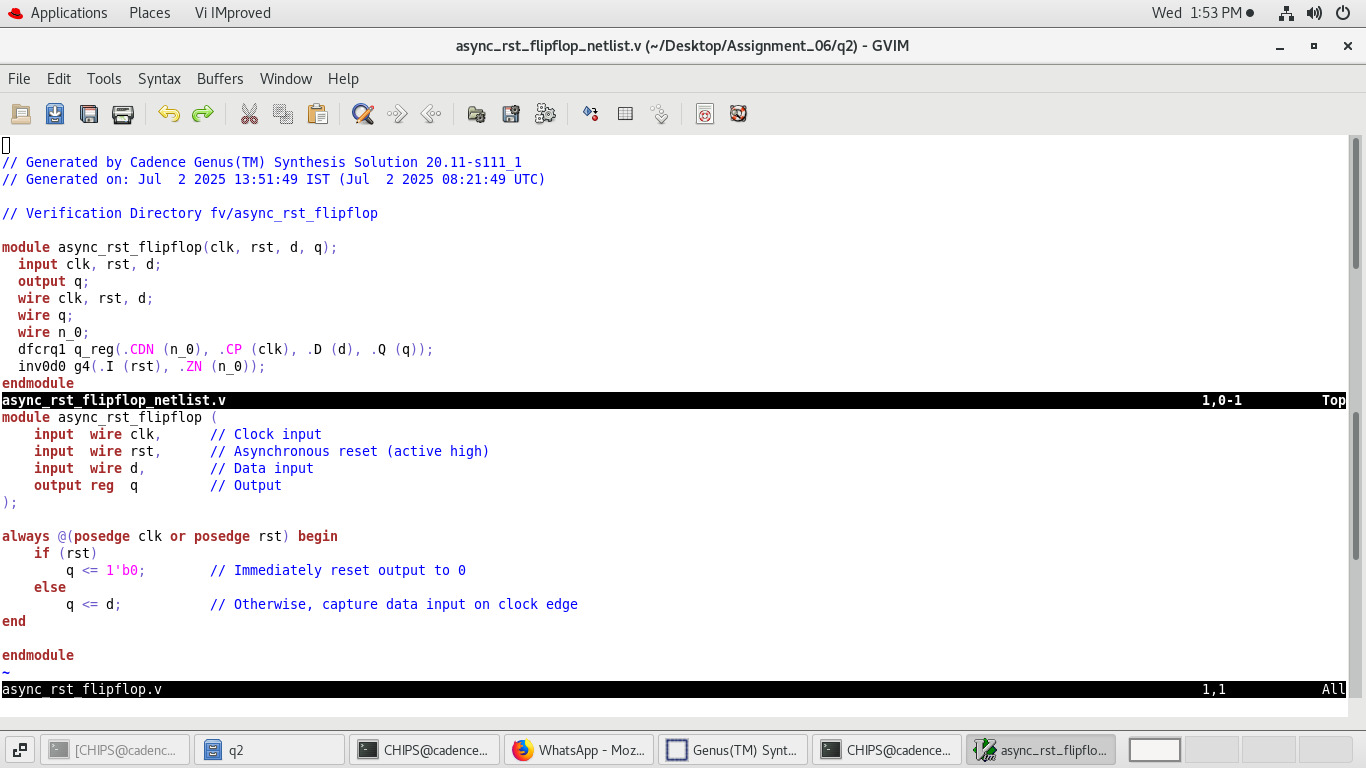
**Notes:**

1)flop name in rtl : q

2)flop name in netlist:q\_reg

***2) sync\_reset\_dff***

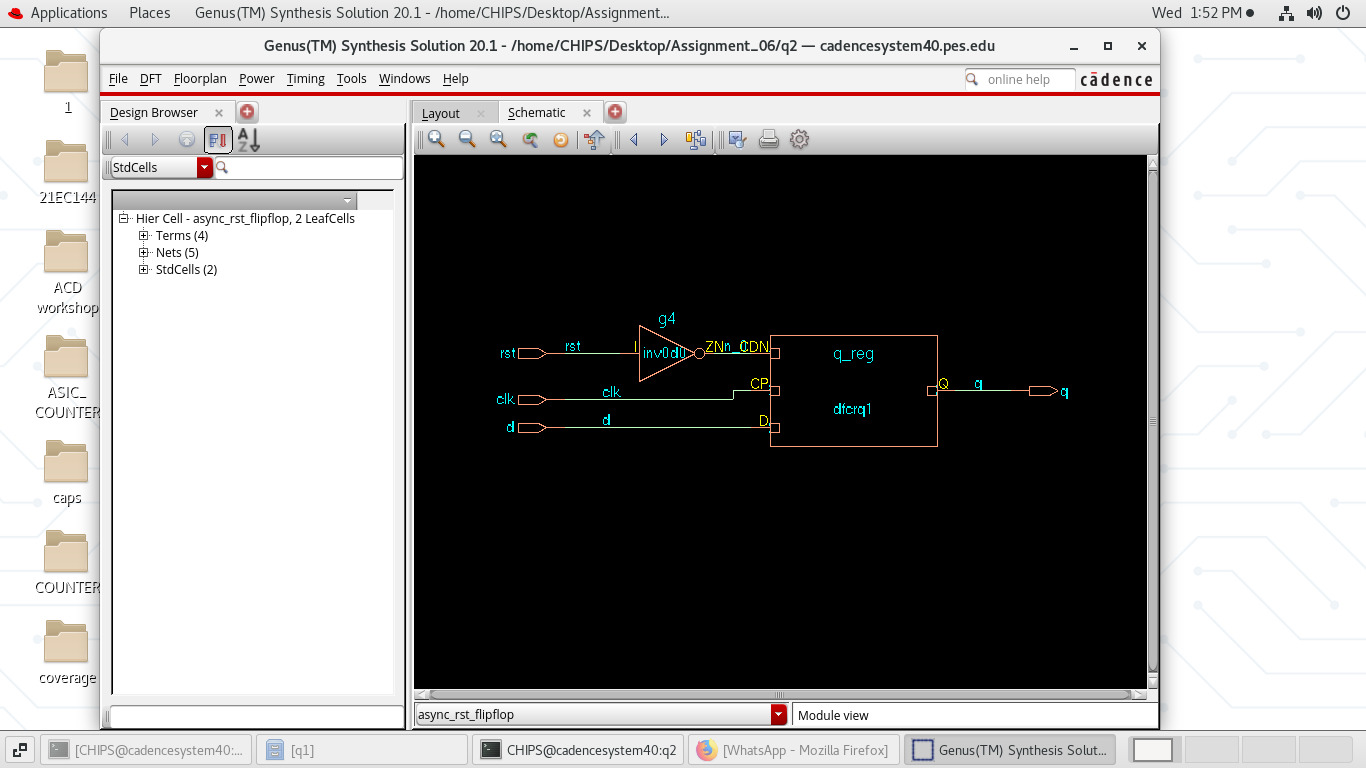
**Verilog/Netlist:**



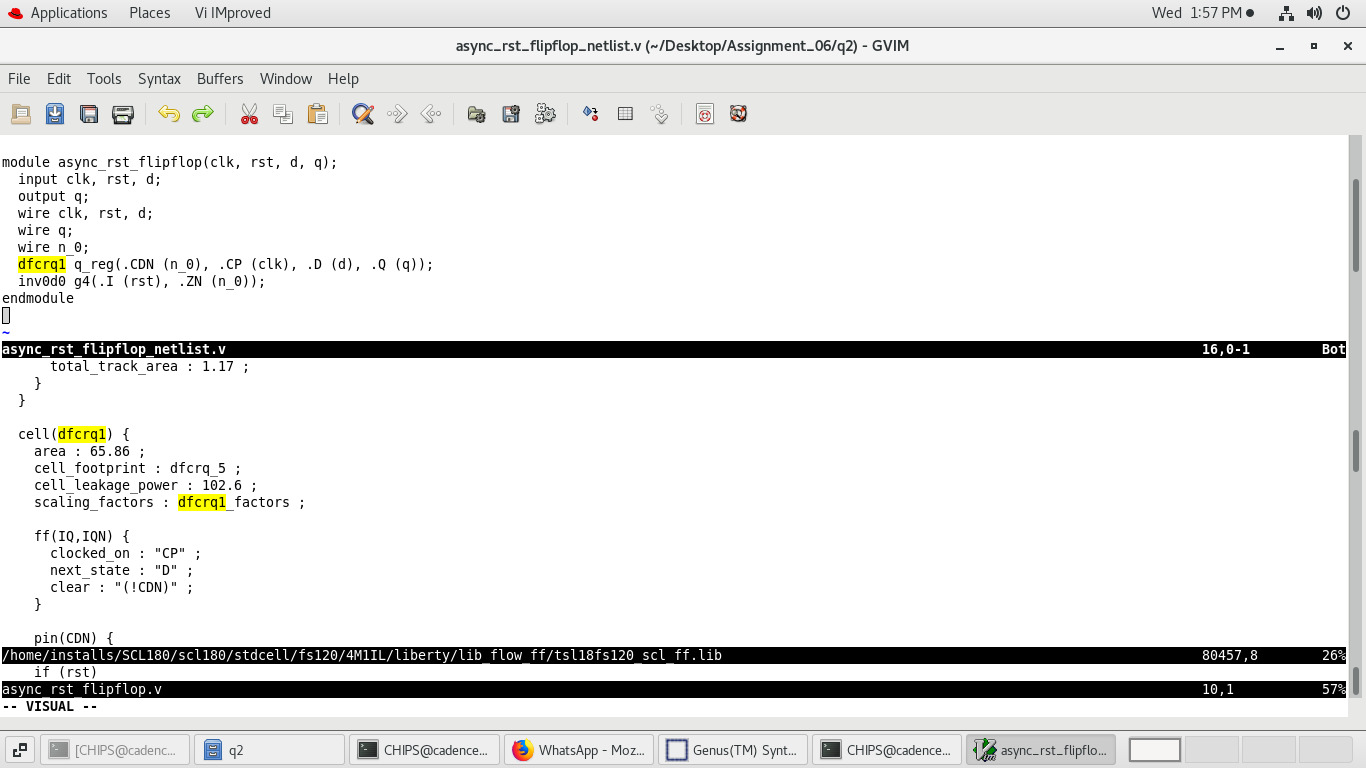
**Mark lib / instans / cell / nets**

1. n\_0 is traced and is driven by ZN/g4 its load is CDN/q\_reg

**Genus Schematic:**



**Lib Mapping:**

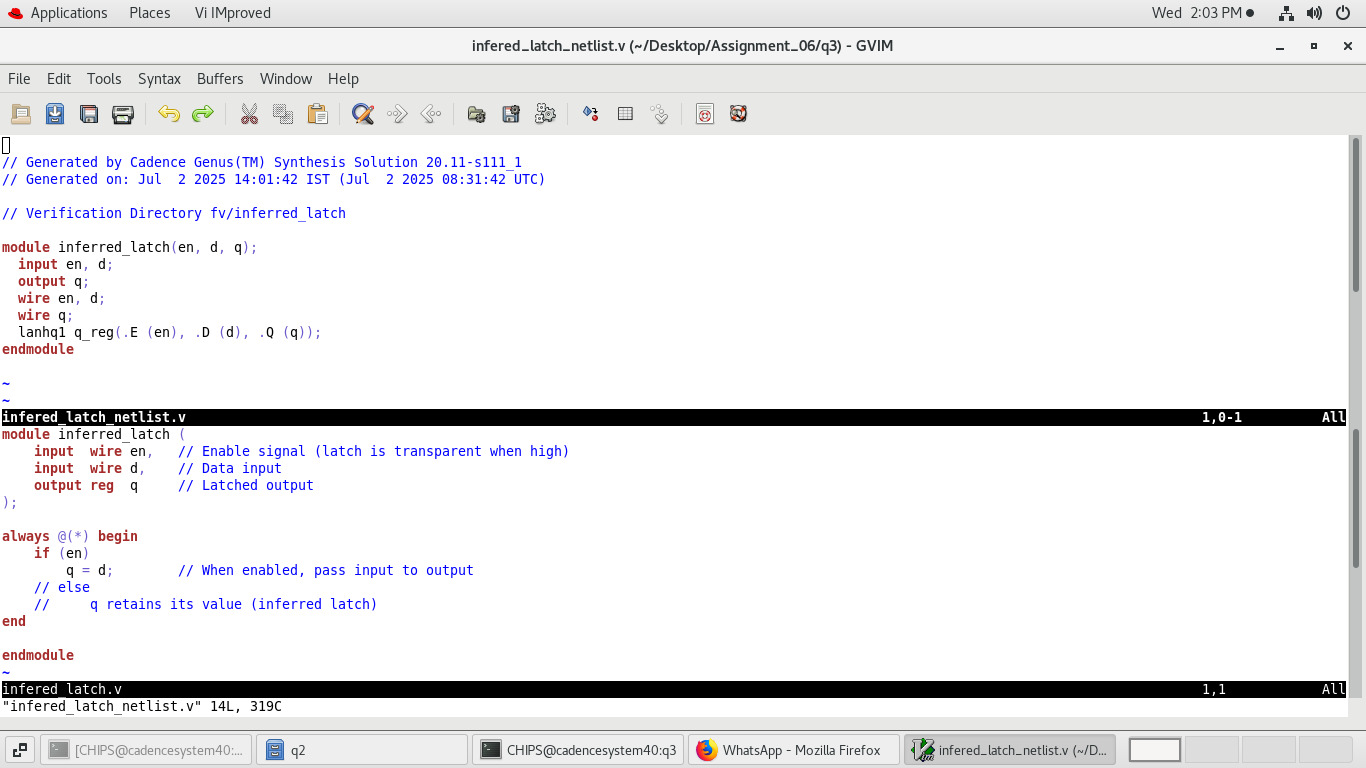


**Notes:**

1. Flop name in rtl: q
2. Flop name in netlist: q\_reg

***3) Inferred Latch***

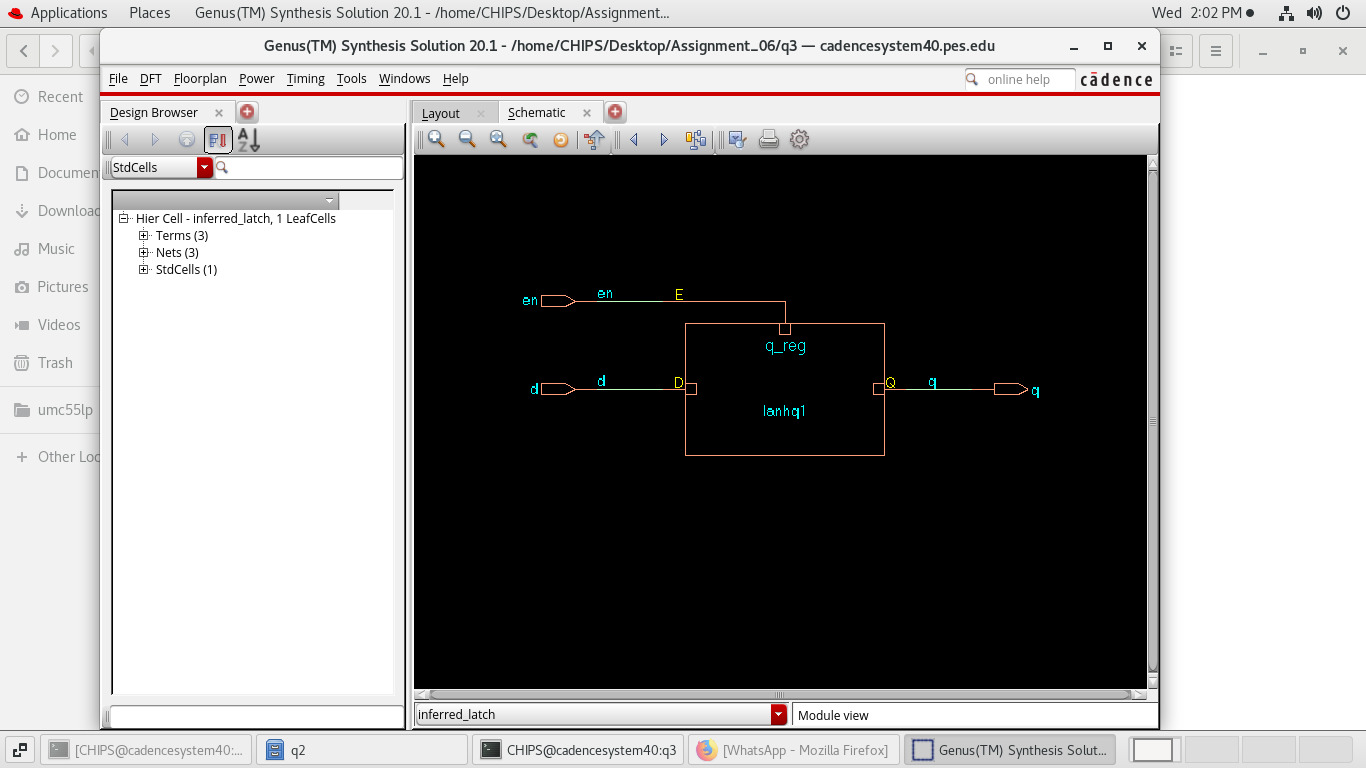
***Verilog/Netlist***



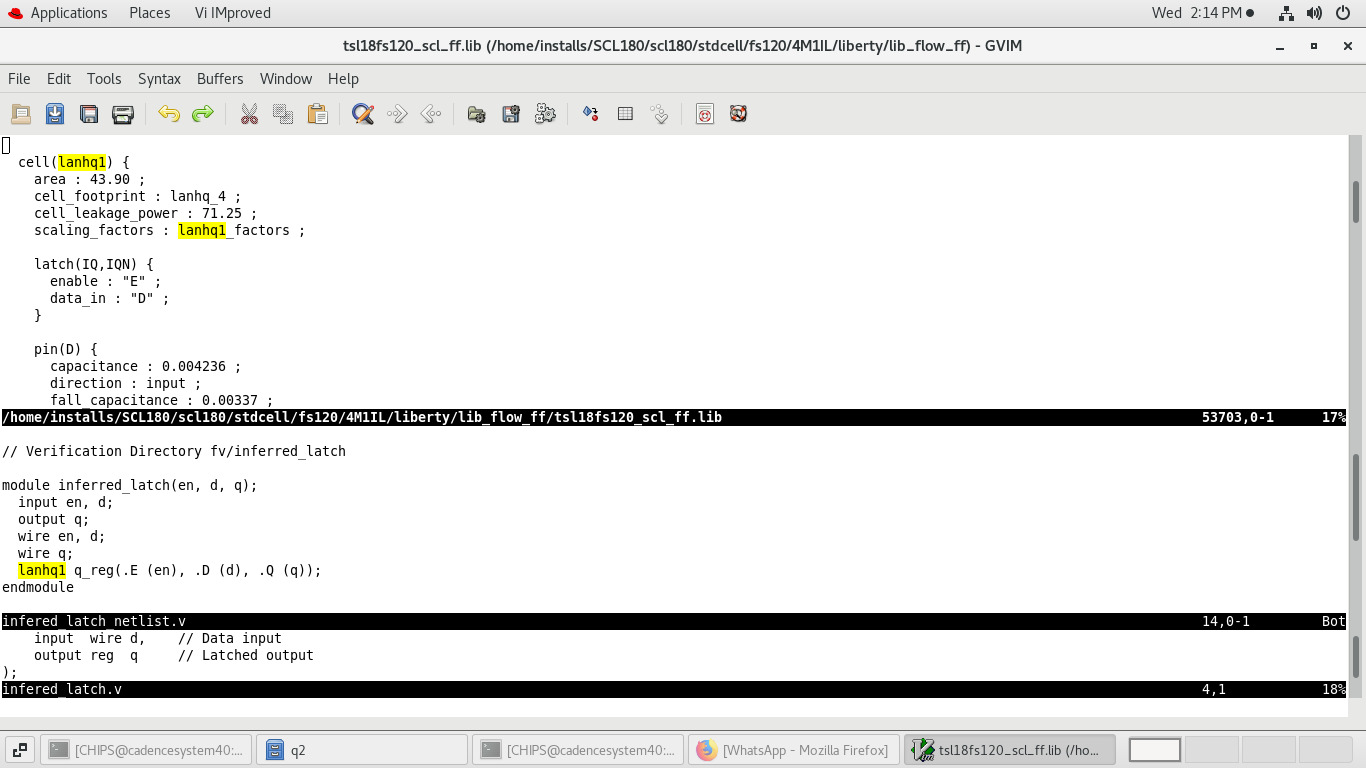
**Mark lib / instans / cell / nets**

Instance: lanhq1

**Genus Schematic:**



**Lib mapping:**

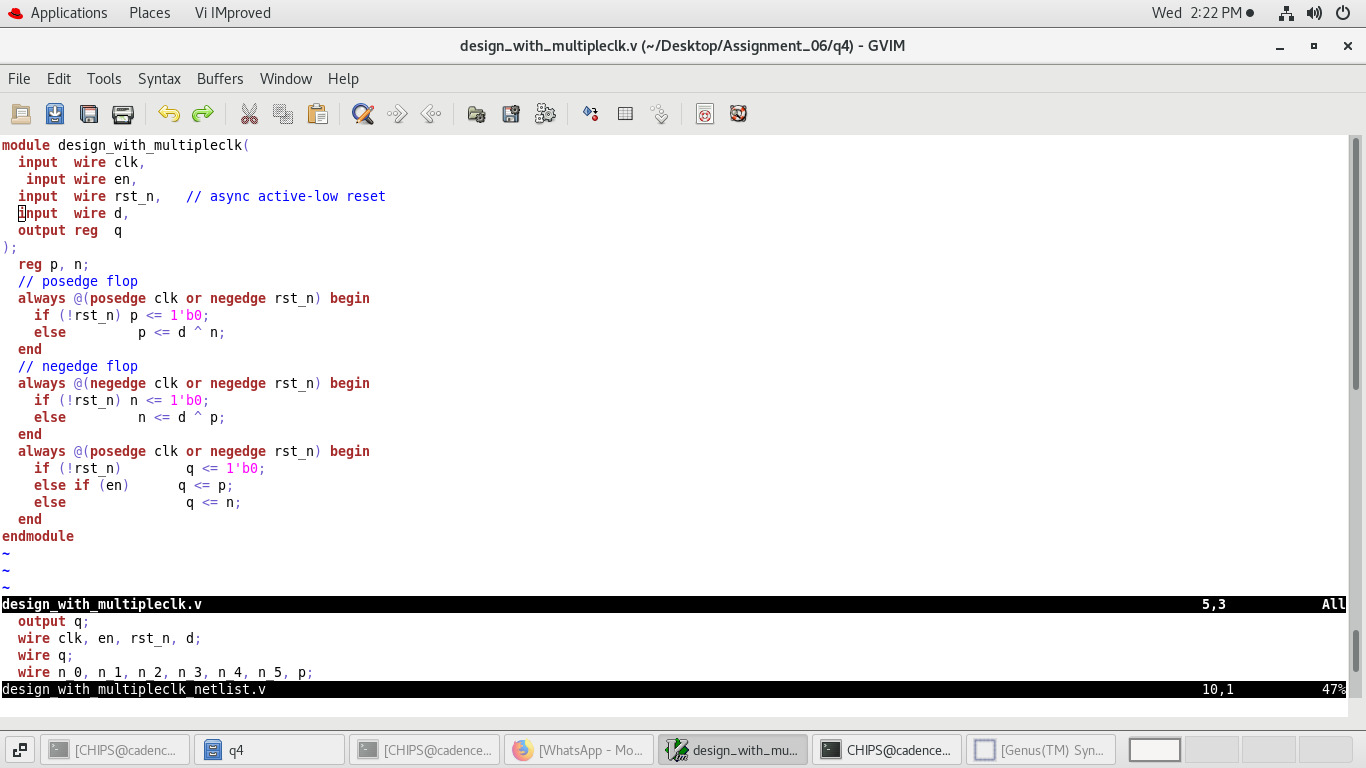


Flop name in rtl:q

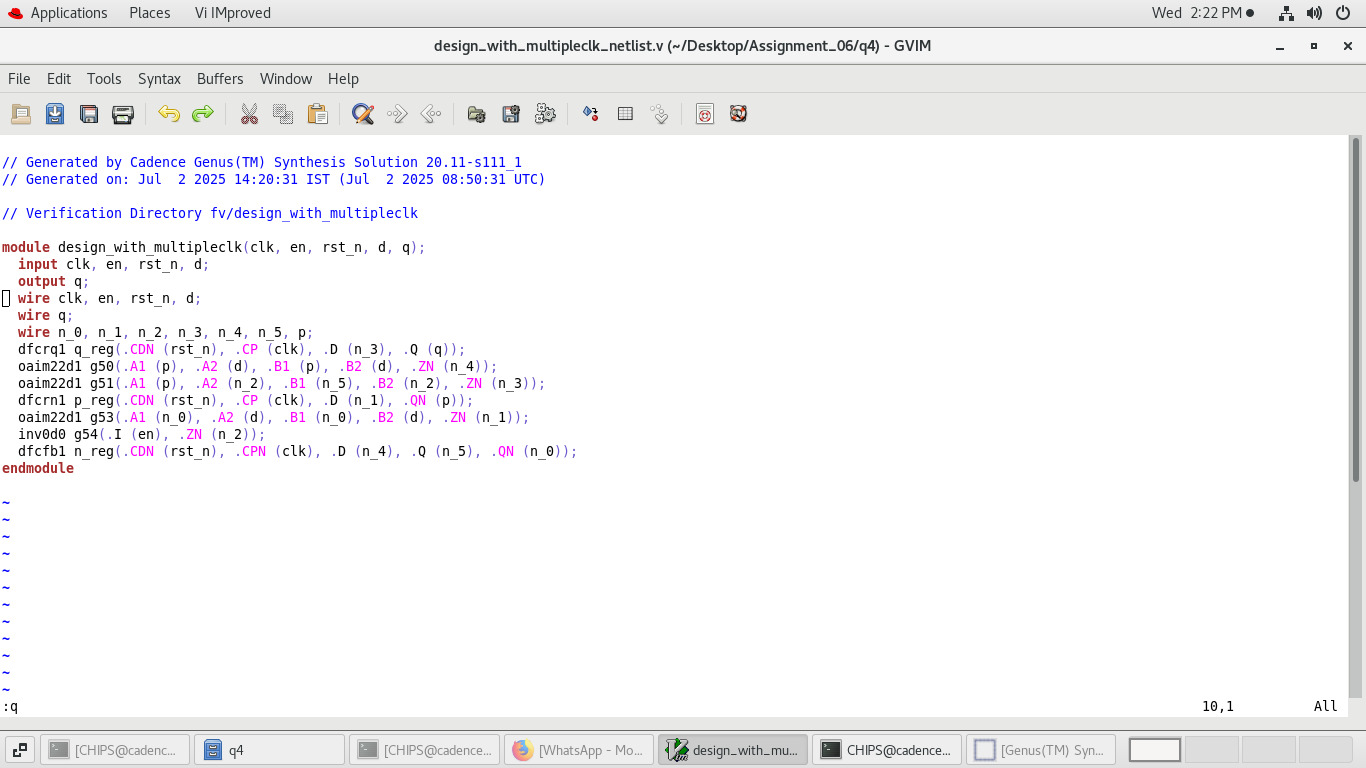
Flop name in Netlist:q\_reg

***4) design with multiple clock***

**Verilog:**



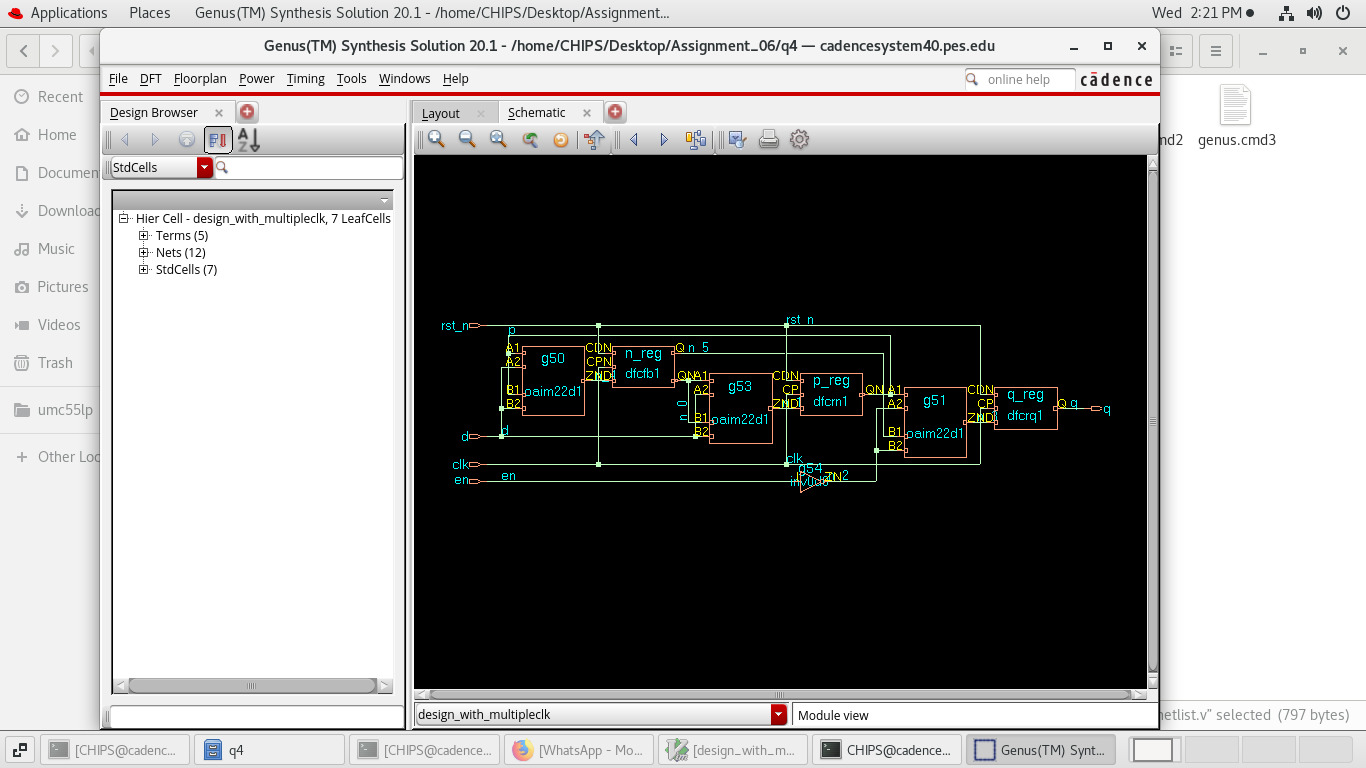
**Netlist:**



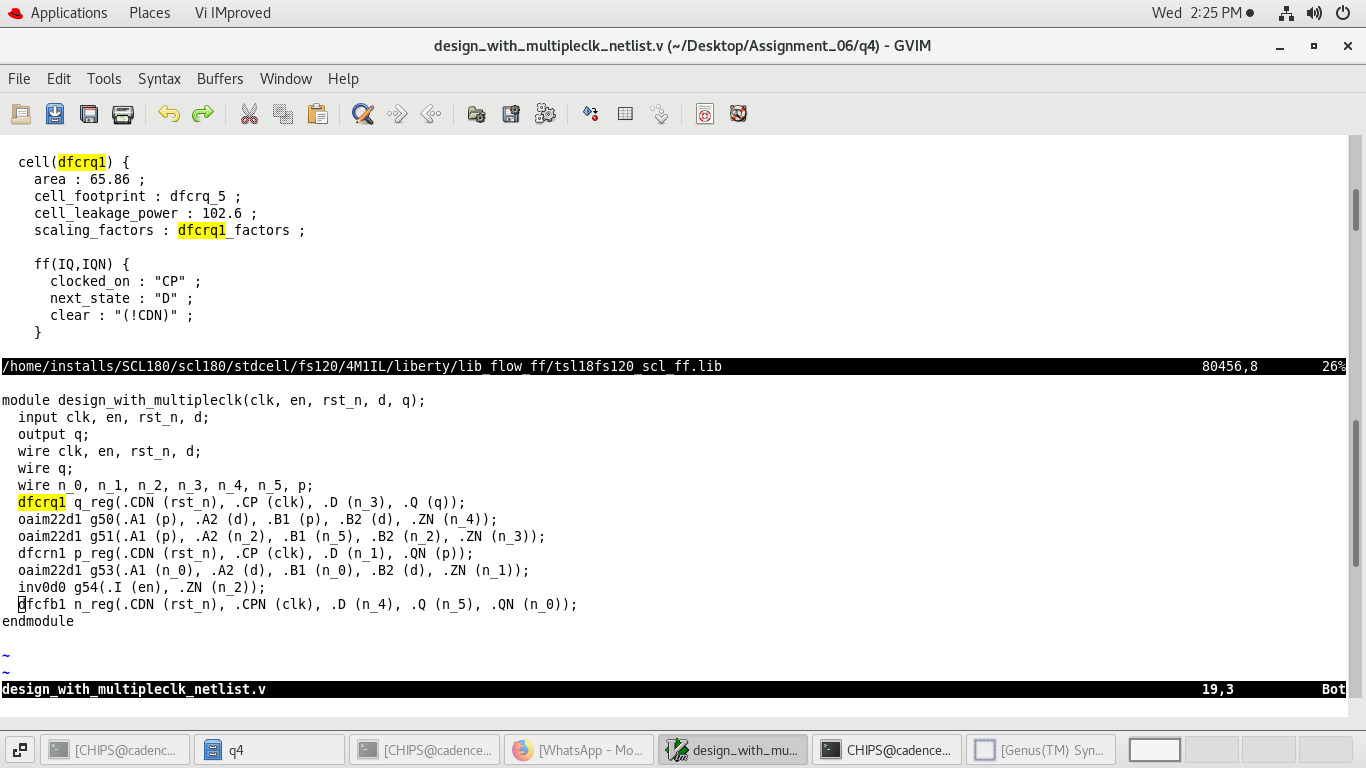
**Mark lib / instans / cell / nets**

1. n\_0 is traced and is driven by g53/B1 its load is n\_reg/QN
2. n\_1 is traced and is driven by g53/ZN its load is p\_reg/D
3. n\_2 is traced and is driven by g54/ZN its load is g51/A2
4. n\_3 is traced and is driven by g51/ZN its load is q\_reg/D
5. n\_4 is traced and is driven by g50/ZN its load is n\_reg/D
6. n\_5 is traced and is driven by g51/B1 its load n\_reg/Q

**Genus Schematic:**



**Lib mapping:**



Flop name rtl: p, n, q

Flop name in netlist:p\_reg, n\_reg, q\_reg