

**Tribhuvan University**  
**Faculty of Humanities & Social Sciences**  
**OFFICE OF THE DEAN**  
**2018**

**Bachelor in Computer Application**  
**Course Title: Digital Logic**  
**Semester: 1<sup>st</sup>**

**Full Marks:- 60**  
**Pass Marks:- 24**  
**Time:- 3hrs**

**Candidates are required to answer the questions in their own words as far as possible.**

**Group B**

**Attempt any SIX questions.**

**[6x5=30]**

11. Subtract 675.6 - 456.4 using 10's and 9's complement. [5]
12. What is universal logic gate? Realize NAND and NOR as universal logic gates. [1+2+2]
13. Simplify (using K-map) the given Boolean function F in both SOP and POS using don't care conditions A:  
 $F = B'C'D + BCD' + ABCD' + B'CD' + A'BC'D$  [2+3]
14. Define encoder. Draw logic diagram and truth table of octal-to-binary encoder. [1+4]
15. What is D flip-flop? Explain clocked RS flip-flop with its logic diagram and truth table. [1+4]
16. Design MOD-5 counter with state and timing diagram. [2+1+2]
17. Design a 4-bit serial into parallel-out shift register with timing diagram. [3+2]

**Group C**

**Attempt any TWO questions.**

**[2x10=20]**

18. Write difference between PLA and PAL. Design PLA circuit with given functions,  
 $F_1(A, B, C) = \sum (2, 3, 5)$   
 $F_2(A, B, C) = \sum (0, 4, 5, 7)$ . Design PLA program table also. [3+7]
19. Define D flip-flop. Design a Master-slave flip-flop by using JK flip-flop along with its circuit diagram and truth table. [2+8]
20. Write down the difference between asynchronous and synchronous counter. Design a 4-bit binary ripple counter along with its circuit, state and timing diagram. [3+7]