



Tribhuvan University

Faculty of Humanities & Social Sciences

OFFICE OF THE DEAN 2018

Bachelor in Computer Applications

Full Marks: 60

Course Title: Digital Logic

Pass Marks: 24

Code No: CACS 105

Time: 3 hours

Semester: Ist

Candidates are required to answer the questions in their own words as far as possible.

Group B

Attempt any SIX questions.

[6×5 = 30]

11. Subtract: $675.6 - 456.4$ using both 10's and 9's complement. [5]
12. What is university logic gate? Realize NAND and NOR as an universal logic gates. [1+2+2]
13. Simplify (using K- map) the given Boolean function F in both SOP and POS using don't care conditions D: $B'CD' + A'BC'D$
$$F = B'C'D' + BCD' + ABCD'$$
 [2+3]
14. Define encoder: Draw logic diagram and truth table of octal - to - binary encoder. [1 + 4]
15. What is D flip-flop? Explain clocked RS flip-flop with its logic diagram and truth table. [1+4]
16. Design MOD - 5 counter with state and timing diagram. [2+1+2]
17. Design a 4 - bit serial into parallel- out shift register with timing diagram. [3+2]

Group C

Attempt any TWO questions.

[2×10 = 20]

18. Write difference between PLA and PAL. Design a PLA circuit with given functions.
$$F_1(A, B, C) = \sum_{m=2,3,5}^{\times}$$

$$F_2(A, B, C) = \sum_{m=0,4,5,7}^{\times} (0, 4, 5, 7)$$
. Design PLA program table also. [3+7]
19. Define D flip-flop. Design a Master-slave flip-flop by using JK flip-flop along with its circuit diagram and truth table. [2+8]
20. Write down the difference between asynchronous and synchronous counter. Design a 4-bit binary ripple counter along with its circuit, state and timing diagram. [3+7]