MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : ES-201 (PART-II)

BASIC ELECTRICAL & ELECTRONIC ENGINEERING - II

Time Allotted : $1\frac{1}{2}$ Hours | *Full Marks* : 35

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

PART - II (Electronics)

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *five* of the following : $5 \times 1 = 5$

   i) A source follower using an FET has a voltage gain which is

      a) exactly unit but negative

      b) slightly less than unity but positive

      c) greater than + 100

      d) none of these.

ii) The threshold voltage of an enhancement PMOS is

a) Positive

b) Negative

c) Zero with respect to drain

d) Zero with respect to source.

iii) The slew rate of an ideal OP-AMP is

a) Zero b) Infinite

c) Exactly unity d) none of these.

iv) Which of the following feedback topologies offers high input and output impedance ?

a) Voltage series b) Voltage shunt

c) Current series d) Current shunt.

v) Which of the following gate is called 'coincidence' gate ?

a) AND b) X-OR

c) NAND d) X-NOR.

vi) The decimal equivalent of 10111·1011 is

a) 25·125 b) 32·4185

c) 23·6875 d) 32·6785.

GROUP – B
(Short Answer Type Questions)

Answer any *two* of the following. $2 \times 5 = 10$

2. With proper sketch explain the drain characteristics of an *n*-channel JFET.

3. Derive suitable expressions to show the effects of negative feedback on input and output impedances of an amplifier. $2\frac{1}{2} + 2\frac{1}{2}$

4. Mention the differences between ideal and practical Op-Amp. What do you mean by virtual ground in an Op-Amp ? 3 + 2

5. a) What do you mean by Universal gates ? 2

   b) Realise the following expression using NOR gates only —

   $Y = A'B' + AB.$ 3

GROUP – C
(Long Answer Type Questions)

Answer any *two* of the following. $2 \times 10 = 20$

6. a) Determine the value of g_{mo} for the graph shown in the Figure 1 :

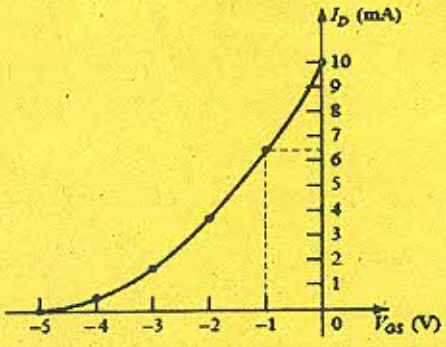

Figure 1

b) Find out g_m for $V_{gs} = -1.5$ V.

c) Draw the Transfer Characteristics of an N-Ch FET. Explain the curve with the help of Shockley's Equation.

d) Draw the small signal equivalent circuits for an FET.

e) The Fixed Bias circuit has operating point defined by $V_{gs} = -2$ V, $I_{DQ} = 5.625$ mA as shown in Figure 2. If the output conductance is 40 μS then find the following :

i) g_m

ii) r_d

iii) R_i

iv) R_o

v) A_v.

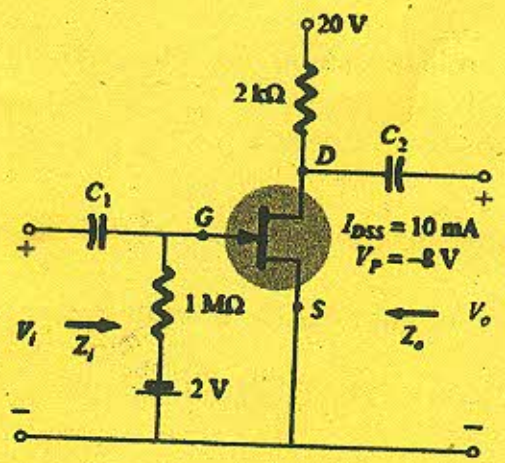

Figure 2

1 + 1 + 2 + 3 + 3

7. a) Design an adder circuit using an Op-Amp to get the output expression as –

$V_{out} = V_1 + 10V_2 + 100V_3$, where V_1, V_2, V_3 are inputs to the Op-Amp and R_F = 100 K.

b) How can an Op-Amp be used as an integrator ?

c) What is an integrated circuit ? What are its advantages ? 3 + 4 + (1 + 2)

8. a) State and explain the Barkhausen criteria.

b) Derive an expression for the gain of an amplifier using positive feedback.

c) A negative feedback of $\beta = 0.002$ is applied to an amplifier of gain 1000. Calculate the change in the overall gain of the feedback amplifier if the internal gain of the amplifier is subjected to gain reduction of 15%.

d) How does negative feedback affects the bandwidth of an amplifier ? 3 + 2 + 3 + 2

9. Write short notes on any *two* of the following : 2 × 5

a) Enhancement type MOSFET

b) Feedback amplifier topologies

c) De Morgan's theorem

d) CMRR and Slew rate

e) Pinch-off condition to JFET

f) Emitter-follower circuit