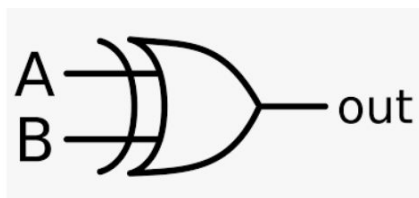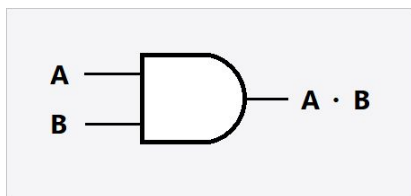# EXPERIMENT-3

AIM: To verify the operation of a half and full adder.

HARDWARE / SOFTWARE APPARATUS : Power supply , bread board , connecting wires , respective IC
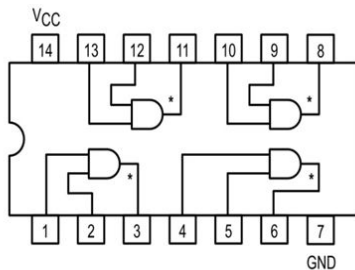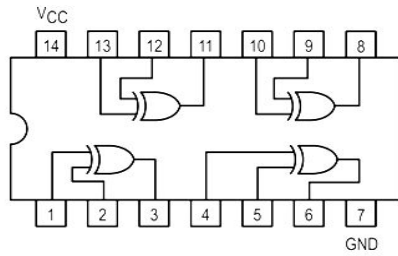
(7408,7486)

CIRCUIT:

AND GATE

PIN-DIAGRAM:

AND GATE

XOR GATE

TRUTH TABLE:

AND Truth Table		
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

XOR Truth Table		
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Input			Output	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

THEORY: Half adder can add two bits individually. The output of a half adder has a sum bit and carries for the sum bit.

Similarly, the full adder can be used to add three bits together.

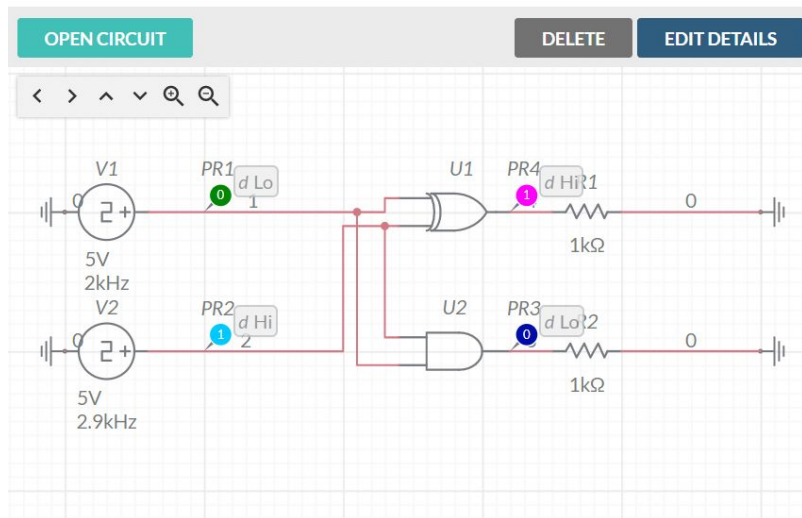Both these adders can be formed by using the logic gates of and and xor.

The full adder can also be seen as a sum of two individual half adders.

PROCEDURE (MULTISIM):

- Select the required gate symbol from the digital section of the tool bar on the left .
- Select a resistor from the same toolbar.
- Select the voltage sources and ground symbols from that toolbar.
- Ground both the voltage sources(clock) and then connect them to the input terminal of the gate.
- Connect the output terminal to 1kohm resistor and ground it.

CIRCUIT DIAGRAMS:

HALF ADDER

V1
5V
2kHz

V2
5V
2.9kHz

PR1 *d Lo*
PR2 *d Hi*
PR4 *d Hi*R1
1kΩ
PR3 *d Lo*R2
1kΩ

U1
U2

FULL ADDER

A *d Lo*
d Lo
U1
U2
SUM *d Lo*R1
1kΩ
U3
C *d Lo*
U4
U5
CARR *d Lo*
1kΩ

V1
5V
2kHz

V2
5V
2.9kHz

V3
5V
3.9kHz
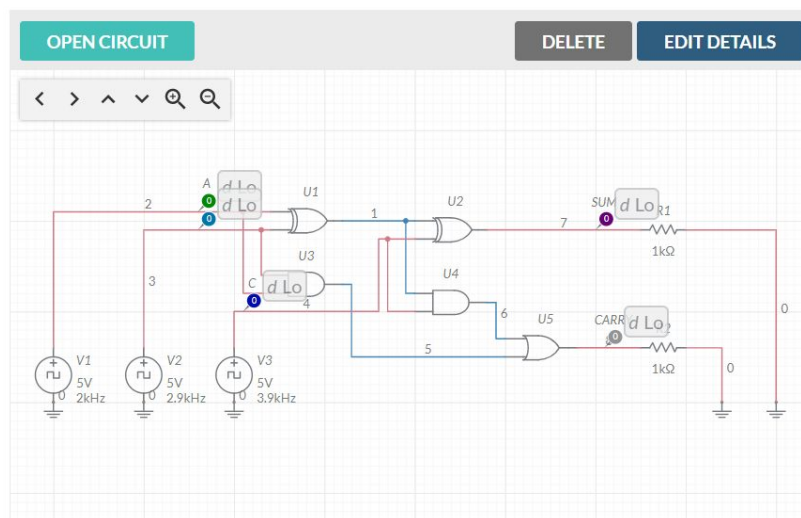
 INPUT /OUTPUT WAVEFORMS:

HALF ADDER

Circuit Graph

Interactive 1

FULL ADDER

Circuit Graph ✕

Interactive 1
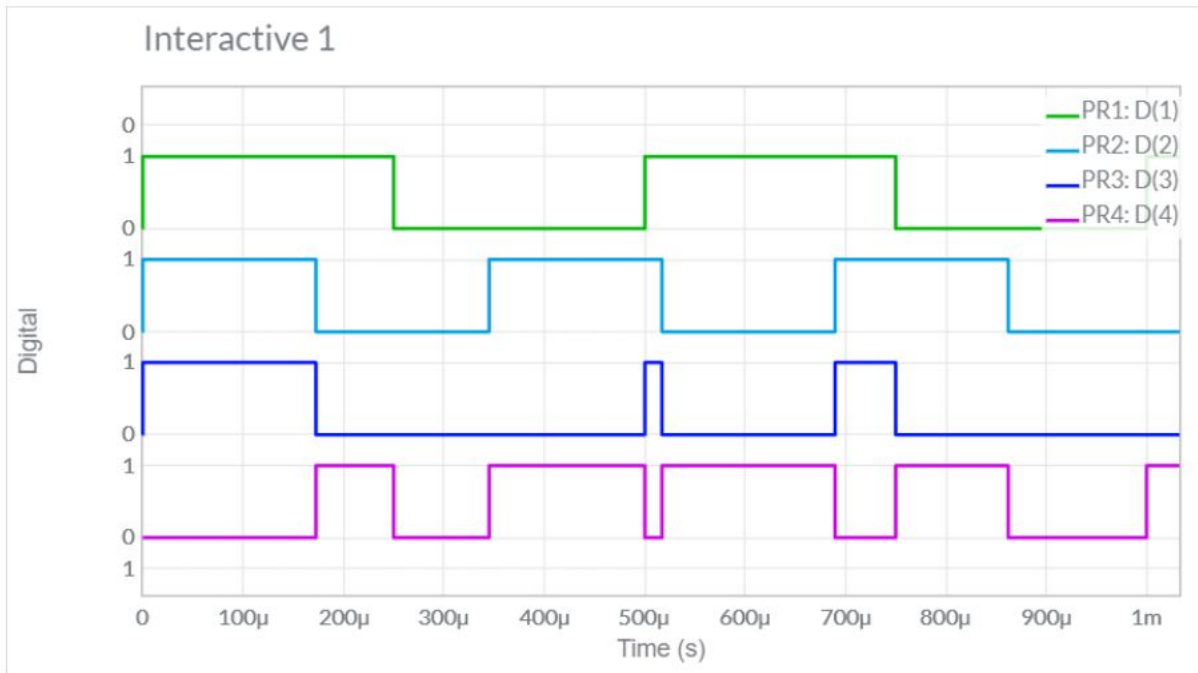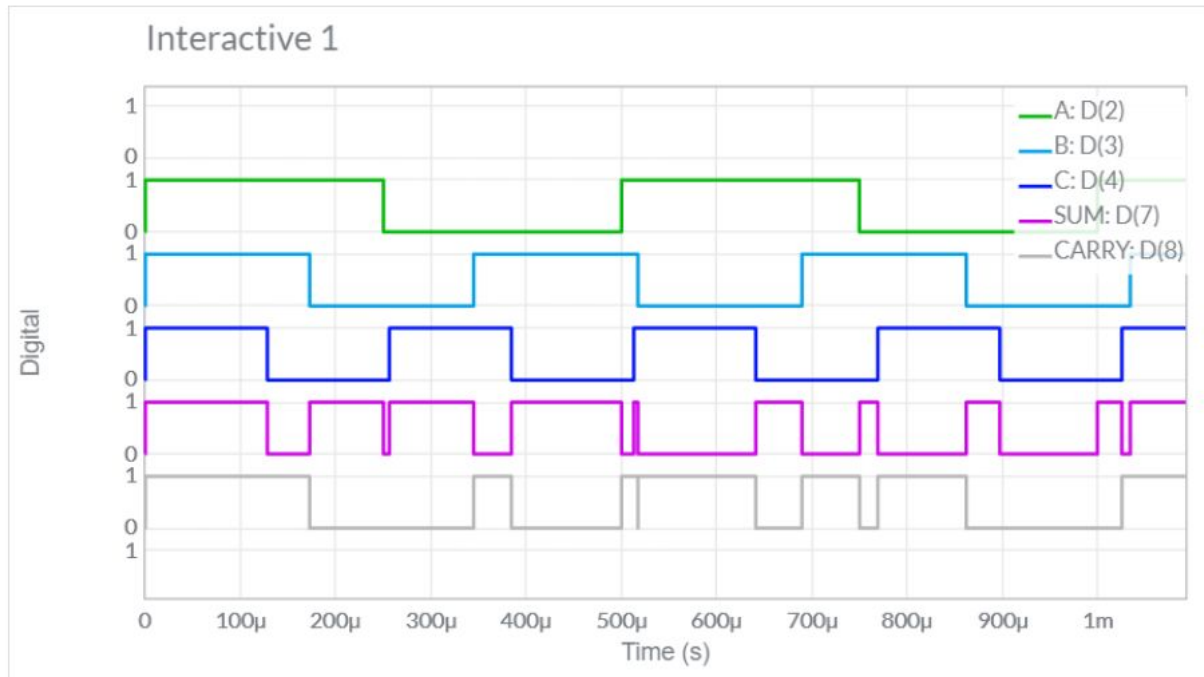
PRECAUTIONS:

- Power supply should not exceed than 5V.
- Connections should be tight.
- Components should be tested before the practical.