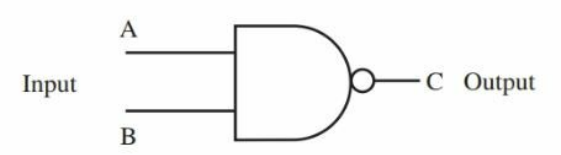
EXPERIMENT-2a

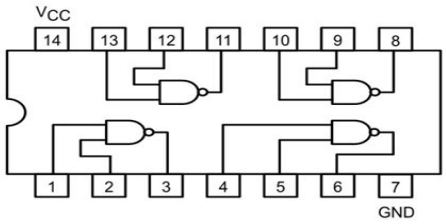
AIM: To realize all the gates using NAND gate

HARDWARE / SOFTWARE APPARATUS : Power supply , Bread Board , Connecting Wires, respective IC (7400)

CIRCUIT:



PIN-DIAGRAM:



TRUTH TABLE:

NAND Truth Table		
A	**B**	**Q**
0	0	1
0	1	1
1	0	1
1	1	0

THEORY: NAND gate is actually a combination of two logic gates: AND and NOT gate it's output is complement of AND gate

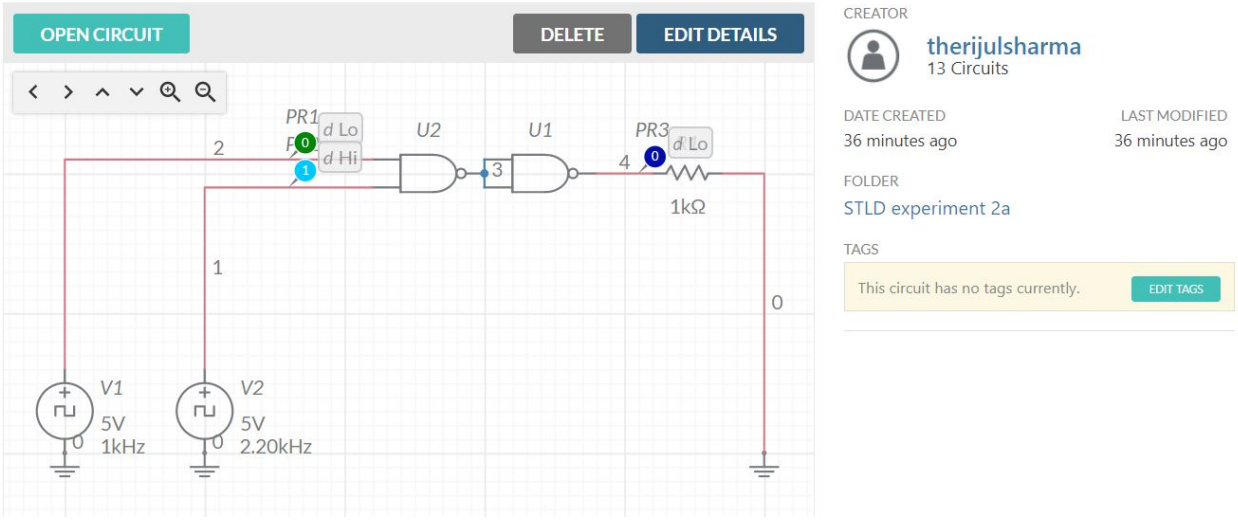
This gate can have a minimum of two inputs while the output is limited to one. Using this gate, we can realise all other gates. This is why this gate is also known as a universal gate.

PROCEDURE (MULTISIM):

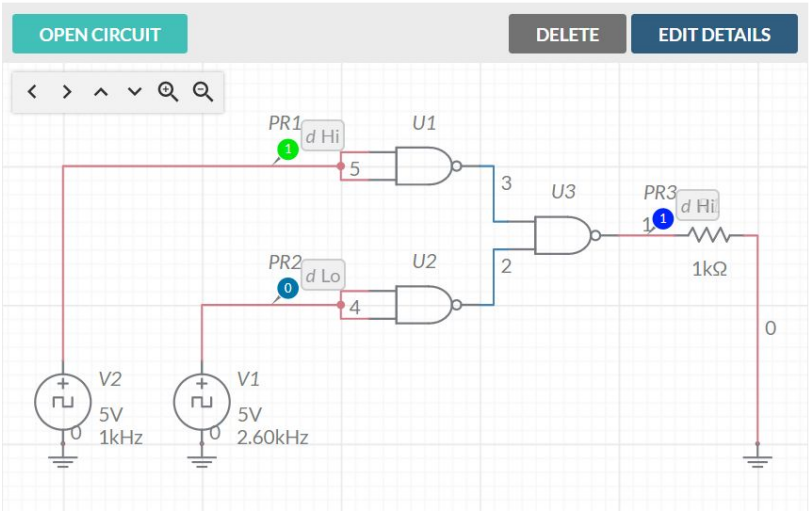
- Select the gate symbol from the digital section of the tool bar on the left .
- Select a resistor from the same toolbar.
- Select the voltage sources and ground symbols from that toolbar.
- Ground both the voltage sources(clock) and then connect them as in the circuit diagram so as to recreate a different gate.
- Connect the output terminal to 1kohm resistor and ground it.

CIRCUIT DIAGRAMS:

AND GATE



OR GATE



CREATOR
therijulsharma
13 Circuits

DATE CREATED
28 minutes ago

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FOLDER
STLD experiment 2a

TAGS
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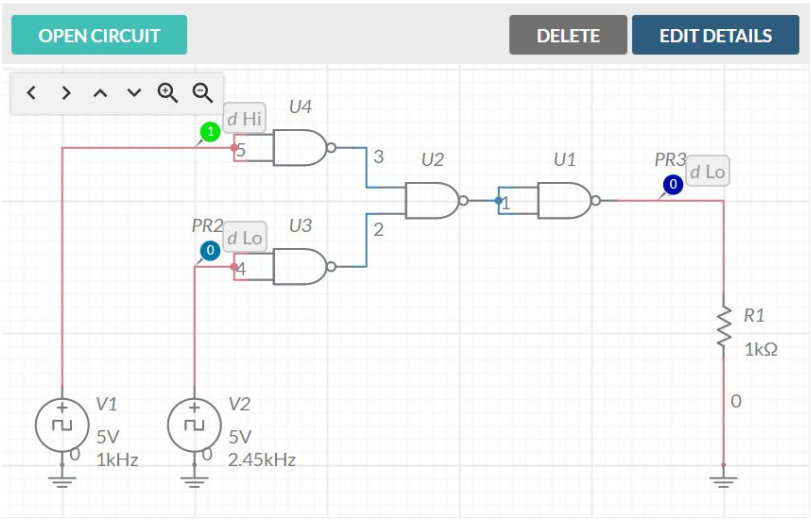
NOR GATE



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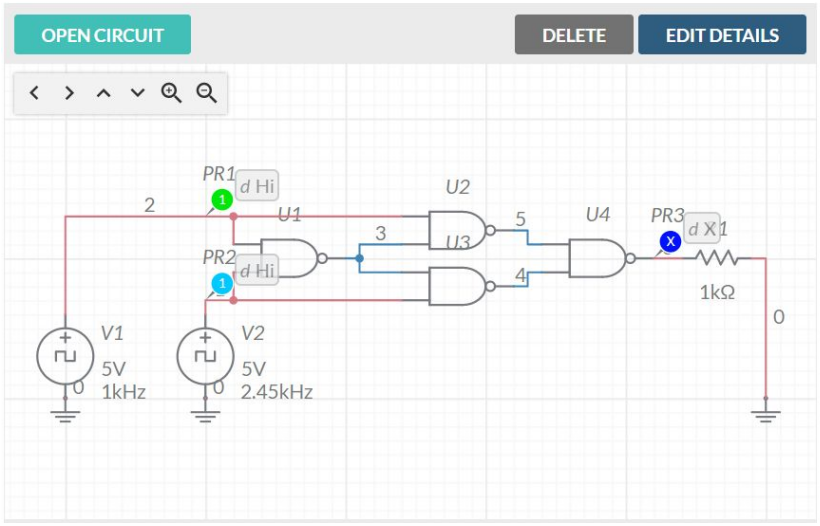
XOR GATE



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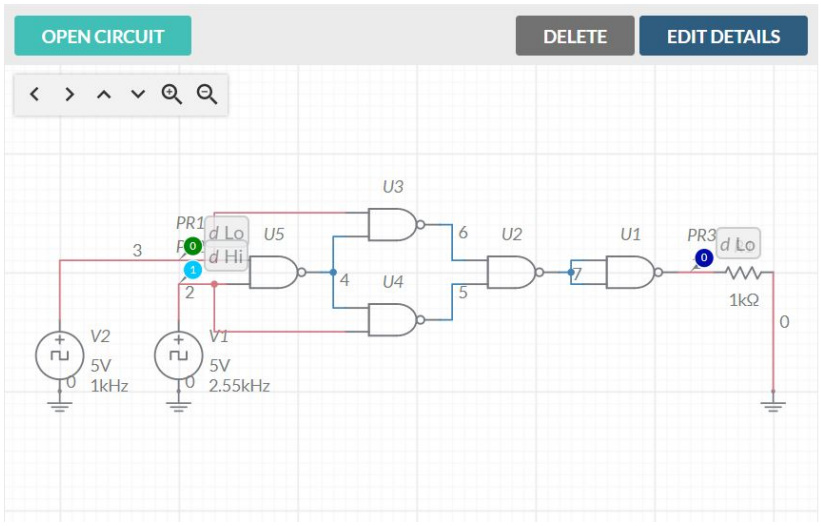
XNOR GATE



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FOLDER
STLD experiment 2a

TAGS
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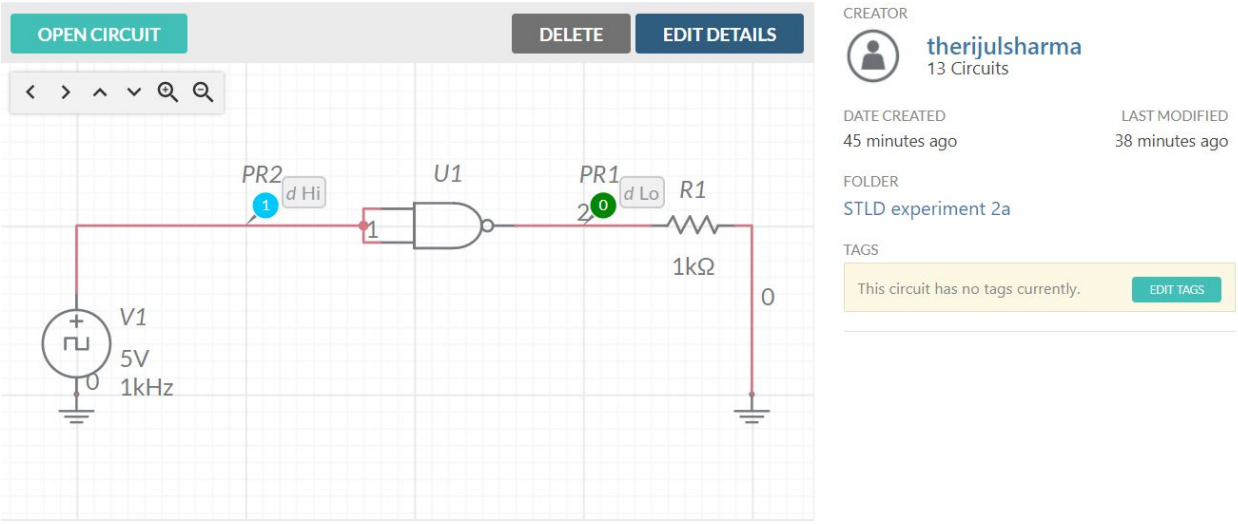
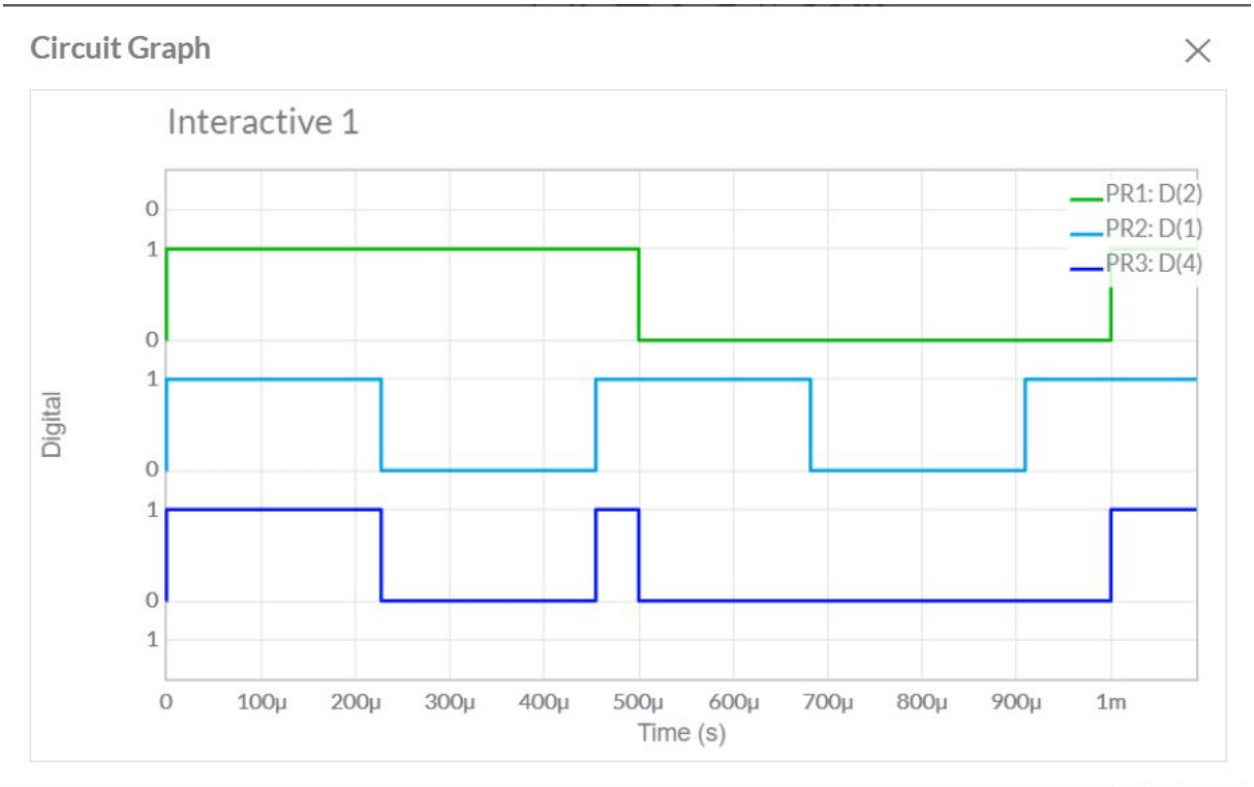
NOT GATE

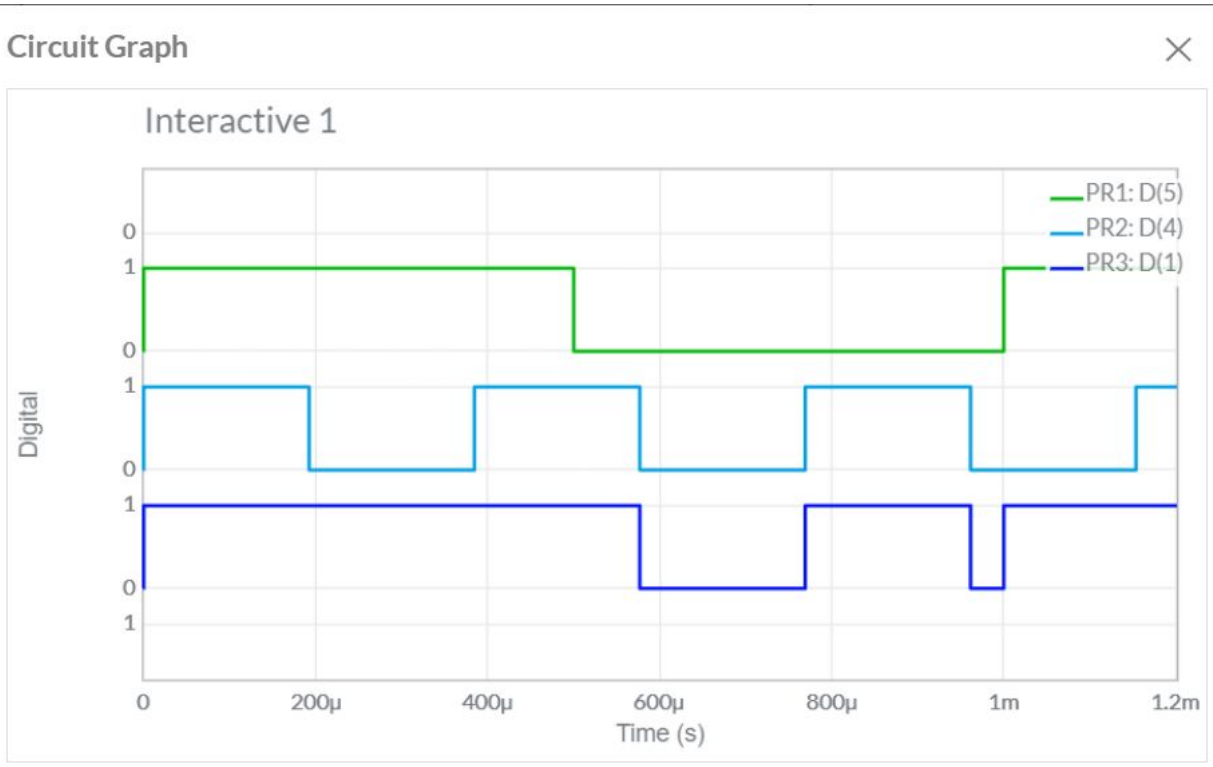


INPUT /OUTPUT WAVEFORMS:

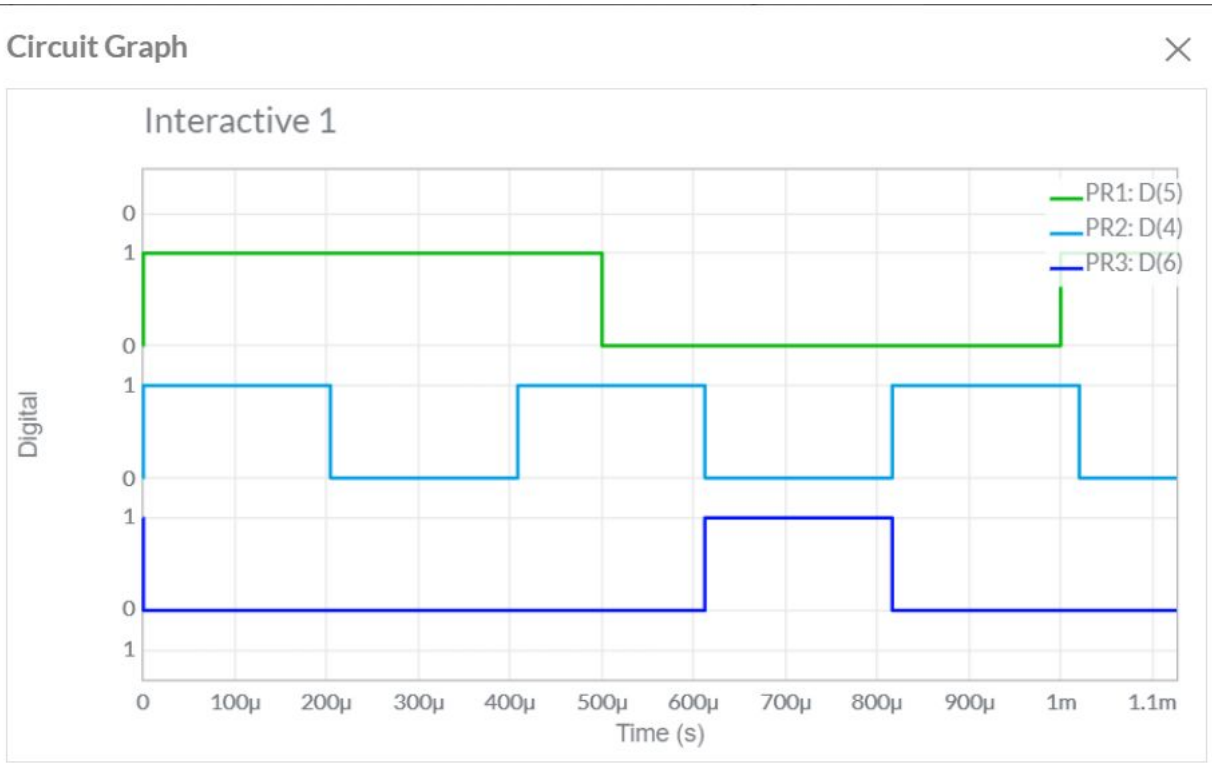
AND GATE



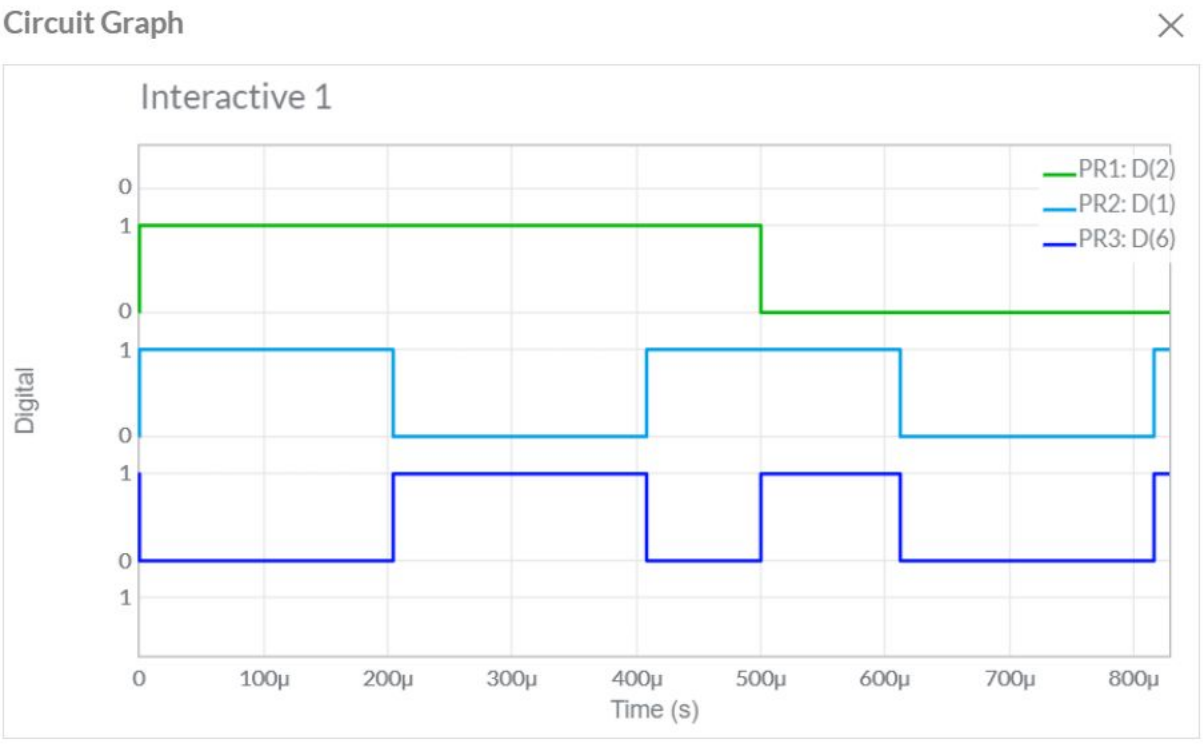
OR GATE


Circuit Graph
Interactive 1
PR1: D(5)
PR2: D(4)
PR3: D(1)
Digital
0
1
0
1
0
1
0
1
0
200µ
400µ
600µ
800µ
1m
1.2m
Time (s)

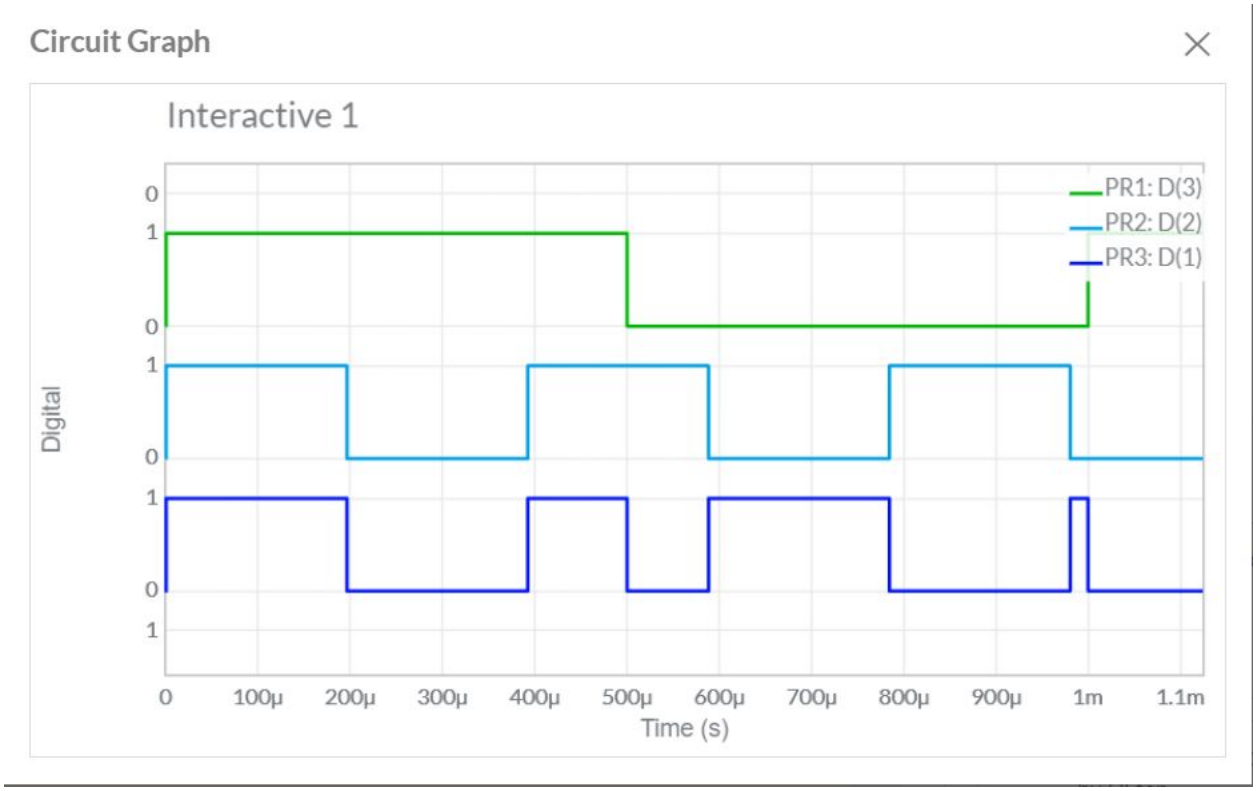
NOR GATE


Circuit Graph
Interactive 1
PR1: D(5)
PR2: D(4)
PR3: D(6)
Digital
0
1
0
1
0
1
0
1
0
100µ
200µ
300µ
400µ
500µ
600µ
700µ
800µ
900µ
1m
1.1m
Time (s)

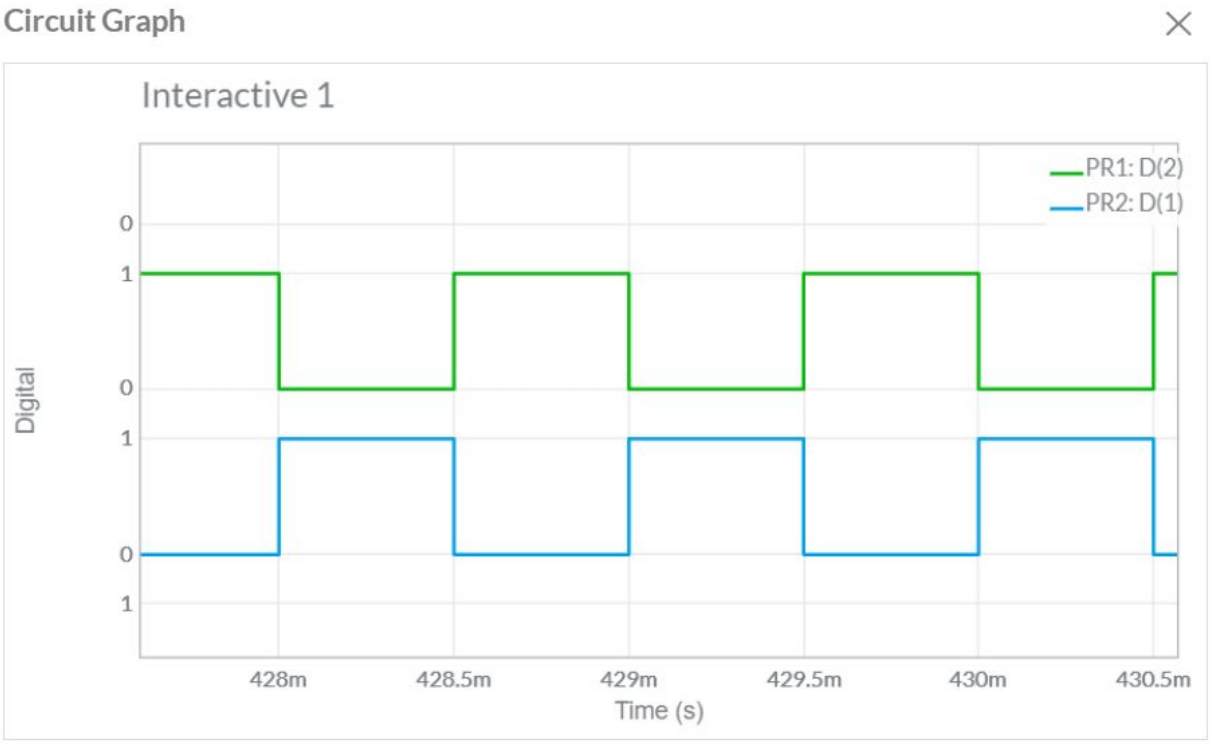
XOR GATE


Circuit Graph
Interactive 1
PR1: D(2)
PR2: D(1)
PR3: D(6)
Digital
0
1
0
1
0
1
0
1
0
100µ
200µ
300µ
400µ
500µ
600µ
700µ
800µ
Time (s)

XNOR GATE


Circuit Graph
Interactive 1
PR1: D(3)
PR2: D(2)
PR3: D(1)
Digital
0
1
0
1
0
1
0
1
0
100µ
200µ
300µ
400µ
500µ
600µ
700µ
800µ
900µ
1m
1.1m
Time (s)

NOT GATE



PRECAUTIONS:

- Power supply should not exceed 5V.
- All the connections should be tight.
- Components should be tested before the practical.