EXPERIMENT-10

AIM: To design a JK flip flop using NAND gate

HARDWARE / SOFTWARE APPARATUS : Power supply , bread board , connecting wires , respective IC

TRUTH TABLE:

Inputs		Outputs	
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

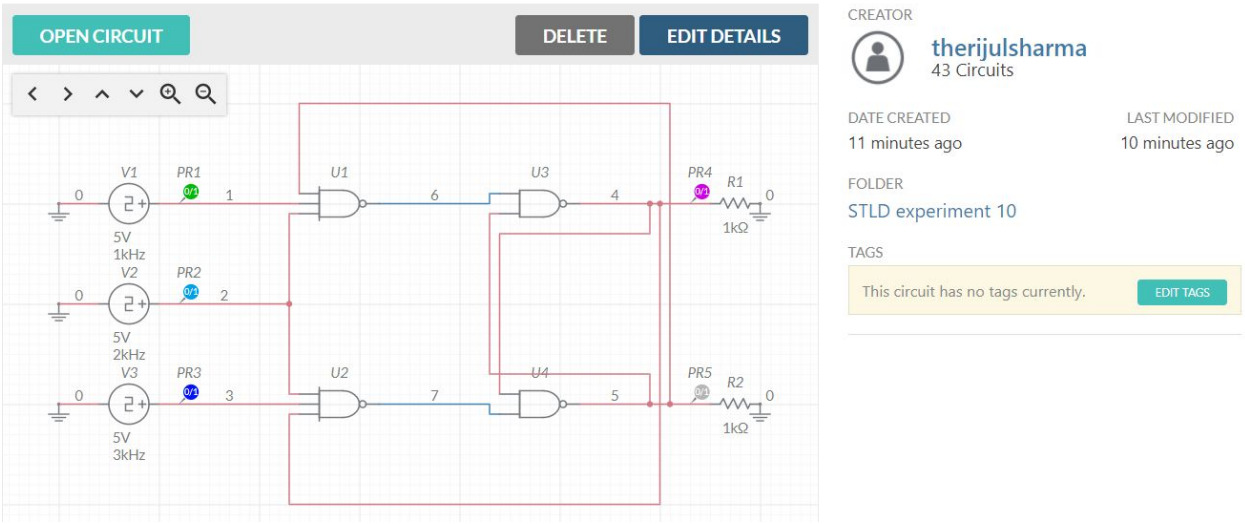
THEORY: The JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”. Due to this additional clocked input, a JK flip-flop has four possible input combinations, “logic 1”, “logic 0”, “no change” and “toggle”. The symbol for a JK flip flop is similar to that of an SR Bistable Latch as seen in the previous tutorial except for the addition of a clock input.

PROCEDURE (MULTISIM):

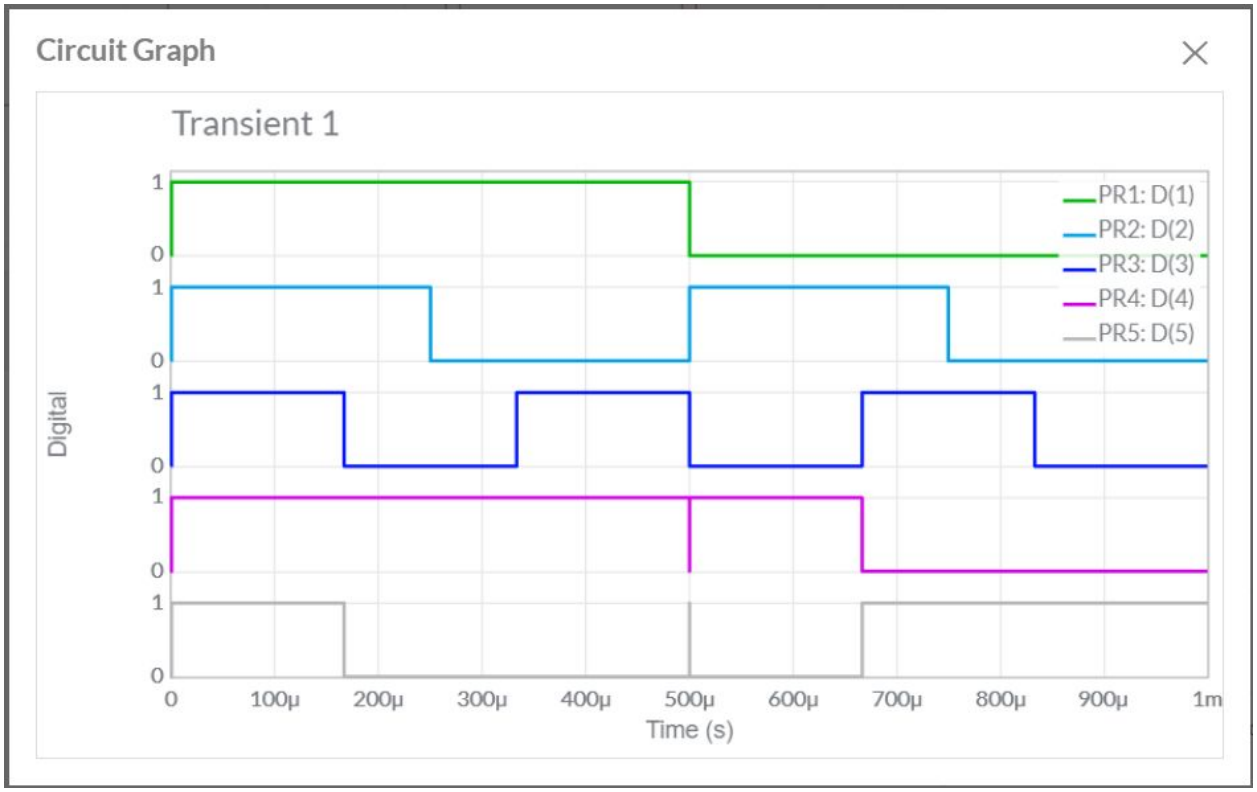
- Select the required gate symbol from the digital section of the tool bar on the left .
- Select a resistor from the same toolbar.
- Select the voltage sources and ground symbols from that toolbar.
- Ground both the voltage sources(clock) and then connect them to the input terminal of the gate.

- Connect the output terminal to 1kohm resistor and ground it.

CIRCUIT DIAGRAMS:



INPUT /OUTPUT WAVEFORMS:



PRECAUTIONS:

- Power supply should not exceed more than 5V.
- Connections should be tight.
- Components should be tested before the practical.