VLSI LABORATORY EXPERIMENT

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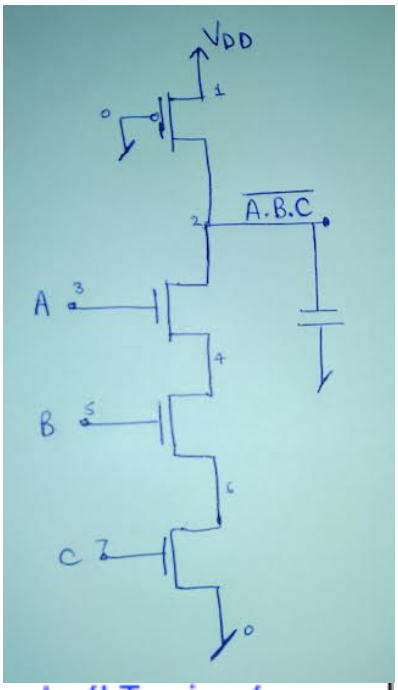
AIM

Simulate following 3 input Psedo NMOS gates

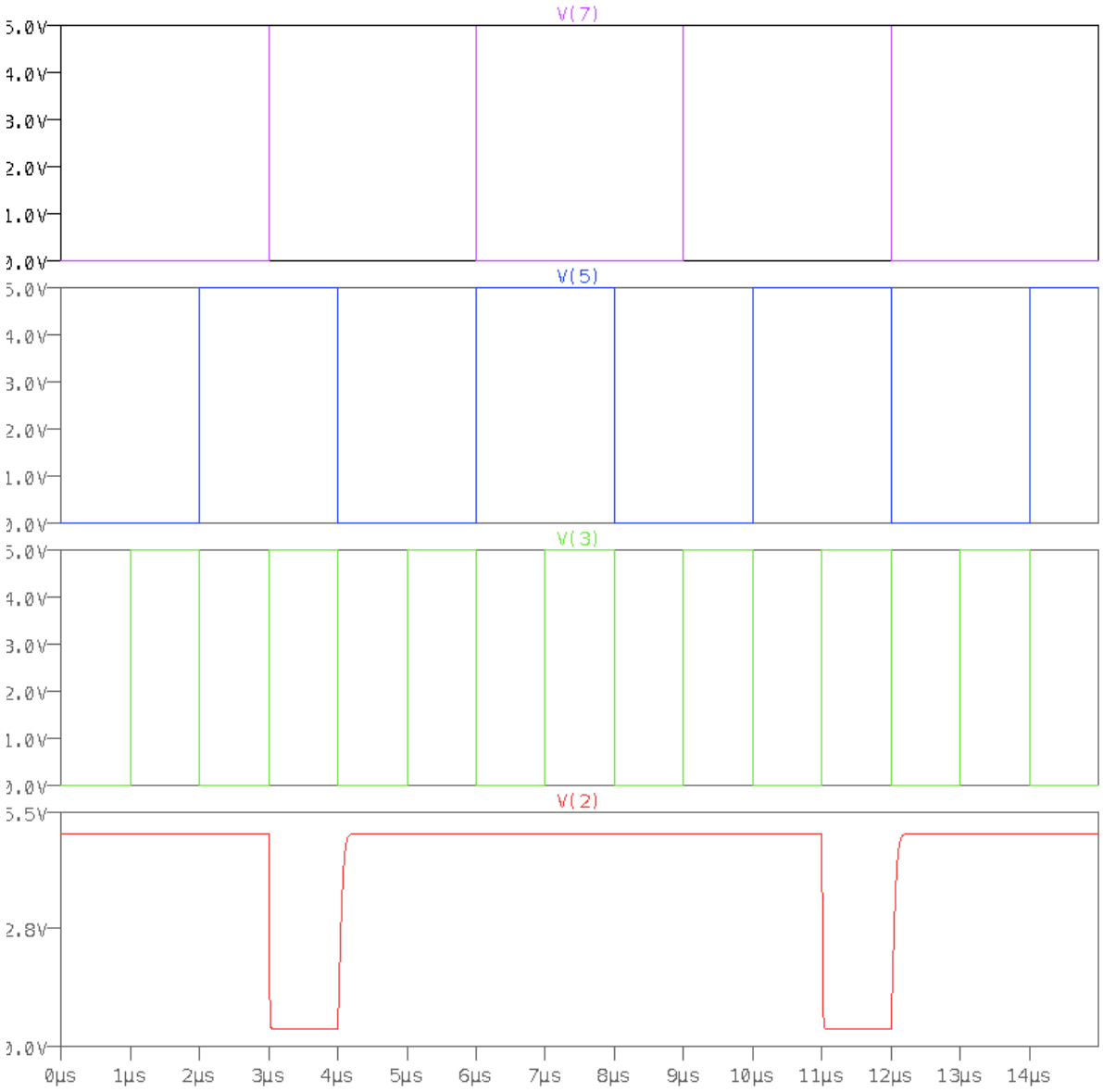
a. **NAND Gate**
b. **NOR Gate**



A. NAND GATE

Circuit:

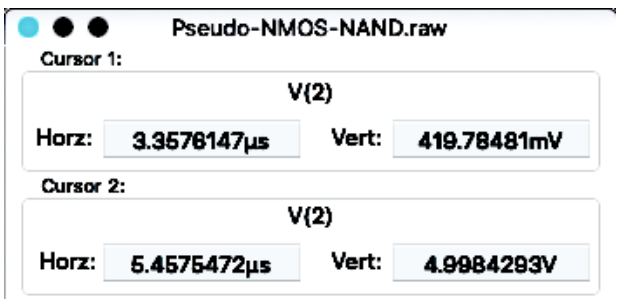
```
.include /Users/sanujkul/Documents/LTspice/
Workspace/VLSI/libraries/180nm_model.txt

*MSOFETS
*NMOS - Driver
M1 2 3 4 4 N_180 w=1.25u l=.18u
M2 4 5 6 6 N_180 w=1.25u l=.18u
M3 6 7 0 0 N_180 w=1.25u l=.18u
*PMOS - Load
M4 2 0 1 1 P_180 w=0.2u l=.18u

Cl 2 0 4p

Vdd 1 0 DC 5v

*Vid 100 0 PULSE(0 5V 0.2us 0.1fs 0.1fs 1us 2us)
Va 3 0 PULSE(0 5v 1us 0.1fs 0.1fs 1us 2us)
Vb 5 0 PULSE(0 5v 2us 0.1fs 0.1fs 2us 4us)
Vc 7 0 PULSE(0 5v 3us 0.1fs 0.1fs 3us 6us)

.TRAN 0 15us
```



Observation

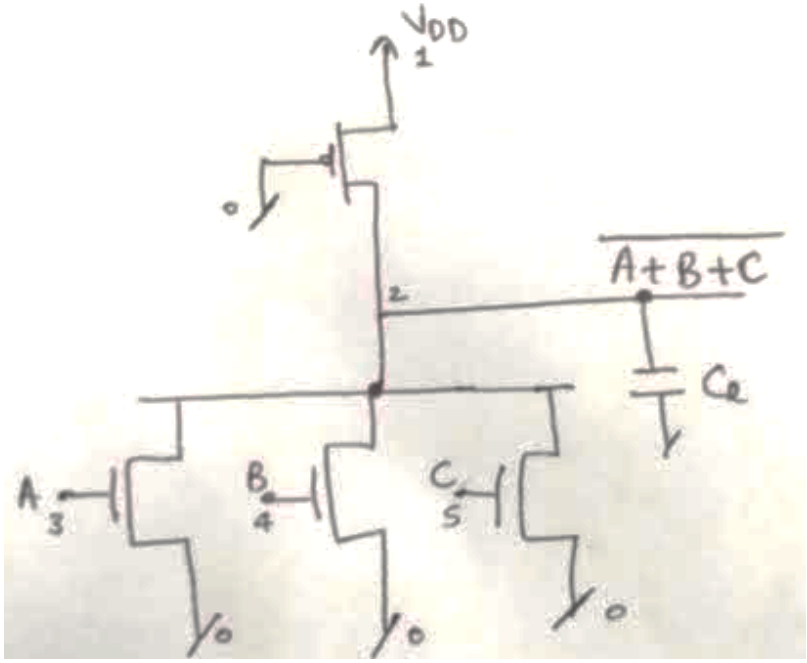
1. Output goes LOW only when
   a. A = 1
   b. B = 1
   c. C = 1

   Otherwise it remains HIGH.
2. V_{OH} = 4.998V
3. V_{OL} = 0.419V



B. NOR GATE

Circuit



Code

```
*4 input Pseudo NMOS NAND Gate
.include /Users/sanujkul/Documents/LTspice/Workspace/VLSI/libraries/
180nm_model.txt

*MSOFETS
*NMOS - Driver
M1 2 3 0 0 N_180 w=1.25u l=.18u
M2 2 4 0 0 N_180 w=1.25u l=.18u
M3 2 5 0 0 N_180 w=1.25u l=.18u
*PMOS - Load
M4 2 0 1 1 P_180 w=0.25u l=.18u

Cl 2 0 4p

Vdd 1 0 DC 5v

*Vid 100 0 PULSE(0 5V 0.2us 0.1fs 0.1fs 1us 2us)
Va 3 0 PULSE(0 5v 1us 0.1fs 0.1fs 1us 2us)
Vb 4 0 PULSE(0 5v 2us 0.1fs 0.1fs 2us 4us)
Vc 5 0 PULSE(0 5v 3us 0.1fs 0.1fs 3us 6us)

.TRAN 0 15us
```

Observations:

1. Output goes LOW only either of A, B, C is LOW.
   Otherwise it remains HIGH.
2. V_{OH} = 4.994V
3. V_{OL} = 0V