VLSI LABORATORY EXPERIMENT

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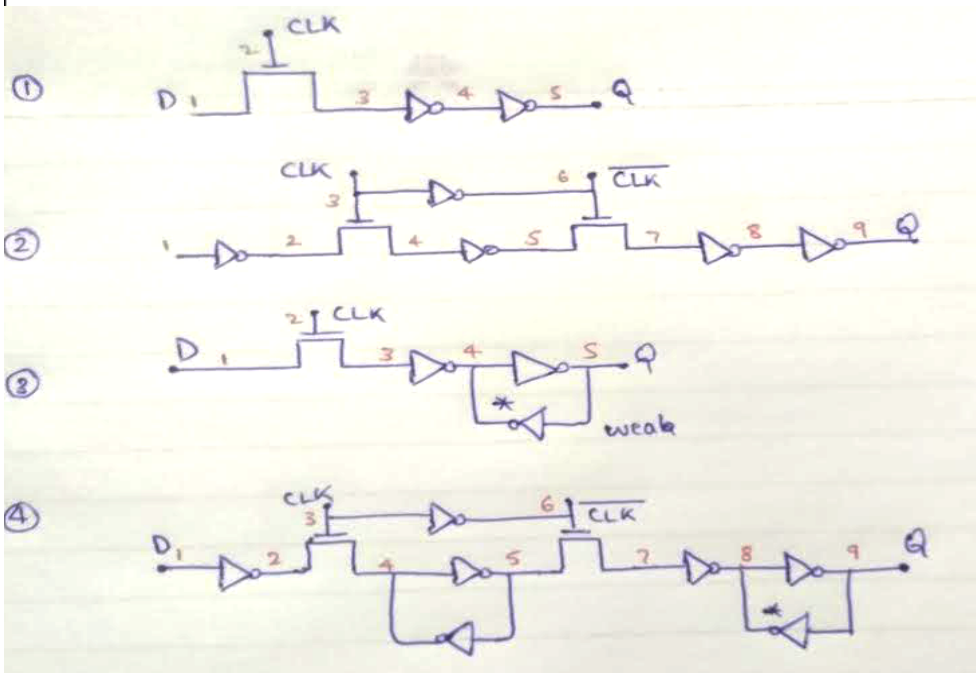
AIM

Simulate following using pass transmission logic

a. **Dynamic D-Latch**
b. **Dynamic D Flip Flop**
c. **Static D-Latch**
d. **Static D Flip Flop**

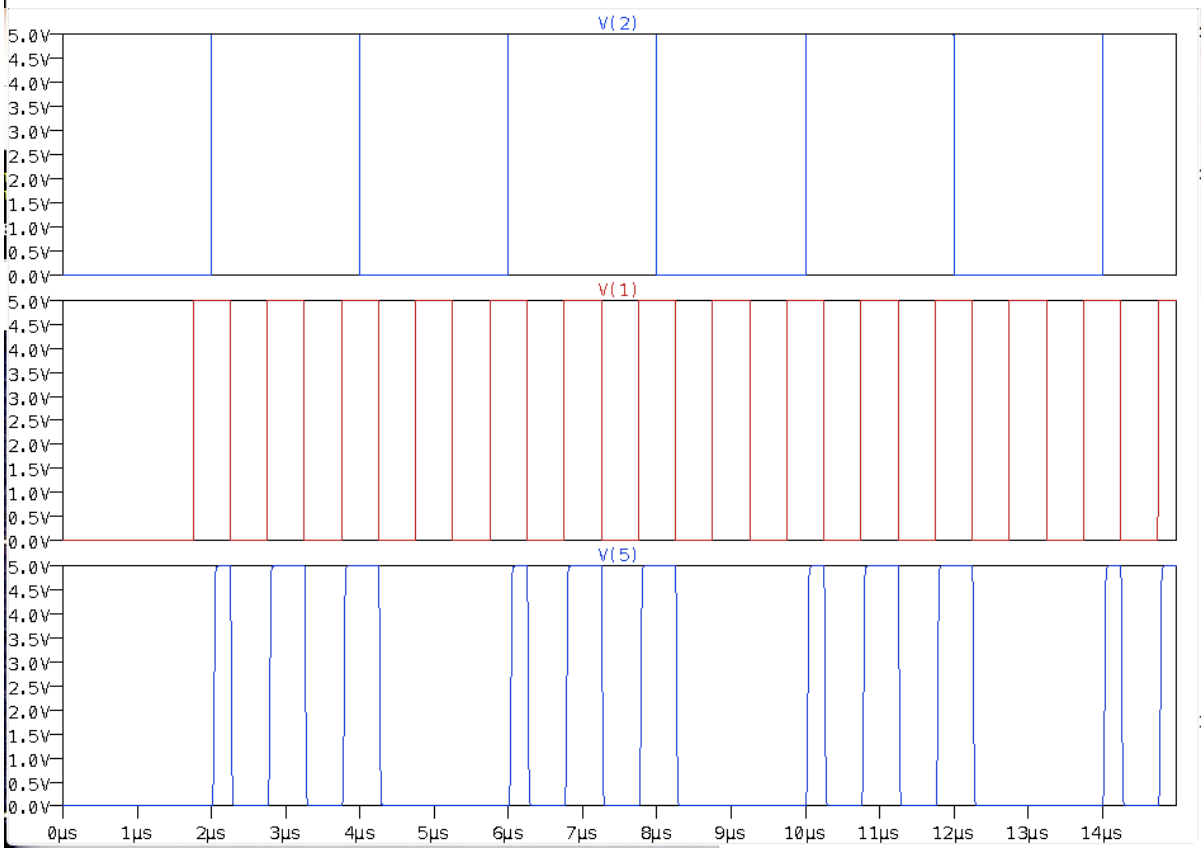
(I) For easy coding, making a SUBCKT of CMOS NOT Gate and WEAK CMOS NOT GATE. It will be included in all four netlists of this experiment.

```
*Following is circuit implementation of CMOS NOT GATE
* 1 - Vdd
* 2 - Input
* 3 - Output

*********************************************************************
.SUBCKT CMOS_NOT 2 3 1

*Use following statement to vary model parameters
.include /Users/sanujkul/Documents/LTspice/libraries/180nm_model.txt

M1 3 2 1 1 P_180 w=5u l=.18u
M2 3 2 0 0 N_180 w=1.25u l=.18u

.ENDS CMOS_NOT
*********************************************************************
.SUBCKT CMOS_WEAK_NOT 2 3 1

*Use following statement to vary model parameters
.include /Users/sanujkul/Documents/LTspice/libraries/180nm_model.txt

M1 3 2 1 1 P_180 w=0.36u l=.18u
M2 3 2 0 0 N_180 w=0.36u l=.18u

.ENDS CMOS_NOT
```



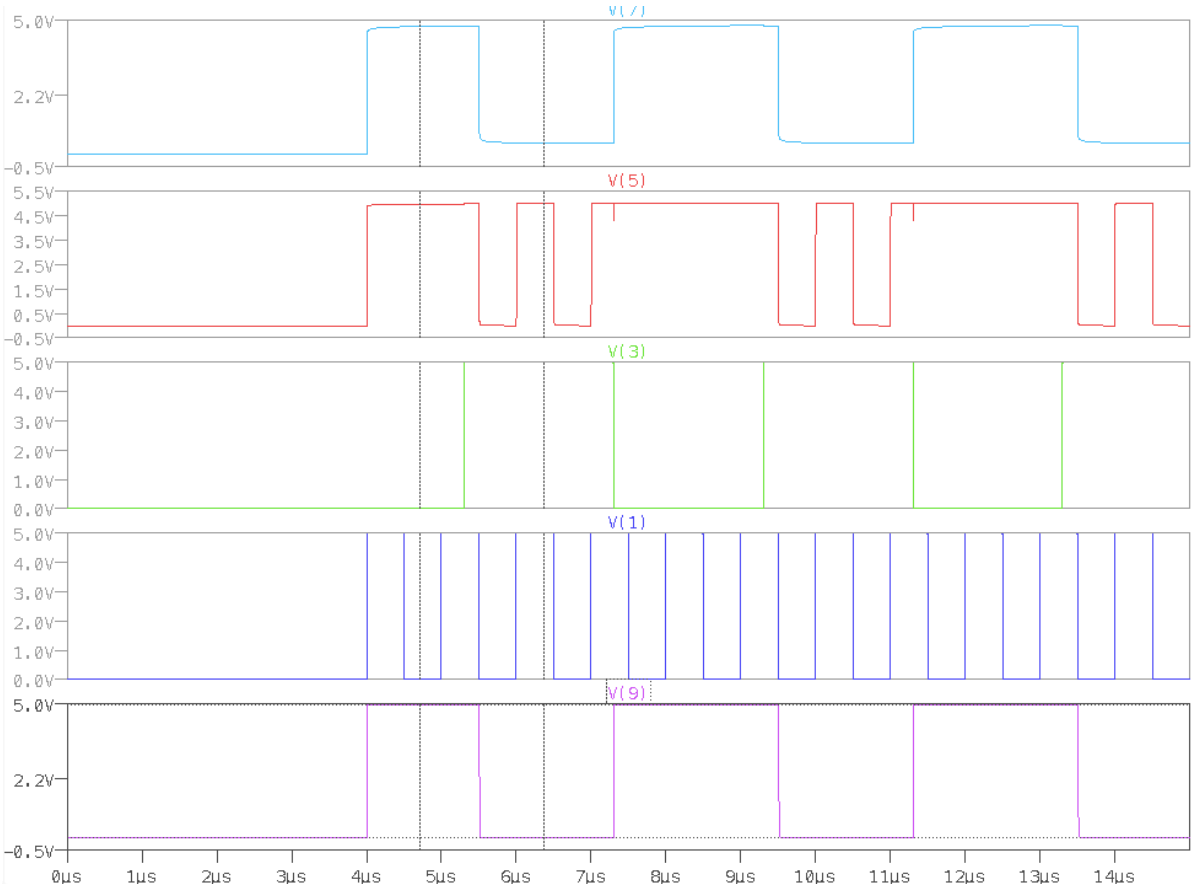
A. Dynamic D-Latch

```
.include /Users/sanujkul/Documents/LTspice/libraries/180nm_model.txt
.include /Users/sanujkul/Documents/LTspice/Workspace/VLSI/libraries/CMOS-NOT.cir

M2 1 2 3 3 N_180 w=1.25u l=.18u

XNOT1 3 4 6 CMOS_NOT
XNOT2 4 5 6 CMOS_NOT

Vdd 6 0 DC 5v

C3 3 0 10p
C4 4 0 10p
C5 5 0 10p

Vd 1 0 PULSE(0 5v 1.75us 0.1fs 0.1fs 0.5us 1us)
Vclk 2 0 PULSE(0 5v 2us 0.1fs 0.1fs 2us 4us)

***** OUTPUT CODES **********
.TRAN 0 15us
```



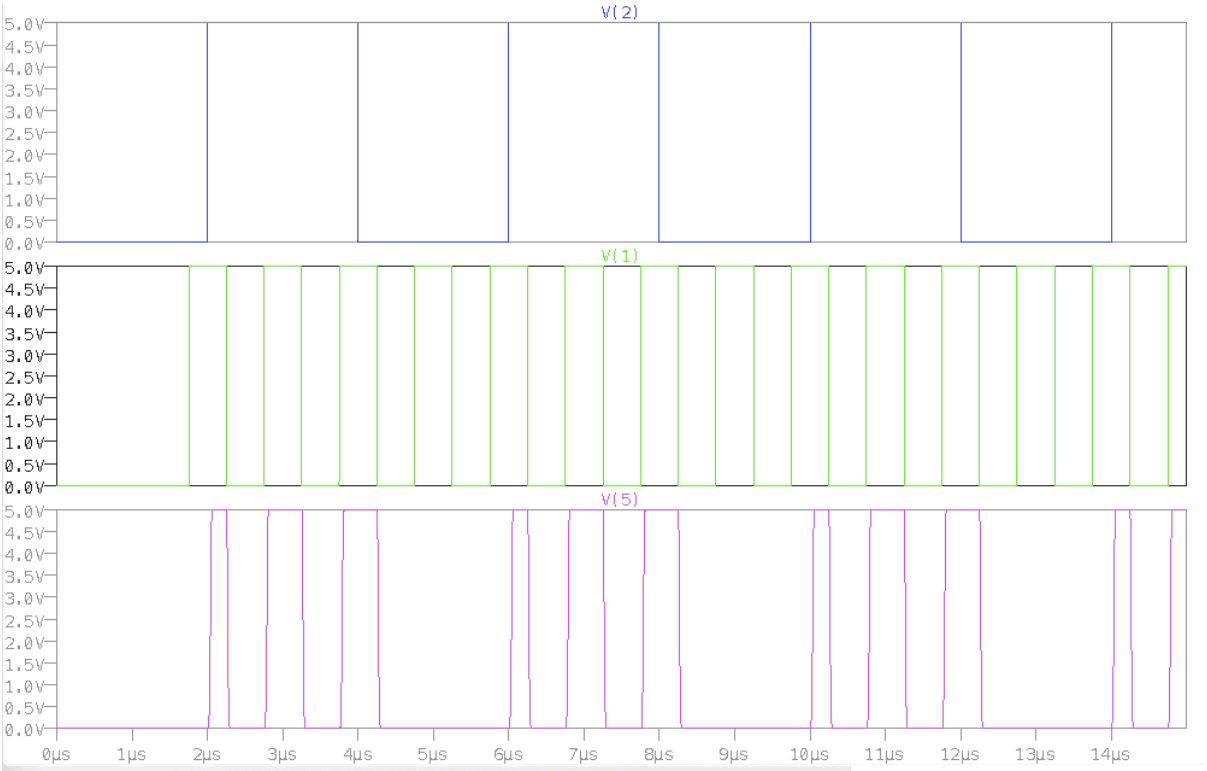
B. Dynamic D Flip Flop

```
.include /Users/sanujkul/Documents/LTspice/libraries/180nm_model.txt
.include /Users/sanujkul/Documents/LTspice/Workspace/VLSI/libraries/CMOS-NOT.cir

XNOT1 1 2 100 CMOS_NOT
XNOT2 3 6 100 CMOS_NOT
XNOT3 4 5 100 CMOS_NOT
XNOT4 7 8 100 CMOS_NOT
XNOT5 8 9 100 CMOS_NOT

M1 2 3 4 4 N_180 w=2.5u l=.18u
M2 5 6 7 7 N_180 w=2.5u l=.18u

CL 9 0 5p
C2 2 0 1p
C4 4 0 1p
C5 5 0 1p
C6 6 0 1p
C7 7 0 1p

Vdd 100 0 DC 5v

Vd 1 0 PULSE(0 5v 4us 0.1fs 0.1fs 0.5us 1us)
Vclk 3 0 PULSE(0 5v 5.3us 0.1fs 0.1fs 2us 4us)


***** OUTPUT CODES **********
.TRAN 0 15us
```



C. Static D-Latch

```
.include /Users/sanujkul/Documents/LTspice/libraries/180nm_model.txt
.include /Users/sanujkul/Documents/LTspice/Workspace/VLSI/libraries/
CMOS-NOT.cir

M2 1 2 3 3 N_180 w=1.25u l=.18u

XNOT1 3 4 6 CMOS_NOT
XNOT2 4 5 6 CMOS_NOT
XNOT3 5 4 6 CMOS_WEAK_NOT

Vdd 6 0 DC 5v

C3 3 0 10p
C4 4 0 10p
C5 5 0 10p

Vd 1 0 PULSE(0 5v 1.75us 0.1fs 0.1fs 0.5us 1us)
Vclk 2 0 PULSE(0 5v 2us 0.1fs 0.1fs 2us 4us)

***** OUTPUT CODES **********
.TRAN 0 15us
```



D. Static D Flip Flop

```
.include /Users/sanujkul/Documents/LTspice/libraries/180nm_model.txt
.include /Users/sanujkul/Documents/LTspice/Workspace/VLSI/libraries/CMOS-NOT.cir

XNOT1 1 2 100 CMOS_NOT
XNOT2 3 6 100 CMOS_NOT
XNOT3 4 5 100 CMOS_NOT
XNOT4 7 8 100 CMOS_NOT
XNOT5 8 9 100 CMOS_NOT

XNOT6 5 3 100 CMOS_WEAK_NOT
XNOT7 9 8 100 CMOS_WEAK_NOT


M1 2 3 4 4 N_180 w=2.5u l=.18u
M2 5 6 7 7 N_180 w=2.5u l=.18u

CL 9 0 5p
C2 2 0 1p
C4 4 0 1p
C5 5 0 1p
C6 6 0 1p
C7 7 0 1p

Vdd 100 0 DC 5v

Vd 1 0 PULSE(0 5v 4us 0.1fs 0.1fs 0.5us 1us)
Vclk 3 0 PULSE(0 5v 5.3us 0.1fs 0.1fs 2us 4us)


***** OUTPUT CODES **********
.TRAN 0 15us
```