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RTL8211FS(I)-VS
RTL8211FG(I)-VS

INTEGRATED 10/100/1000M ETHERNET TRANSCEIVER

PRECISION TIME PROTOCOL (PTP) APPLICATION NOTES

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

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- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2016/03/18	First release.
1.1	2018/09/05	Corrected minor typing errors.

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1. General Description

The Realtek RTL8211FS(I)-VS/RTL8211FG(I)-VS* provides full hardware support for high-precision clock synchronization based on the Precision Time Protocol (PTP) of the IEEE 1588 and 802.1AS standard. The integrated PTP functionality accurately timestamps each PTP packet on the Tx/Rx path, and the upper layer software can use this timing information to determine the timing offset to the PTP master's clock. The RTL8211F PHY also provides GPIOs as PTP application interfaces.

**Note: For simplicity, if not individually specified, the RTL8211FS(I)-VS and RTL8211FG(I)-VS will be called the 'RTL8211F series' or 'RTL8211F PHY' in the rest of this document.*

2. Precision Time Protocol (PTP)

The Precision Time Protocol (PTP) is a series of IEEE specifications, including IEEE 1588 Ver. 1, IEEE 1588 Ver. 2, and IEEE 802.1AS, that synchronize the time of day or a standard time among a network of computer devices. The PTP protocol is typically used in Audio Video Bridging (AVB) applications, industrial and factory automation applications, or test and measurement systems.

The fundamental concept of PTP is time-stamping the specified PTP frames with high precision as close to the transmission media as possible. Time-stamping in the PHY increases the accuracy as compared to time-stamping in the MAC or higher layers.

The PTP core in the RTL8211F consists of three main blocks:

- Packet Time Stamping
- Synchronized PTP Clock
- Time Application Interface (TAI)
- Hardware offload timestamp update (one-step and two-step mode)

By combining the functions, the RTL8211F series provides complete and accurate support for applications in a time-synchronous system.

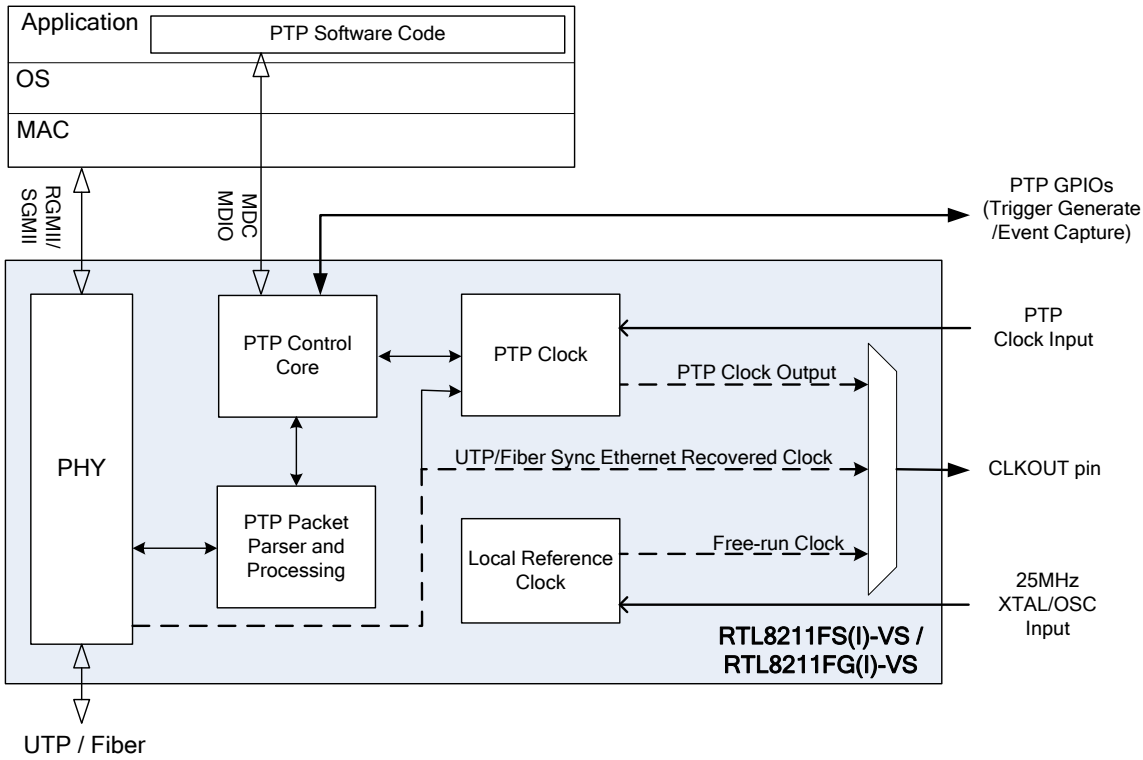


Figure 1. PTP and Sync Ethernet Application Diagram

2.1. Synchronized PTP Clock

Based on the PTP specification requirements, the integrated PTP clock of the RTL8211F series provide the following time fields:

- Seconds (48 bits)
- Nanoseconds (30 bits)
- Fractional nanoseconds (in units of 2^{-32}ns).

The RTL8211F series provide several ways to access and update this internal PTP clock, the methods are listed below:

- Direct Read/Write
- Step Adjustment
- Rate Adjustment

A **Direct Write** of the time value is done by setting a new value to all time fields. This function may be used when initializing a PTP synchronization that needs an immediate setting to the time value due to the local PTP time being far apart from the Master clock time.

A **Step Adjustment** is an alternative method for making a quick compensation to the PTP clock time. Note that the adjustment can be both incremented and decremented.

When the local time is close enough to the PTP Master, **Rate Adjustment** is the better way to fine-tune the time and frequency drift. The Rate Adjustment allows for correction on the order of 2^{-32} ns per clock cycle; it can correct the offset over time accurately.

See Table 6, page 28 for detailed register settings.

2.2. Packet Time Stamping

The PTP packet parser in the RTL8211F series monitor transmit/receive packet data in order to detect IEEE 1588 Ver. 1 and Ver 2, or 802.1AS Event Messages. The PTP packets transported in Layer 2 Ethernet, IPv4/UDP, or IPv6/UDP packet formats can be recognized accordingly. Upon detection of a PTP Event Message, the RTL8211F series will capture the specific transmit/receive timestamp and provide it to the software at the upper layer through PTP_TRX_TS registers (see Table 19, page 33). A PTP interrupt can be generated, if enabled, upon a transmit/receive timestamp ready.

2.2.1. One-Step and Hardware-Assisted Two-Step Operation

In some transmission cases, the RTL8211F PHY supports One-Step operation: The egress timestamp of the Sync message is on-the-fly inserted to the Sync itself; no need for Follow-Up messages.

A Hardware-assisted Timestamp Insertion feature is imbedded. This can insert receive timestamps directly into the next Follow-Up/Delay-Response packets via hardware; software does not need to access timestamp registers.

After gathering the timestamp information, the upper layer software can compute the difference between the local time and the PTP Master's central clock time, and use one of the three methods in section 2.1 Synchronized PTP Clock, page 3, to synchronize the local PTP clock to the master clock.

2.3. Time Application Interface (TAI)

When the end-point's PTP clock is synchronized to the PTP Master clock, its time information and local clock can be provided to peripheral time applications that need to work synchronously with the central clock. TheRTL8211F PHY enables these time application interfaces (via the PTP GPIOs and CLKOUT pins) in the following:

Event Capture Interface

- Monitor the selected GPIO, and record the timestamp of incoming pulses, edges, or time alignment signals, e.g., a stopwatch.

Trigger Generate Interface

- Arms the selected GPIO to generate a pulse, edge, or periodic clock signal at a specific time, e.g., an alarm clock. The pulse has configurable period and duty cycles.
- Low-jitter synchronized 1588 clock output with frequency of 25M/125MHz via the CLKOUT pin.
- PTP clock input from an external reference clock source with 10M/25M/125MHz via GPIOs.

The related TAI configurations can be set by PTP_TAI registers (see Table 12 PTP_TAI_CFG (PTP Application I/F Config Register, Page 0xe42, Address 0x10), page 30).

3. PTP Function Configuration

3.1. Enable & Disable PTP Function

PTP capability configuration is defined in section 6.2, page 27, including the protocol types supported and the PTP enable register. The PTP capabilities should be set at the initial stage of the PTP program.

After setting the PTP capabilities, we MUST complete a GPHY reset to allow the PTP function to begin operating.

3.2. PTP Synchronization Mechanism

Two-Step PTP Synchronization

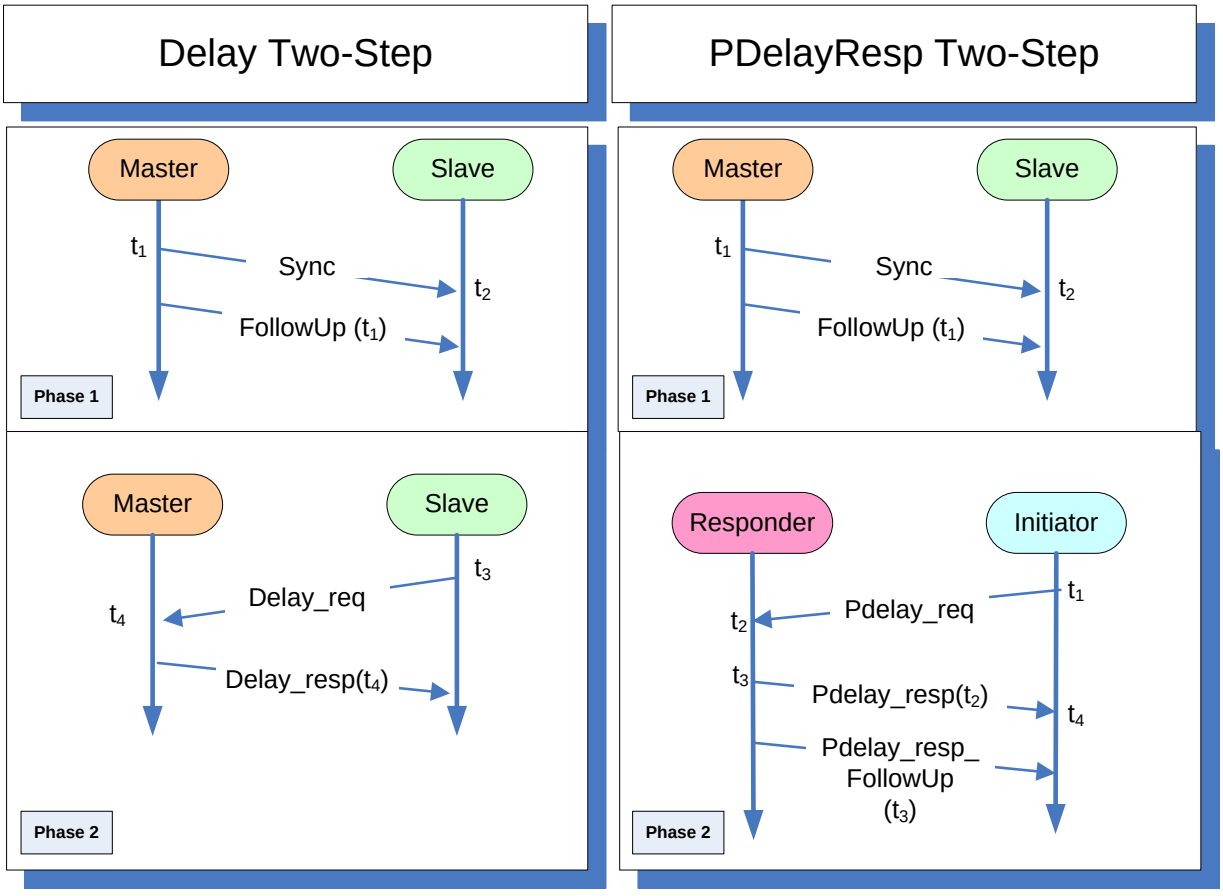


Figure 2. Two-Step PTP Synchronization

One-Step PTP Synchronization

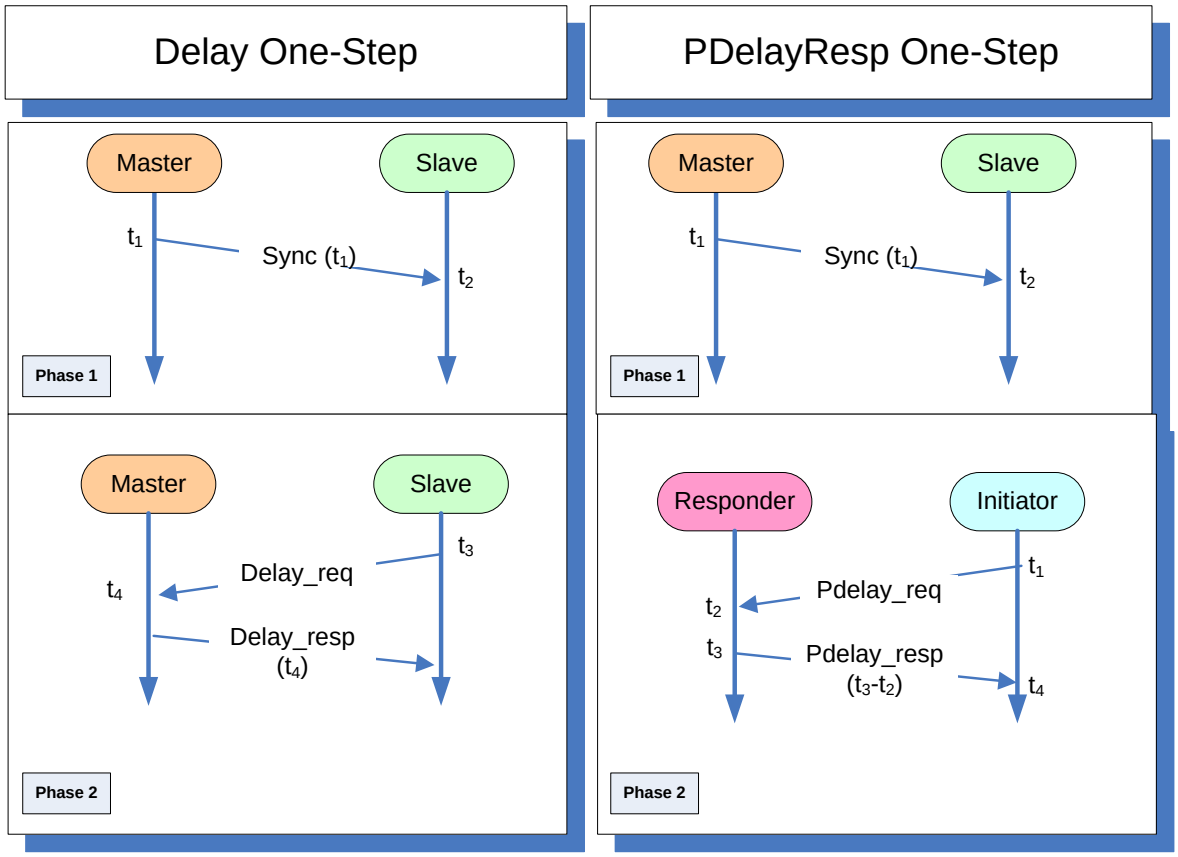


Figure 3. One-Step PTP Synchronization

Calculation of Offset_from_Master

The time offset between a Slave and a Master clock is defined as follows:

$$Offset\_from\_Master = t_2 - t_1 - MeanPathDelay$$

Calculation of Mean_Path_Delay

For delay between Master & Slave: Calculate the timestamp at both phase 1 & phase 2 stages.

$$MeanPathDelay = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$

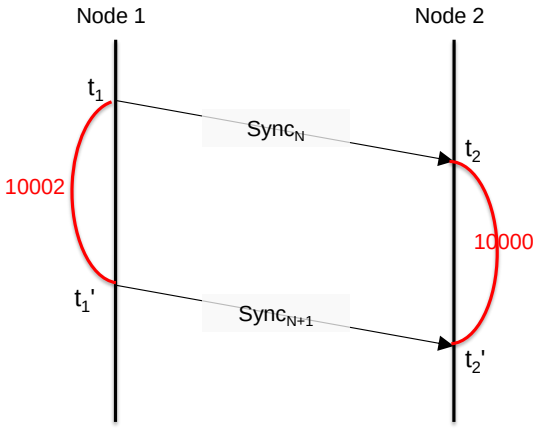
Calculation of Delay Between Responder & Initiator

Calculate the timestamp at phase 2 stage.

$$\text{MeanPathDelay} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$

Note: For the RTL8211F PHY, PDelayResp one-step correctionField update will not exactly match <PDelayResp Egress Timestamp (t3) > - <PDelayReq Ingress Timestamp (t2) >, as a more accurate timer with resolution 2^{-3} ns is used to calculate the value. The difference would be smaller than 1ns compared to the result of <PDelayResp Egress Timestamp (t3) > - <PDelayReq Ingress Timestamp (t2) >.

Calculation of Frequency_Drift



$$neighborRateRatio = \frac{t_1' - t_1}{t_2' - t_2} = \frac{10002}{10000} = 1.0002 = 1 + 200ppm$$

Figure 4. Calculation of neighborRateRatio

3.2.1. Read Tx/Rx Timestamp

The timestamp is recorded by the chip after receiving or transmitting a PTP message packet.

Before reading the time stamp value, we should check the READY flag. If the READY flag is set, it means the timestamp is prepared and recorded completely. The chip can detect the ‘read’ event, and clear the flag automatically. The Ready flag register is defined in section 6.18, page 33, - bit [15:8].

After checking the timestamp READY flag, we must select the protocol message type and the message direction (Transmit/Receive) for the corresponding timestamp. Next we set the Transmit/Receive Timestamp Read Enable bit. The register is defined in section 6.18, page 33, - bit [4:0].

Timestamp information is shown in PTP TxRx Timestamp registers (see sections 6.18~6.26, Table 19 ~Table 27).

The PTP version is shown in ‘trxts_ptpver’ and ‘trxts_transpec’ fields in Table 20, page 34.

IEEE 1588 v1: ptpver = 1

IEEE 1588 v2: ptpver = 2; transpec = 0

802.1AS: ptpver = 2; transpec = 1

The PTP packet type will be indicated in 'trxts_msgtype' in Table 20, page 34, which is summarized in the table below:

Table 1. Summary of PTP Packet Types

Value of 'trxts_msgtype' (in HEX)	IEEE 1588 v1 Packet Type	IEEE 1588 v2 & 802.1AS Packet Type
0	Sync	Sync
1	Delay_Req	Delay_Req
2	Follow_Up	Pdelay_Req
3	Delay_Resp	Pdelay_Resp
4-7	Management	Reserved
8	-	Follow_Up
9	-	Delay_Resp
A	-	Pdelay_Resp_Follow_Up
B	-	Announce
C	-	Signaling
D	-	Management
E-F	-	Reserved

The Source Port ID of each PTP packet will be indicated by a 16-bit 'trxts_srchash' field in the RTL8211F PHY in order to distinguish the packet sender by the software (see Table 21, page 34). The formula for transforming the Source Port ID into its Hash Value (trxts_srchash) is shown in the following examples:

For IEEE 1588 v1

SourcePortIdentity (8-byte, in HEX) = 11 22 33 44 55 66 AA BB

Hash Value Computation:

Step 1. Convert to a 10-byte SourcePortIdentity (in HEX) = 11 22 33 00 00 44 55 66 AA BB

Step 2. Sum the SourcePortIdentity every 2 bytes:

0x1122 + 0x3300 + 0x0044 + 0x5566 + 0xAABB = 0x0001_4487

Step 3. Add high 16-bit with low 16-bit:

Hash Value (trxts_srchash[15:0]) = 0x0001 + 0x4487 = **0x4488**

For IEEE 1588 v2 & 802.1AS

SourcePortIdentity (10-byte, in HEX) = 11 22 33 FF FE 44 55 66 AA BB

Hash Value Computation:

Step 1. Sum the SourcePortIdentity every 2-byte:

0x1122 + 0x33FF + 0xFE44 + 0x5566 + 0xAABB = 0x0002_4386

Step 2. Add high 16-bit with low 16-bit:

Hash Value (trxts_srchash[15:0]) = 0x0002 + 0x4386 = **0x4388**

3.2.2. Set PTP Clock Time

There are three modes for PTP clock adjustment to PTP Local Time through PTP Time Config registers

(1) Direction Read/Write clock

(2) Increment/Decrement step adjustment

(3) Read/Write rate adjustment

The register is defined in section 6.5 PTP_CLK_CFG (PTP Clock Config Register, Page 0xe41, Address 0x10), page 28 – bit[3:1]

The PTP Clock adjustment clock register is defined at PTP Time Config register (sections 6.6~6.10, Table 7 ~ Table 11).

After setting the PTP Clock adjustment value, set the PTP clock adjustment enable register.

The register is defined in section 6.5 PTP_CLK_CFG (PTP Clock Config Register, Page 0xe41, Address 0x10), page 28 – bit[0] .

Note: We suggest that the time differences from the Egress Timestamp point to the MDI, and from the MDI to the Ingress Timestamp point should all be taken into account in order to attain more accurate PTP clock tuning.

3.2.3. Read PTP Clock Time

Set the PTP clock Direction Read register and enable register.

The PTP clock Direction Read register is defined in Table 5. PTP_CLK_CFG (PTP Clock Config Register), page 28 – bit[3:1] .
The enable register is defined in Table 5. PTP_CLK_CFG (PTP Clock Config Register), page 28 – bit[0] .

After setting the above steps, the PTP Clock is shown in PTP Time Config registers (sections 6.6~6.10, Table 7~Table 11).

3.3. PTP TAI Configuration

The RTL8211F series supports four PTP GPIO pins as the Time Application Interface (TAI), and four modes for PTP TAI configuration.

The PTP TAI configuration modes are listed below:

(1) Disable function

(2) Trigger Generate

(3) Event Capture

(4) Trigger start time/Event timestamp read (according to current GPIO settings)

The register is defined in section 6.11, page 30. Mode selection is at bit[2:1], and GPIO selective number is at bit[4:3].

3.3.1. PTP TAI Timestamp

The PTP TAI Time stamp register is defined in sections 6.14~6.17, Table 15~Table 18, the value can be read or write, set by PTP TAI interface configuration mode selection.

3.3.2. Set PTP TAI Interface

3.3.2.1 If the PTP TAI interface Configuration Mode is Trigger Generated

The Trigger start at time is specified in PTP TAI Timestamp registers (see sections 6.14~6.17, Table 15~Table 18).

We can set the Trigger Generate mode in the PTP_TAI_CFG register (Table 12, page 30) – bit[9:8] for edge, pulse or periodic type selection.

The duty cycle, unit and period of a trigger pulse also can be specified at the register PTP_TRIG_CFG (Table 13, page 31). When ‘pulse_amt’ is set under 64ns (i.e. periodic pulses with frequency > 15.625MHz), theRTL8211F series only supports a ‘50%’ duty cycle configuration for periodic trigger function due to the clock frequency limitations.

After the PTP TAI Enable bit is set (Table 12, page 30, bit[0]), the GPIO trigger function will start operating.

Due to time needed for hardware to process the trigger setting, some fixed latency would be induced from the specified ‘trigger start time’ to the trigger actually starting. The value is 6 * PTP_CLK period, that is, 48ns. We suggest that users take this offset into account when setting the ‘trigger start time’.

3.3.2.2 If the PTP TAI Interface Configuration Mode is Event Generated

Set the Event Generate mode in the PTP_TAI_CFG register (Table 12, page 30, – bit[6] for edge type selection.

After the PTP TAI Enable bit is set (Table 12, page 30, bit[0]), the GPIO trigger function will start working.

Note 1: Users should always disable the current function of the GPIO pin before setting a new GPIO function.
Note 2: If a GPHY reset is asserted during GPIO arming (e.g. periodic pulses are toggling), after the reset, the PTP TAI Enable bit (Table 14, page 31, bit[0]) must be set again in order to restart the same GPIO configuration.

3.4. PTP Reference Clock Input

The RTL8211F PHY provides an option for the local PTP clock to be sourced from an external reference clock, e.g. a GPS-based clock, with frequencies of 10M, 25M, and 125MHz supported.

To enable the reference clock input mode, follow the steps below:

(1) Disable the TAI function armed at PTP GPIO0 of the RTL8211F PHY

(2) Connect the external reference clock to the PTP GPIO0 pin

(3) Select the frequency of the input reference clock via bit[6:5] of PTP_CLK_CFG register (see Table 6, page 28), and enable the clock input function by asserting bit[4] =1

(4) Issue a PHY reset to allow the new setting to take effect

Note: The maximum jitter of the external clock should be within 400 ps.

4. PTP Sample Flow

4.1. Overview

The following figures show the PTP handshaking protocol - 802.1AS and PTPv2 one-step protocol.

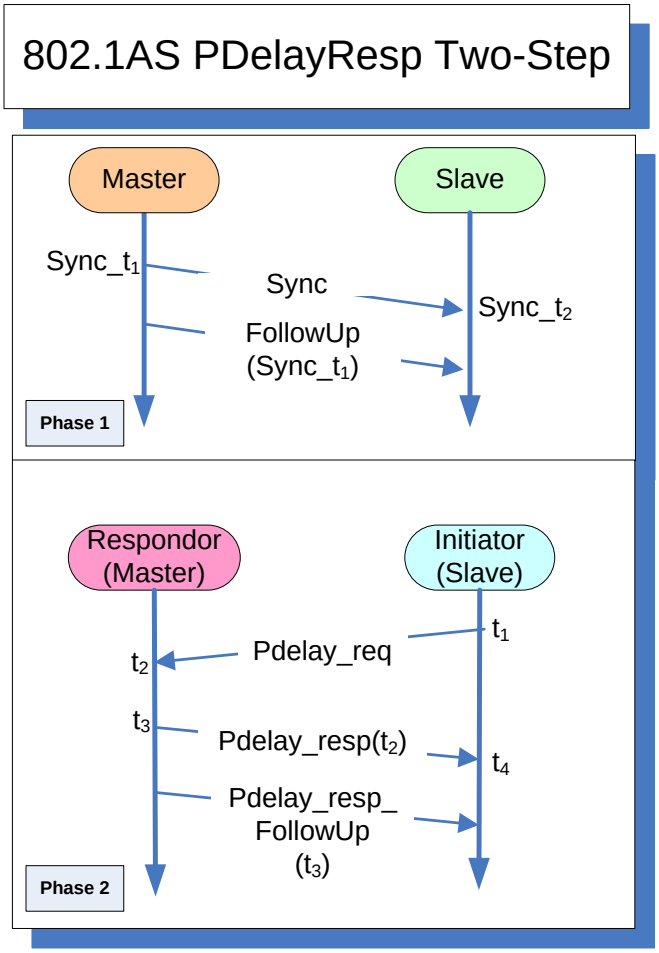


Figure 5. 802.1AS Two Step Protocol

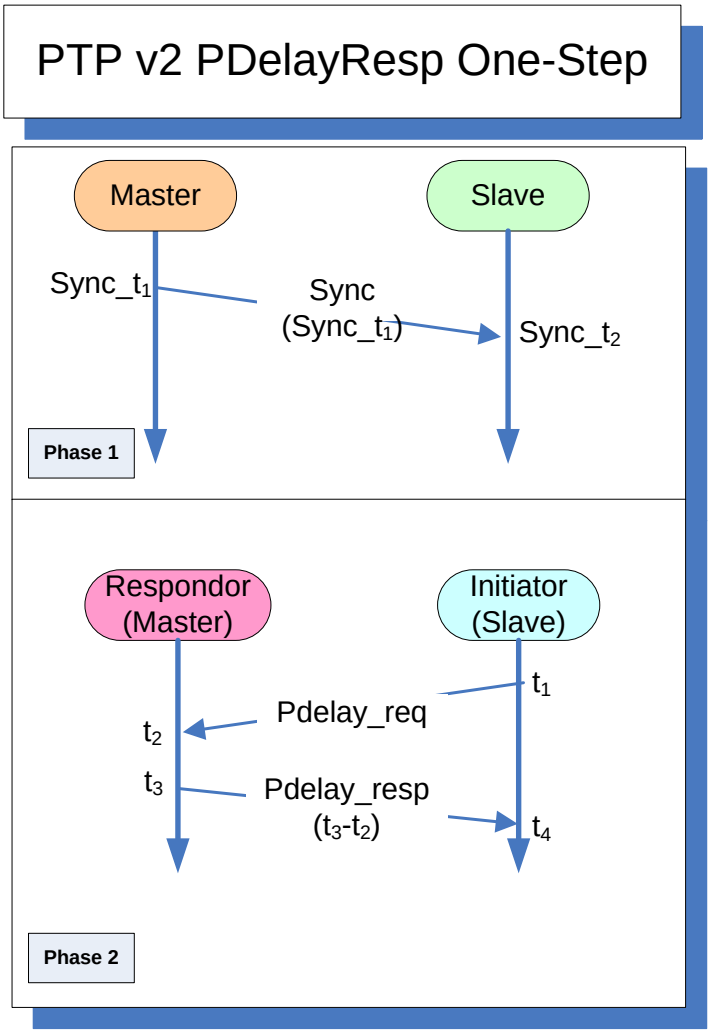


Figure 6. PTPv2 One-Step Protocol

4.2. 802.1AS Two-Step Example Flow Chart

The following PTP example is based on the Two-Step 802.1AS protocol. The Master transmits PTP messages each second (Sync interval = 1 second).

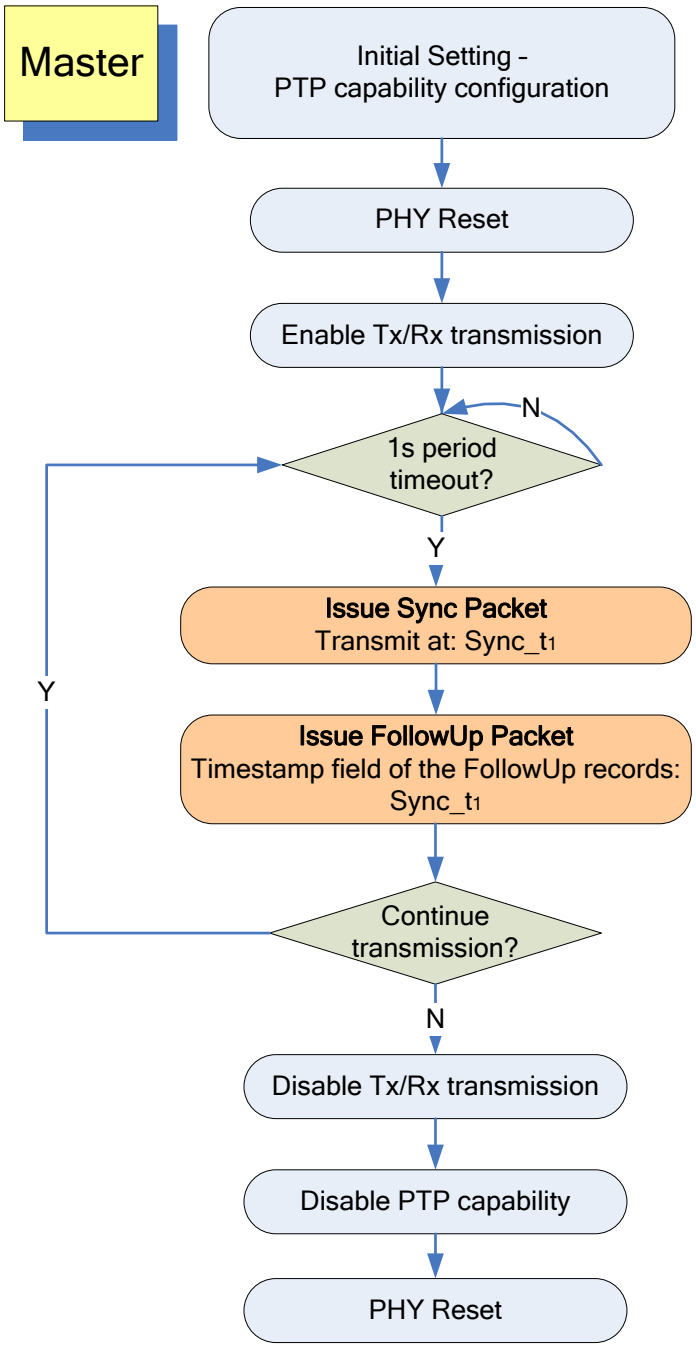


Figure 7. Master Flow Chart of 802.1AS Two-Step Example

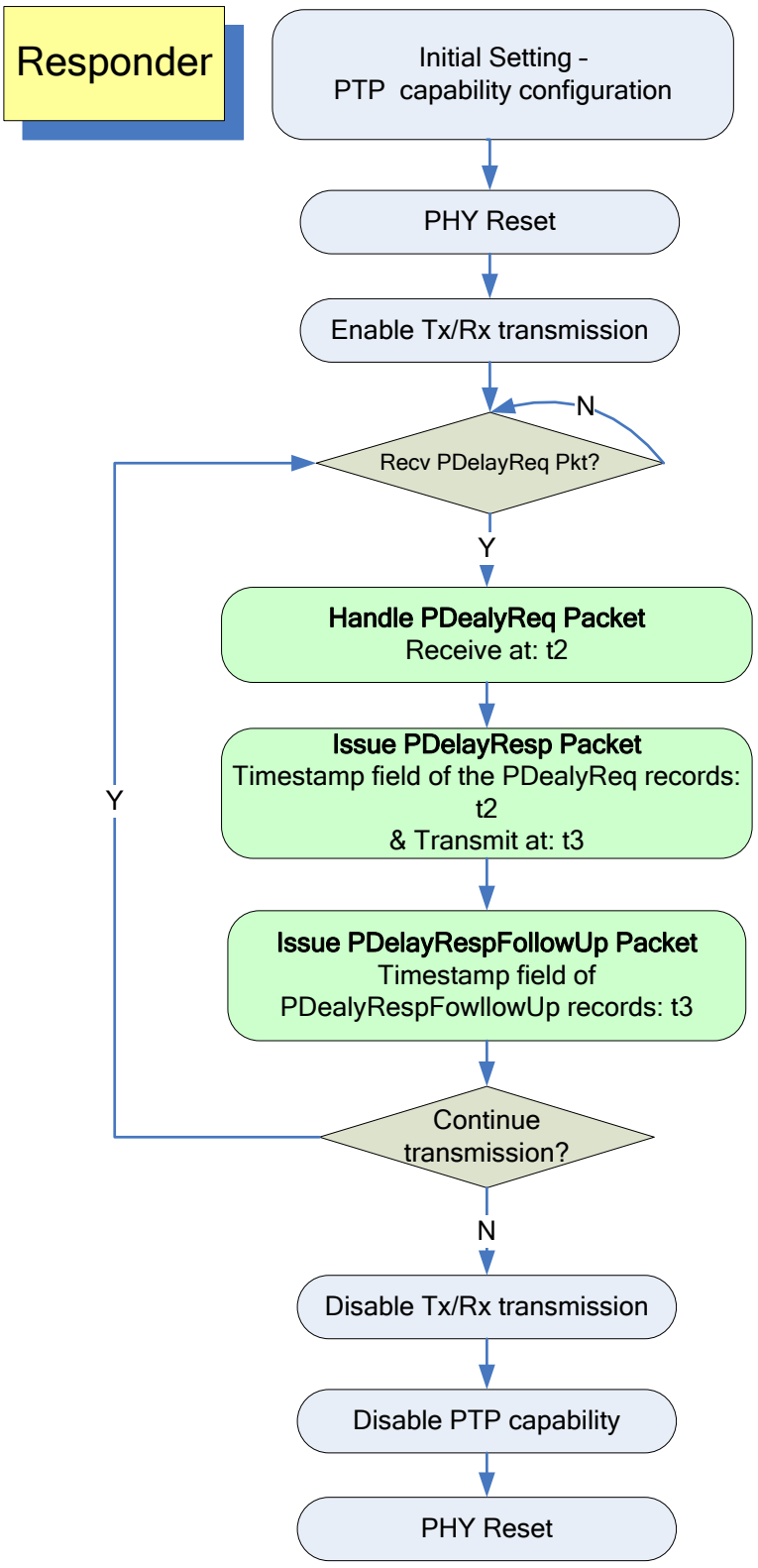


Figure 8. Responder Flow Chart of 802.1AS Two-Step Example

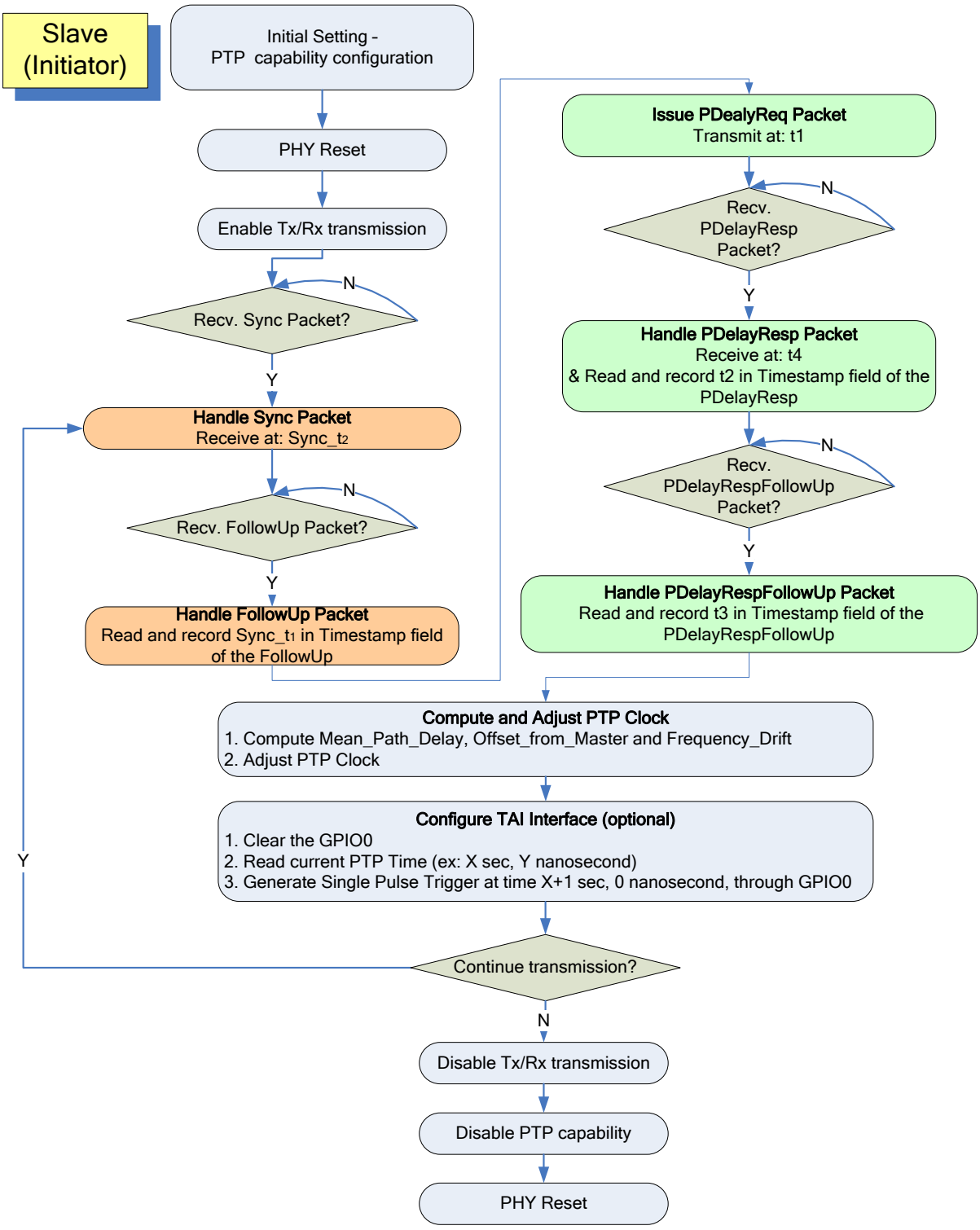


Figure 9. Slave Flow Chart of 802.1AS Two-Step Example

4.3. PTPv2 One-Step Example Flow Chart

The following PTP example is based on One-Step PTPv2 protocol. Master transmits PTP messages each second (Sync interval = 1 second).

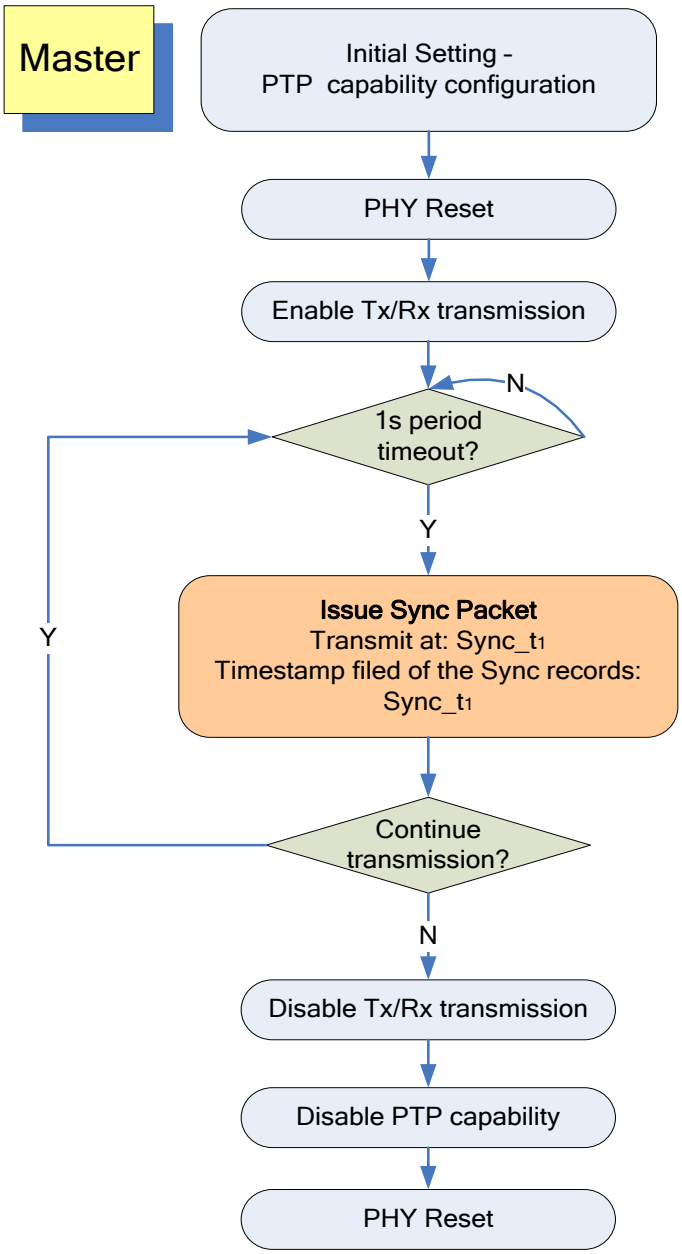


Figure 10. Master Flow Chart of PTPv2 One-Step Example

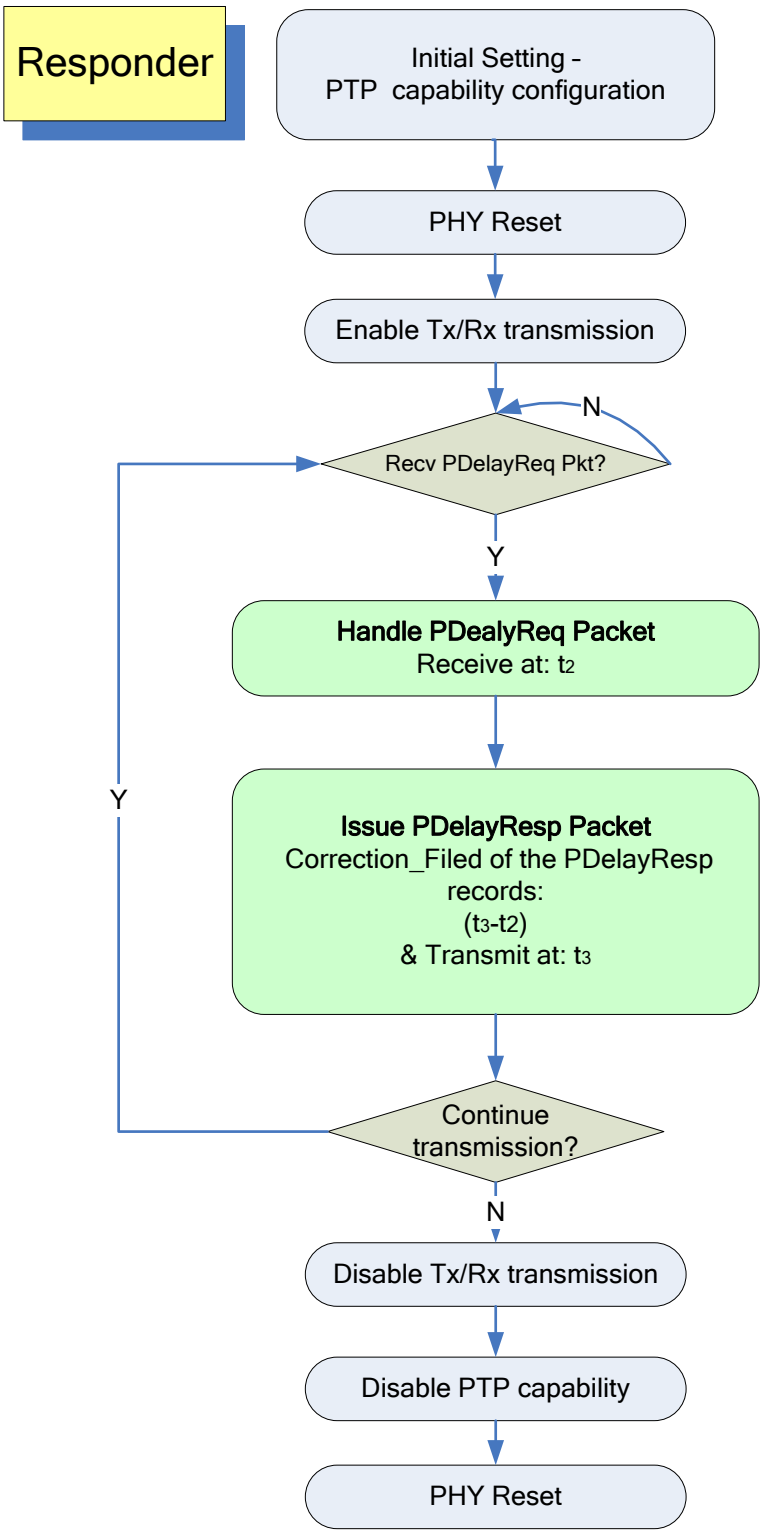


Figure 11. Responder Flow Chart of PTPv2 One-Step Example

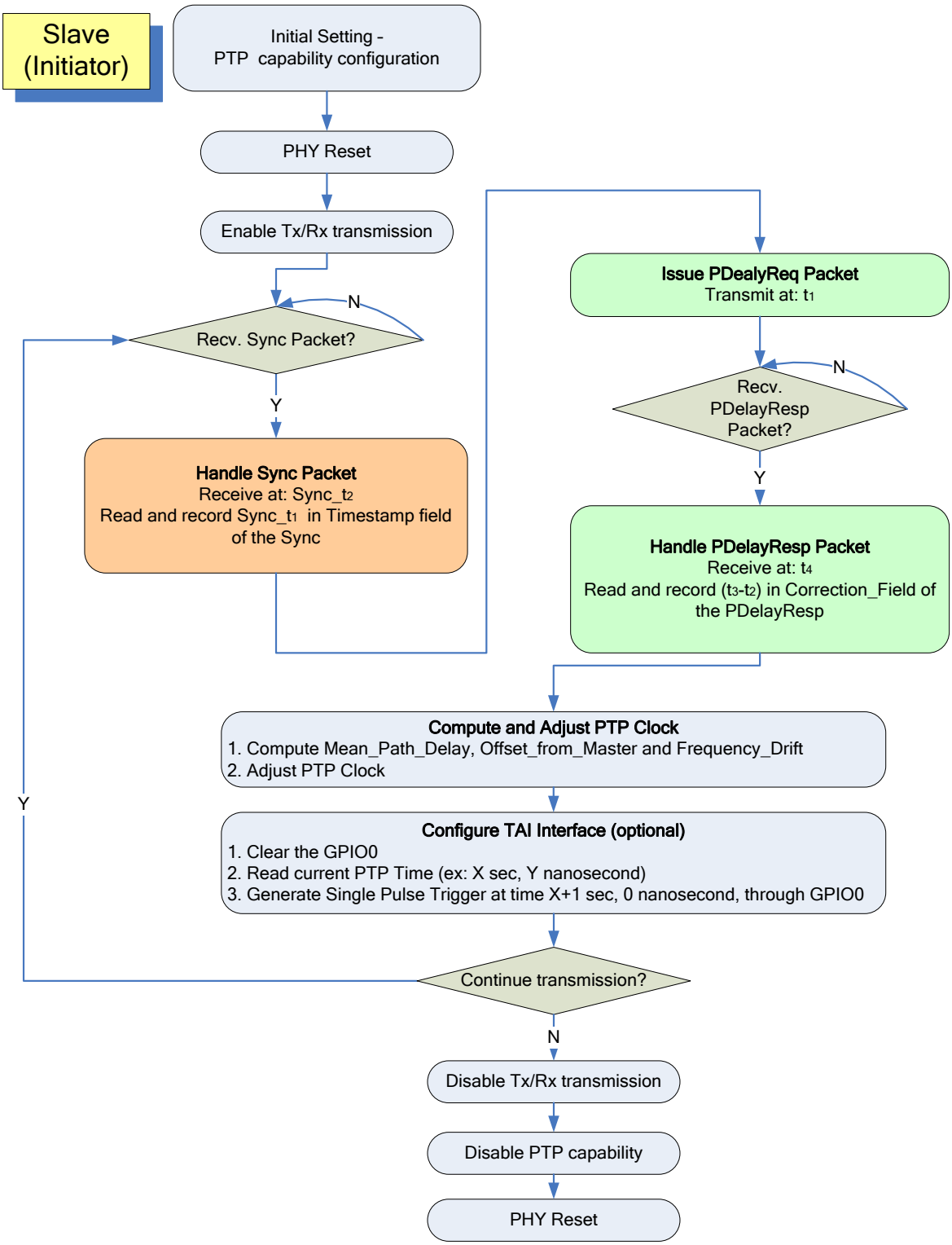


Figure 12. Responder Flow Chart of PTPv2 One-Step Example

5. Register Configuration Examples

5.1. Initial Setting – PTP Capability Configuration

(1) Switch the GPHY base address to 0xe40

Register: 0x1f

Value = 0x0e40

(2) Set the PTP_CTL value to 0x003F or 0x007F

Register: 0x10

Value = 0x003F (two-step Timestamp Insertion (t3-t2) to Pdelay_Response messages)

/0X007F (one-step Timestamp Insertion (t3-t2) to Pdelay_Response messages)

5.2. PHY Reset

(1) Switch the GPHY base address to 0xa40

Register: 0x1f

Value = 0xa4

(2) Set GPHY reset

Register: 0x00

Value = 0x9200

5.3. PTP Clock Adjustment

5.3.1. Direct Write

(1) Switch the GPHY base address to 0xe41

Register: 0x1F

Value = 0x0e41

(2) Set the clock config time

Register: 0x11 - 0x12

Value = ‘Direct offset’

(3) Offset adjustment of PTP_CLK_CFG

Register: 0x10

Value = 0x0007

5.3.2. Rate Adjustment

(1) Switch the GPHY base address to 0xe41

Register: 0x1f

Value = 0xe41

(2) Set clock config time

Register: 0x11-0x12

Value = ‘Desired Rate’

(3) Rate adjustment of PTP_CLK_CFG

Register: 0x10

Value = 0x000F

5.3.3. Step Adjustment

5.3.3.1 If Master is Faster Than Slave

(1) Switch the GPHY base address to 0xe41

Register: 0x1f

Value = 0x0e41

(2) Set clock config time

Register: 0x11-0x15

Value = Offset from master

(3) Increase step adjustment of PTP_CLK_CFG

Register: 0x10

Value = 0x0009

5.3.3.2 If Slave is Faster Than Master

(1) Switch the GPHY base address to 0xe41

Register: 0x1f

Value = 0xe41

(2) Set clock config time

Register: 0x11-0x15

Value = Offset from master

(3) Increase step adjustment of PTP_CLK_CFG

Register: 0x10

Value = 0x000B

5.4. PTP Example Steps for PTP Synchronization

The following steps are implemented at the PTP sample described at the Compute and Adjust PTP Clock Stage of Slave Round #1:

(1) Calculate the MeanPathDelay

$$\text{MeanPathDelay} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$

(2) Calculate the Offset_from_master

$$\text{Offset\_from\_Master} = t_2 - t_1 - \text{meanPathDelay}$$

(3) Step Adjustment* with the value of Offset_from_master

The config value is offset_from_master.

If (Synct1 + MeanPathDelay) > Synct2, it means the master is faster than the slave; see section 5.3.3.1, page 21. If (Synct1 + MeanPathDelay) < Synct2, it means the slave is faster than the master; see section 5.3.3.2, page 21.

**Note: Where a setup with a whole new time value is needed, a Direct Write would be another suitable method of initialization.*

Round #2:

(1) Calculate the MeanPathDelay

$$\text{MeanPathDelay} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$

(2) Calculate the Offset_from_master

$$\text{Offset\_from\_Master} = t_2 - t_1 - \text{meanPathDelay}$$

(3) Step Adjustment with the value of Offset_from_master

The config. value is offset_from_master.

If (Synct1 + MeanPathDelay) > Synct2, it means the master is faster than the slave; see section 5.3.3.1, page 21.

If (Synct1 + MeanPathDelay) < Synct2, it means the slave is faster than the master; see section 5.3.3.2, page 21.

(4) Rate adjustment by phase 1 SYNC packet

Calculate the mean delay of SYNC packet at Round #1 and Round #2.

$$\Delta Sync\ t1 = Sync\ t1\_round2 - Sync\ t1\_round1$$

$$\Delta Sync\ t2 = Sync\ t2\_round2 - Sync\ t2\_round1$$

$$Rate = \Delta Sync\_t2 - \Delta Sync\_t1$$

If $\Delta Synct1 > \Delta Synct2$, finetune the Rate (nanosecond) to a larger value.

If $\Delta Synct1 < \Delta Synct2$, finetune the Rate (nanosecond) to a smaller value.

The config value is the Rate. Follow the flow in section 5.3.2.

(5) Record the current Rate for the next Round.

$$currRate = Rate$$

Round >= #3:

(1) Calculate the MeanPathDelay

$$MeanPathDelay = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$$

(2) Calculate the Offset_from_master

$$Offset\_from\_Master = t_2 - t_1 - meanPathDelay$$

(3) Step Adjustment with the value of Offset_from_master

The config value is offset_from_master.

If (Synct1 + MeanPathDelay) > Synct2, it means the master is faster than the slave; see section 5.3.3.1, page 21.

If (Synct1 + MeanPathDelay) < Synct2, it means the slave is faster than the master; see section 5.3.3.2, page 21.

(4) Rate adjustment by reference to Offset_from_master*

If (Synct1 + MeanPathDelay) > Synct2, finetune the currRate (nanosecond) to a larger value.

If (Synct1 + MeanPathDelay) < Synct2, finetune the currRate (nanosecond) to a smaller value.

Rate = currRate.

(5) The config value is the Rate. Follow the flow in section 5.3.2, page 21.

**Note: Where the value of Offset_from_Master is greater than 100µs, for more efficient clock tuning we suggest that Step Adjustment should be utilized instead of Rate Adjustment.*

5.5. Disable PTP Capability

(1) Switch the GPHY base address to 0xe40

Register: 0x1f

Value = 0x0e40

(2) Set the PTP_CTL value 0x0000

Register: 0x10

Value = 0x0000

(3) Switch the GPHY base address to 0x0a40

Register: 0x1f

Value = 0x0a40

(4) Set GPHY reset

Register: 0x00

Value = 0x9200

5.6. PTP Example Steps for PTP TAI Configuration

The following steps are implemented at the PTP sample described in the Configure TAI Interface Stage of slave configuration.

(1) Switch the GPHY base address to 0xe42

Register: 0x1f

Value = 0x0e42

(2) Disable GPIO 0 TAI Interface

Register: 0x10

Value = 0x0001

(3) Set start trigger time

Register: 0x13 – 0x16

Value = current timestamp + 1 (s)

(4) Config trigger pulse mode

Register: 0x11

Value = (50% dutyCycle<<12) | (ms unit << 10) | period = (0x02<<12) | (0x02<<10)| 1000

(5) Config PTP_TAI_CFG

Register: 0x10

Value = (Trigger Generate<<1) | (Periodic pulses<< 8) | 0x01 = (0x01 << 1) | (0x03 << 8) | 0x01

6. Register Tables

6.1. PHYCR2 (PHY Specific Control Register 2, Page 0xa43, Address 0x19)

Table 2. PHYCR2 (PHY Specific Control Register 2, Page 0xa43, Address 0x19)

Bit	Name	Type	Default	Description
25.15:14	RSVD	RO	00	Reserved.
25.13:12	CLKOUT Source	RW	00	Source select of the CLKOUT pin clock output. 00: Free run clock generated from internal PLL. 01: UTP recovery receive clock for Sync Ethernet. (Valid only if in UTP mode) 10: Fiber recovery receive clock for Sync Ethernet. (Valid only if in FIBER mode) 11: PTP synchronized clock output.
25.11	CLKOUT Frequency Select	RW	1	Frequency select of the CLKOUT pin clock output. 0: 25MHz 1: 125MHz
25.10:8	RSVD	RO	000	Reserved.
25.7	CLKOUT SSC Enable	RW	0	1: Enable Spread-Spectrum Clocking (SSC) on CLKOUT output clock.
25.6	RSVD	RO	1	Reserved.
25.5	PHY-mode EEE Enable	RW	1	1: Enable EEE in PHY mode.
25.4	RSVD	RO	0	Reserved.
25.3	SYSCLK SSC Enable	RW	0	1: Enable Spread-Spectrum Clocking (SSC) on System Clock.
25.2	RSVD	RO	0	Reserved.
25.1	RXC Enable	RW	1	1: RXC clock output enabled.
25.0	CLKOUT Enable	RW	1	1: CLKOUT clock output enabled.

Note: Issue a Software Reset (0.15) in order to allow the setting to take effect after setting these bits in the PHYCR2 register.

6.2. PTP_CTL (PTP Control Register, Page 0xe40, Address 0x10)

Table 3. PTP_CTL (PTP Control Register, Page 0xe40, Address 0x10)

Bit	Name	Type	Default	Description
16.15:13	RSVD	RO	000	Reserved.
16.12	UDP_CHKSUM Update	RW	0	Enable auto-correction of UDP Checksum if One-Step Timestamp Insertion is enabled. Only effective to IPv6/UDP packets. 0: Set 0x0000 to the UDP Checksum field 1: Re-compute the UDP Checksum
16.11	P_DRFU_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to PDelaly_Resp_Follow_Up messages.
16.10	P_DR_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to PDelay_Resp messages.
16.9	DR_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to Delay_Resp messages.
16.8	FU_2STEP_INS Enable	RW	0	Enable Hardware-assisted Timestamp Insertion to Follow_Up messages.
16.7	P_DR_1STEP Enable	RW	0	Enable One-Step Timestamp Insertion (t3-t2) to Pdelay_Response messages.
16.6	SYNC_1STEP Enable	RW	0	Enable One-Step Timestamp Insertion (t1) to Sync messages.
16.5	AVB_802.1AS Support	RW	1	1: AVB 802.1AS standard support.
16.4	PTPv2_Layer2 Support	RW	1	1: PTPv2 Layer 2 packets support.
16.3	PTPv2_UDPIPV4 Support	RW	1	1: PTPv2 UDP/IPv4 packets support.
16.2	PTPv2_UDPIPV6 Support	RW	1	1: PTPv2 UDP/IPv6 packets support.
16.1	PTPv1 Support	RW	1	1: PTPv1 packets support.
16.0	PTP_Enable	RW	1	PTP function enable *Note: Issue a Software Reset (0.15) after setting this bit in order to enable/disable the PTP function.*

6.3. PTP_INER (PTP Interrupt Enable Register, Page 0xe40, Address 0x11)

Table 4. PTP_INER (PTP Interrupt Enable Register, Page 0xe40, Address 0x11)

Bit	Name	Type	Default	Description
17.15:4	RSVD	RO	0x000	Reserved.
17.3	Tx Timestamp Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Transmit Timestamp ready interrupt.
17.2	Rx Timestamp Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Receive Timestamp ready interrupt.
17.1	TrigGen Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Trigger Generate complete interrupt.
17.0	EventCap Interrupt	RW	0	1: Interrupt Enable 0: Interrupt Disable Event Capture timestamp ready interrupt.

6.4. PTP_INSR (PTP Interrupt Status Register, Page 0xe40, Address 0x12)

Table 5. PTP_CLK_CFG (PTP Clock Config Register)

Bit	Name	Type	Default	Description
18.15:4	RSVD	RO	0x000	Reserved.
18.3	Tx Timestamp Interrupt	RO, RC	0	1: Transmit Timestamp ready interrupt detected.
18.2	Rx Timestamp Interrupt	RO, RC	0	1: Receive Timestamp ready interrupt detected.
18.1	TrigGen Interrupt	RO, RC	0	1: Trigger Generate complete interrupt detected.
18.0	EventCap Interrupt	RO, RC	0	1: Event Capture timestamp ready interrupt detected.

6.5. PTP_CLK_CFG (PTP Clock Config Register, Page 0xe41, Address 0x10)

Table 6. PTP_CLK_CFG (PTP Clock Config Register, Page 0xe41, Address 0x10)

Bit	Name	Type	Default	Description
16.15:7	RSVD	RO	0	Reserved.
16.6:5	ptp_clkin_freq_sel	RW	0	PTP CLKIN Frequency Select. 00: 125MHz 01: 25MHz 10: 10MHz 11: Reserved *Note: Issue a Software Reset (0.15) in order to allow the setting to take effect.*
16.4	ptp_clkin_en	RW	0	PTP CLKIN function at GPIO 0 enable *Note: Issue a Software Reset (0.15) in order to allow the setting to take effect.*
16.3:1	ptp_clkadj_mod	RW	0	PTP Clock Adjustment Mode Select. 000: No function 001: Reserved - Issue Direct Read/Write to PTP_Local_Time through PTP_Time_Config registers 010: Direct Read 011: Direct Write - Issue Step Adjustment to PTP_Local_Time through PTP_Time_Config registers 100: Increment Step 101: Decrement Step - Issue Rate Adjustment Read/Write to PTP_Rate_Adj_Amt through PTP_Time_Config_ns registers [24:0]. A 2's complement representation should be used if a negative rate adjustment is needed. 110: Rate Read 111: Rate Write
16.0	ptp_clkadj_mod_set	RW, SC	0	PTP Clock Adjustment Mode Set. 1: Activate the selected clock adjustment mode as related parameters are properly inserted.

6.6. PTP_CFG_NS_LO (PTP Time Config Nano-Sec Low Register, Page 0xe41, Address 0x11)

Table 7. PTP_CFG_NS_LO (PTP Time Config Nano-Sec Low Register, Page 0xe41, Address 0x11)

Bit	Name	Type	Default	Description
17.15:0	PTP_Time_Config_ns[15:0]	RW	0x0000	Time configuration nano-sec field [15:0] / Rate adjustment multiplier field [15:0] A 2's complement representation should be used if a negative rate adjustment is needed.

6.7. PTP_CFG_NS_HI (PTP Time Config Nano-Sec High Register, Page 0xe41, Address 0x12)

Table 8. PTP_CFG_NS_HI (PTP Time Config Nano-Sec High Register, Page 0xe41, Address 0x12)

Bit	Name	Type	Default	Description
18.15:14	RSVD	RO	00	Reserved.
18.13:0	PTP_Time_Config_ns[29:16]	RW	0	Time configuration nano-sec field_ns [29:16]/ Rate adjustment multiplier field [24:16]; [24]: Rate adjustment Sign bit (1: higher rate; 0: lower rate); [29:25]: No effect when write, Reflect Sign Extension result when read. A 2's complement representation should be used if a negative rate adjustment is needed.

6.8. PTP_CFG_S_LO (PTP Time Config Sec Low Register, Page 0xe41, Address 0x13)

Table 9. PTP_CFG_S_LO (PTP Time Config Sec Low Register, Page 0xe41, Address 0x13)

Bit	Name	Type	Default	Description
19.15:0	PTP_Time_Config_s[15:0]	RW	0x0000	Time configuration sec field [15:0].

6.9. PTP_CFG_S_MI (PTP Time Config Sec Mid Register, Page 0xe41, Address 0x14)

Table 10. PTP_CFG_S_MI (PTP Time Config Sec Mid Register, Page 0xe41, Address 0x14)

Bit	Name	Type	Default	Description
20.15:0	PTP_Time_Config_s[31:16]	RW	0x0000	Time configuration sec field [31:16].

6.10. PTP_ CFG_S_HI (PTP Time Config Sec High Register, Page 0xe41, Address 0x15)

Table 11. PTP_S_HI (PTP Time Config Sec High Register, Page 0xe41, Address 0x15)

Bit	Name	Type	Default	Description
21.15:0	PTP_Time_Config_s[47:32]	RW	0x0000	Time configuration sec field [47:32].

6.11. PTP_TAI_CFG (PTP Application I/F Config Register, Page 0xe42, Address 0x10)

Table 12. PTP_TAI_CFG (PTP Application I/F Config Register, Page 0xe42, Address 0x10)

Bit	Name	Type	Default	Description
16.15:10	RSVD	RO	000000	Reserved.
16.9:8	trig_mod_sel	RW	00	Trigger Generate mode select. Trigger(s) start at time specified in TAI_TS_RW registers. Valid if tai_func_sel = 01. 00: Single rising edge 01: Single falling edge (The high/low level of the GPIO will be adjusted by HW automatically.) 10: Single pulse. The pulse width can be set by pulse_amt fields 11: Periodic pulses. The pulse period and duty cycle can be set by pulse_amt (Page 0xe42, Reg 17, bit[9:0]) and pulse_dc (Page 0xe42, Reg 17, bit[13:12]) fields, see section 6.12.
16.7	trig_iflate	RW	0	Trigger-if-Late Control. Valid if tai_func_sel (Bit 16.2:1) = 01. 1: Allow an immediate Trigger when setting a time value which is earlier than the current time.
16.6	evnt_rf_det	RW	0	Event Capture rising/falling edge detect selection. Valid if tai_func_sel (Bit 16.2:1) = 10. 0: Detection of a rising edge 1: Detection of a falling edge SW should take care of the high/low level of GPIO with this setting.
16.5	evnt_overwr_en	RW	1	Event Capture timestamp overwrite enable. Valid if tai_func_sel (Bit 16.2:1) = 10. 0: Keep the old value, 1: Cause the event timestamp to be overwritten if a new event is detected at the specific GPIO if the upper layer has not yet read the old event timestamp.
16.4:3	tai_gpio_num	RW	00	The GPIO number that is going to be armed.

Bit	Name	Type	Default	Description
16.2:1	tai_func_sel	RW	00	PTP Application Interface function select of selected GPIO. 00: Disable function 01: Trigger Generate 10: Event Capture 11: Trigger start time/Event timestamp read (according to current GPIO settings)
16.0	tai_cfg_set	RW, SC	0	PTP Application Interface configuration set. Setting this bit will issue a TAI Configuration 'Set' to the selected GPIO via tai_gpio_num

6.12. PTP_TRIG_CFG (PTP Trigger Config Register, Page 0xe42, Address 0x11)

Table 13. PTP_TRIG_CFG (PTP Trigger Config Register, Page 0xe42, Address 0x11)

Bit	Name	Type	Default	Description
17.15:14	RSVD	RO	00	Reserved.
17.13:12	pulse_dc	RW	00	Duty Cycle of a Trigger Pulse. Valid if tai_func_sel (Page 0xe42, Reg 16, bit[2:1]) = 01. Takes effect only on GPIO 0/1. 00: 0% 01: 25% 10: 50% 11: 75%. *Note: The options of 0%, 25%, and 75% are available only when pulse_amt_unit >= 8*PTPCLK period (64 ns).*
17.11:10	pulse_amt_unit	RW	00	The unit of pulse_amt field. 00: nano-second (ns) 01: micro-second (us) 10: milli-second (ms) 11: second (s)
17.9:0	pulse_amt	RW	0	Period of periodic pulses/Width of the single pulse. *Note 1: when pulse_amt_unit = 2'b00, the value that pulse_amt take effect will be floored to the multiple of PTPCLK period (8ns).* *Note 2: pulse_amt should be greater than 0.*

6.13. PTP_TAI_STA (PTP Application I/F Status Register, Page 0xe42, Address 0x12)

Table 14. PTP_TAI_STA (PTP Application I/F Status Register, Page 0xe42, Address 0x12)

Bit	Name	Type	Default	Description
18.15	tai_gpio0_func	RO	0	Indicate GPIO0's function 0: Trigger Generate 1: Event Capture
18.14	tai_gpio0_en	RO	0	GPIO0 function is enabled.

Bit	Name	Type	Default	Description
18.13	tai_gpio0_notify	RO,RC	0	Indicate if a Trigger is generated or Event Detected at GPIO0.
18.12	tai_gpio0_err	RO,RC	0	Indicate the start-time of the Trigger is earlier than the current time/an old Event timestamp value is kept at GPIO0.
18.11	tai_gpio1_func	RO	0	Indicate GPIO1's function 0: Trigger Generate 1: Event Capture
18.10	tai_gpio1_en	RO	0	GPIO1 function is enabled.
18.9	tai_gpio1_notify	RO,RC	0	Indicate if a Trigger is generated or Event Detected at GPIO1.
18.8	tai_gpio1_err	RO,RC	0	Indicate the start-time of the Trigger is earlier than the current time/an old Event timestamp value is kept at GPIO1.
18.7:0	RSVD	RO	0x00	Reserved.

6.14. PTP_TAI_TS_NS_LO (PTP TAI Timestamp Nano-Sec Low Register, Page 0xe42, Address 0x13)

Table 15. PTP_TAI_TS_NS_LO (PTP TAI Timestamp Nano-Sec Low Register, Page 0xe42, Address 0x13)

Bit	Name	Type	Default	Description
19.15:0	TAI_TS_ns[15:0]	RW	0x0000	PTP Application Interface timestamp Read/Write interface nanosec field [15:0].

6.15. PTP_TAI_TS_NS_HI (PTP TAI Timestamp Nano-Sec High Register, Page 0xe42, Address 0x14)

Table 16. PTP_TAI_TS_NS_HI (PTP TAI Timestamp Nano-Sec High Register, Page 0xe42, Address 0x14)

Bit	Name	Type	Default	Description
20.15:14	RSVD	RO	00	Reserved.
20.13:0	TAI_TS_ns[29:16]	RW	0	PTP Application Interface timestamp Read/Write interface nanosec field [29:16].

6.16. PTP_TAI_TS_S_LO (PTP TAI Timestamp Sec Low Register, Page 0xe42, Address 0x15)

Table 17. PTP_S_LO (PTP Time Config Sec Low Register, Page 0xe41, Address 0x13)

Bit	Name	Type	Default	Description
21.15:0	TAI_TS_s[15:0]	RW	0x0000	PTP Application Interface timestamp Read/Write interface sec field [15:0].

6.17. PTP_TAI_TS_S_HI (PTP TAI Timestamp Sec High Register, Page 0xe42, Address 0x16)

Table 18. PTP_S_MI (PTP Time Config Sec Mid Register, Page 0xe41, Address 0x14)

Bit	Name	Type	Default	Description
22.15:0	TAI_TS_s[31:16]	RW	0x0000	PTP Application Interface timestamp Read/Write interface sec field [31:16].

6.18. PTP_TRX_TS_STA (PTP TxRx Timestamp Status Register, Page 0xe43, Address 0x10)

Table 19. PTP_TRX_TS_STA (PTP TxRx Timestamp Status Register, Page 0xe43, Address 0x10)

Bit	Name	Type	Default	Description
16.15	txts_sync_rdy	RO	0	Sync message Transmit timestamp ready.
16.14	txts_dlyreq_rdy	RO	0	Delay_Request Transmit timestamp ready.
16.13	txts_pdlyreq_rdy	RO	0	PDelay_Request Transmit timestamp ready.
16.12	txts_pdlyrsp_rdy	RO	0	PDelay_Response Transmit timestamp ready.
16.11	rxts_sync_rdy	RO	0	Sync message Receive timestamp ready.
16.10	rxts_dlyreq_rdy	RO	0	Delay_Request Receive timestamp ready.
16.9	rxts_pdlyreq_rdy	RO	0	PDelay_Request Receive timestamp ready.
16.8	rxts_pdlyrsp_rdy	RO	0	PDelay_Response Receive timestamp ready.
16.7:5	RSVD	RO	000	Reserved.
16.4	trxts_overwr_en	RW	1	Transmit/Receive timestamp overwrite enable. When a new PTP packet comes that needs to be time stamped, HW will 0: Keep the old timestamp value, 1: Overwrite the old timestamp value if the older one has not been read by the upper layer.
16.3:2	trxts_msgtype_sel	RW	00	Message Type of Transmit/Receive timestamp select. 00: Sync 01: Delay_Request 10: PDelay_Request 11: PDelay_Response
16.1	trxts_sel	RW	0	Transmit/Receive timestamp read select. 0: Tx 1: Rx
16.0	trxts_rd	RW, SC	0	Transmit/Receive timestamp read enable. Issue a ‘Read’ for Transmit/Receive timestamp.

6.19. PTP_TRX_TS_INFO (PTP TxRx Timestamp Info Register, Page 0xe44, Address 0x10)

Table 20. PTP_TRX_TS_INFO (PTP TxRx Timestamp Info Register, Page 0xe44, Address 0x10)

Bit	Name	Type	Default	Description
16.15:12	trxts_transspec	RO	0000	Transmit/Receive timestamp Transport Specific field.
16.11:8	trxts_msgtype	RO	0000	Transmit/Receive timestamp Message Type field.
16.7:4	RSVD	RO	0000	Reserved.
16.3:0	trxts_ptpver	RO	0000	Transmit/Receive timestamp PTP Version field.

6.20. PTP_TRX_TS_SH (PTP TxRx Timestamp Source Hash Register, Page 0xe44, Address 0x11)

Table 21. PTP_TRX_TS_SH (PTP TxRx Timestamp Source Hash Register, Page 0xe44, Address 0x11)

Bit	Name	Type	Default	Description
17.15:0	trxts_srchash	RO	0x0000	Transmit/Receive timestamp Source Port ID Hash field.

6.21. PTP_TRX_TS_SID (PTP TxRx Timestamp Seq ID Register, Page 0xe44, Address 0x12)

Table 22. PTP_TRX_TS_SID (PTP TxRx Timestamp Seq ID Register, Page 0xe44, Address 0x12)

Bit	Name	Type	Default	Description
18.15:0	trxts_seqid	RO	0x0000	Transmit/Receive timestamp Sequence ID field.

6.22. PTP_ TRX_TS NS_LO (PTP TxRx Timestamp Nano-Sec Low Register, Page 0xe44, Address 0x13)

Table 23. PTP_ TRX_TS NS_LO (PTP TxRx Timestamp Nano-Sec Low Register, Page 0xe44, Address 0x13)

Bit	Name	Type	Default	Description
19.15:0	TXRX_TS_ns[15:0]	RO	0x0000	Transmit/Receive timestamp nanosec field [15:0].

6.23. PTP_ TRX_TS NS_HI (PTP TxRx Timestamp Nano-Sec High Register, Page 0xe44, Address 0x14)

Table 24. PTP_ TRX_TS NS_HI (PTP TxRx Timestamp Nano-Sec High Register, Page 0xe44, Address 0x14)

Bit	Name	Type	Default	Description
20.15:14	RSVD	RO	00	Reserved.
20.13:0	TXRX_TS_ns[29:16]	RW	0	Transmit/Receive timestamp nanosec field [29:16].

6.24. PTP_ TRX_TS S_LO (PTP TxRx Timestamp Sec Low Register, Page 0xe44, Address 0x15)

Table 25. PTP_ TRX_TS S_LO (PTP TxRx Timestamp Sec Low Register, Page 0xe44, Address 0x15)

Bit	Name	Type	Default	Description
21.15:0	TXRX_TS_s[15:0]	RW	0x0000	Transmit/Receive timestamp sec field [15:0].

6.25. PTP_ TRX_TS S_MI (PTP TxRx Timestamp Sec Mid Register, Page 0xe44, Address 0x16)

Table 26. PTP_ TRX_TS S_MID (PTP TxRx Timestamp Sec Mid Register, Page 0xe44, Address 0x16)

Bit	Name	Type	Default	Description
22.15:0	TXRX_TS_s[31:16]	RW	0x0000	Transmit/Receive timestamp sec field [31:16].

6.26. PTP_ TRX_TS S_HI (PTP TxRx Timestamp Sec High Register, Page 0xe44, Address 0x17)

Table 27. PTP_ TRX_TS S_LO (PTP TxRx Timestamp Sec High Register, Page 0xe44, Address 0x17)

Bit	Name	Type	Default	Description
23.15:0	TXRX_TS_s[47:32]	RW	0x0000	Transmit/Receive timestamp sec field [47:32].

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