DESIGN INTERNSHIP(DI-45)

FOR

MAVEN SILICON

AHB TO APB BRIDGE DESIGN

PROJECT REPORT

SUBMITTED BY-

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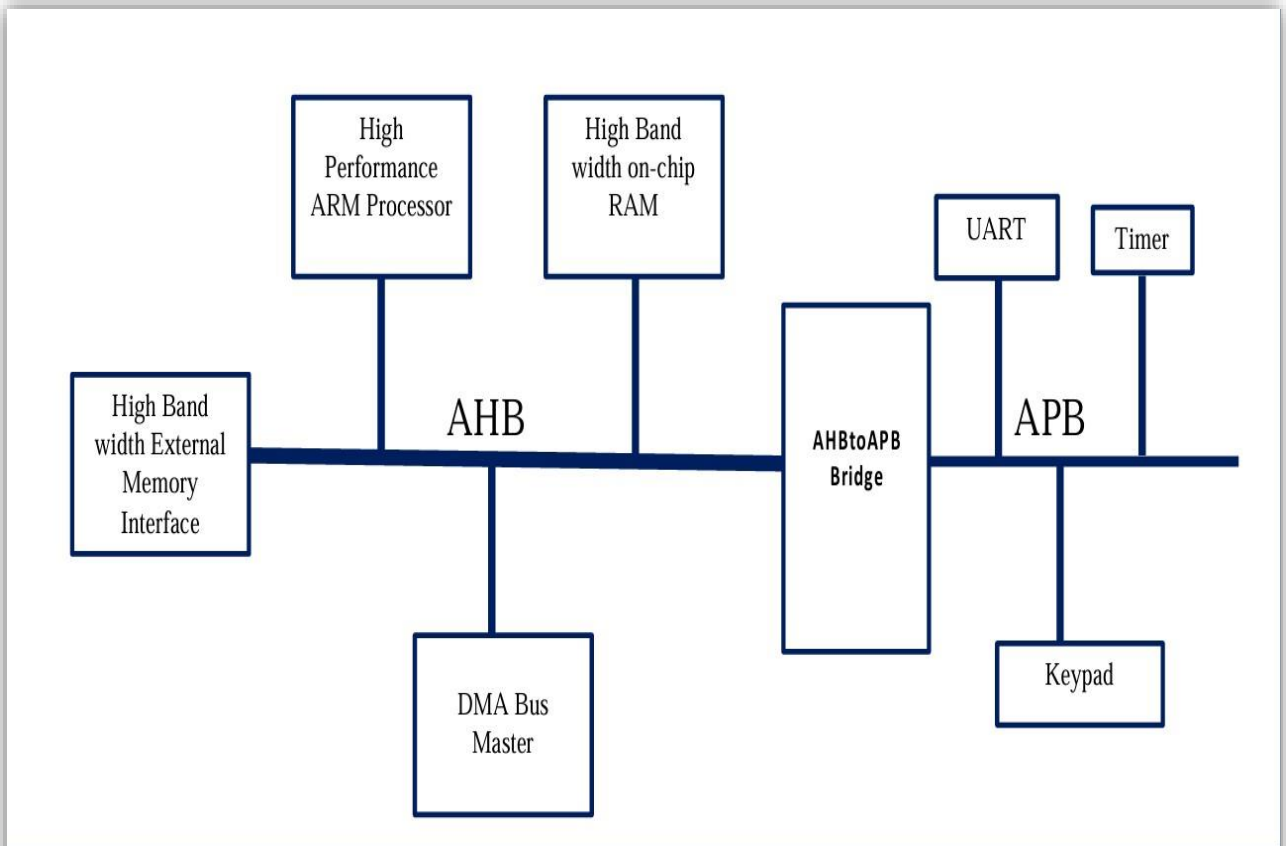
1. PROTOCOL:

The Advanced Micro controller Bus Architecture (**AMBA**) bus protocols is a set of interconnect specifications from ARM that standardizes on chip communication mechanisms between various functional blocks (or IP) for building high performance SOC designs. These designs typically have one or more micro controllers or microprocessors along with several other components—internal memory or external memory bridge, DSP, DMA, accelerators and various other peripherals like USB, UART, PCIE, I2C etc—all integrated on a single chip. The primary motivation of AMBA protocols is to have a standard and efficient way to interconnecting these blocks with re-use across multiple designs. These are available in three standards: AHB, APB, AXI, ASB.

The following diagram below illustrates a typical AMBA based SOC design which uses AHB (Advanced High-Performance Bus) and APB (Advanced Peripheral Bus)



Typical AMBA System

AHB (Advanced High-Performance Bus):

The AMBA AHP is for high performance, high clock frequency system modules.

The AHP acts as the high frequency system backbone bus. AHB supports the efficient connection of processors, on chip memories and off chip external interfaces with low power peripheral functions.

AMBA AHB implements the following features required for high performance, high clock including: burst transfer, split transactions, single cycle bus master, handover, single clock edge operation, non tri slate implementation, wider bus data configurations.

Typical AMBA AHB system design consists the following components:

- AHB Master,
- AHB Slave,
- AHB Arbiter

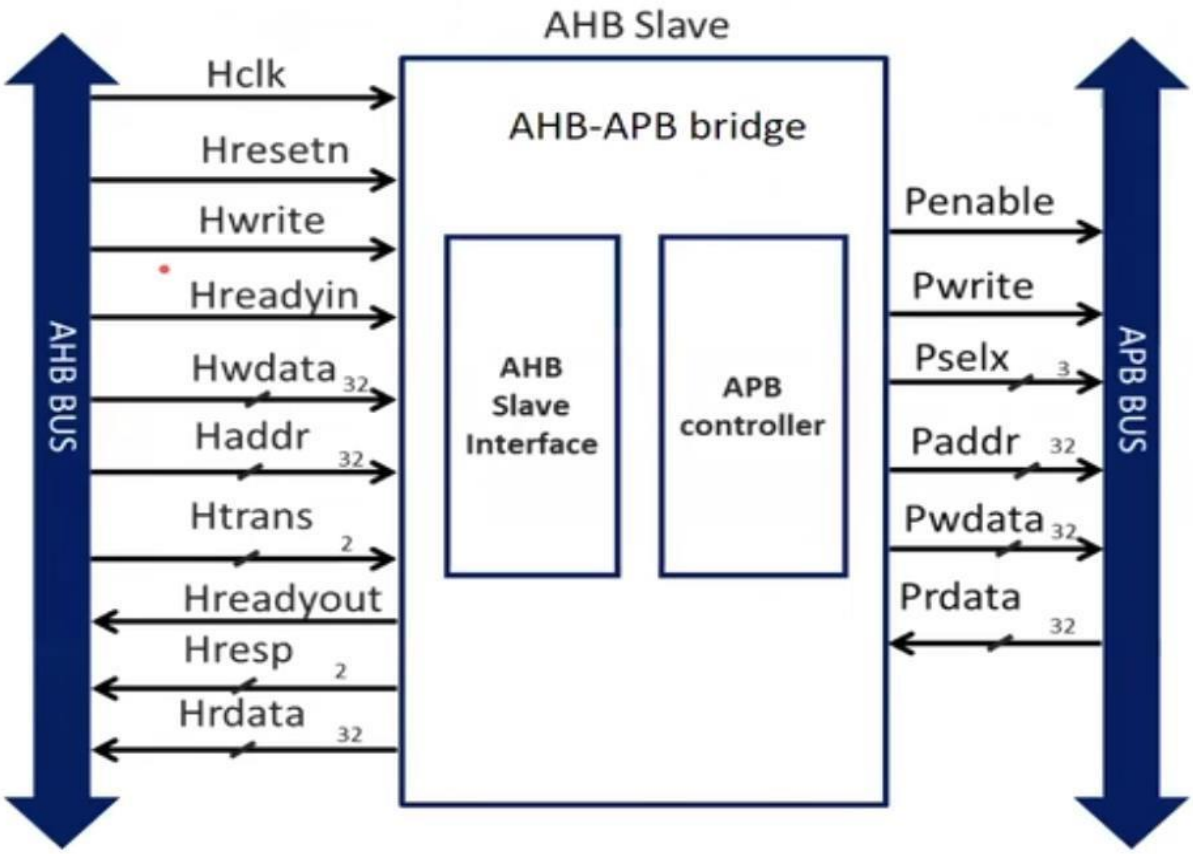
APB (Advanced Peripheral Bus):

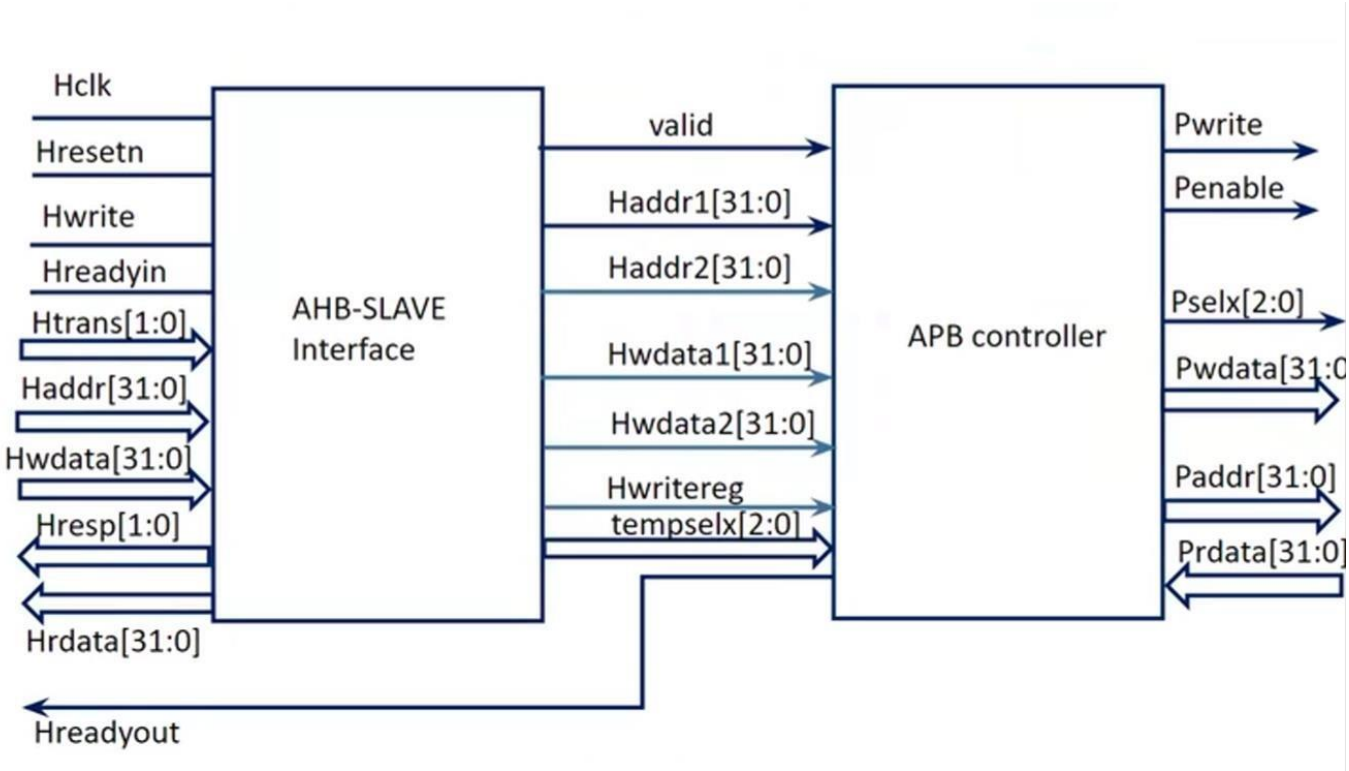
The Advanced Peripheral Bus (APB) is used for connecting low bandwidth peripherals. It is a simple non-pipelined protocol that can be used to communicate (read or write) from a bridge/master to a number of slaves through the shared bus. The reads and writes share the same set of signals and no burst data transfers are supported.

Following are the advantages of APB peripherals:

- The frequency operation easy to achieve.
- Performance is independent of mark space ratio of clock.
- Static time analysis is simplified by the use of single clock edge. No special consideration is required for automatic test insertion . Easy integration with clock-based simulators.

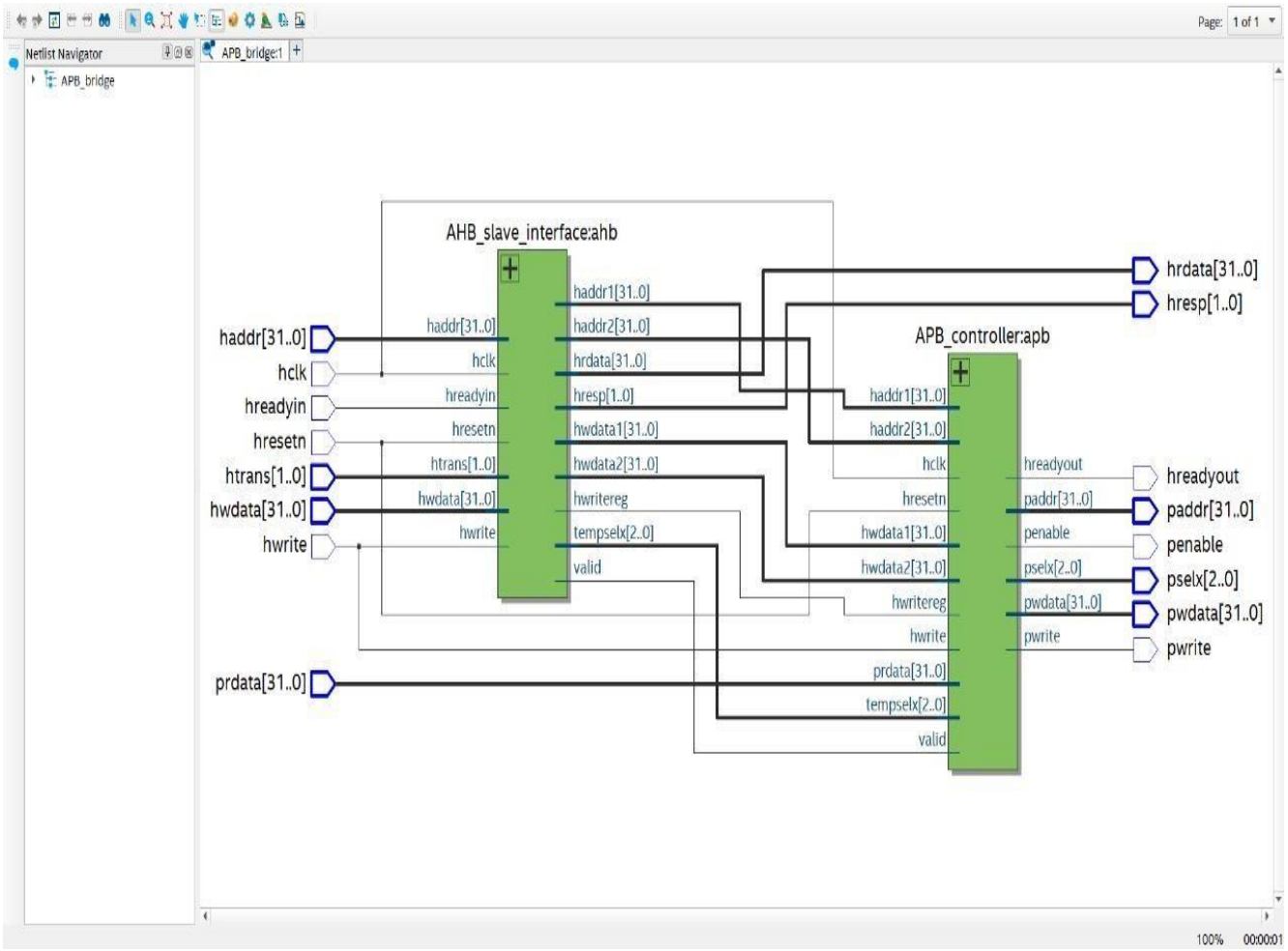
2. BLOCK DIAGRAM:





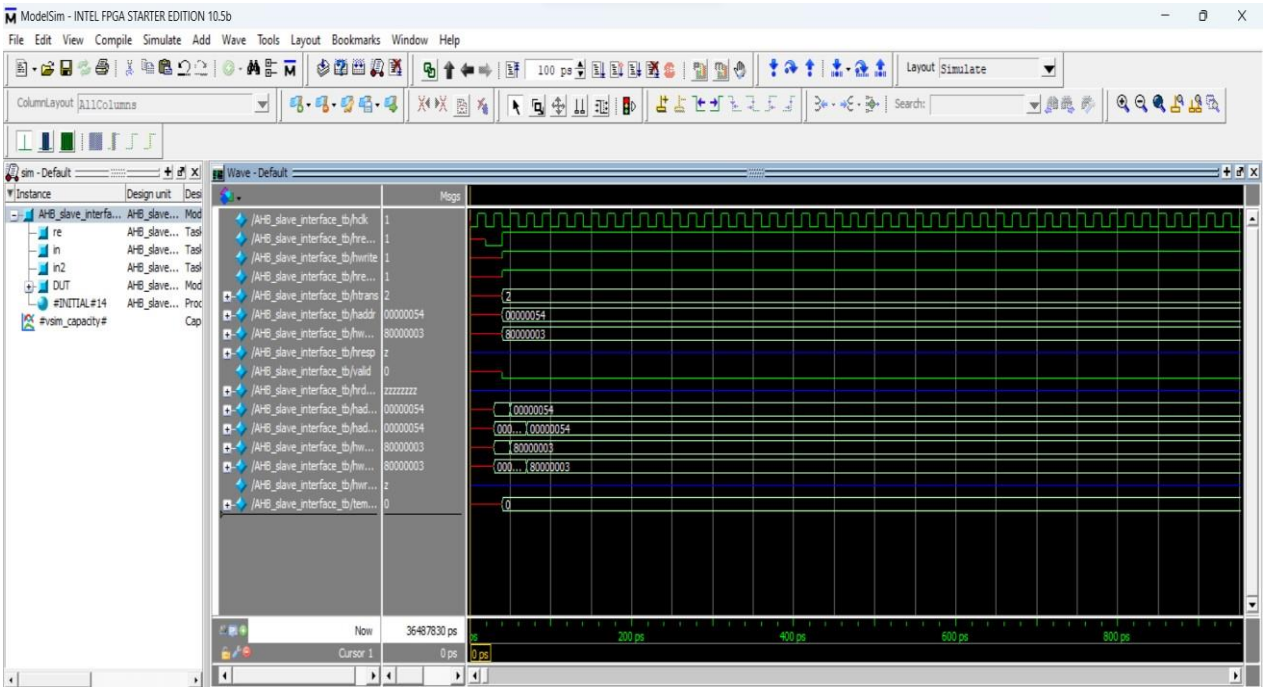
3. SYNTHESIS:

AHB2APB BRIDGE:

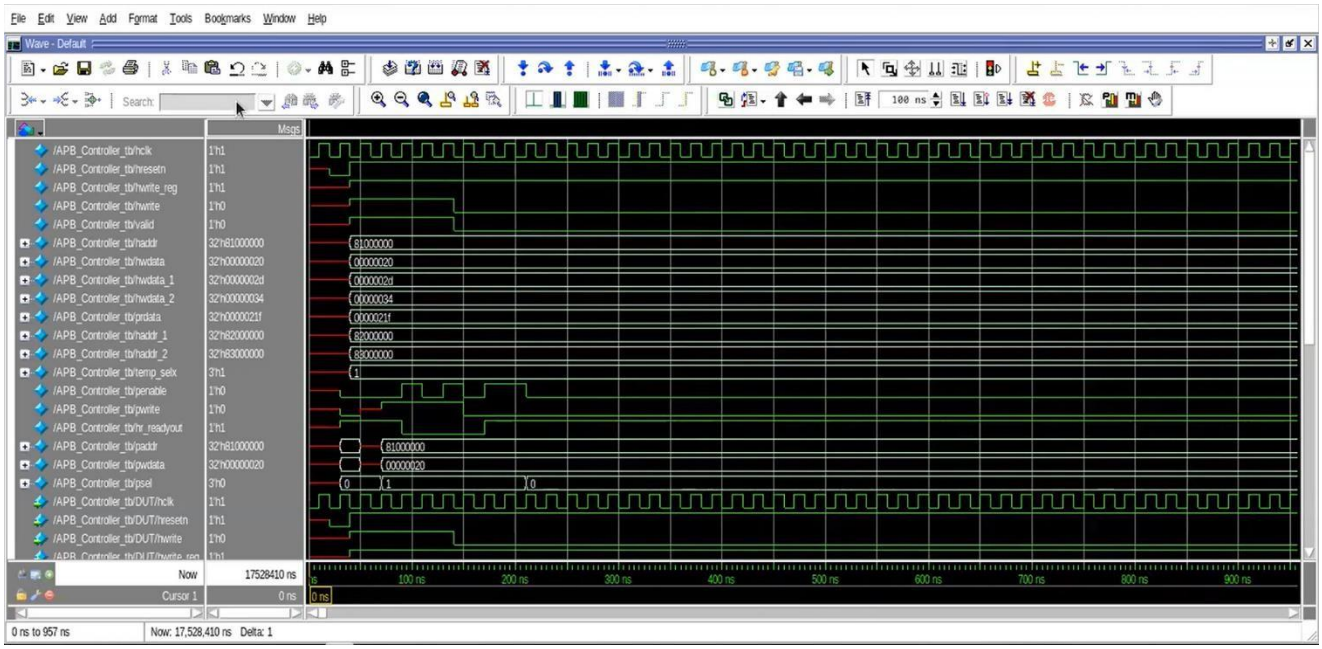


4. STIMULATION:

A) AHB_SLAVE_INTERFACE:

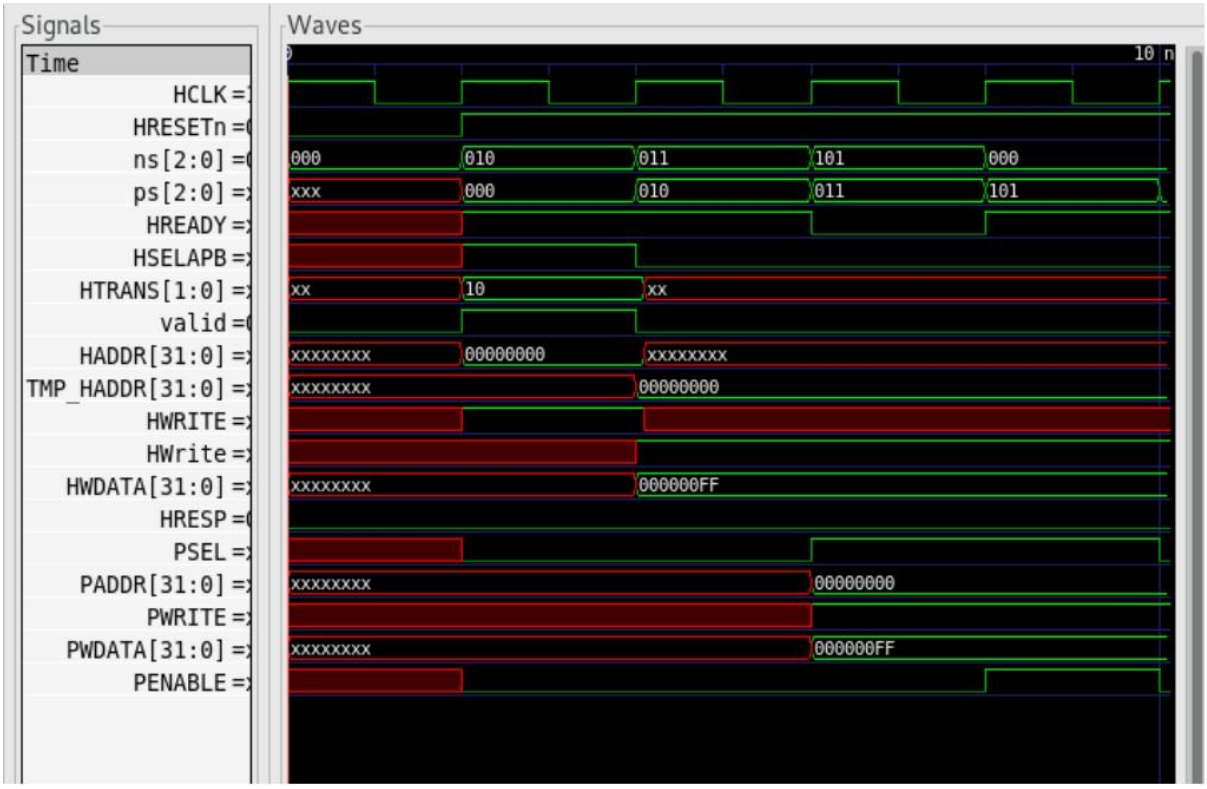


B) APB_CONTROLLER_INTERFACE:

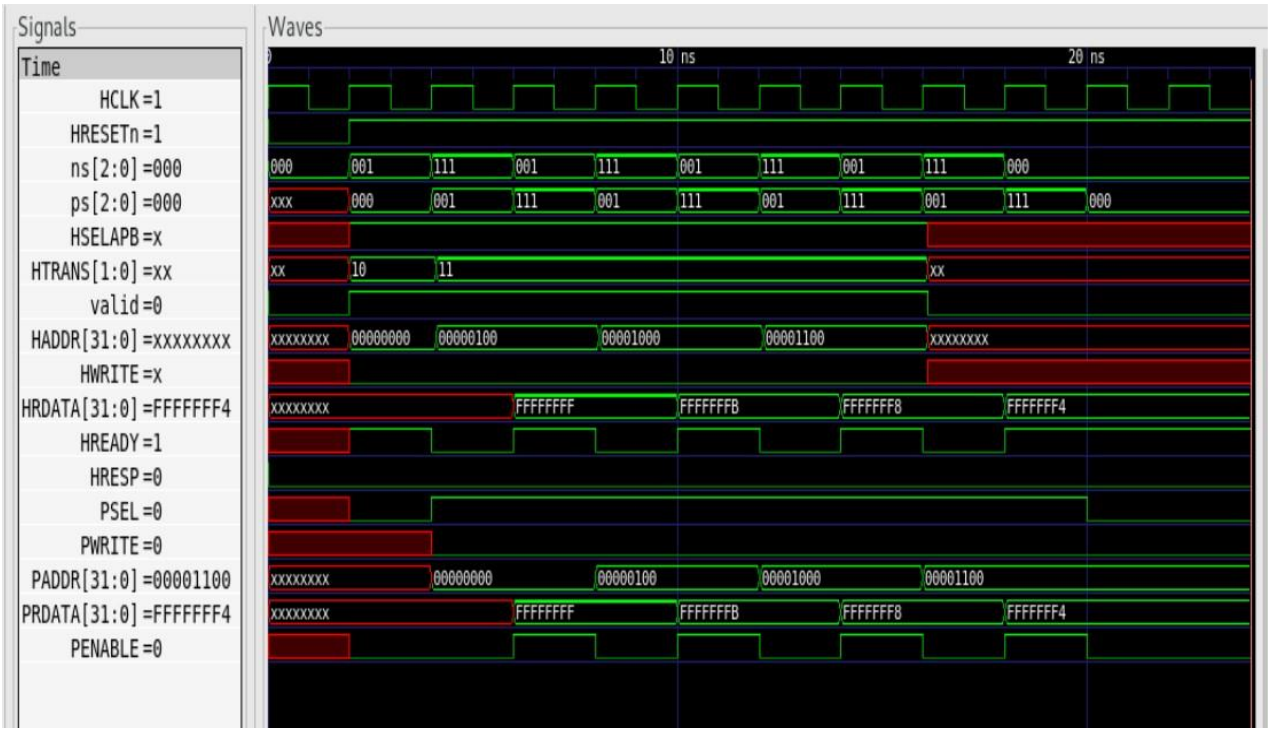


C) SINGLE_READ:

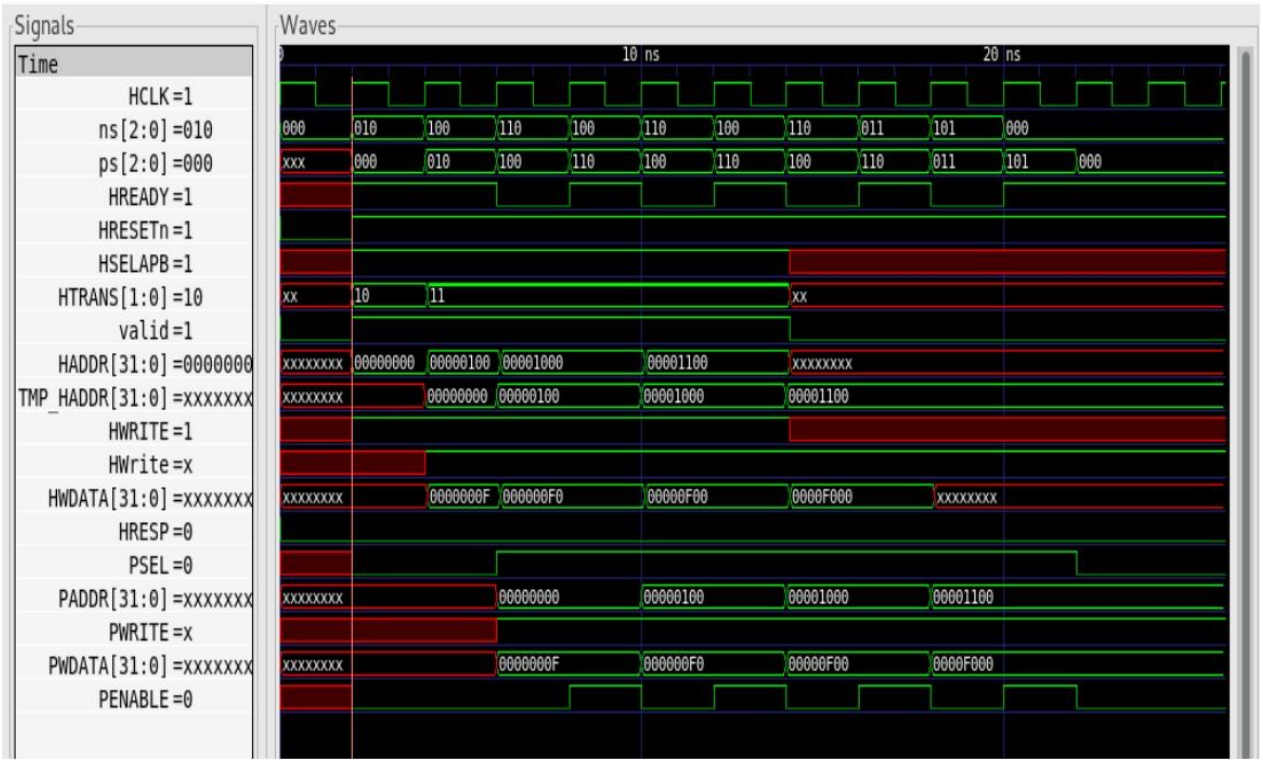
D) SINGLE_WRITE:



E) BURST_READ:



F) BURST_WRITE:



CONCLUSION:

The AHB2APB design project has been a significant endeavor aimed at achieving efficient communication between AHB (Advanced High-performance Bus) and APB (Advanced Peripheral Bus) interfaces. Through the course of this project, several key observations and outcomes have been identified.

First and foremost, the successful integration of the AHB2APB bridge demonstrates the feasibility of bridging communication between these distinct bus architectures. The design has shown promising results in terms of data transfer speed, latency, and overall system performance. The adherence to industry standards and protocols, such as the Arm AMBA specifications, has ensured compatibility and interoperability within existing systems.

The AHB2APB design project has provided valuable insights into the intricacies of bus bridging and has laid the foundation for future developments in this field. The successful implementation opens doors to a wide range of applications where seamless communication between AHB and APB interfaces is essential. With continuous refinement and adaptation.