Indian Institute of Technology Kharagpur

AUTUMN Semester, 2021
COMPUTER SCIENCE AND ENGINEERING

Computer Organization Laboratory

Assignment-6: Verilog Design and Implementation of Useful Arithmetic Circuits

Full Marks: 40

Time allowed: 6 hours

INSTRUCTIONS: Make one submission per group in the form of a single zipped folder containing your Verilog source code files(s) and Verilog testbench(es). Name your submitted zipped folder as `Assgn_6_Grp_<Group_no>.zip` and (e.g. `Assgn_6__Grp_25.zip`). Inside each submitted source and testbench files, there should be a clear header describing the assignment no., problem no., semester, group no., and names of group members. Liberally comment your code to improve its comprehensibility.

1. [**Bidirectional Barrel Shifter**] Design (using Verilog), simulate (using an appropriate Verilog testbench) and implement an 8-bit *Bidirectional Barrel Shifter* circuit, which can perform logical shift by a specified amount `shamt`, either in right or in left direction depending on a control signal `dir`. The design should consist only of 2:1 multiplexors. The interface of your circuit should be the following:
   `module barrel_shifter (input [7:0] in, input [2:0] shamt, input dir, output [7:0] out)`,
   where `dir = 1` for left shifts and `dir = 0` for right shifts. An example architecture that can only perform unidirectional shifts has been shown in Fig. 1. (10 marks)
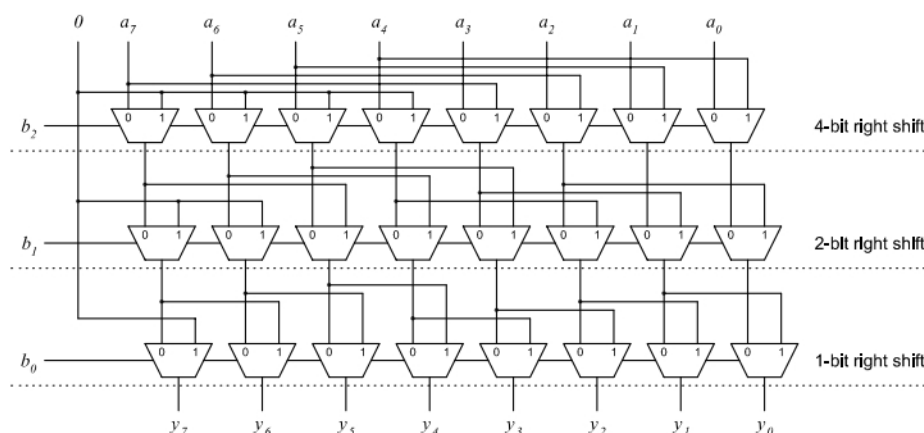

Figure 1: An 8-bit unidirectional barrel shifter circuit.

2. [**Bit-serial Adder**] Design (using Verilog), simulate (using an appropriate Verilog testbench), and implement (on a FPGA platform supported by your CAD software tool), a *Bit-serial Adder* circuit. The input-side shift-registers used in the datpath of your bit-serial adder should have "parallel load" capabilities, such that the 8-bit operands can be loaded in each of them in one clock cycle. Come up with a proper interface of your design, which includes all input control signals and a clock signal. Suggestion: you can adopt synchronous control signals in your design, to minimize the hardware footprint.   (10 marks)

3. [**Sequential Signed Binary Multiplier (Booth Multiplier)**] Design (using Verilog), simulate (using an appropriate Verilog testbench), and implement (on a FPGA platform supported by your CAD software tool), a circuit for multiplication of two 8-bit two's complement integers, using the *Booth Multiplication Algorithm*. The input-side operand registers used in the datpath of your multiplier should have "parallel load" capabilities such that the 8-bit operands can be loaded in each of them in one clock cycle. Come up with a proper interface for your design. Suggestion: you can adopt synchronous control signals in your design, to minimize the hardware footprint.   (20 marks)

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