

Concept of sequential circuit

A sequential circuit is one whose output depend not only on its current inputs but also on the past sequence of inputs. There are two main type sequential circuit.

- Asynchronous sequential circuit
- Synchronous sequential circuit.

- Asynchronous sequential circuit:

A system whose output depend upon other order in which its input variables change and can be affected at any instant of time.

- Synchronous sequential circuit: If all the output of sequential circuit change affect with respect to active transition of clock signal then sequential circuit is called synchronous sequential circuit. Therefore output of synchronous sequential circuit are in synchronous with either only positive edge or only negative edge of clock signal.

Clock signal and Triggering

- Clock signal: Clock signal is a periodic signal and its ON time & off time need not be the same. It can be represent the clock

Signal as a square wave, When both it ON time and off time are same. The clock signal is shown in the following figure:



The reciprocal of time period of clock signal is known as the frequency of the clock signal. The frequency at which the Sequential circuit can be operated accordingly the clock signal frequency has to be chosen.

Type of triggering

There are two type of triggering level and edge are

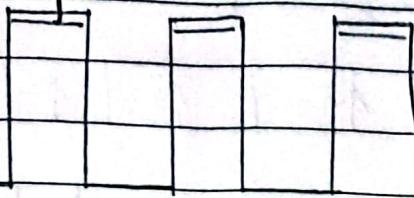
- Level triggering
- Edge triggering

- level triggering: There are two levels namely logic high and logic low in clock signal. following are two type

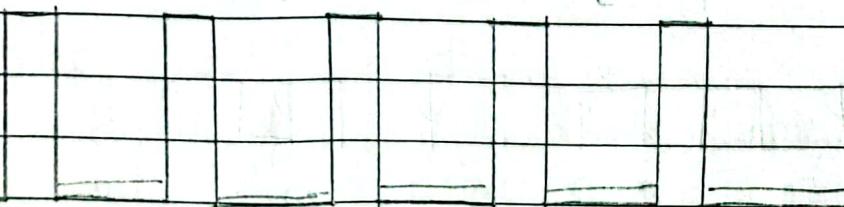
Positive level triggering
Negative level triggering

If the sequential circuit is operated with clock signal when it is high then that type of triggering is known as positive level

triggering.



If the Sequential circuit is operated with clock signal when it is in logic low, then that type of triggering is known as Negative triggering.



Edge triggering:

There are two type of transition that occur in clock signal. That means, the clock signal transition either from logic low to logic high or logic high to logic low.

following are the type of edge triggering based on the transition of clock signal.

Positive edge triggering

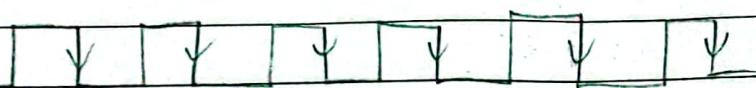
Negative edge triggering.

If the Sequential circuit is operated with the clock signal that is transitioning from logic low to logic high, then that type of triggering known as positive edge triggering. It is also called as rising

edge triggering.



If the sequential circuit is operated with the clock signal that is transitioning from logic high to low, then that type of triggering is known as Negative edge triggering. It is also called falling edge triggering.



latches

Latches operate with enable signal, which is level sensitive. The following table shows state table of SR latches are

SR latches

S	R	Qn+1
0	0	Qn
0	1	0
1	0	1
1	1	-

circuit diagram of SR latch is shown in the following figure:

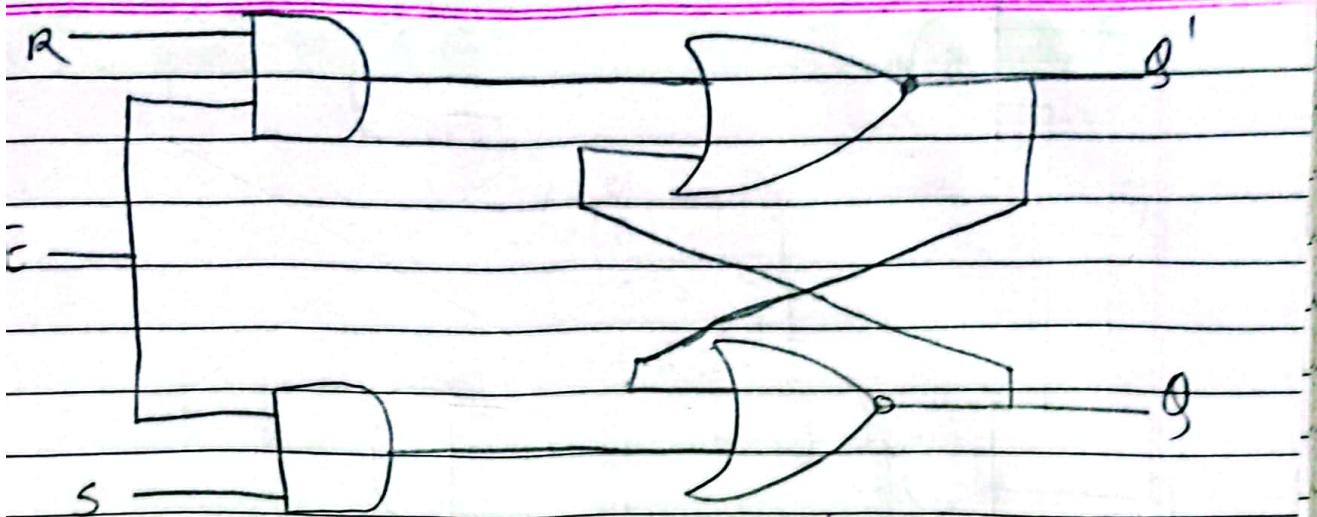


FIGURE-1

Flip-flops

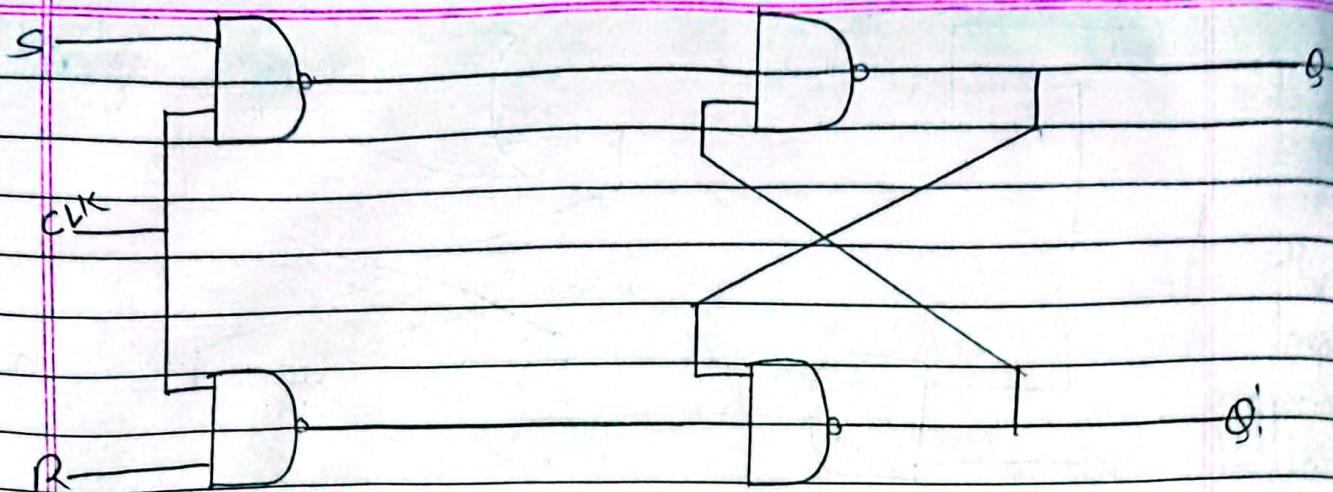
A flip flop is a device which store a single bit of data; one of its two state represents as "one" and the other represents a "zero".

SR Flip flop:

SR flip flop operates with only positive clock transitions or negative clock transitions. Whereas SR latch operate with enable signal.
The following table of SR flip flop

S	R	Q	Q'
0	0	0 _n	0 _n
0	1	1	0
1	0	0	1
1	1	0 _n	0 _n

The circuit diagram of SR flip flop

 $Q_n = \text{memory}$

Clk	S	R	Q	Q'
0	*	*	Q_n	Q_n
1.	0	0	Q_n	Q_n
1.	0	1	0	1
1.	1	0	1	0
1.	1	1	Invali d	Invali d

case I

I $Clk = 0$

$S' = S' + 1 = 1$

$R' = R' + 1 = 1$

II $Clk = 1$

$S' = 0$ $R' = 0$

$S = 0 = R = 1$

$S' = 1 = R' = 0$

$S = 1 \quad R = 0$

$S' = 0 \quad R' = 1$

The following table shows the characteristic table of SR flip flop:

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	*
1	0	0	*
1	0	1	1
1	1	0	1
1	1	1	*

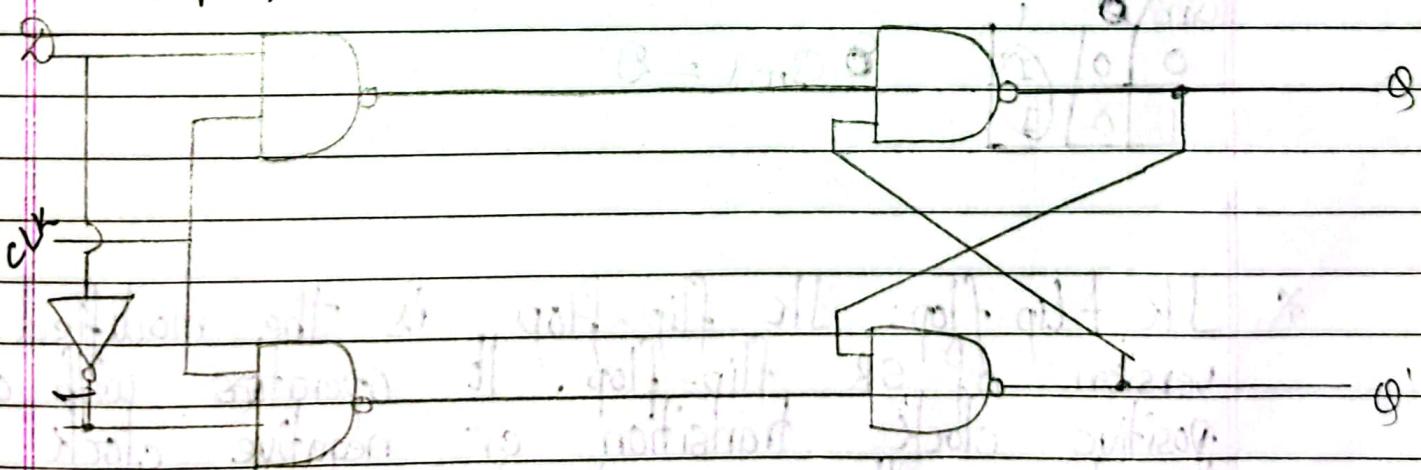
K-map

Q_n	SK	00	01	11	10
0		0	0	*	1
1	1	1	0	*	1

$$Q_{n+1} = S + R'Q_n$$

D - flip flop

D flip flop operate with only positive clock transitions or negative clock transitions. The output of D flip-flop is insensitive to the changes in the input. D expect for active transition of the clock signal. The circuit diagram of D flip-flop



This circuit has single input, D and output Q & Q'. The operation of D flip-flop is similar to D latch. But, this flip flop affects the outputs only when positive transition of clock signal is applied instead of active enable.

Truth table

clk	J	K	Q'
0	x	Q _n	Q _n
1	0	0	1
1	1	1	0

* flip-flop always hold the information, which is available on data input, \ominus of earlier positive transition of clock signal.

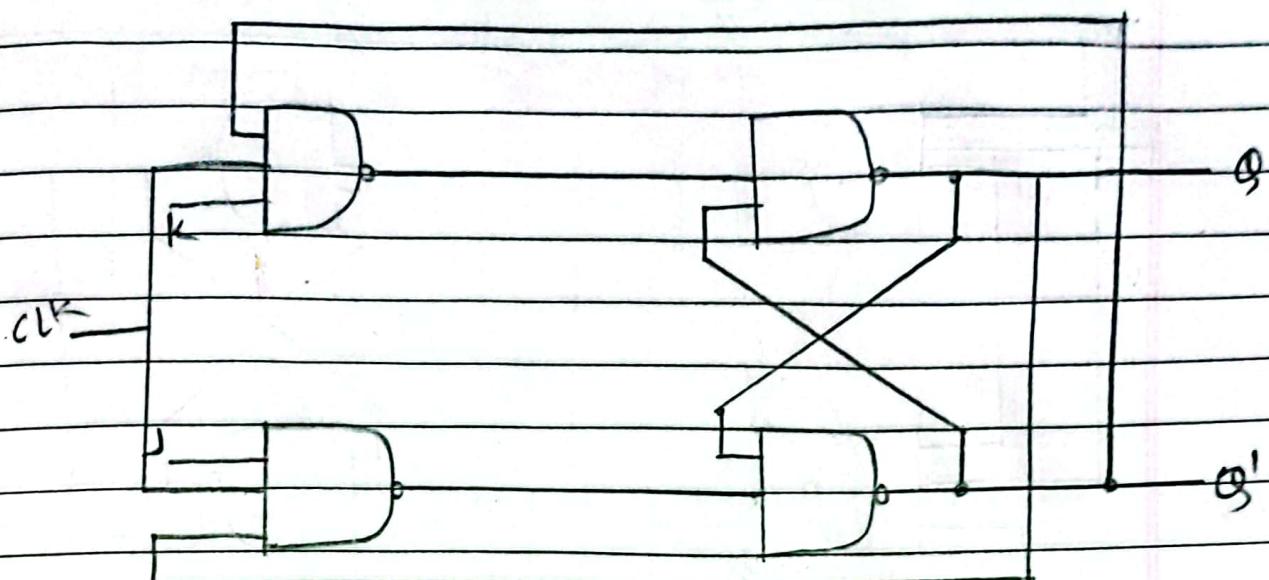
Characteristic table

Q _n	D	Q _{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

k-map for D

Q _n	D	Q _{n+1} = D
0	0	1
1	0	1

* JK Flip flop: JK flip-flop is the modified version of SR flip-flop. It operates with only positive clock transition or negative clock transition. The circuit diagram:



This circuit has two inputs, J or K and two outputs Q and Q'. The operation of JK flip-flop is similar to SR flip-flop.

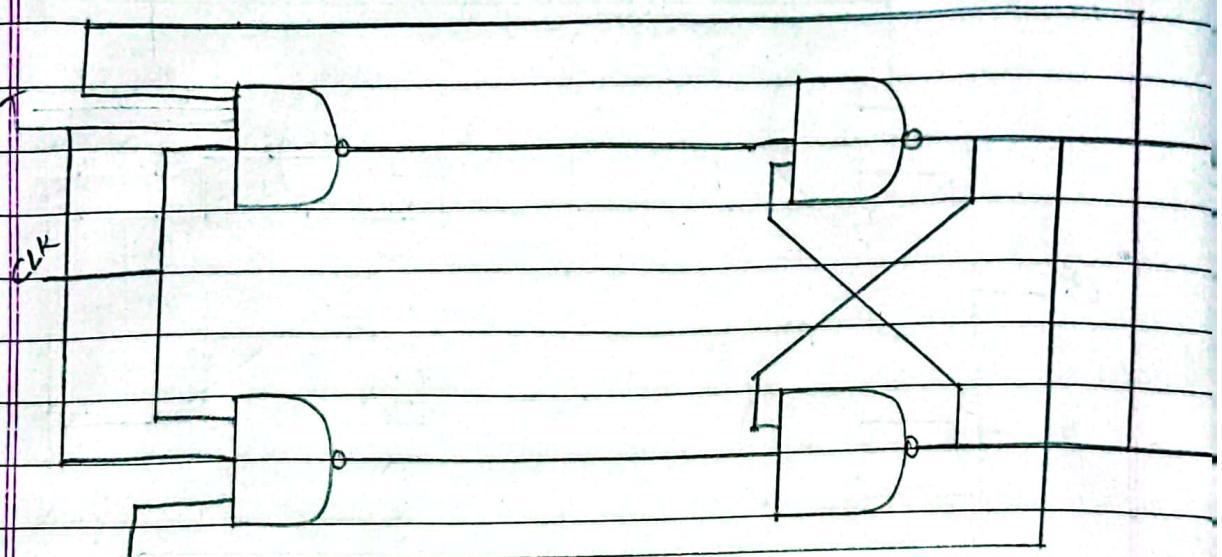
Truth table:

clk	J	K	Q	Q'
0	X	X	Qn	Qn
1	0	0	Qn	Qn
1	0	1	0	1
1	1	0	1	0
1	1	1	Qn	Qn'

Characteristic table:

Qn	J	K	Qnti	k-map for JK flip
0	0	0	0	Qn 00 01 11 10
0	0	1	0	00 01 (11)
0	1	0	1	00 01 (11)
0	1	1	1	00 01 (11)
1	0	0	1	Qnti = Qn' + QnK'
1	0	1	0	
1	1	0	1	
1	1	1	0	

T flip-flops: T flip flop is the simplified version of JK flip flop. It is obtained by connecting the same input 'T' to both inputs of JK ff. It is operate with only positive clock transition or negative clock transition.



This circuit has single input T and two output Q and Q' . The operation of T flip flop is same as that of JK flip flop.

Truth table

clk	T	Q_n	Q'_n
0	X	Q_n	Q'_n
1	0	Q_n	Q'_n
1	1	Q'_n	Q_n

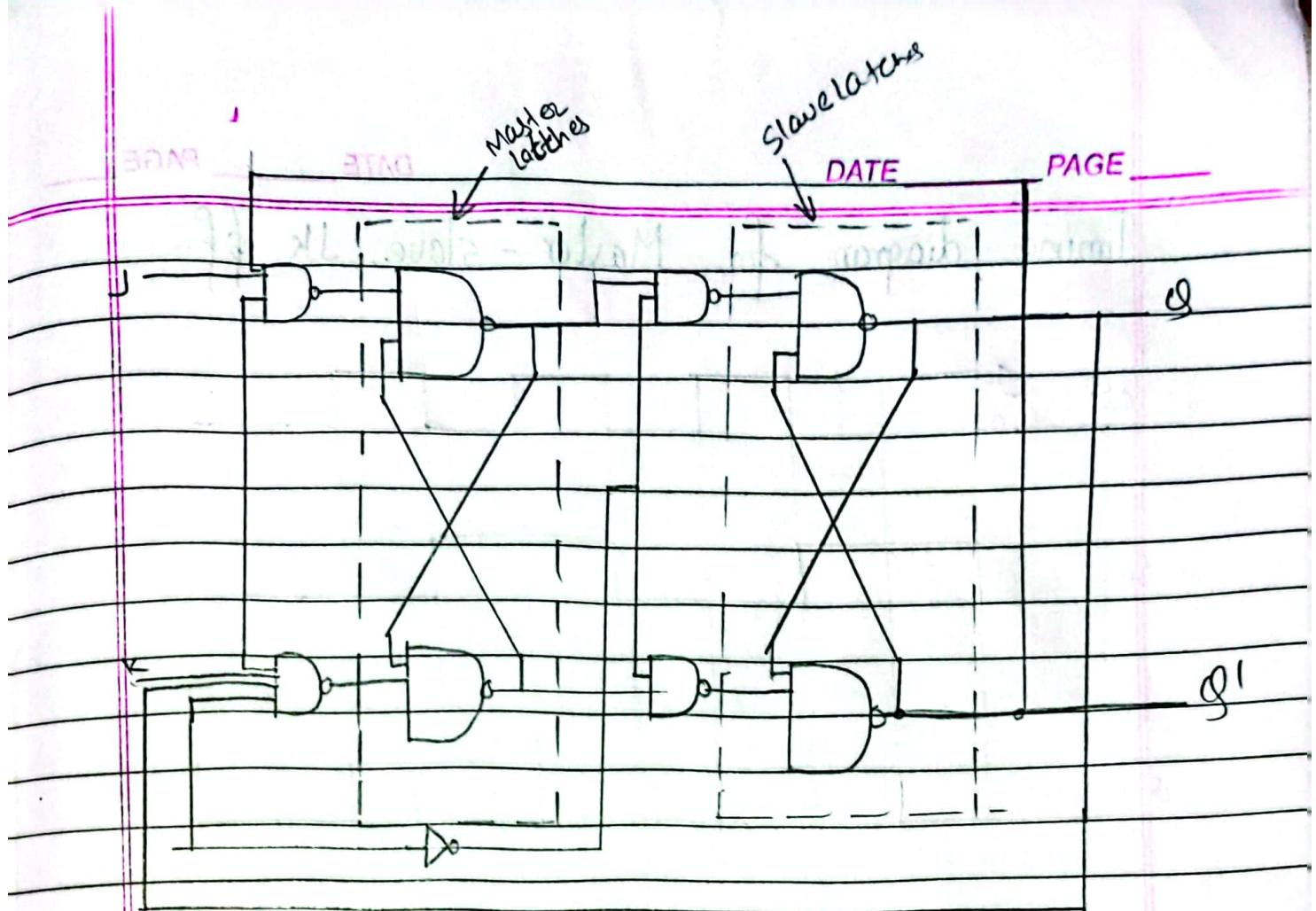
Characteristic table

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$Q_n \backslash T$	0	1
0	1	1
1	1	0

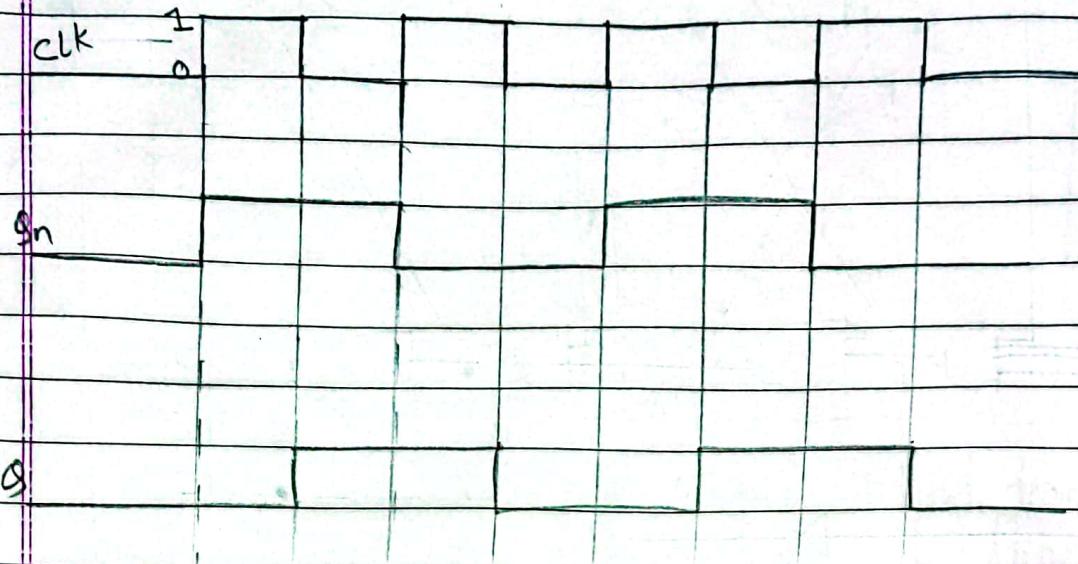
$$Q_{n+1} = T Q_n + T' Q_n'$$

Design Master slave flip flop.



- Assume in 1 state $c=0, j=k=1$
- Due to feedback, the output of the j -gate is 0, output of k -gate is 1.
- If clock is changed to $c=1$ then master is reset.
- Assume in 0 state, $c=0, j=k=1$.
- Due to feedback, the output of j -gate is 1, output of k gate is 0.
- If clock is changed + $c=1$, then master is set.
- 1 on J input line, 0 on K input line sets the ff.
- If in 1-state unchanged blk SR set to 0.
- If in 0-state, S set to 1, R set to 0.

Timing diagram for Master - slave JK ff.



Combinational circuit

- Outputs depend only on present input

- feedback path is not present

- Memory element are not required

Sequential circuit

- Output depend on both present input and present state.

- feedback path is present

- Memory element are required

Clock signal is not required

Easy to design

Difficult to design