

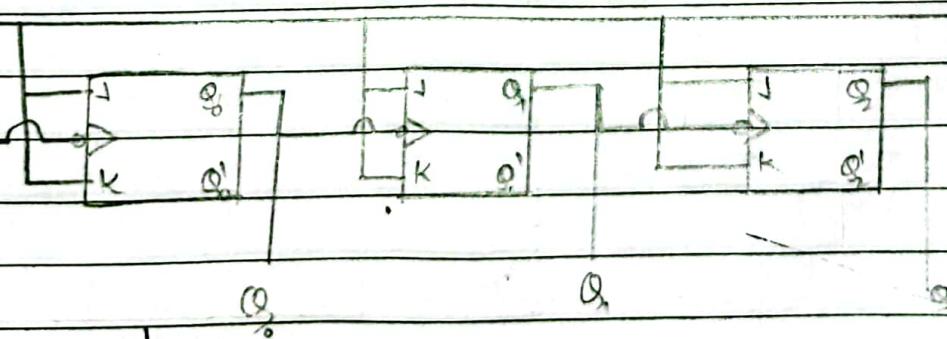
Concept of counter: A special type of sequential circuit used to count the pulse is known as counter. Based on the clock pulse, the output of the counter contain a predefined states.

There are two type of Counter based on the flip-flops that are connected in synchronous

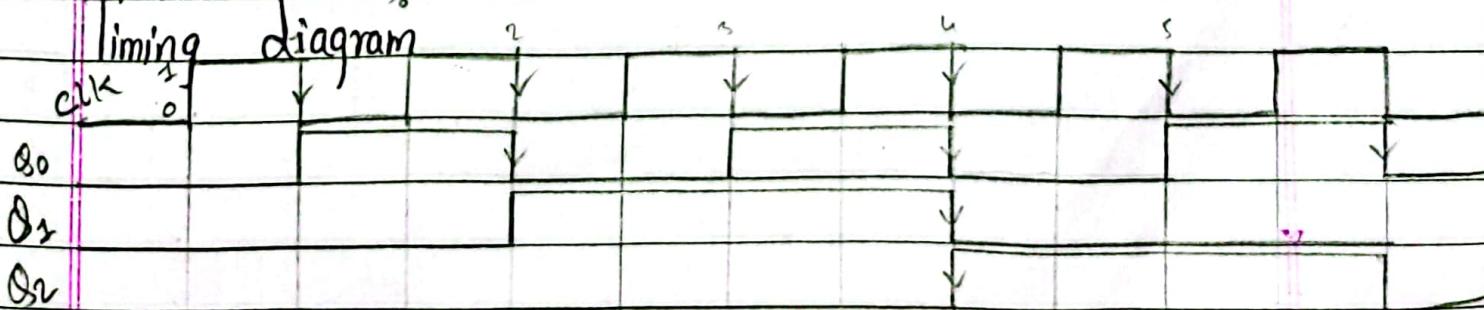
- Asynchronous Counter (Ripple counter)
- Synchronous Counter.

Asynchronous Counter: Asynchronous counters are those counters which do not operate on simultaneous clocking. In asynchronous counter, Only the flip-flop is externally clocked using clock pulse while the clock input for the successive flip-flops will be the output from previous flip-flops.

The figure given below show the circuit of 3 bit asynchronous.



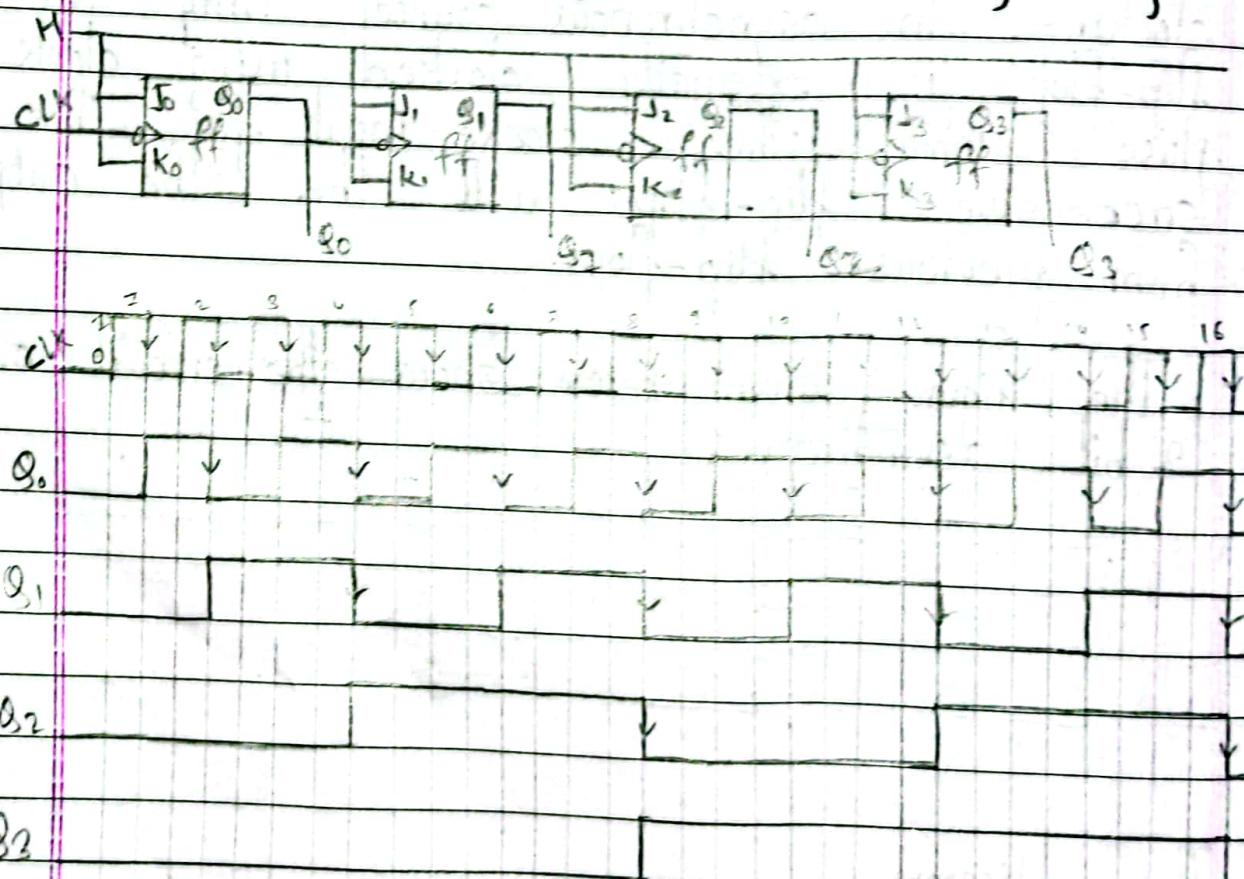
Timing diagram



dk	$Q_2$	$Q_1$	$Q_0$
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

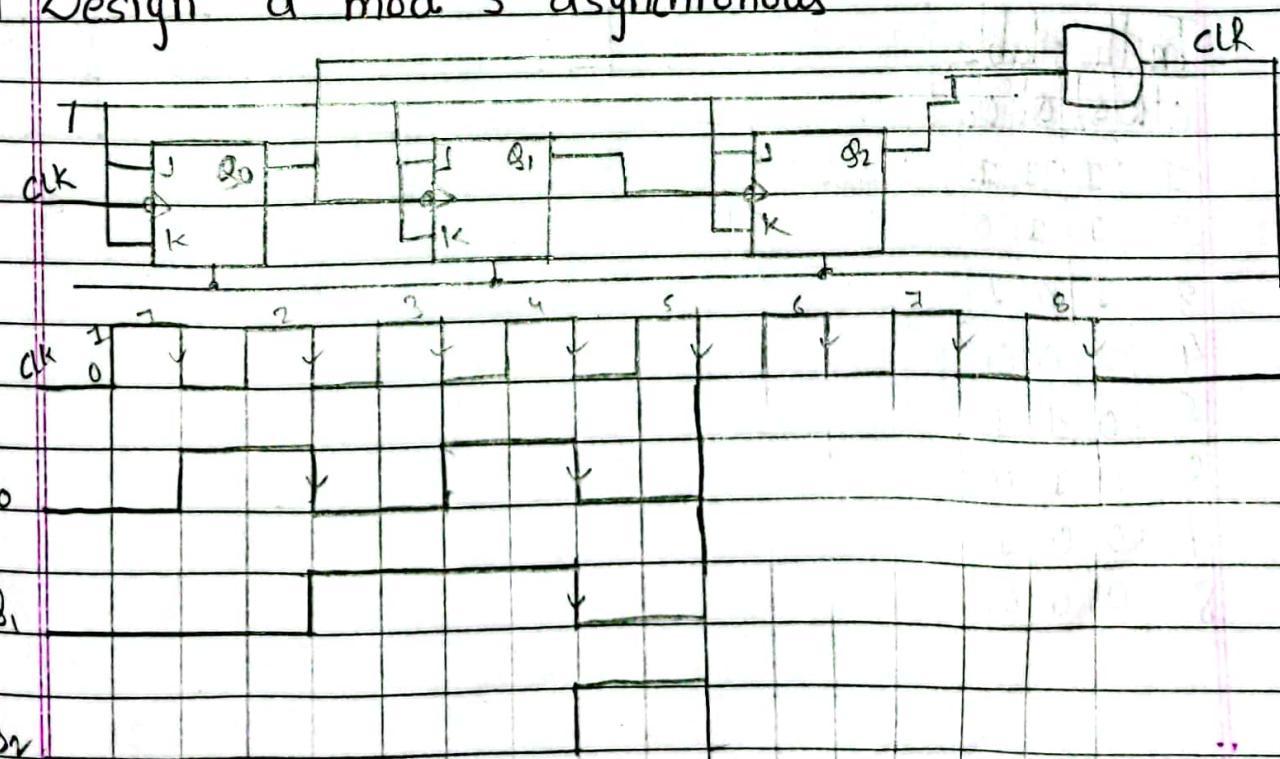
Here,  $Q_0$  toggled for every negative edge of clock signal.  $Q_1$  toggle for every  $Q_0$  that goes from 1 to 0, otherwise  $Q_1$  remained in the previous state. The initial status of j/k of clock signal is  $Q_2 Q_1 Q_0 = 000$ .

\* Design 4 bit asynchronous timing diagram.

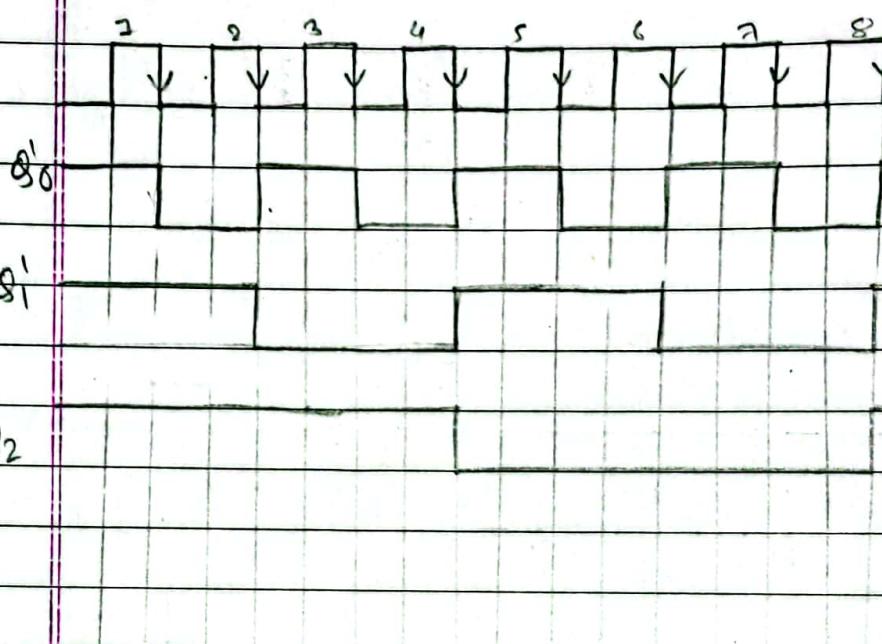
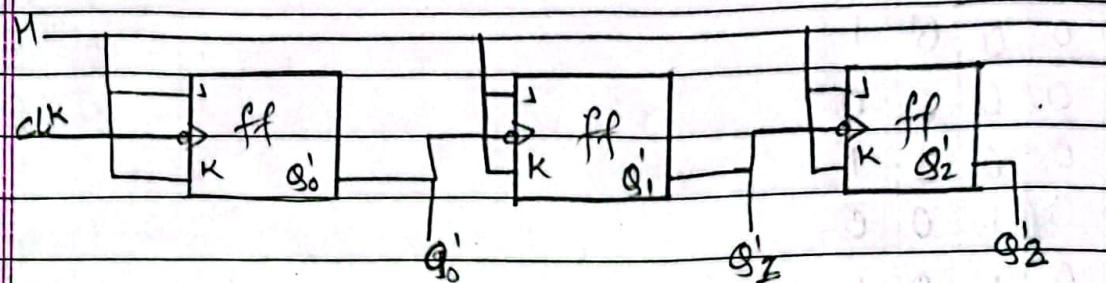


dk	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

H Design a mod 5 asynchronous



① Design a 3 bit asynchronous Down counter



Truth table

clk	$Q'_2$	$Q'_1$	$Q'_0$
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0

Design 3 bit up down counter.

$d=0$	M	$Q_1$	$Q_2$	$y$	$y_1$
$d=1$	0	0	0	0	0
	0	0	1	0	1
	0	1	0	1	0
	0	1	1	1	1
	1	0	0	0	0
	1	0	1	1	0
	1	1	0	0	1
	1	1	1	1	1

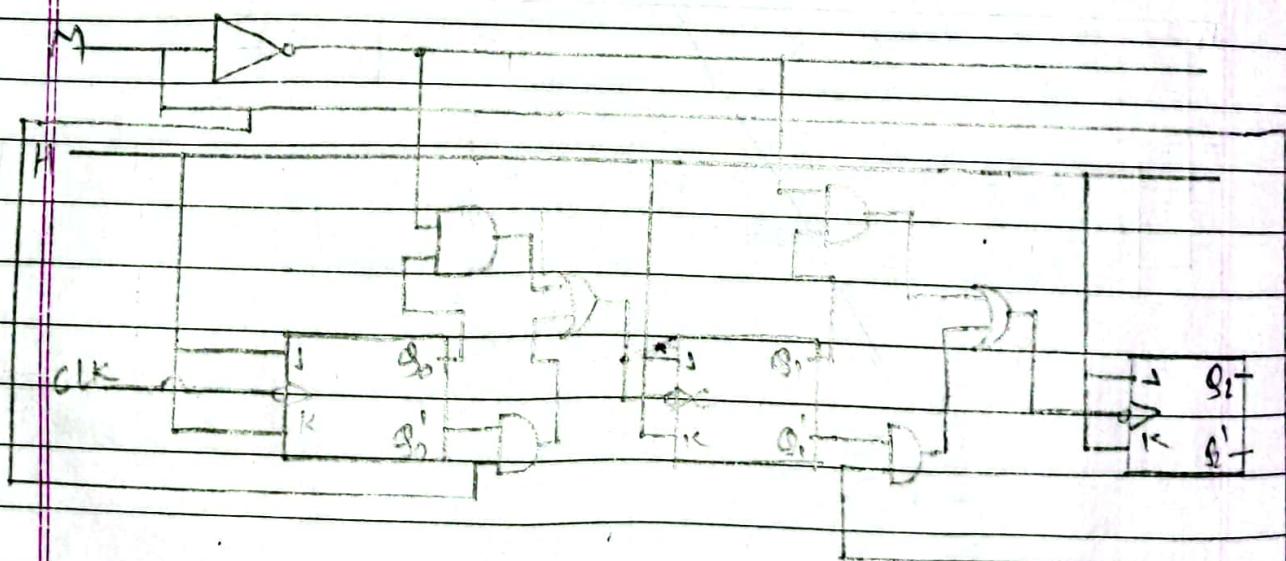
$m=0$  up

$m=1$  down

$m=2$  up

$m=0$  down

$$y = m'q + mq'$$



M	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	1	1	q
9	1	0	0
10	1	0	1
11	1	0	0
12	0	1	1
13	0	1	0
14	0	0	1
15	0	0	0

### = Synchronous Counter

If all the flip flops receive the same clock signal, then counter called Synchronous counter. Hence, the outputs of all flip-flops change affect.

### Requirement of designing of synchronous counter

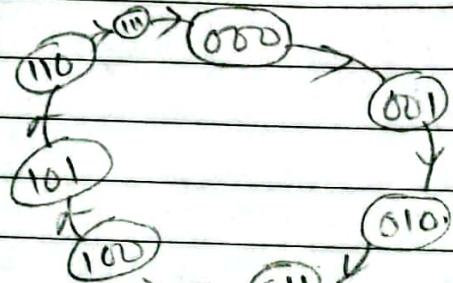
- Determine the number of Flip flops.
- Excitation table of Flip flops.
- State diagram and circuit diagram's excitation table.
- Simplified boolean expression (Kmap)
- Draw the logic diagram.

# Design 3 bit synchronous

## Excitation table of flip flop

Qn	Qn+1	T
0	0	0
0	1	1
1	0	1
1	1	0

- State diagram



Circuit excitation table

Present state			Next state			Output		
$Q_3$	$Q_2$	$Q_1$	$Q_3^*$	$Q_2^*$	$Q_1^*$	$T_3$	$T_2$	$T_1$
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

K-map for  $T_3$

$Q_3$	$Q_2 Q_1$	00	01	11	10
0			(1)		
1			(1)		

$$T_3 = Q_2 Q_1$$

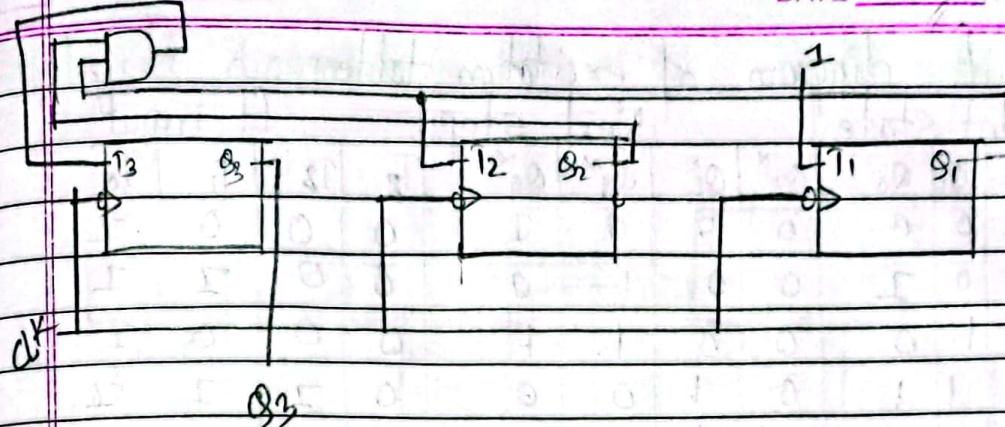
K-map for  $T_2$

$Q_3$	$Q_2 Q_1$	00	01	11	10
0		0	0	1	1
1		1	0	1	0

$$T_2 = Q_1$$

$Q_3$	$Q_2 Q_1$	00	01	11	10
0		0	1	1	1
1		1	1	1	1

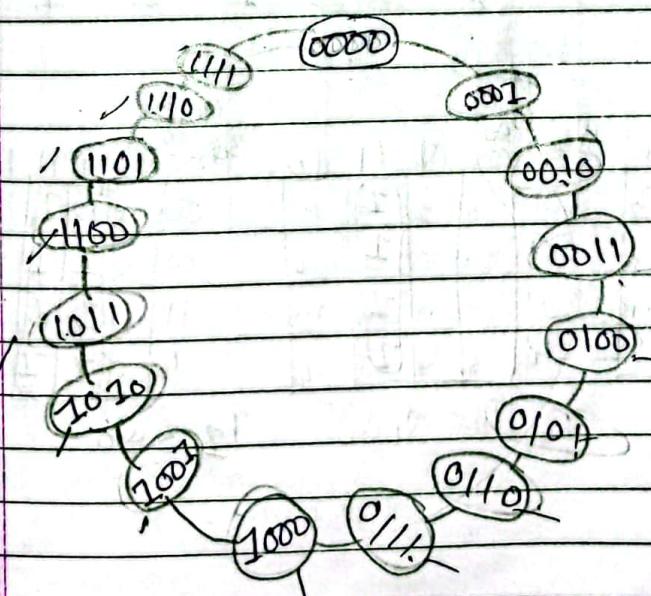
$$T_1 = 1$$



Design 4 bit synchronous  
Excitation table

Q <sub>n</sub>	Q <sub>n+1</sub>	T
0	0	0
0	1	1
1	0	1
1	1	0

state diagram



0	1	1	0
1	1	1	1
1	1	1	1

T<sub>1</sub>=1

circuit diagram of excitation table

Present State				Next step				ff input			
$Q_3$	$Q_2$	$Q_1$	$Q_0$	$Q_3^*$	$Q_2^*$	$Q_1^*$	$Q_0^*$	$T_3$	$T_2$	$T_1$	$T_0$
0	0	0	0	0	0	0	1	0	0	0	1
1	0	0	0	1	0	0	1	0	0	1	1
2	0	0	1	0	0	0	1	1	0	0	1
3	0	0	1	1	0	1	0	0	0	1	1
4	0	1	0	0	1	0	1	0	0	0	1
5	0	1	0	1	0	1	1	0	0	1	1
6	0	1	1	0	0	1	1	0	0	0	1
7	Q	1	1	-1	0	0	0	1	1	1	1
8	1	0	0	0	1	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0	0	0	1
10	1	0	1	0	1	0	1	1	0	0	1
11	1	0	1	1	1	0	0	0	1	1	1
12	1	1	0	0	1	1	0	1	0	0	0
13	1	1	0	1	1	1	0	0	0	1	1
14	1	1	1	0	1	1	1	0	0	0	1
15	1	1	1	1	0	0	0	1	1	1	1

Kmap for  $T_3$

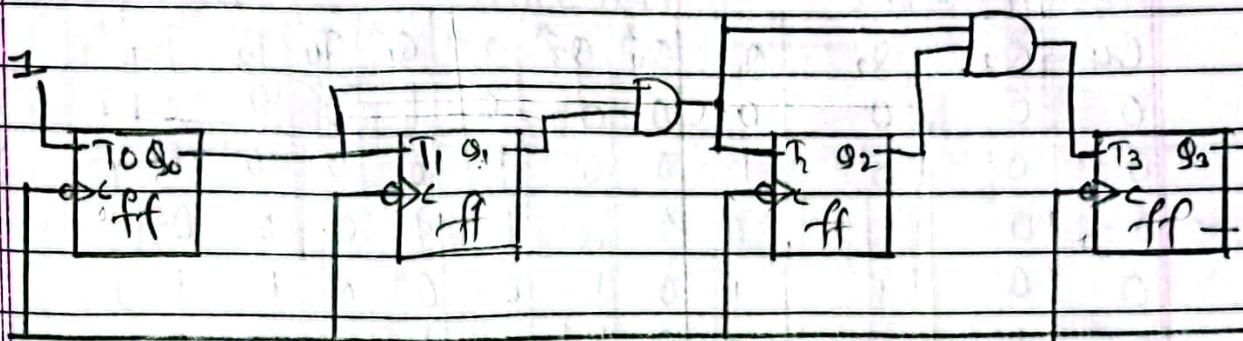
$Q_3 Q_2$		$Q_1 Q_0$		$Q_3 Q_2$		$Q_1 Q_0$		$Q_3 Q_2$		$Q_1 Q_0$	
00	01	11	10	00	01	11	10	00	01	11	10
00	-	3	2	00	0	1	1	00	0	1	1
01	4	5	12	01	4	5	12	01	4	5	12
11	13	14	15	11	12	13	14	11	12	13	14
10	9	10	11	10	8	9	11	10	8	9	11

$$T_3 = Q_2 Q_1 Q_0$$

$$T_2 = Q_1 Q_0 \quad T_1 = Q_0$$

$$T_0 = 1$$

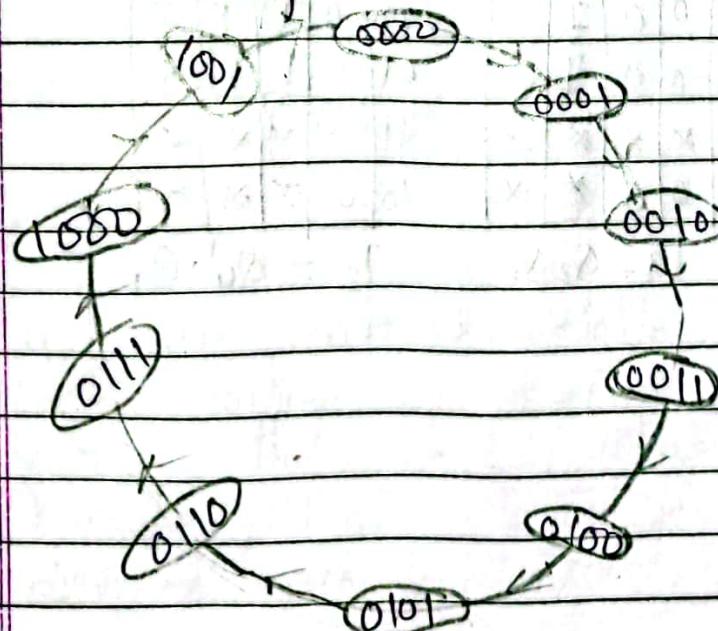
logical diagram.



Design a synchronous decade counter  
Excitation table

$Q$	$Q^*$	$T$
0	0	0
0	1	1
1	0	1
1	1	0

State diagram



# Excitation table of circuit diagram

Present state				Next state				ff input			
$Q_4$	$Q_3$	$Q_2$	$Q_1$	$Q_4^*$	$Q_3^*$	$Q_2^*$	$Q_1^*$	$T_u$	$T_2$	$T_2$	$T_1$
0	0	0	0	0	0	0	0	1	0	0	0
0	0	0	1	0	0	0	1	0	0	0	1
0	0	1	0	0	0	0	1	1	0	0	0
0	0	1	1	0	1	0	0	0	0	1	1
0	1	0	0	0	1	0	1	0	0	0	0
0	1	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	0	1	0	0	0
1	0	0	1	0	0	0	0	0	1	0	0

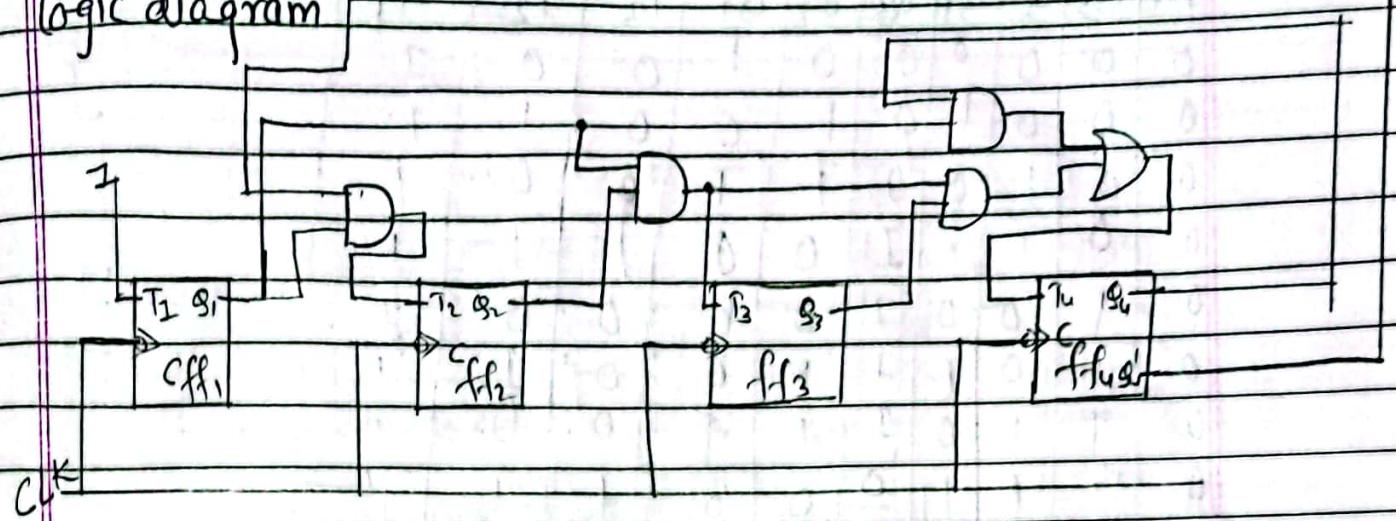
K-map for  $T_4$

$Q_4$	$Q_3$	$Q_2$	$Q_1$	$T_4$	$Q_4$	$Q_3$	$Q_2$	$Q_1$	$T_3$	$Q_4$	$Q_3$	$Q_2$	$Q_1$	$T_2$
0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
0	1	0	0	1	0	1	0	0	1	0	1	1	1	0
1	1	x	x	x	1	x	x	x	x	1	x	x	x	x
1	0	1	x	x	1	0	0	x	x	1	0	x	x	x

$T_4 = Q_4 Q_1 + Q_3 Q_2 Q_1$ ,       $T_3 = Q_2 Q_1$ ,       $T_2 = Q_4' \cdot Q_1$

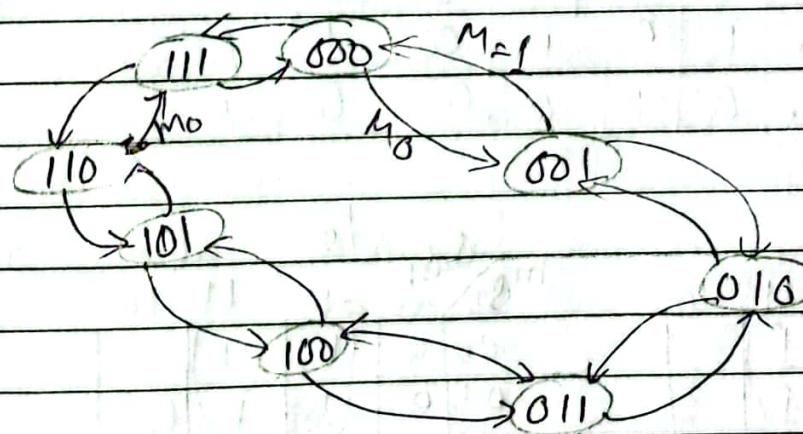
	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

logic diagram



## # Design up down synchronous counter

When  $M=0$  then counter will perform up counting &  $M=1$  then counter will perform down counting.



In circuit excitation table, represent state of the counting sequence and the next state after the clock pulse is applied and input  $T$  of the flip flop. The table is designed according to the required counting sequence.

M	$Q_3$	$Q_2$	$Q_1$	$Q_3^*$	$Q_2^*$	$Q_1^*$	$T_3$	$T_2$	$T_1$
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	1	1	0	0	1
0	1	1	1	0	0	0	1	1	1
1	0	0	0	1	1	1	1	2	1
1	0	0	1	0	0	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	0	1
1	1	0	0	0	1	1	1	1	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	1	0	1	0	1	1
1	1	1	1	0	1	0	0	0	1

Kmap

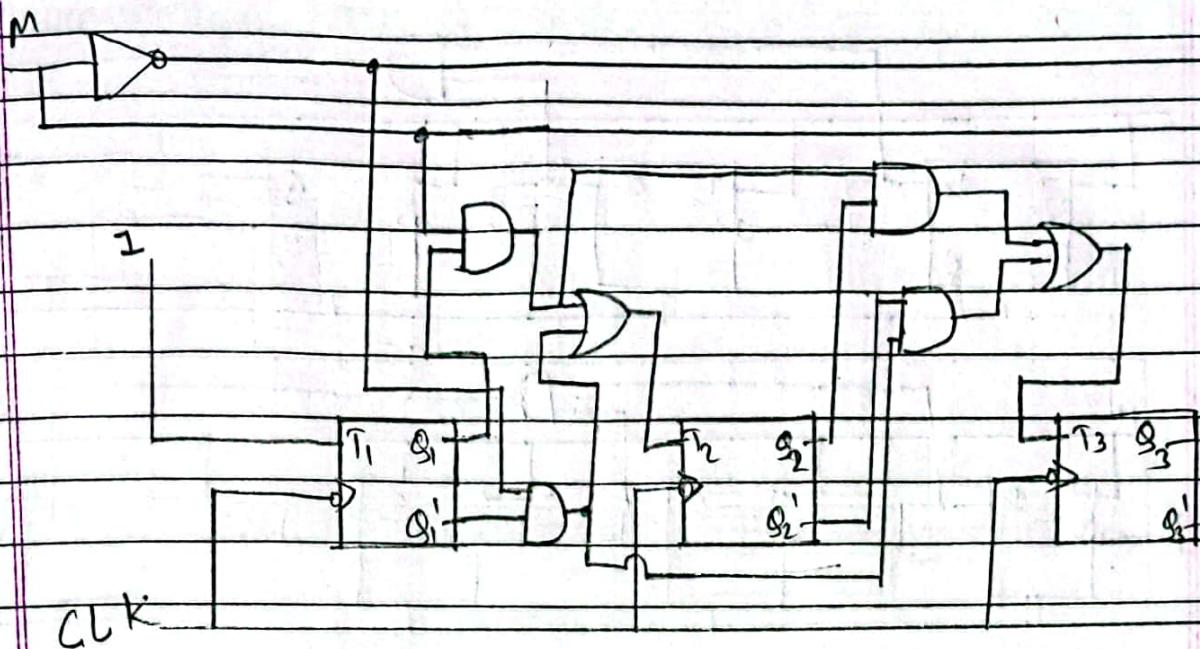
				$T_3$					$T_2$
$m_{Q_3}$	$Q_2 Q_1$	00	01	11	10	00	01	11	10
00				(1)		00	01	(1)	0
01			(1)			01	0	(1)	0
11	A					11	1	0	0
10	(1)					10	1	0	1

$$T_3 = M'Q_2Q_1 + MQ_2'Q_1'$$

$$T_2 = M'(Q_1 + MQ_1')$$

				$T_1$	
$m_{Q_3}$	$Q_2 Q_1$	00	01	11	10
00		1	1	1	2
01		1	1	1	2
11		1	1	1	1
10		1	2	1	2

$$T_1 = 1$$

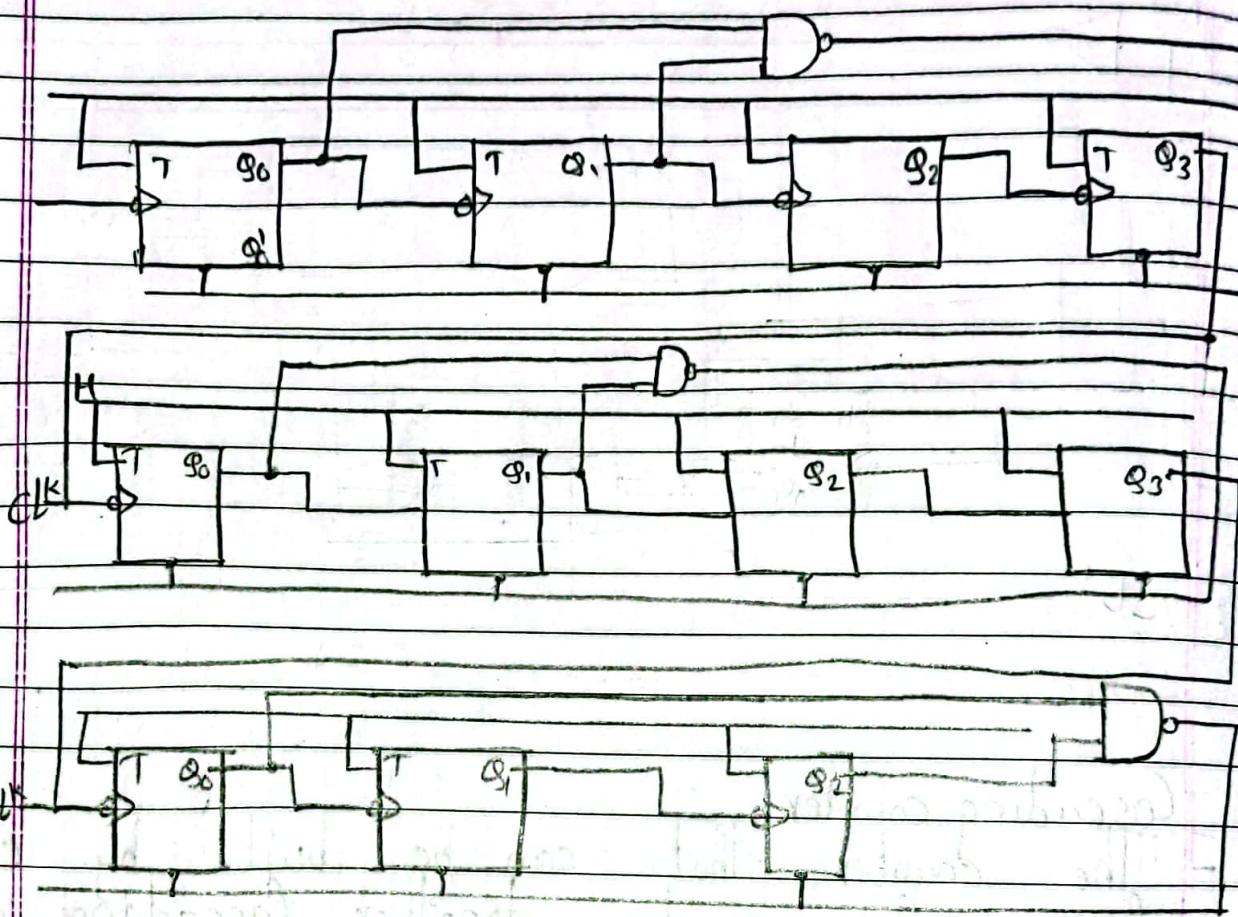


### Cascading counter

- The counter that can be built by combining of smaller counter together. Cascading counter will increment only when the counter below it is at its terminal count and being incremented.

### Mod 720

In mod 720, we required 11 flip flop. In first 4 flip flop count up to 12 and another count up to 12. After coming both counter output we get : 144 in result for that purpose clock pulse provided in asynchronous way. In the position of Q<sub>0</sub> and Q<sub>1</sub> of two flip flop CLR or glitch is applied.



## # Digital clock:

A digital clock is a type of clock that displays the time digitally as opposed to an analog clock, where the time is indicated by the position of rotating hands. With the perfecting of multivibrator chips electrical circuits could be built that could accurately keep time under a wide range of conditions. The time base had switched from mechanical to electrical, the time display had to follow suit. Display device, called 7 segment displays were designed to allow the time to be shown.

60Hz AC  
60 min

waveshaping  
circuit

CTR DIV 10

CTR DIV 10

242

ff Hour

C CCO

CTR DIV 10

BCE/7seg

BCE/7seg

BCE/7seg

BCE/7seg

BCE/2  
segm

I

I

I

I

I

(0-1)

(0-9)

(0-5)

(0-9)

(0-5)

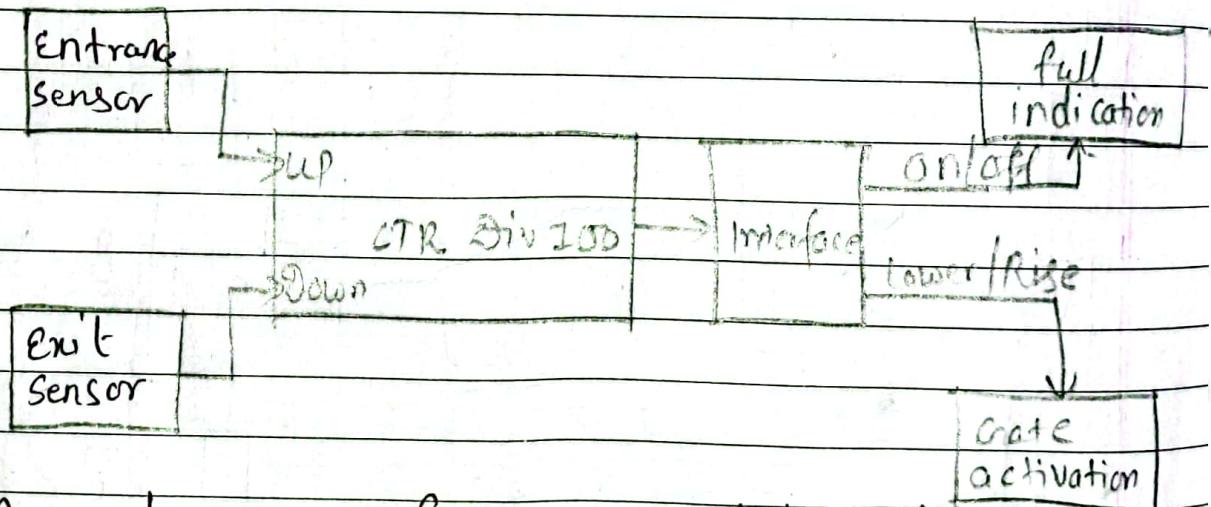
Hours

minutes

second

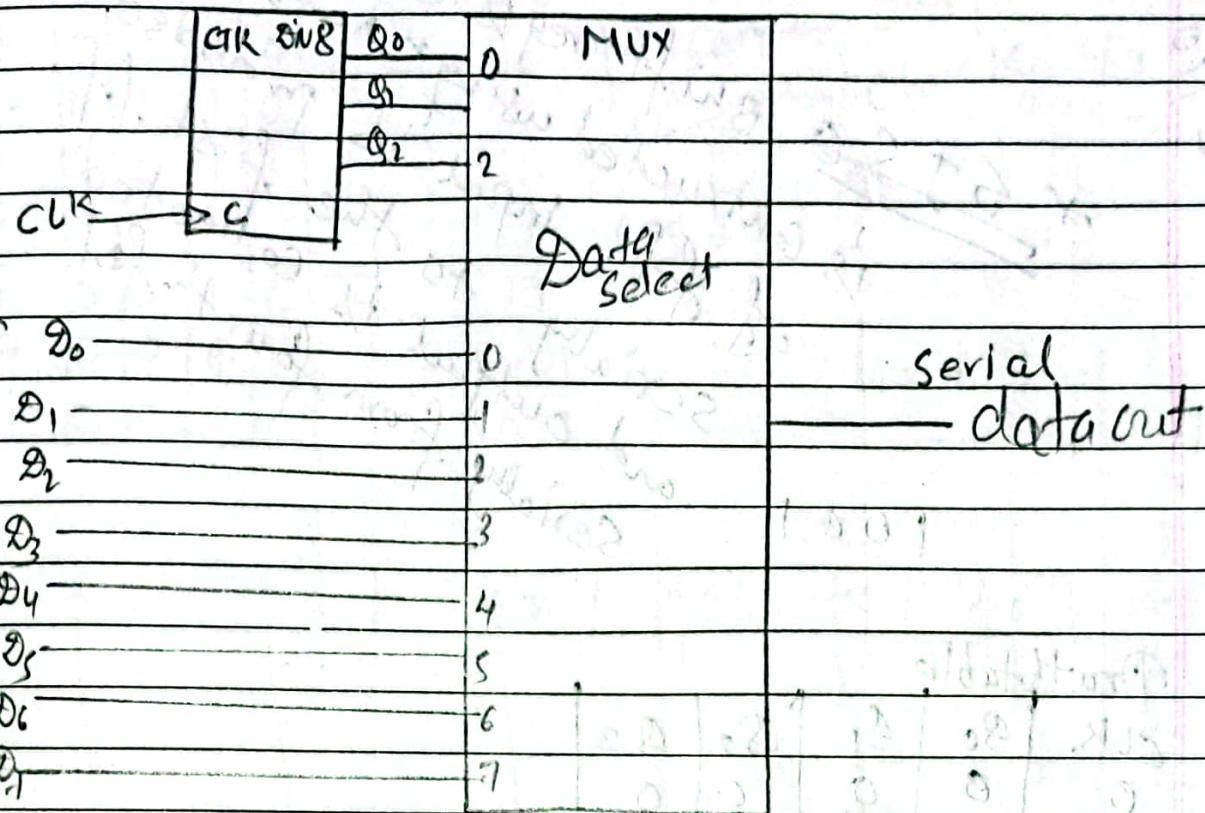
Initially, a 60 Hz sinusoidal ac voltage is converted to a 60 Hz pulse waveform and divided down to a 1 Hz pulse. Waveform formed by a divide - by - 60 counter followed by a divide by 10 counter. These counter from 0 to 59 and recycle to 0. Synchronous decade counter are used in this particular implementation.

## ii Automobile Parking Control :



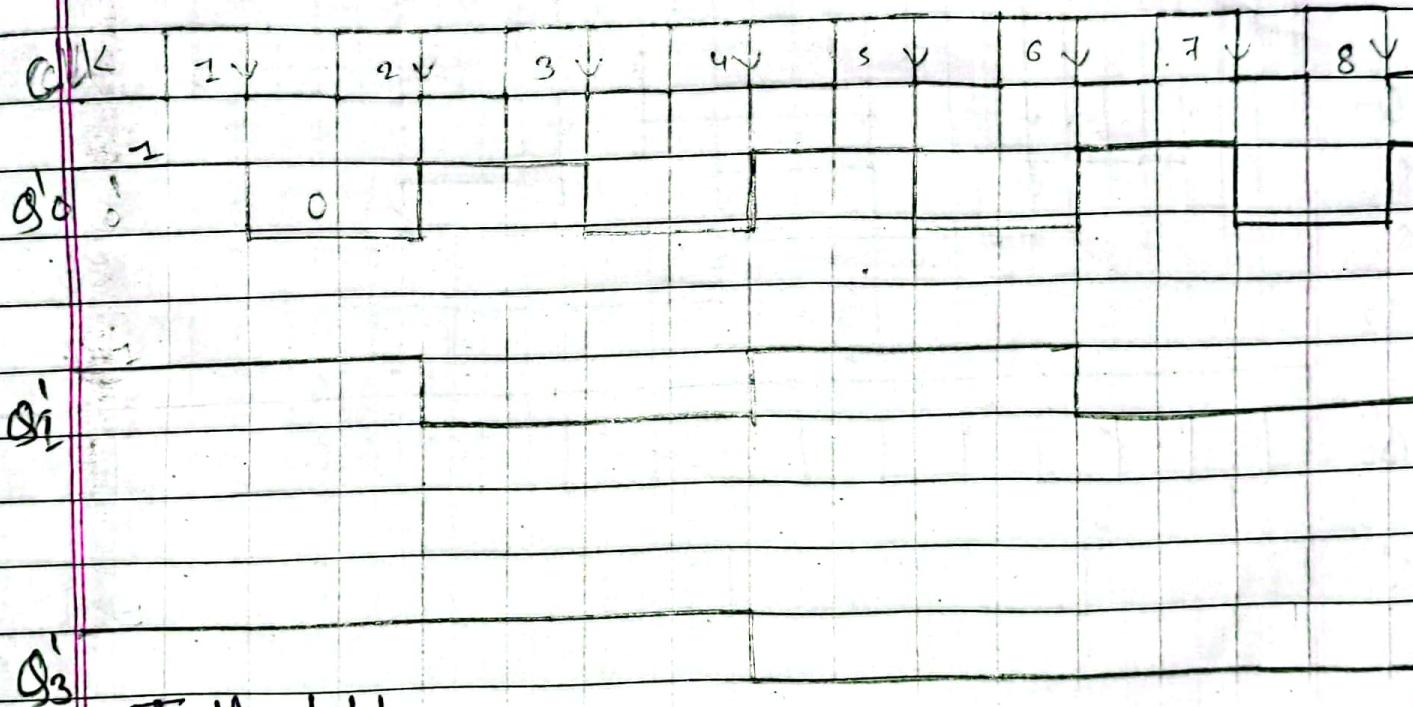
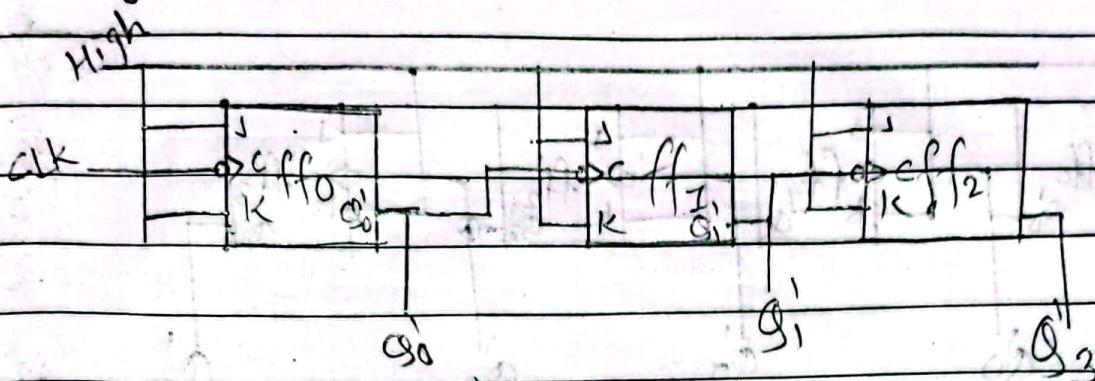
As shown in figure given below the Up/Down counter connected to sensors update the count sequence and hence shows that if the parking is full or more parking space is available with the help of interfacing unit.

## ii) Parallel to Serial Data Conversion:



The parallel data bit on the multiplexer inputs are converted to serial data bit on the single transmission line. A group of bit appearing simultaneously on parallel line is called parallel data. A group of bit appearing on a single line in a time sequence is called serial data.

Design a 3 bit asynchronous Down Counter

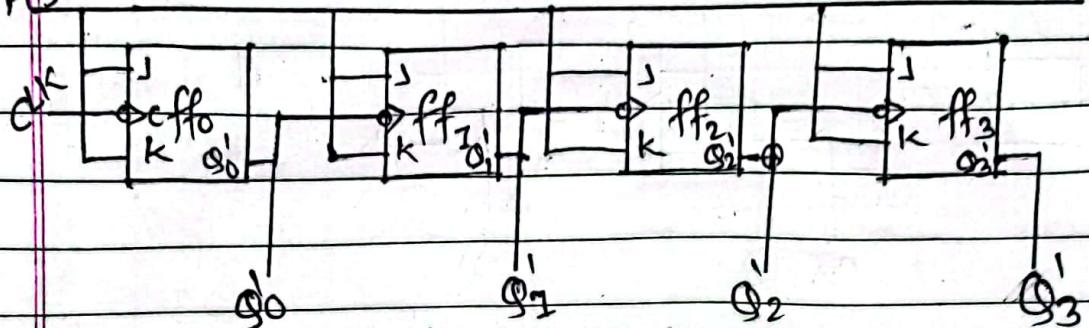


Truth table

clk	$Q_2'$	$Q_1'$	$Q_0'$
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0

# Design 4 bit down asynchronous

High

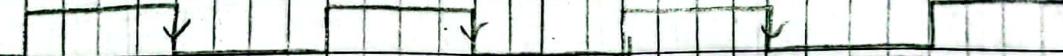


CLK 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

$Q_0$



$Q_1$



$Q_2$



$Q_3$



$Q'_0$



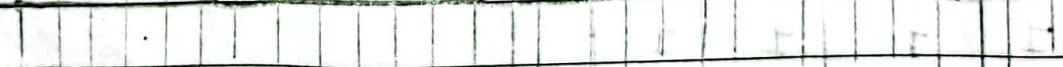
$Q'_1$



$Q'_2$

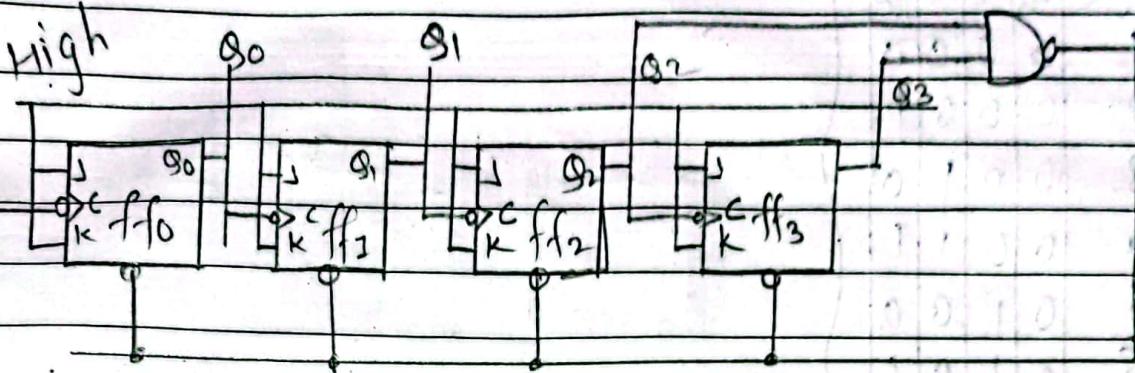


$Q'_3$



0	0	5	6
1	3	7	8
2	4	9	10
3	5	10	11

## Design modulus 12



clk <sup>2</sup> 0 1 2 3 4 5 6 7 8 9 10 11 12

Q<sub>0</sub> 1 1 0 1 1 0 1 1 0 1 1 0 1

Q<sub>1</sub> 1 0 1 0 1 0 1 0 1 0 1 0 1

Q<sub>2</sub> 0 1 1 0 1 1 0 1 1 0 1 1 0

Q<sub>3</sub> 0 1 1 0 1 1 0 1 1 0 1 1 0

Truth table

clk

1

2

3

4

5

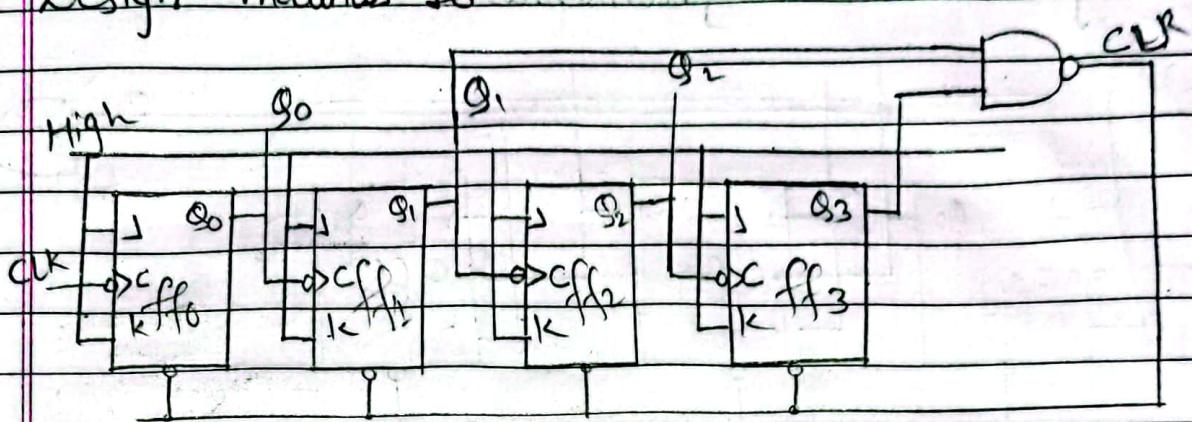
6

7

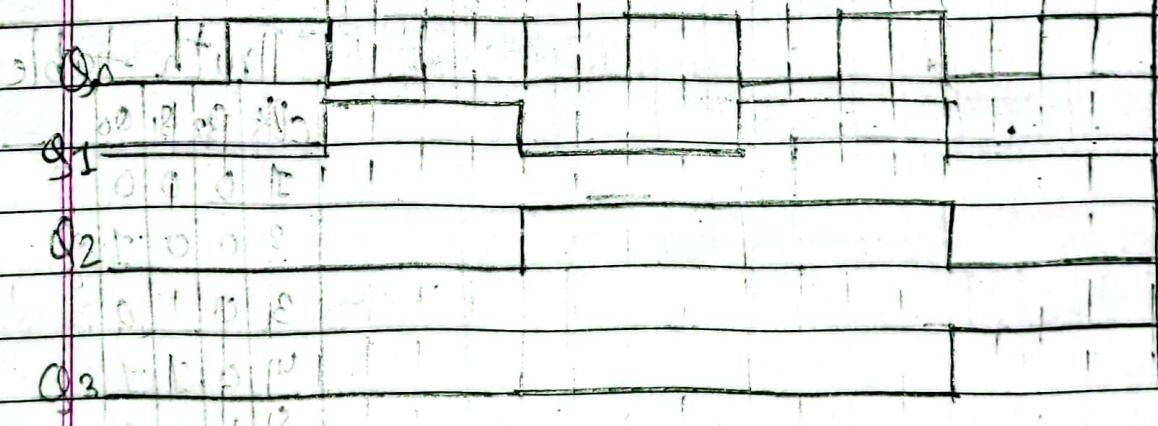
8

9

## Design modulus 10



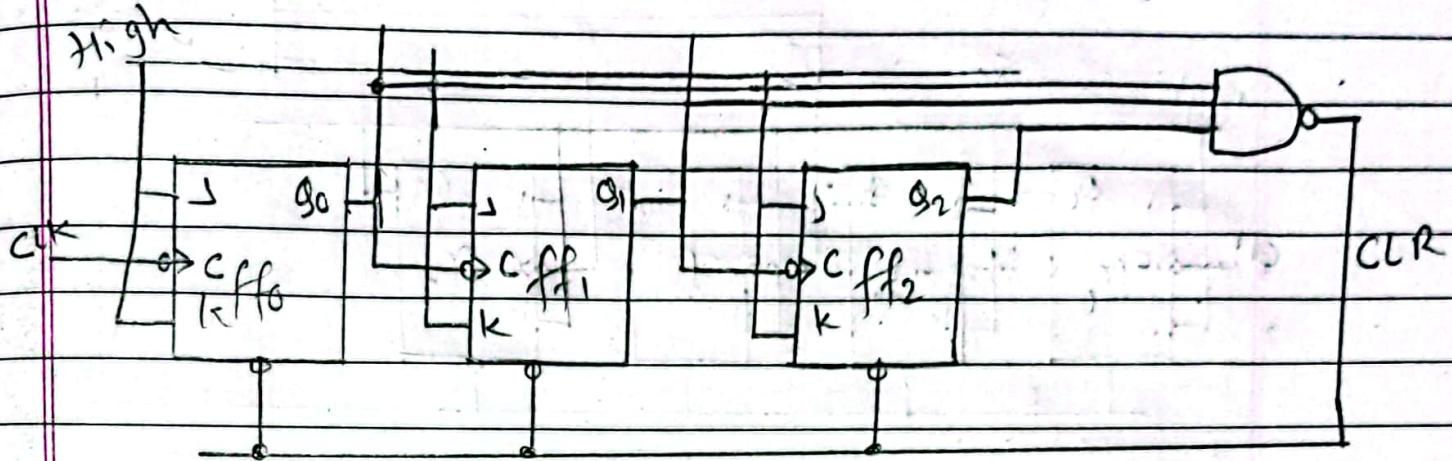
clk	0	1	2	3	4	5	6	7	8	9	10
-----	---	---	---	---	---	---	---	---	---	---	----



clk	Q3	Q2	Q1	Q0
-----	----	----	----	----

0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	0	1

Design a mod 7 asynchronous.

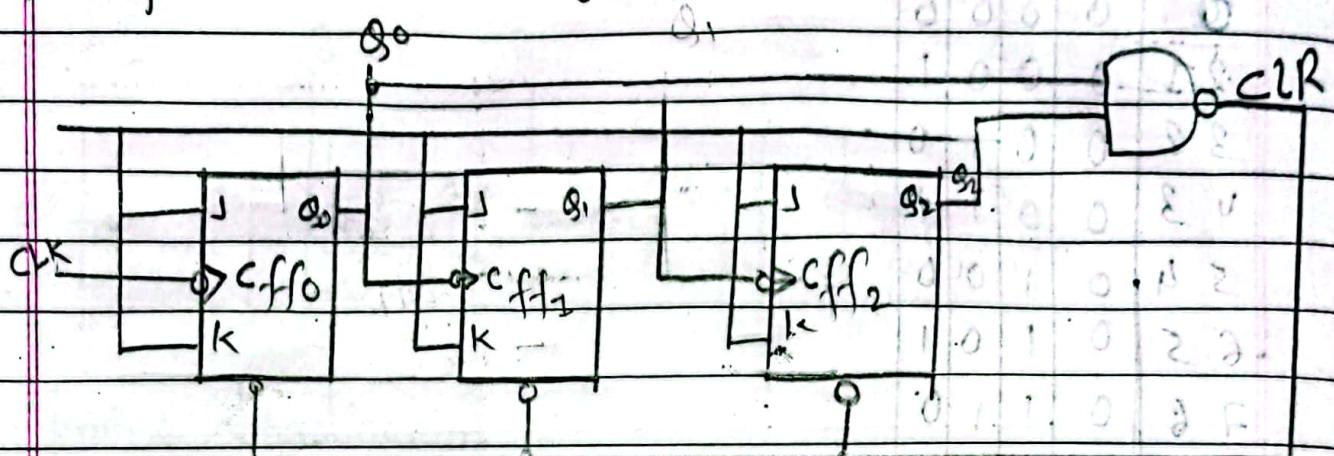


clk 0 1 2 3 4 5 6 7 8

Truth table

clk	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8			

(\*) Design a mod 5 asynchronous



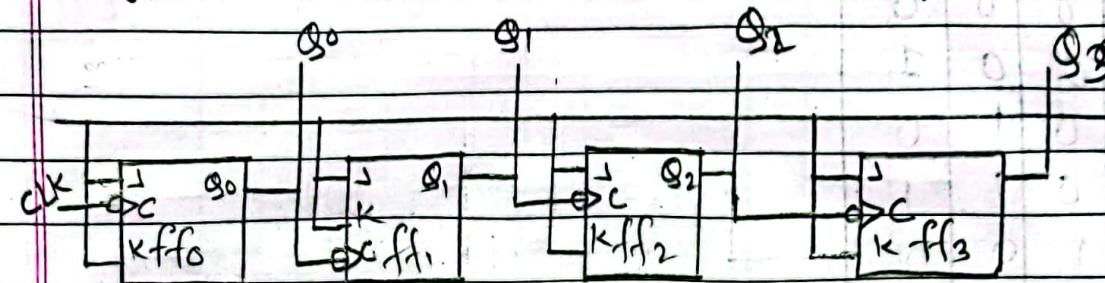
CLK	0	1	2	3	4	5	6	7	8	0	0	0	1	0	0
Q0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Q1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
----	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Q2	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
----	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

CLK	Q2	Q1	Q0
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6			
7			
8			

## Design 4 bit asynchronous timing diagram



Timing diagram

