2EI4 – Electronic Devices and Circuits I
Project 2 Research – Voltage Controlled Switches

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Due: February 16th, 2025

Properties of an Ideal Switch

1. $V_{on} = 0$ and $V_{switch} = 0$

In the ON state of an ideal switch, there is no resistance. This means the switch creates a completely unobstructed path for current flow. As a result, it has no impact on the current, allowing it to pass through as if the switch were a perfect wire. Additionally, the switch acts as an ideal conductor, meaning it does not cause any energy loss in the circuit. Indication of this is evident in the fact that there is no voltage drop across the switch, ensuring that all supplied voltage is available to the connected load. Power dissipation is given by $P = VI$ or $P = I^2R$. Since both the resistance, R_{on}, and voltage drop, V_{drop}, are zero, the power dissipated by the switch is also zero. This makes an ideal switch 100% efficient, meaning no electrical energy is lost as heat, and all power is effectively transferred to the intended circuit components.

2. $R_{off} = \infty$ and $I_{off} = 0$

When an ideal switch is OFF, the resistance increases to infinity. This occurs because an ideal switch is assumed to have perfect insulating properties, meaning there is no conductive path between its terminals. As a result, it acts like a completely open circuit. This ensures that no electrical energy can pass through. Additionally, no current flows through the switch in the OFF state. Since current flow requires a complete circuit and the switch creates a break in the path, the current remains at 0, $I_{off} = 0$. This characteristic is critical for fully isolating different sections of a circuit, preventing unintended current leakage.

3. V_1 and V_2 value is unlimited

There are two terminals in a switch, V_1 and V_2, which represent the voltages at each end of the switch. In an ideal switch, these voltage values can be infinitely large, either positively or negatively. This means the switch has no maximum voltage limitation. When the switch is ON, it acts like a perfect conductor, meaning there is no resistance, and no voltage drop across the terminals ($V_{switch} = 0$). Regardless of the values of V_1 and V_2, the switch ensures that the voltage at both terminals remains equivalent, essentially shorting them together without introducing any losses or resistance. When the switch is OFF, it behaves as a perfect insulator, meaning no current can flow between V_1 and V_2. An ideal switch can withstand any voltage difference between its terminals without failure. This means it can isolate parts of a circuit perfectly, regardless of the applied voltage.

4. Bidirectional

In an ideal switch, current can flow both forward and backward through the terminals. This means the switch is bidirectional and does not impose any restrictions on the direction of current flow. When the switch is ON, it acts as a perfect conductor ($R = 0$), ensuring current flows freely between terminals regardless of directions. There is no voltage drop across the switch ($V_{switch} = 0$), allowing the full voltage to reach the load without loss. When the switch is OFF, it acts as a perfect insulator ($R = \infty$), ensuring no current flows in either direction. This creates complete isolation between the two terminals, regardless of direction and voltage applied.

Non-Idealities of a Real Switch

1. Value of R_{on} measures non-ideality in switch when on

In an ideal switch, R_{on} would be 0. This means that there is no voltage drop and no power dissipation across the switch. However, it a non-ideal switch R_{on} is not 0. When the switch is conduction, it will have a small, finite value that introduces a voltage drop and power loss. The higher the value of R_{on} is, the larger the voltage drop across the switch and the power dissipated by the switch. Both factors result in a reduced efficiency in applications. To measure the value of R_{on}, a multimeter can be used. To do so, the switch must be on, and the multimeter should be connected to both terminals of the switch. Ideally, the multimeter should read a low resistance across the switch.

2. Value of I_{off} measures non-ideality in switch when off

For an ideal switch, when it is off, the resistance is infinite ($R_{on} = \infty$). This means that no current leaks ($I_{off} = 0$). However, in a real switch, there will be some small leakage current even if the switch is off. This is because the switch is not a perfect insulator. This causes a loss of power when the switch is off. To measure the leakage current (I_{off}) connect an ammeter in series with the switch and apply a known DC voltage. Then, turn the switch off and measure the current reading. It will typically be small ($\mu A - nA$).

3. $V_{min} < V_1$ and $V_2 < V_{max}$

An ideal switch can handle any voltage at its terminals. However, non-ideal switches have maximum voltage ratings. Surpassing these values can lead to them breaking down. As well, they have minimum voltage ratings. Going below this value can make operating the switch unreliable. Although V_{max} and V_{min} can be calculated, they should be listed in the component's datasheet. V_{max} values can be found in the datasheet under absolute maximum ratings or electrical characteristics. Although, V_{min} values might not be explicitly listed in the datasheet, they can be inferred from the threshold voltage value.

4. Same value of R_{on} for $V_1 < V_2$ and $V_1 > V_2$

An ideal switch is bidirectional, meaning R_{on} is constant regardless of current direction. However, for a real switch the R_{on} varies based on the direction of current flow. This occurs due to the internal structure of the switch. To see the magnitude of R_{on}based on direction, measure R_{on} in both directions (v1>V2 and V1<V2). This can be done by connecting a current source with known value to the switch, then measuring the voltage across the switch using a voltmeter. Through Ohm's law $\left(R_{on} = \frac{V_{switch}}{I}\right)$, the value of R_{on} can be calculated for.

References

[1] A. S. Sedra, K. C. Smith, T. C. Carusone, and V. Gaudet, Microelectronic circuits, 8th ed. New York, NY: Oxford University Press, 2019.

[2] O. A. Ahmed, "Power semiconductor devices," University of Technology, https://odayahmeduot.wordpress.com/wp-content/uploads/2015/11/lecture-02.pdf (accessed Feb. 15, 2025).

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Test Plan

Switch 1:

Parameter	Values
$V_{control}$	0-5V square wave
$V_{\sup ply}$	5V
V_1	5V

Table 1: Parameters and values of voltage sources

Measured and Calculated Values:

Measured Values	Calculated Values
V_{input}	Voltage drop across the switch $V_{drop} = V_{input} - V_{output}$
V_{output}	Resistance of the switch $R_{switch} = \frac{V_{drop}}{I}$
	Leakage current $I_{leak} = \frac{V_{out}}{R}$

Table 2: Values that will be measured and calculated for the test plan

To test the switch 1 circuit, the values of $V_{\sup ply}$, $V_{control}$ and $V_1$are set to those listed in *Table 1*. These values will be used to help test the non-idealities. The first non-ideality being tested is that when the switch is closed (ON state) and $V_{control} = 0V$, there should be a voltage drop across the switch. This occurs because a real switch has a resistance, which can be measured. V_{drop}will be found by measuring the input and output voltages of the switch and subtracting them to find the drop across the switch ($V_{drop} = V_{input} - V_{output}$). To measure the resistance across the switch, Ohm's Law will be used (R$R_{switch} = \frac{V_{drop}}{I}$). The next non-ideality being tested is that when the switch is open (OFF state) and $V_{control} = 5V$, there should be some current leakage. This occurs because real switches do not have infinite resistance. To measure this, the output voltage of the switch will be measured and divided by the switch's resistance to calculate the current through the switch ($I_{leak} = \frac{V_{out}}{R}$).

Switch 2:

Parameter	Values
$V_{control}$	0-5V square wave
$V_{\sup ply}$	5V
	5V

Table 3: Parameters and values of voltage sources

Measured and Calculated Values:

Measured Values	Calculated Values
V_a	Voltage drop across the switch $$V_{drop} = V_a - V_b$$
V_b	Resistance of the switch $$R_{switch} = \frac{V_{drop}}{I}$$
	Leakage current $$I_{leak} = \frac{V_{out}}{R}$$

Table 4: Values that will be measured and calculated for the test plan

To test the switch 2 circuit, the values of $V_{\sup ply}$, $V_{control}$ and V_1 are set to those listed in *Table 3*. These values will be used to help test the non-idealities. The first non-ideality being tested is that when the switch is closed (ON state) and $V_{control} = 0V$, there should be a voltage drop across the switch. This occurs because a real switch has a resistance, which can be measured. V_{drop} will be found by measuring the voltages at nodes V_a and V_b and subtracting them to find the drop across the switch ($V_{drop} = V_a - V_b$. To measure the resistance across the switch, Ohm's Law will be used ($R_{switch} = \frac{V_{drop}}{I}$). The next non-ideality being tested is that when the switch is open (OFF state) and $V_{control} = 5V$, there should be some current leakage. This occurs because real switches do not have infinite resistance. To measure this, the output voltage of the switch will be measured and divided by the switch's resistance to calculate the current through the switch ($I_{leak} = \frac{V_{out}}{R}$).

Switch 1:

Circuit Schematic

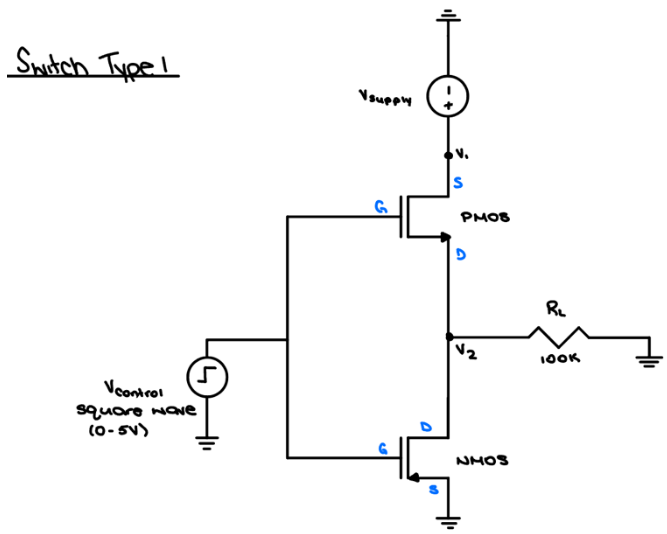

Figure 1: Hand Drawn Circuit Schematic for Switch 1

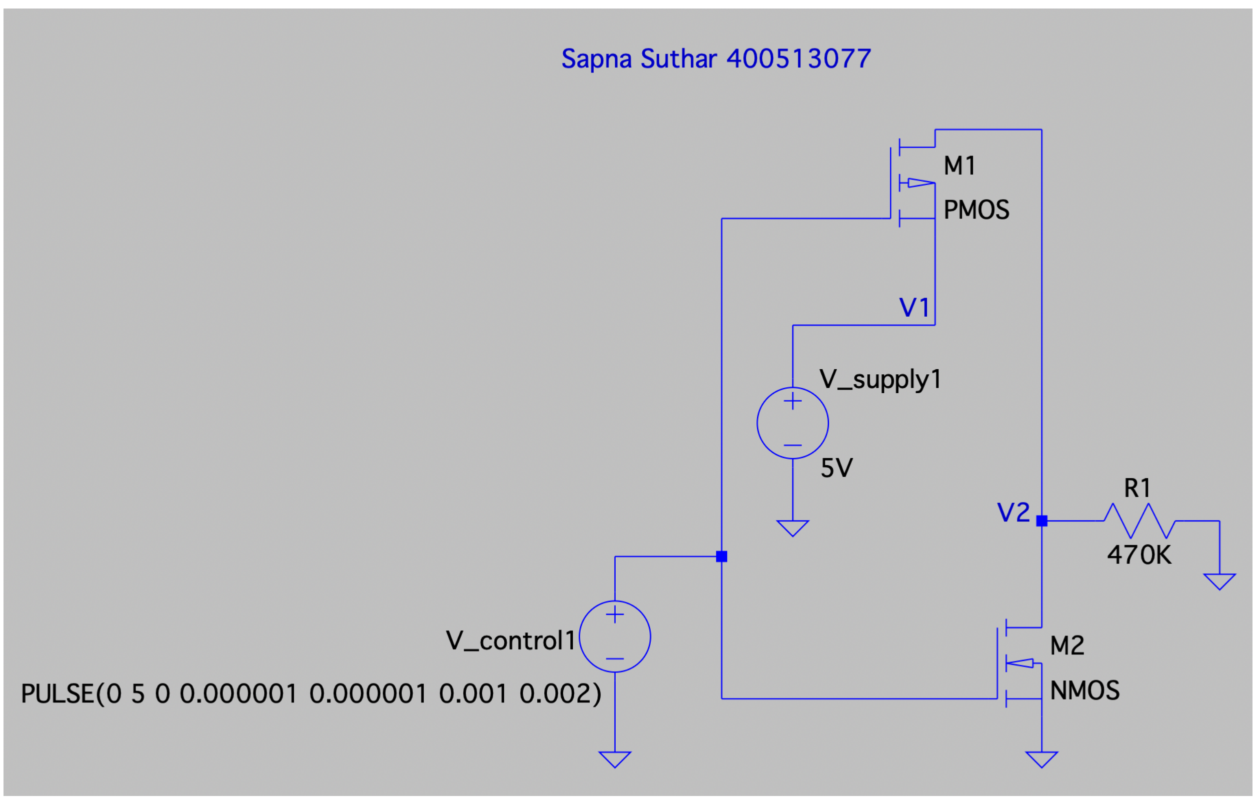

Figure 2: LTSpice Circuit Schematic for Switch 1

Measurements Based on Test Plan

LTSpice Measurements

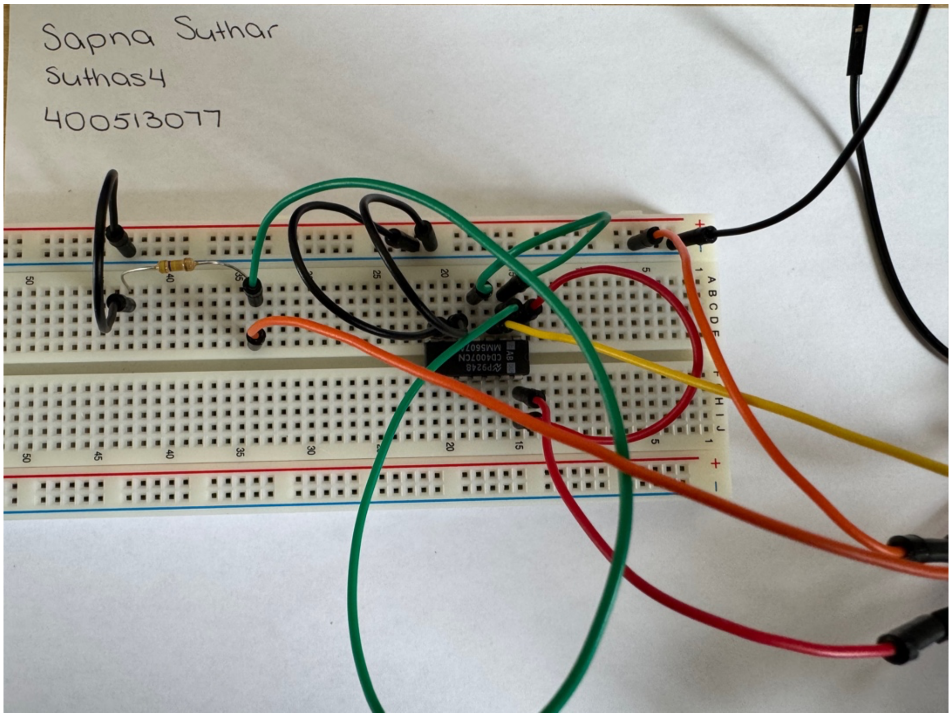

Figure 3: Built Switch 1 Circuit

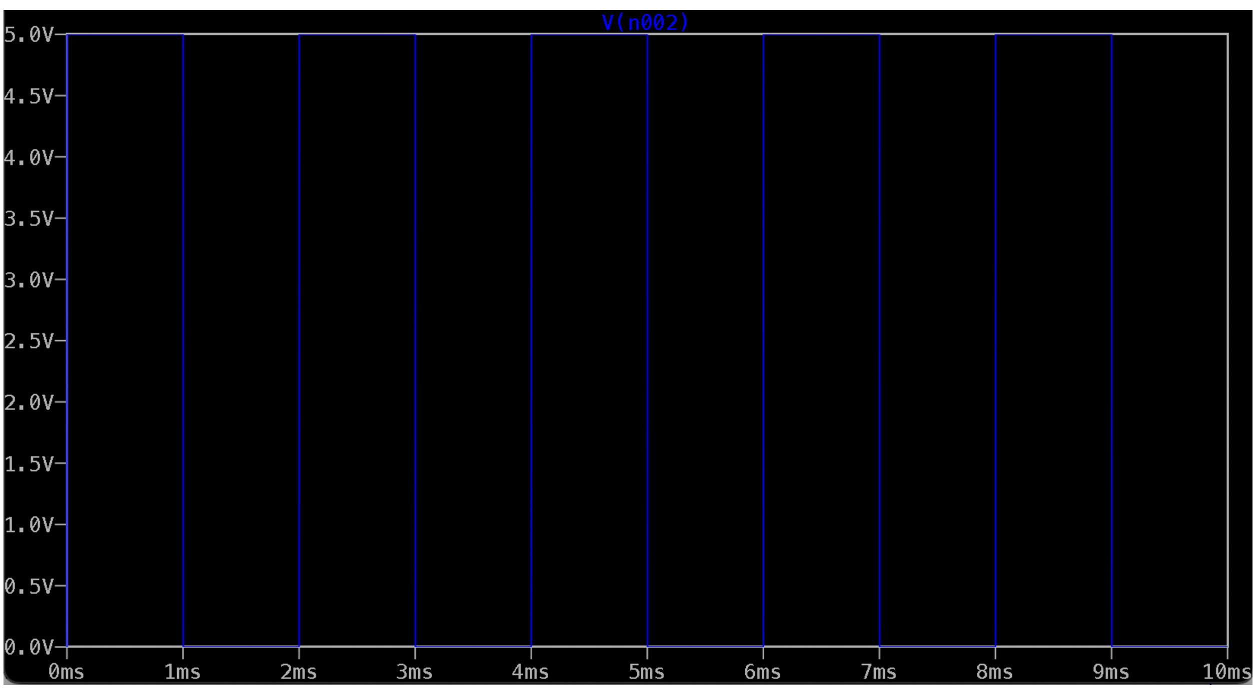

Figure 4: LTSpice Waveform of V_1 ($V_{\sup ply}$)

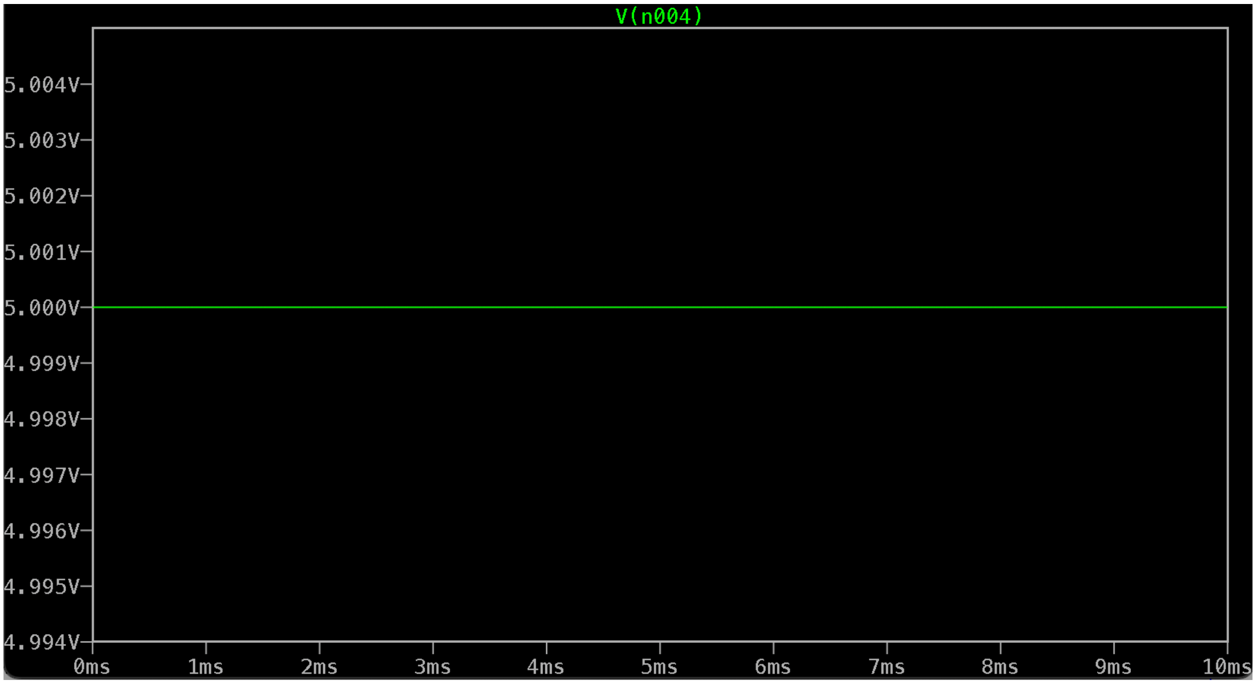

Figure 5: LTSpice Voltage Waveform of $V_{control}$

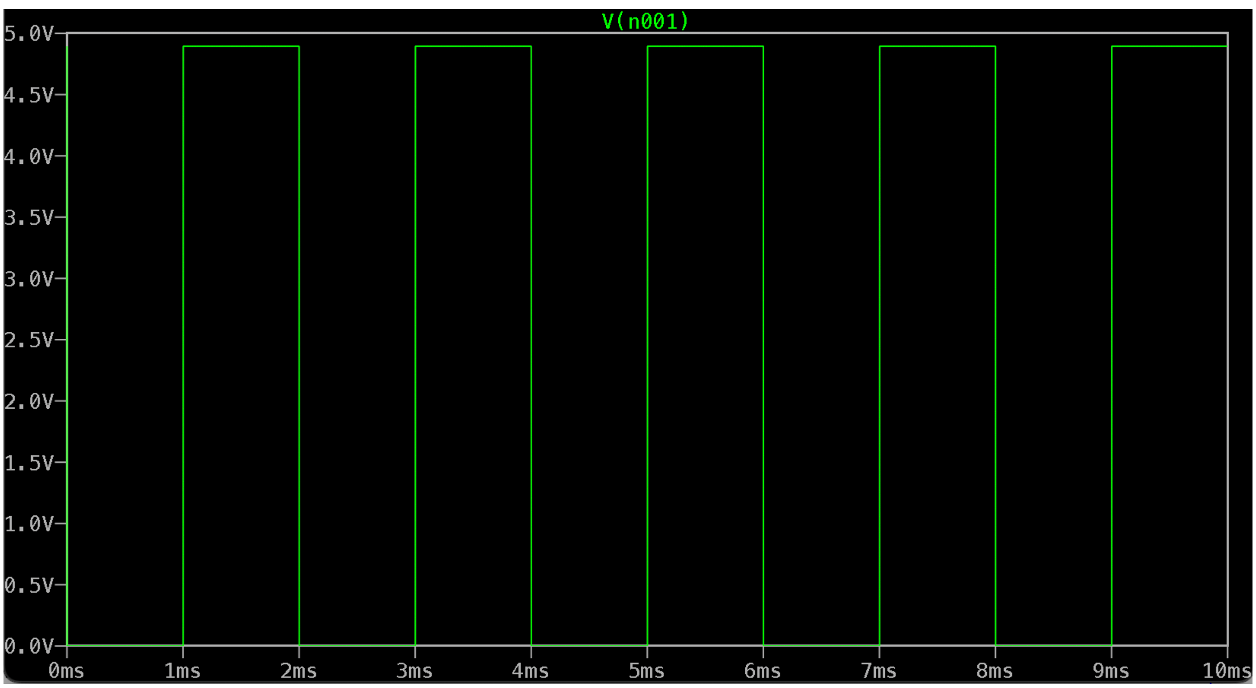

Figure 6: LTSpice Voltage Waveform at Node V2

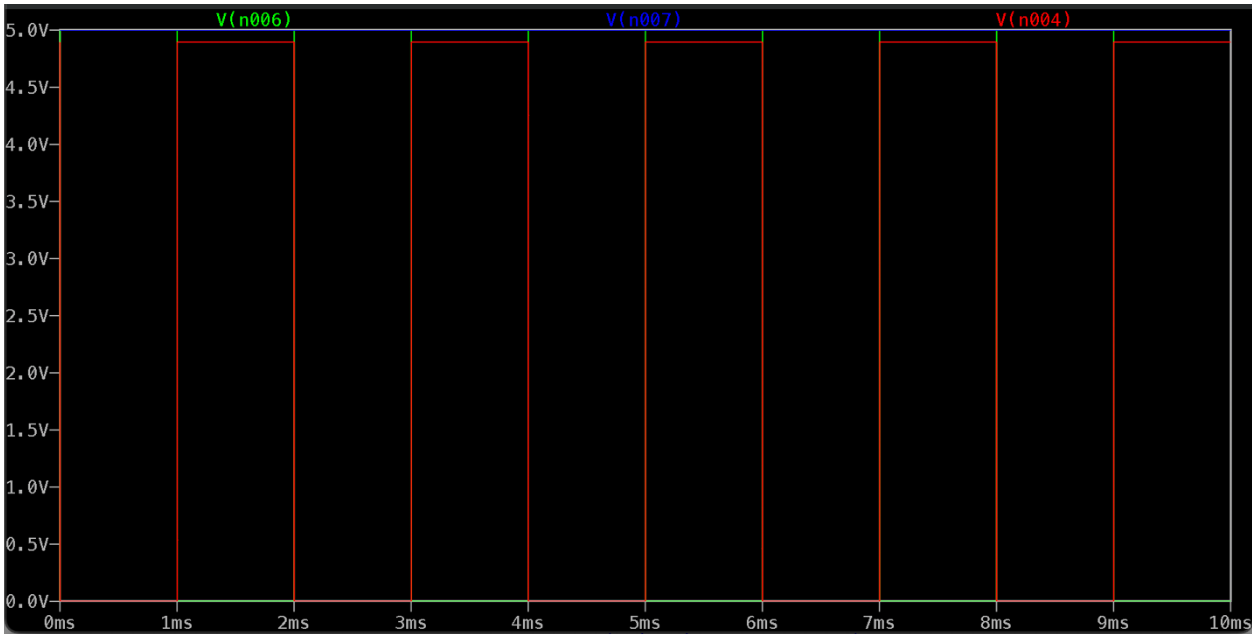

Figure 7: LTSpice Voltage Waveform of $V_{control}$, V_{supply} and V2

Experimental Measurements

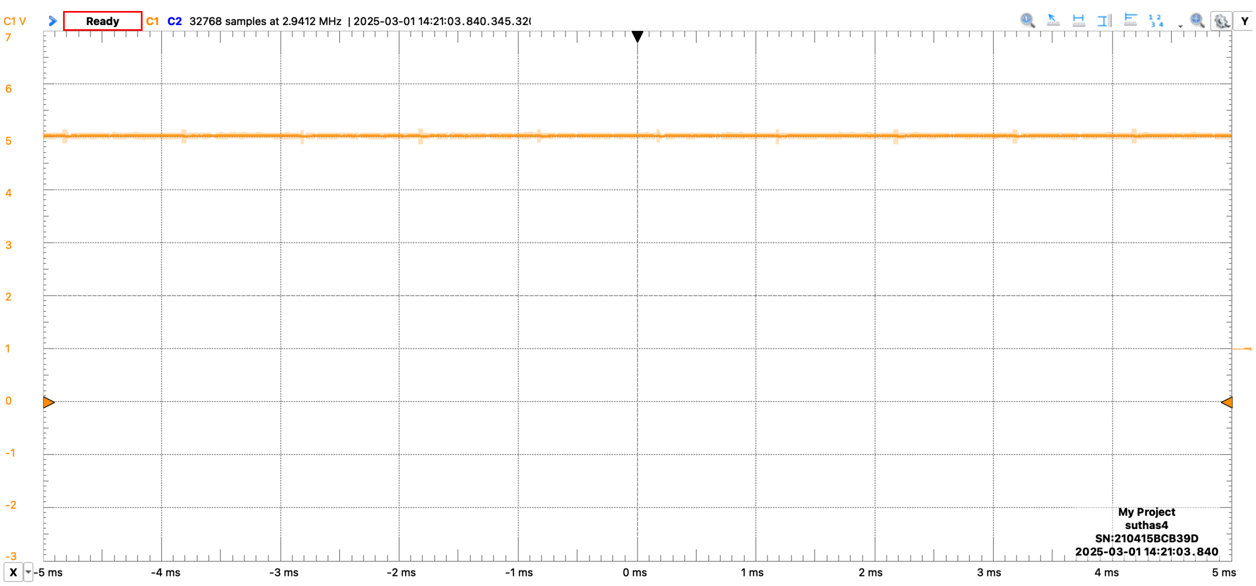

Figure 8: AD3 Voltage Waveform of V_1 (V_{supply})

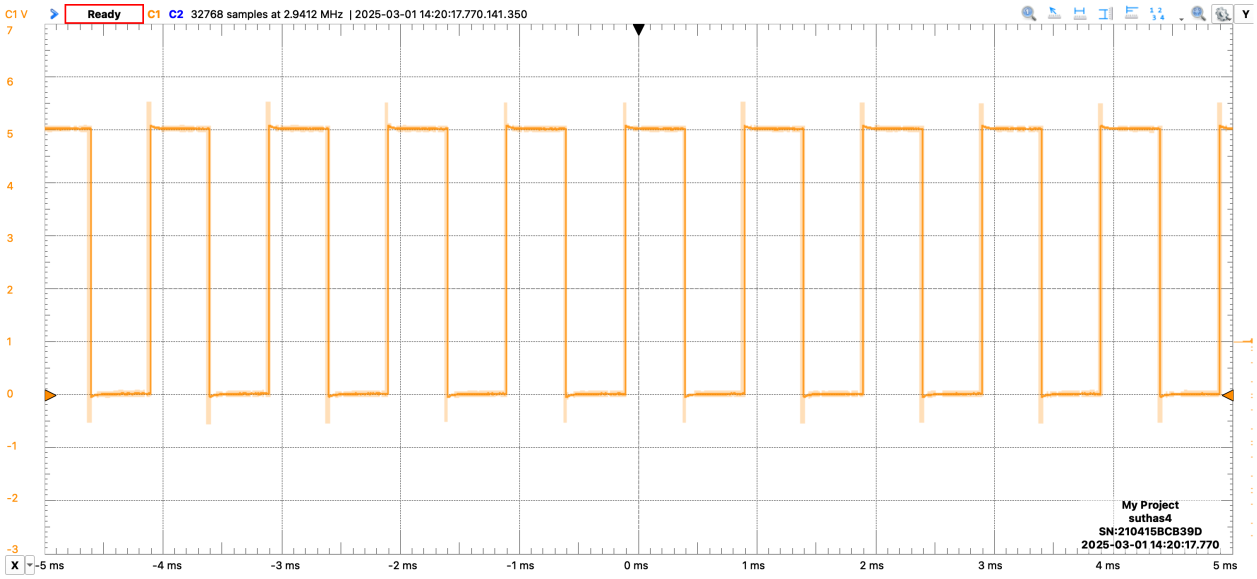

Figure 9: AD3 Voltage Waveform of $V_{control}$

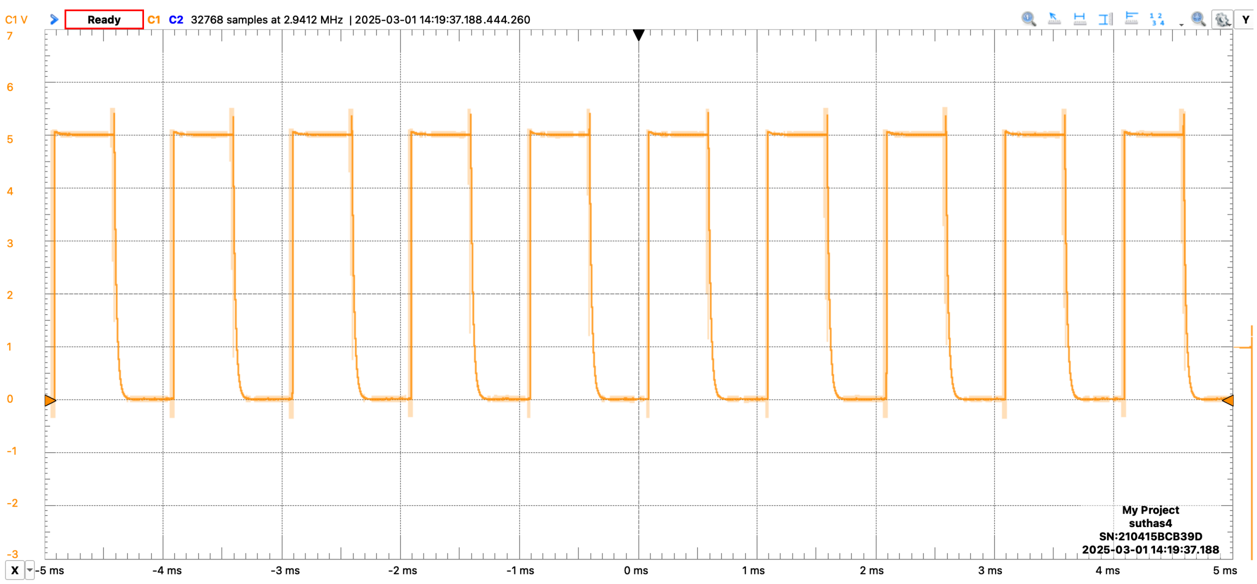

Figure 10: AD3 Voltage Waveform at Node V2

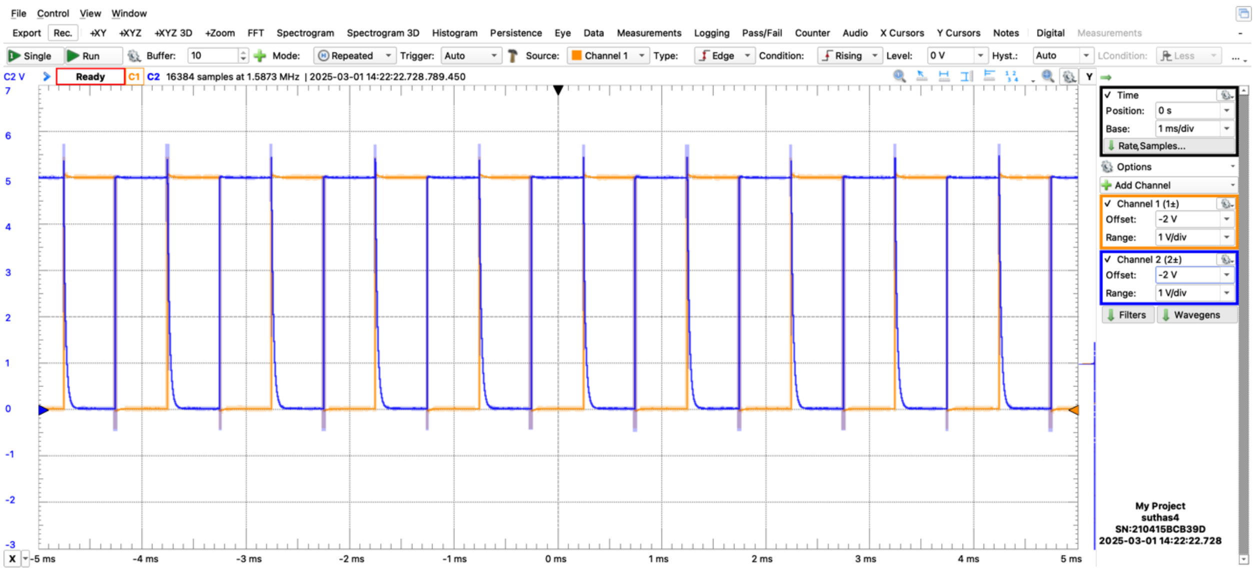

Figure 11: AD3 Voltage Waveform of $V_{control}$ and V2

Theoretical Measurements

These theoretical calculations are based on the threshold voltage (V_T) and transconductance (K) given for the CD4007B IC [3].

<u>PMOS</u>

V_T = 1.7V

$K \ = 4.4\mu A/V$

<u>NMOS</u>

V_T = 1.75V

$K \ = 7.3\mu A/V$

Voltage drop when closed (ON state) $V_{control} = 0V$	**NMOS** $V_{GS1} = 0V$ $V_{GS1} \leq V_{T1}$ NMOS is in cutoff and $I_{DS} = 0mA$ **PMOS** $V_{SG2} = 5V - 0V \geq -V_{T2}$ $V_{SG2} \geq -V_{T2}$ $5V \geq 1.7V$ PMOS is either in saturation or linear mode Assuming saturation, $$I_{DS} = \frac{k}{2}(V_{SG2} + V_{T2})^2$$ $$I_{DS} = \frac{4.4\mu}{2}(5 - 1.7)^2 = 2.39 \times 10^{-5}A$$ Given the current, we can calculate $V_2 = V_{D2}$ $$V_2 = I_D R_L = (2.39 \times 10^{-5}A)(470k\Omega) = 11.233V$$ Since V_2 cannot exceed 5V, PMOS is in linear mode Solving for V_{DS}, $$\frac{V_{DS}}{47k} = 4.4 \times 10^{-6} \times \left((3.3)V_{DS} - \frac{V_{DS}^2}{2}\right)$$ $$V_{DS} = 5.63V$$ $$V_{drop} = V_{SG2} - V_{DS}$$ $$V_{drop} = 5V - 5V = 0V$$

Current leakage when open (OFF state) $V_{control} = 5V$	**PMOS** $V_{SG} = 5V - 5V \leq V_T$ $V_{SG} \leq V_T$ $0V \leq 1.7V$ PMOS is in cutoff and $I_{DS} = 0mA$
Voltage supply range when closed (ON state) $V_{control} = 0V$	PMOS must be in saturation $V_{SD2} \geq (V_{SG2} + V_{T2})$ $V_{SD2} \geq (5V - 1.7V)$ $V_{SD2} \geq 3.3V$
Voltage supply range when open (OFF state) $V_{control} = 5V$	PMOS must be in cutoff $V_{SG2} \leq -V_T$ $V_{SG2} \leq 1.7V$ $V_{S2} - V_{G2} \leq 1.7V$ $V_{S2} \leq 1.7V + 5V \leq 6.2V$ $V_{\sup ply}$ must be below 6.2V. However, for the specifications of this project $V_{\sup ply} \leq 5V$

Table 5: Theoretical Calculations for the Test Cases

Experimental Measurements

Voltage drop when closed (ON state) $V_{control} = 0V$	$V_1 = V_{Supply} = 5.003V$ $V_2 = V_D = 4.988V$ $V_{SD} = 5.003V - 4.988V = 0.015V$ $V_{drop} = 5.003V - 4.988V = 0.015V$
Current leakage when open (OFF state) $V_{control} = 5V$	$I_{RL} = \frac{V_2}{R_L} = \frac{V_D}{R_L}$ $I_{RL} = \frac{-10.52mV}{470k\Omega} = 2.238 \times 10^{-8}A$

Table 6: Experimental Calculations for the Test Cases for Switch 1

Theoretical Explanation of Results

After building and testing the physical circuit, the experimental values were compared to the theoretical values to observe the idealities. Firstly, the voltage drop across the switch was very small at 0.015V. This was better than the simulated drop of 0.254V. However, it was not better than the theoretical voltage drop, which was 0V, since the PMOS should be in linear mode (as seen in *Table* 6). Next, the leakage current was tested when the switch is off. Theoretically, a 0mA leakage current was calculated, however the physical design has a leakage current of $2.238 \times 10^{-8} A$. With the voltage drop and leakage current minimal but not equalling 0, it can be seen that this is not an ideal switch.

Design Trade-offs

The largest trade-off in this design was in balancing the requirements with the components available in the 2EI4 kit.. The simplest feasible design was possible using only one MOSFET, however it was not bidirectional, which is a key characteristic of an ideal switch. Instead, two MOSFETs were used with a $470k\Omega$ resistor to build the best ideal switch with the components available. Ideally, a higher resistance value would have been usen, but $470k\Omega$ was chosen as it was the highest valued resistor available to us in the 2EI4 kit. Although, some component trade-offs were made, the switch still functioned as expected.

Switch 2:

Circuit Schematic

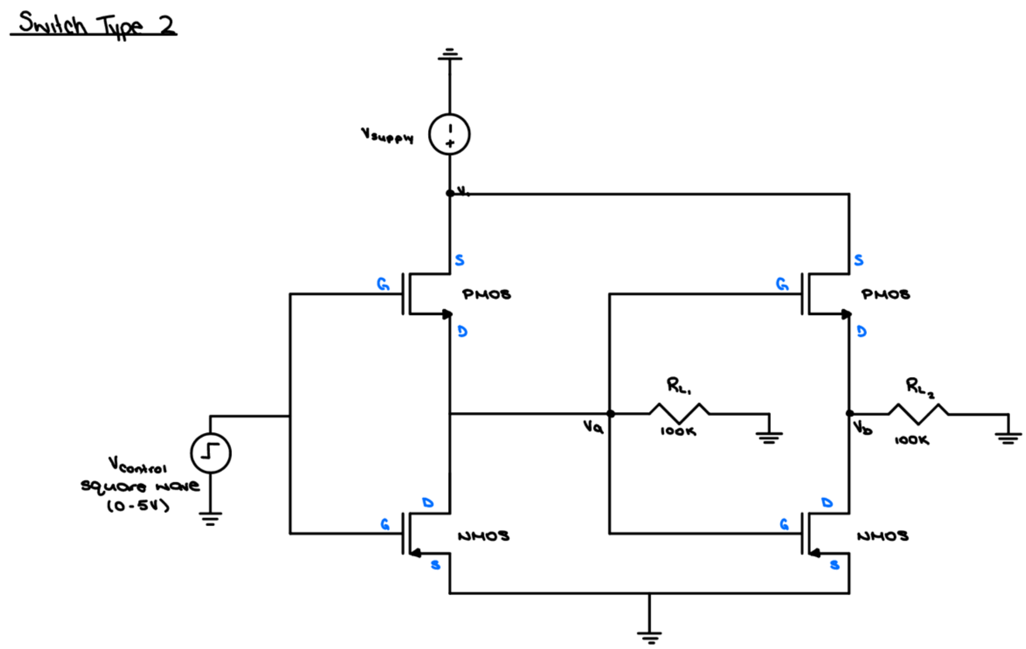

Figure 12: Hand Drawn Circuit Schematic for Switch 2

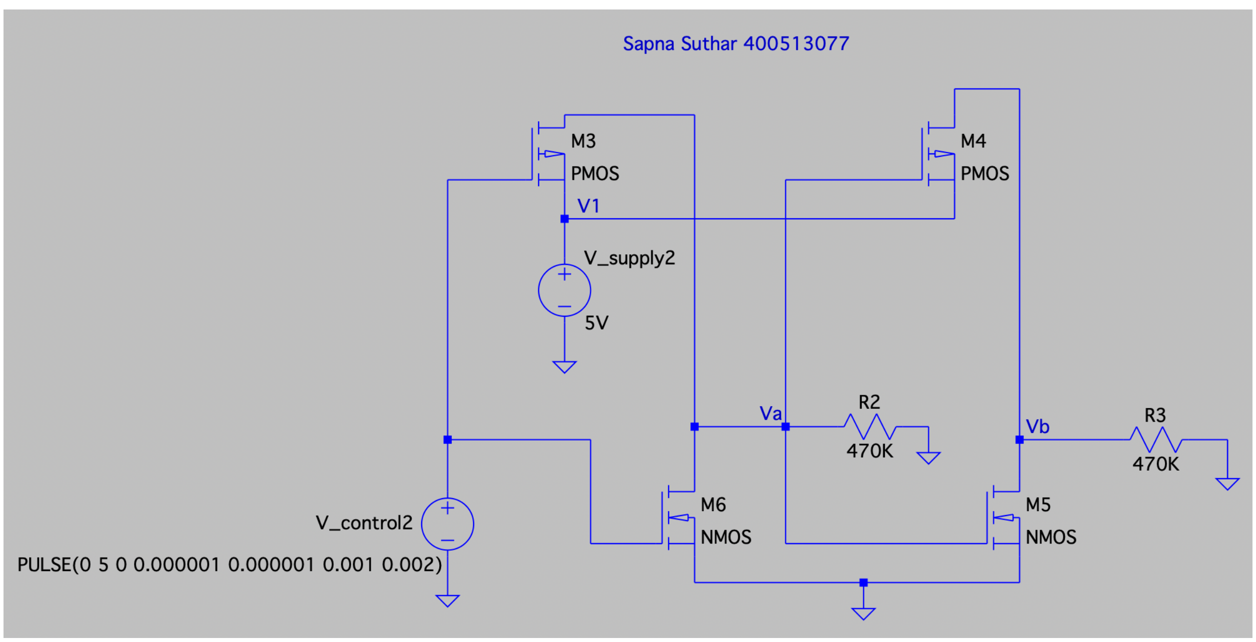

Figure 13: LTSpice Circuit Schematic for Switch 2

Measurements Based on Test Plan

LTSpice Measurements

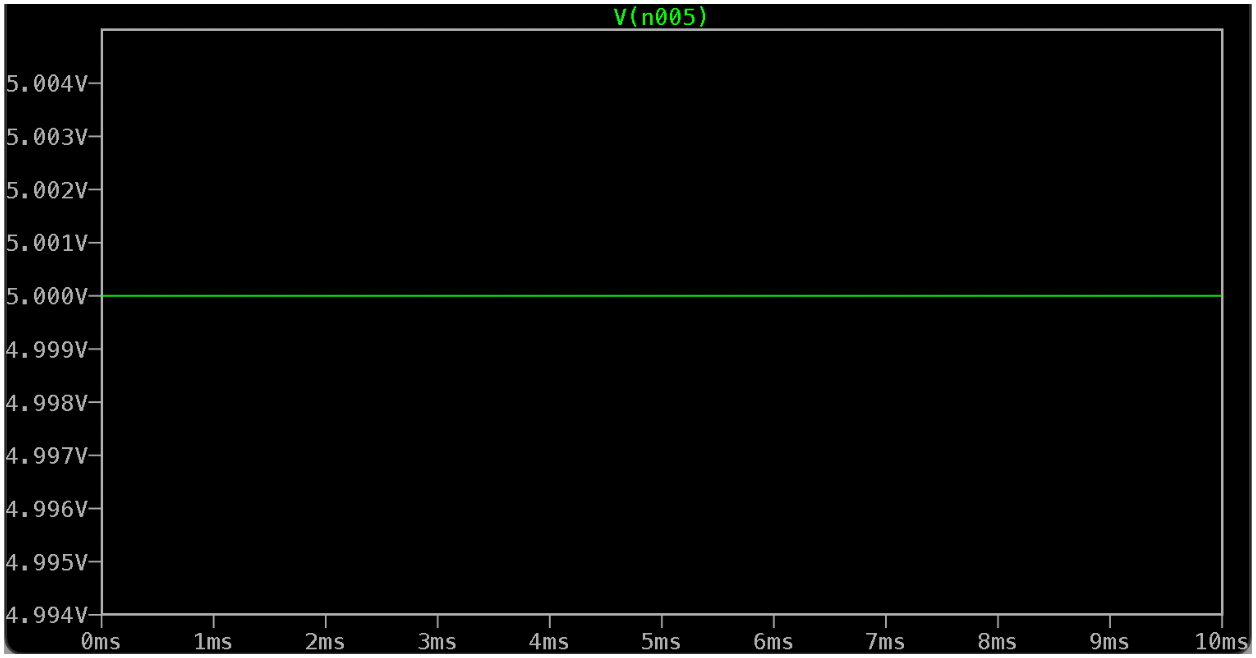

Figure 14: Voltage Waveform of V_1 *(*$V_{sup\,ply}$*)*

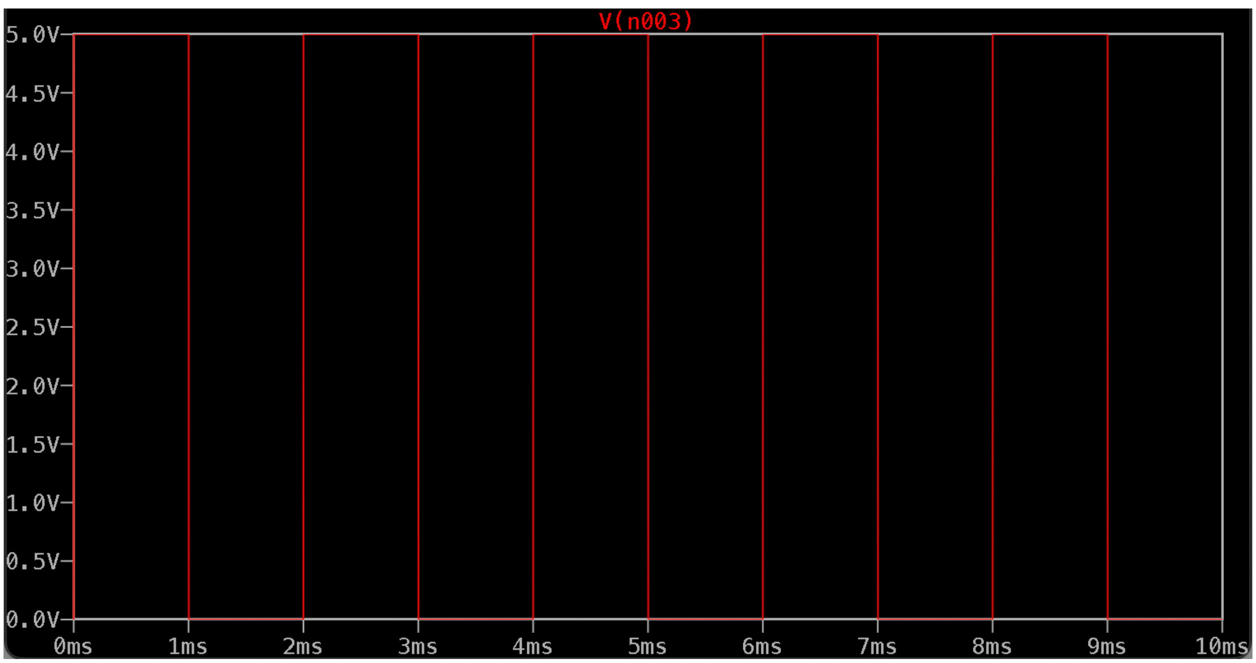

Figure 15: Voltage Waveform of $V_{control}$

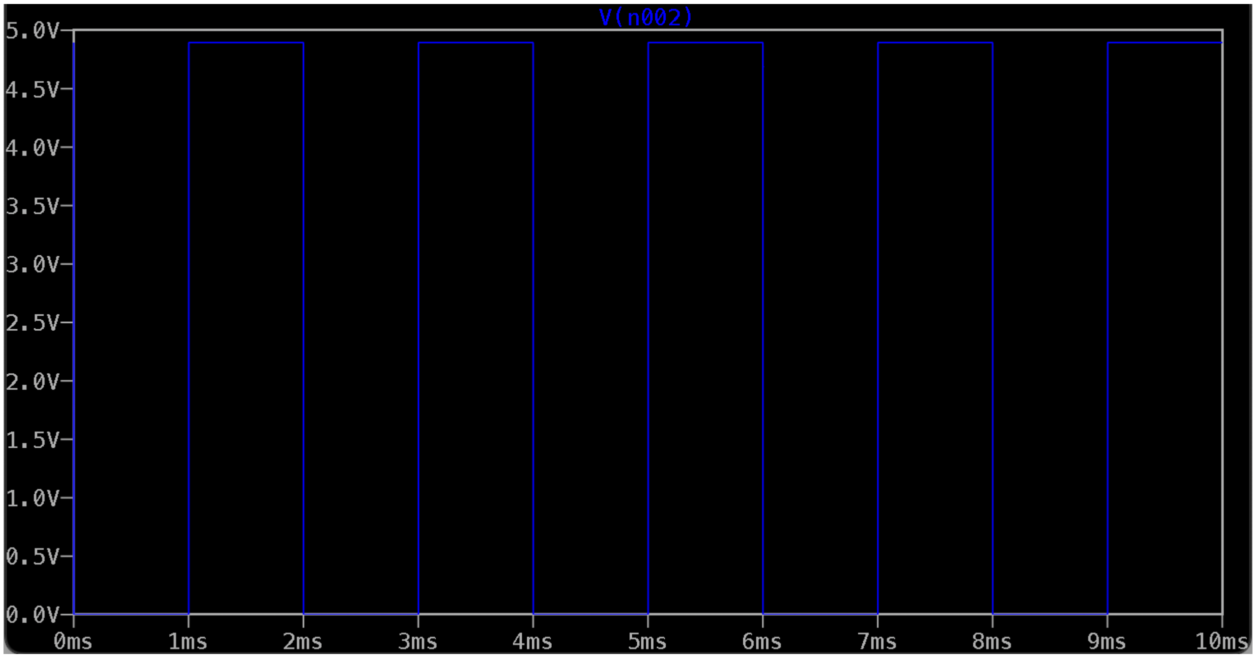

Figure 16: Voltage Waveform at Node V_a

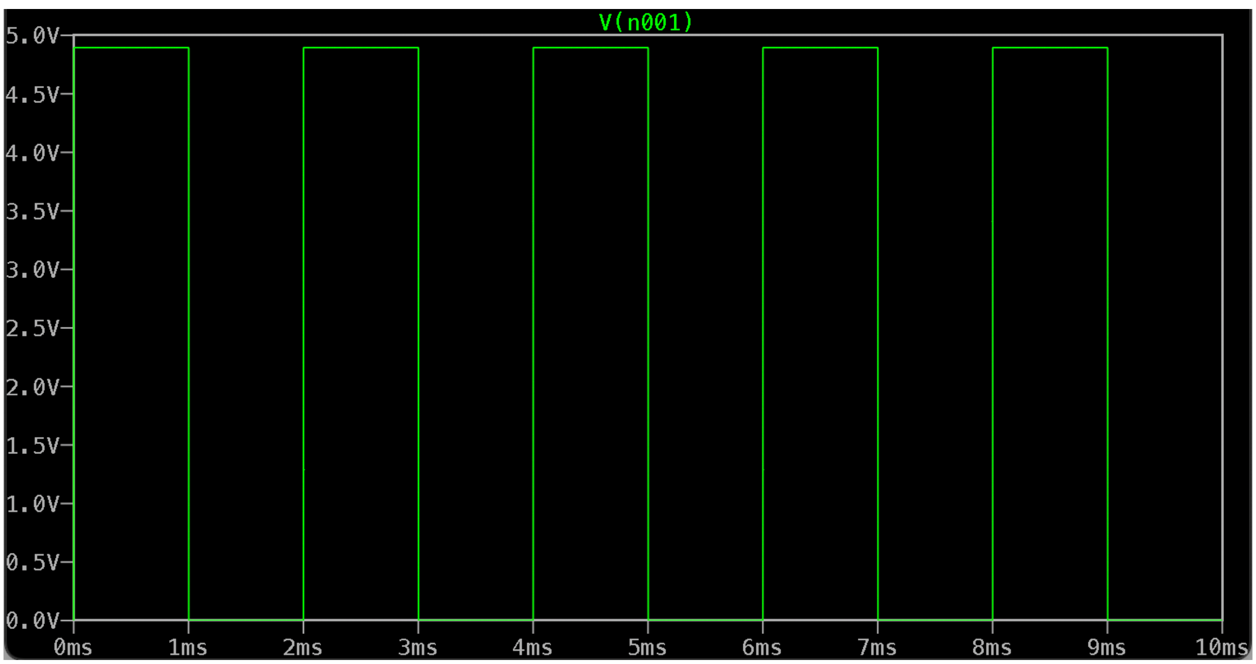

Figure 17: Voltage Waveform at Node V_b

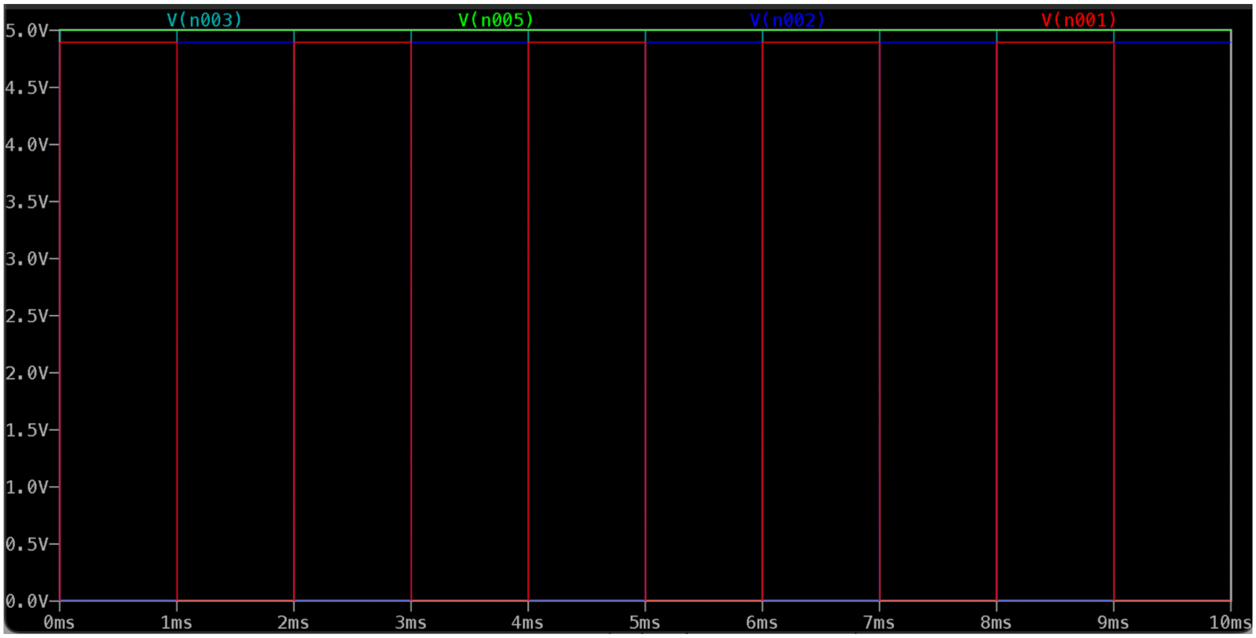

Figure 18: Voltage Waveform of $V_{control}$, V_{supply}, V_a and V_b

Experimental Measurements

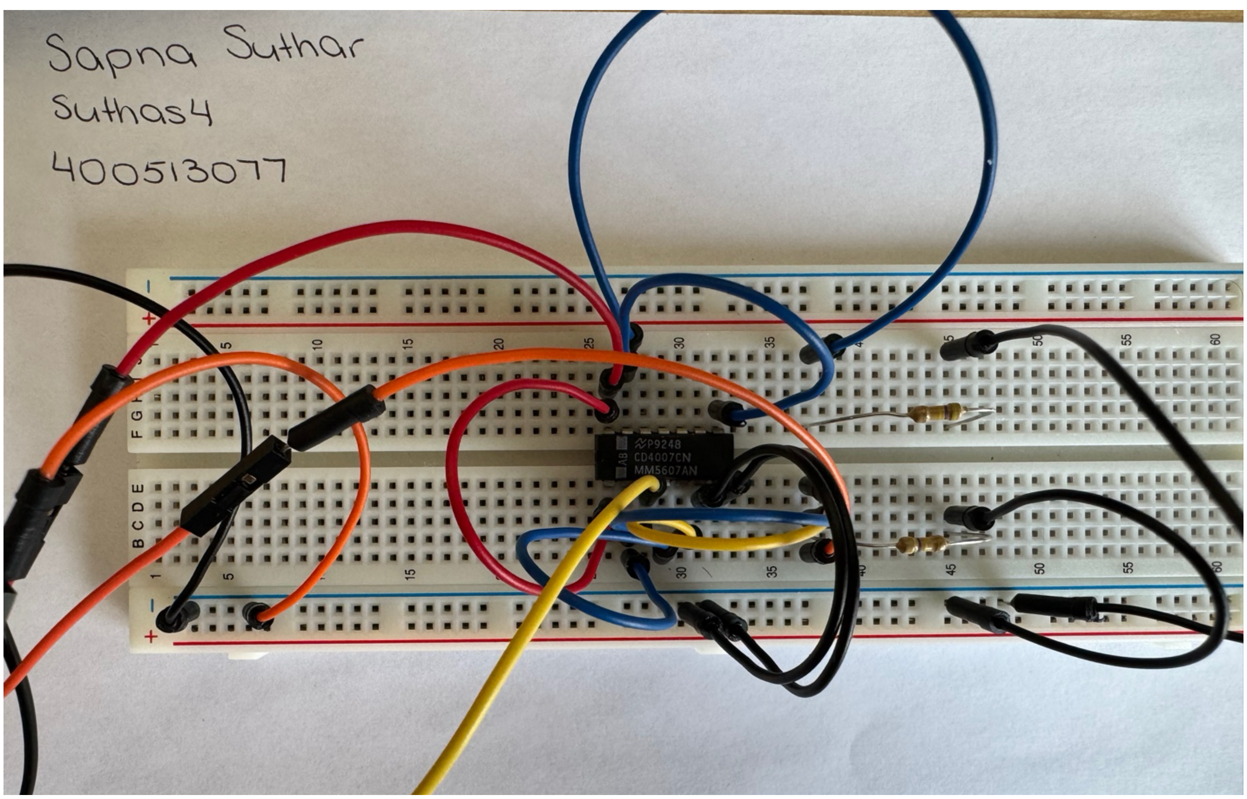

Figure 19: Built Switch 2 Circuit

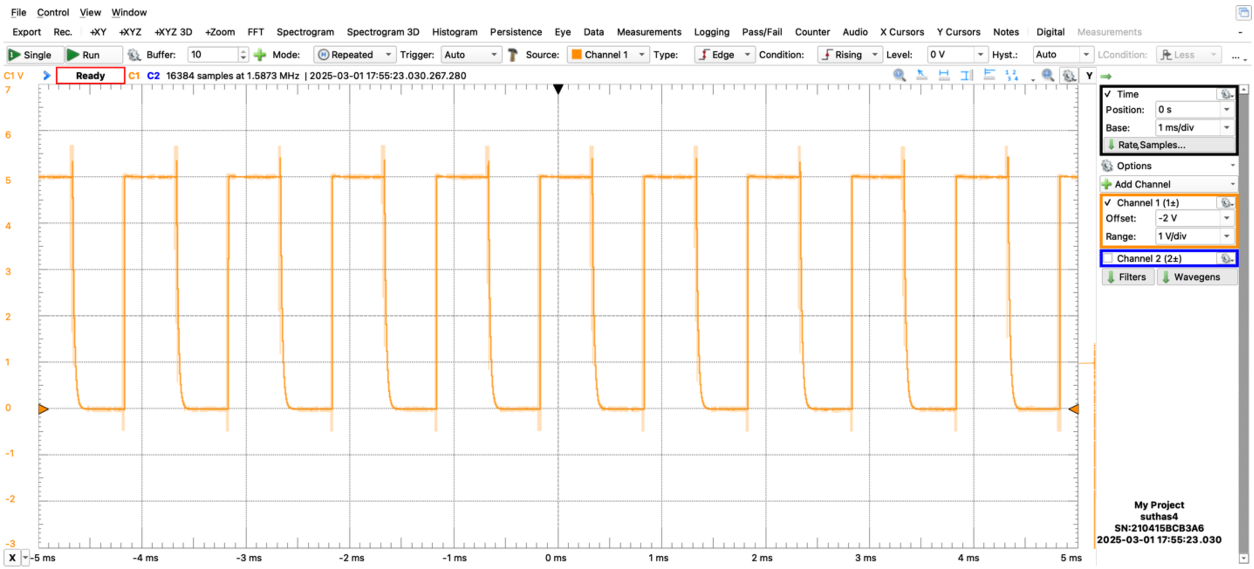

Figure 20: AD3 Voltage Waveform of V_a

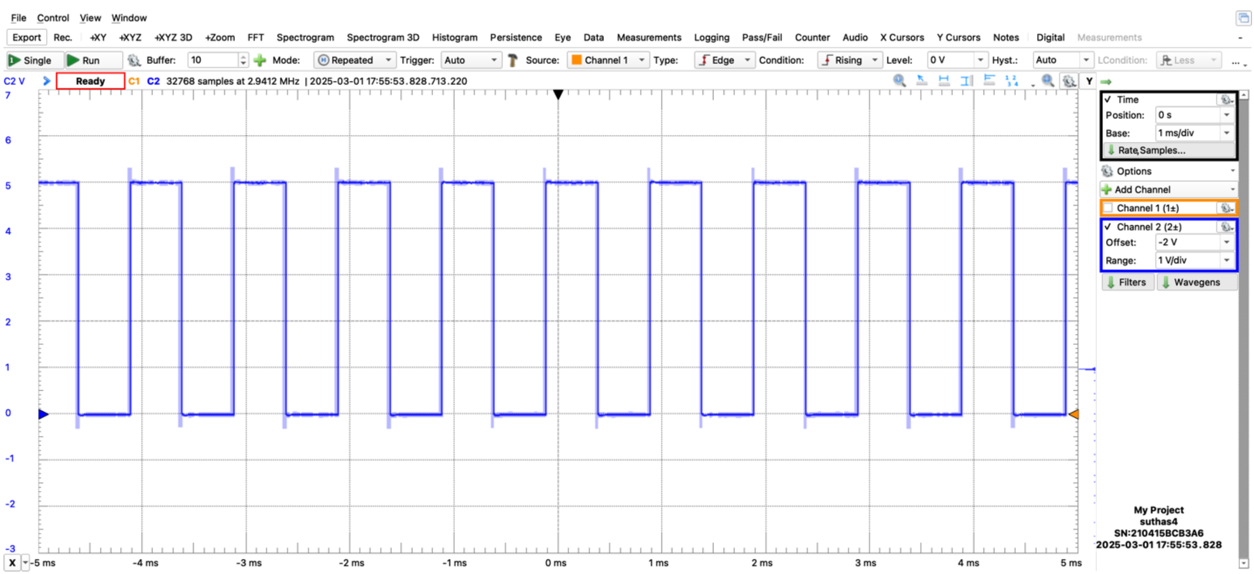

Figure 21: AD3 Voltage Waveform of V_b

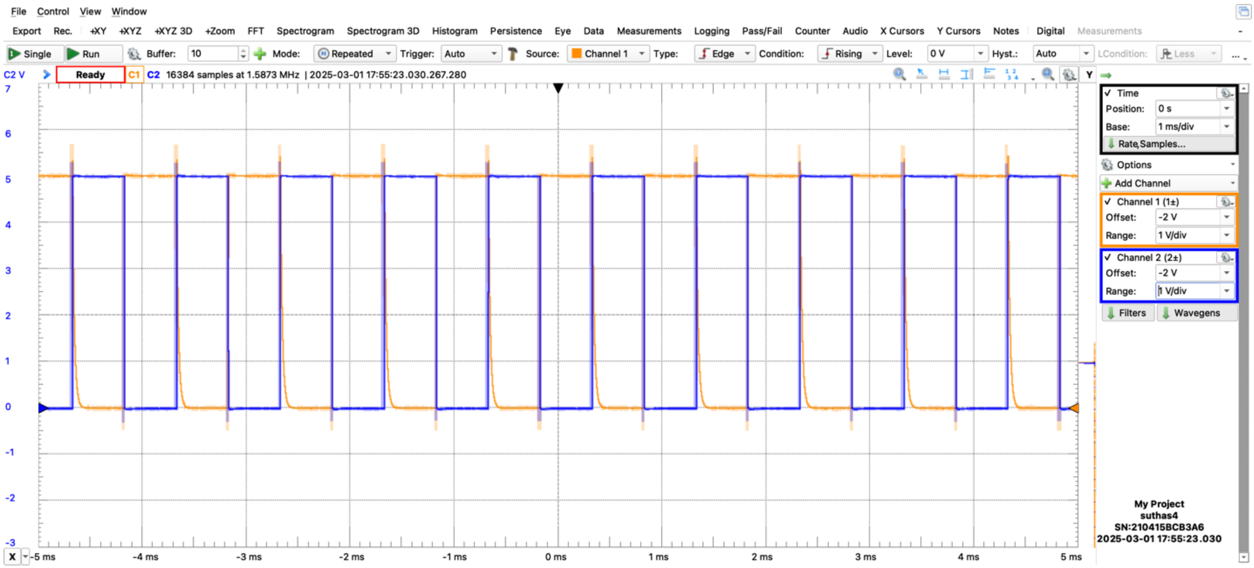

Figure 22: AD3 Voltage Waveform of V_a and V_b

Experimental Measurements

Voltage drop when V_a conducts (1st pair of MOSFETs) $V_{control} = 0V$	$V_1 = V_{Supply} = 5.003V$ $V_a = V_D = 4.989V$ $V_{drop} = 0.014V$
Voltage drop when V_b conducts (2nd pair of MOSFETs) $V_{control} = 5V$	$V_1 = V_{Supply} = 5.003V$ $V_b = V_D = 4.984V$ $V_{drop} = 0.019V$
Current Leakage when V_a conducts (1st pair of MOSFETs) $V_{control} = 0V$	$I_{RL} = \frac{-10.48mV}{470k\Omega} = 2.23 \times 10^{-8}A$
Current leakage when V_b conducts $V_{control} = 5V$	$I_{RL} = \frac{-8.44mV}{470k\Omega} = 1.796 \times 10^{-8}A$

Table 7: Experimental Calculations for the Test Cases for Switch 2

Theoretical Explanation of Results

After building and testing the physical circuit, the experimental values were compared to the theoretical values to observe the idealities. Firstly, the voltage drop across the switch was very small at 0.014V for V_a and 0.019V for V_b. This is better than the theoretical drop based on the simulation of 0.123V for V_a and 0.115V for V_b. This showcases that the physical circuit built is more ideal than the simulated circuit showed.

Next, the leakage current was tested when the switch is off. Theoretically, a 0mA leakage current was calculated, however the physical design has a leakage current of $2.23 \times 10^{-8}A$ when V_a is not conducting and $1.796 \times 10^{-8}A$ when V_b is not conducting. Since, there is a current leakage, it can be seen that the built circuit is not an ideal switch. This shows that the switch does not have the ideal characteristic of infinite resistance.

Design Trade-offs

For this design four MOSFETs were used with two $470k\Omega$ resistors and a voltage source to build the best ideal switch with the components available. Due to the range of the voltage source the circuit itself had to be simpler. Ideally, a larger resistance would have been used in both the simulation and the experimental, however $470k\Omega$ was the largest available resistor in the 2EI4 kit.

References

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