2EI4 – Electronic Devices and Circuits I
Project 4 – XOR Gate

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Circuit Schematic

To build the XOR circuit, 12 MOSFETs were used. This broke down into 6 NMOS and 6 PMOS. The design was necessary to create the inverter circuits for A and B, and then the XOR gate in CMOS. To create the form of the pull-down network needed, DeMorgan's theorem was applied to develop the Boolean expression for the XOR.

$$Y = A \oplus B$$
$$Y = \overline{A}B + \overline{B}A$$
$$Y = \overline{\overline{\overline{A}B + \overline{B}A}}$$
$$Y = \overline{(A + \overline{B}) \cdot (B + \overline{A})}$$
$$Y = \overline{AB + \overline{B}\overline{A}}$$

Based on the created expression, the finalized circuit for the XOR gate was created.

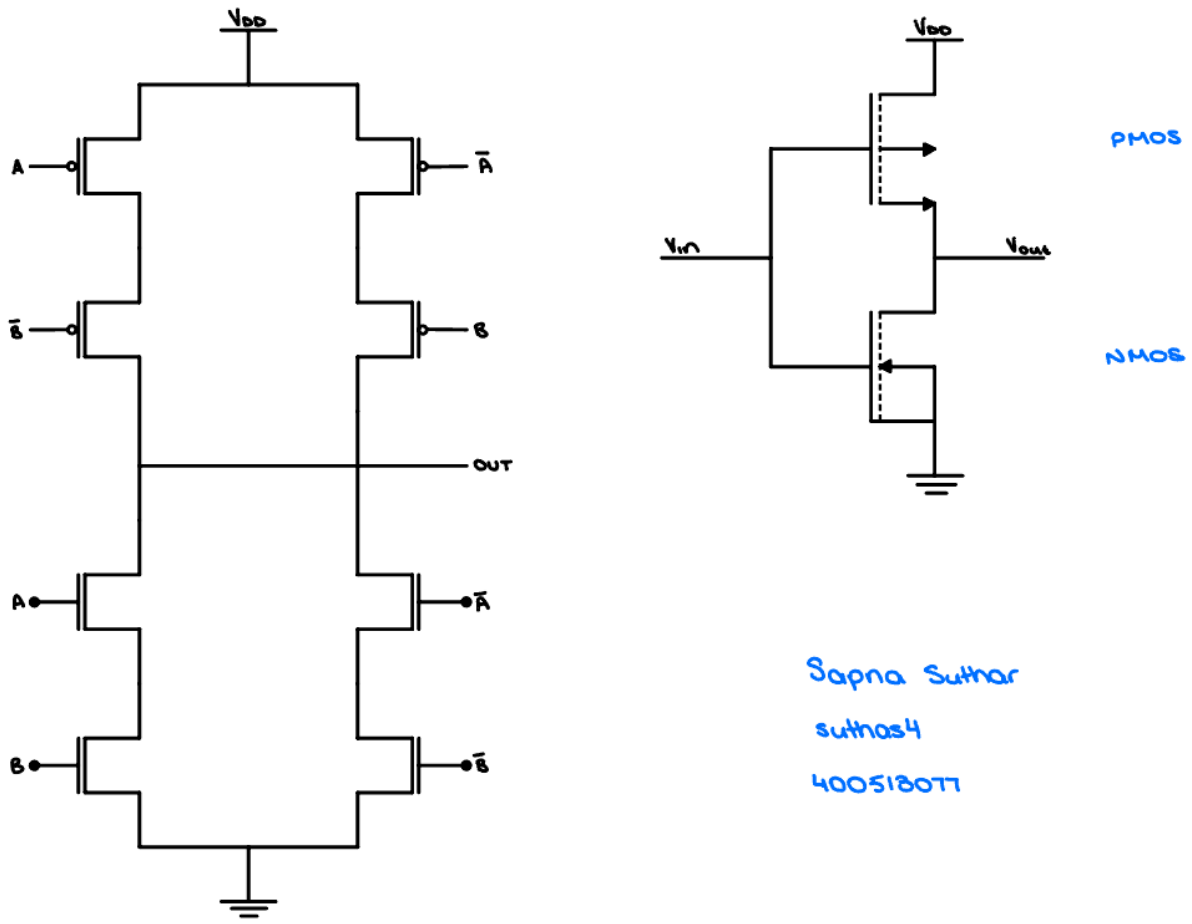

Figure 1: CMOS XOR gate and CMOS Inverter

The XOR gate used 8 MOSFETS. However, to create the inverted A and B, 2 MOSFETS were required for each. This created the total 12 MOSFETS needed in the circuit.

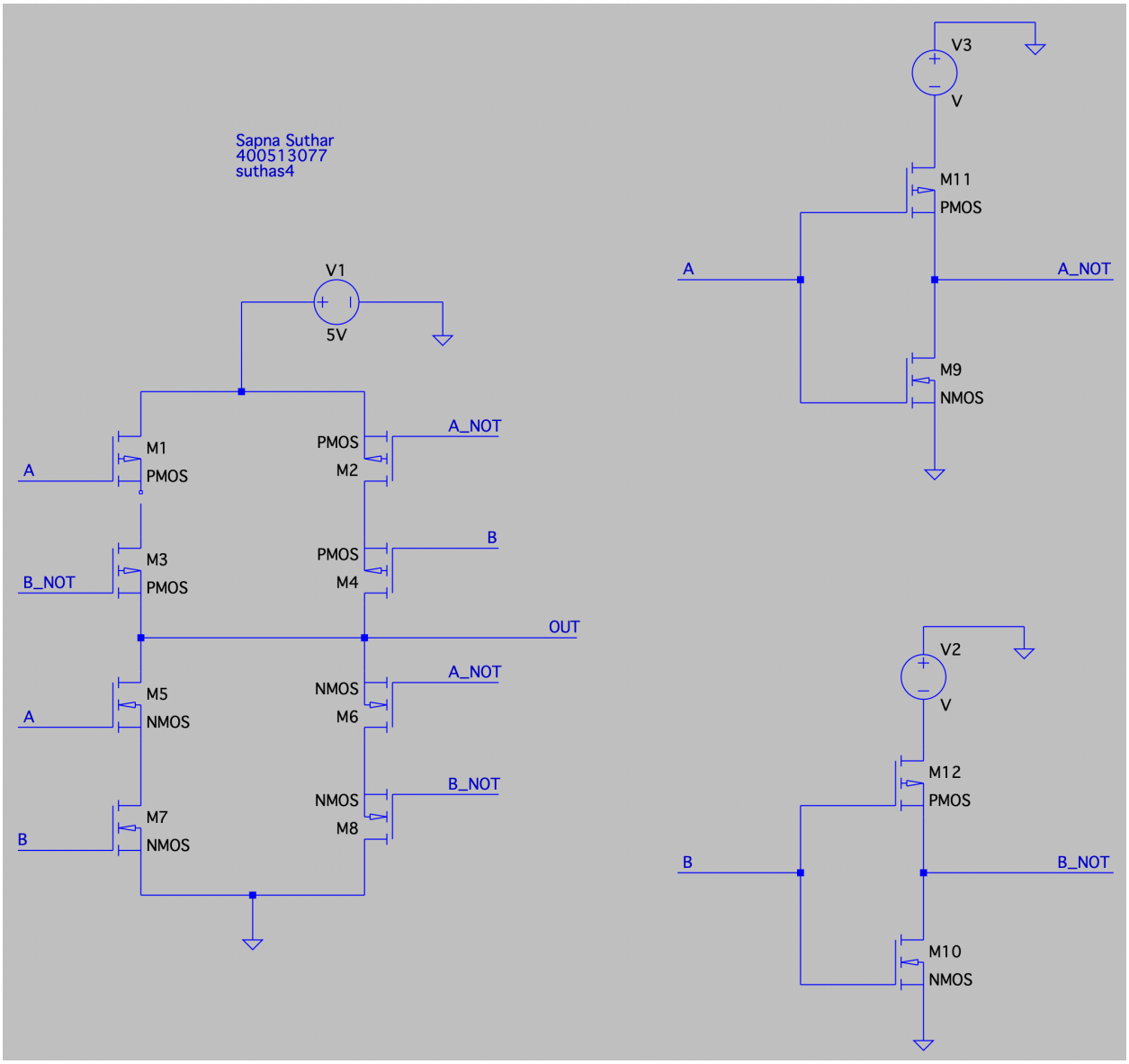

Figure 2: LTSpice CMOS XOR gate and CMOS Inverter

Ideal Sizing

To optimize the time delay of our CMOS XOR circuit, it's essential to ensure symmetry between the pull-up network and the pull-down network. The pull-up network is made of PMOS transistors, and the pull-down network consists of NMOS transistors. A symmetric design ensures both networks have equal propagation delays, minimizing the total delay of the circuit.

Electron mobility in NMOS transistors is higher than hole mobility in PMOS transistors by a factor of 2.5. This difference means that for a PMOS transistor to conduct current as effectively as an NMOS, it must be sized larger. Therefore, the ideal width-to-length ratios (W/L) for PMOS transistors are $\left(\frac{W}{L}\right)_P = 5$ and $\left(\frac{W}{L}\right)_N = 2$ for NMOS transistors.

From the circuit schematic, we observe that the longest paths in both the PUN and PDN consist of 2 transistors in series. This means the total resistance (R_{eq}) for each network is halved. Therefore, $\frac{n}{2}$ for PDN and $\frac{p}{2}$ for PUN.

Since resistance is inversely proportional to transistor sizing, to maintain equal delays across both networks, we must ensure that their total resistances are equivalent. This leads us to enforce a 1:1 delay ratio between PUN and PDN.

Thus, each transistor in the critical path needs to be double the size of the reference inverter sizing. When we account for both transistors in series, the ideal sizing ratio becomes:

$$\frac{2 \times PMOS}{2 \times NMOS} = \frac{5}{2} = 2.5$$

This confirms that to balance conduction speeds and achieve minimum propagation delay, the PMOS must be sized 2.5 times larger than the NMOS transistors in the CMOS XOR gate.

Feasibility of Ideal Sizing

From the circuit diagrams above, the longest path from VDD to GND passes through 2 NMOS and 2 POS transistors. This indicates that the required sizing ratio for the circuit is $\frac{2 \times PMOS}{2 \times NMOS} = \frac{5}{2} = 2.5$. This matches with the ideal ratio calculated above in the Ideal Sizing section, showcasing the feasibility of implementing this sizing. Since the design is symmetric, that also helps make the ideal sizing more achievable. Overall, the structure of the circuit naturally supports balanced sizing between PMOS and NMOS.

Built Circuit

The physical circuit model the CD4007B IC chip was used as it had the necessary number of transistors. This led to the circuit that can be seen below.

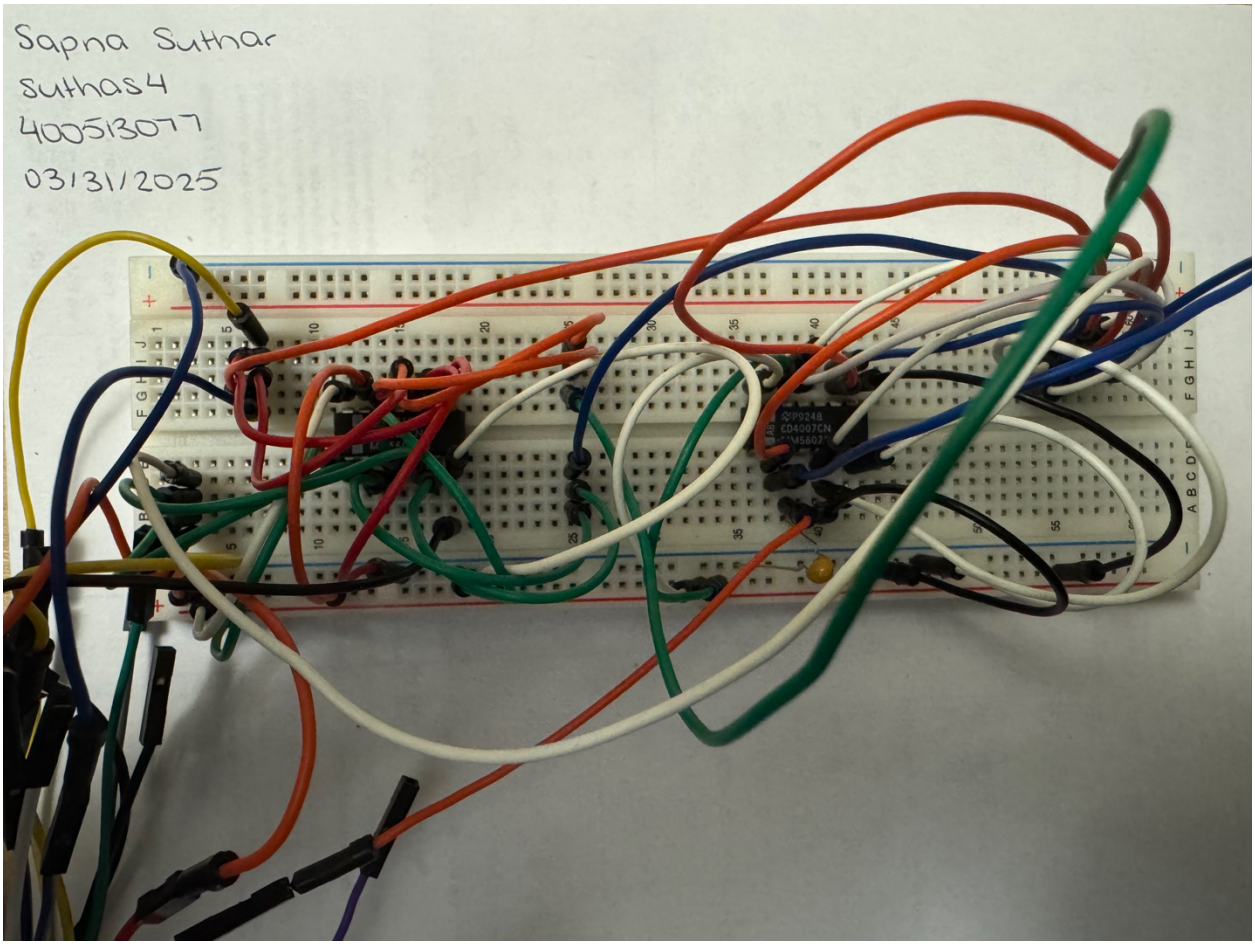

Figure 3: Built Circuit of the XOR Gate

Functional Testing

To test the functionality of the CMOS XOR gate, each combination of inputs had to be tested to ensure the resulting output was correct. The input signals were configured as square waves with a 2.5V offset and a 2.5V amplitude, and the two waveforms were deliberately phase-shifted by 90 degrees to simulate complementary input states over time. Digital IO (DIO) pins were connected to both input lines and the output to allow real-time tracking of logic levels.

Input A (DIO 0)	Input B (DIO 1)	Output (DIO 2)
0	0	0
0	1	1
1	0	1
1	1	0

Table 1: Expected Values of the XOR Gate

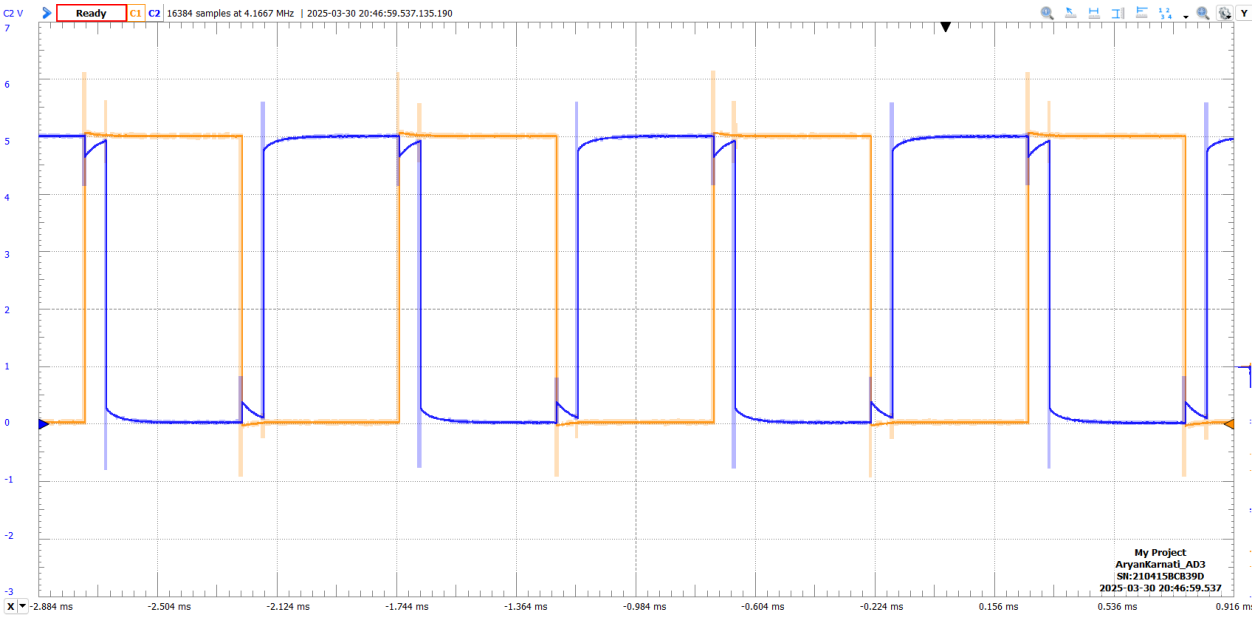

Figure 4: AD3 Logic Analyzer

Static Level Testing

To evaluate the static behavior of the CMOS XOR gate, one input was held at a constant logic high (+5V) while the other input was driven by a square wave alternating between 0V and 5V. After collecting initial data, the input roles were reversed to observe the impact on voltage levels. In the first configuration, where input A was fixed at 5V, the measured logic high and low voltages were $V_H = 4.992V$ and $V_L = 1.29mV$. When the setup was reversed and input B was set to 5V, the output changed significantly to $V_H = 4.979V$ and $V_L = 24.45mV$.

These variations suggest potential issues such as uneven internal resistance, faulty wiring, or impedance mismatch between input sources. A higher impedance on one side may cause greater voltage drop, especially under load, resulting in reduced logic high levels. Another possible cause could be a degraded or partially damaged IC.

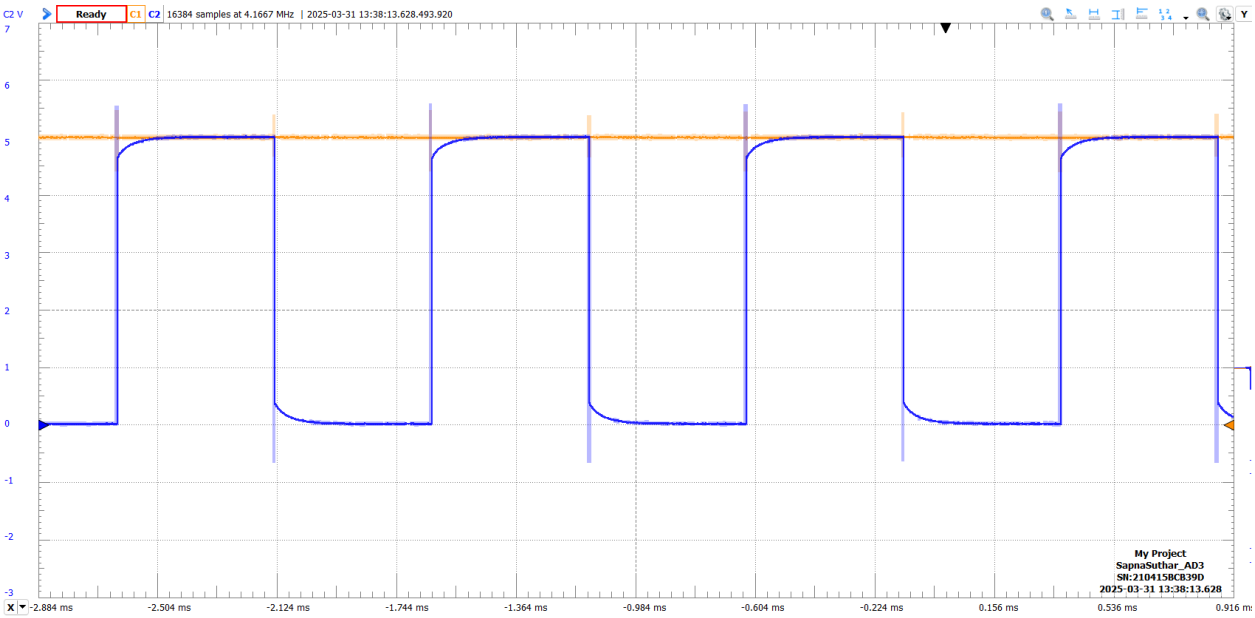

Figure 5: Waveform of Input 1 (A = 5V, B is square waveform 0-5V)

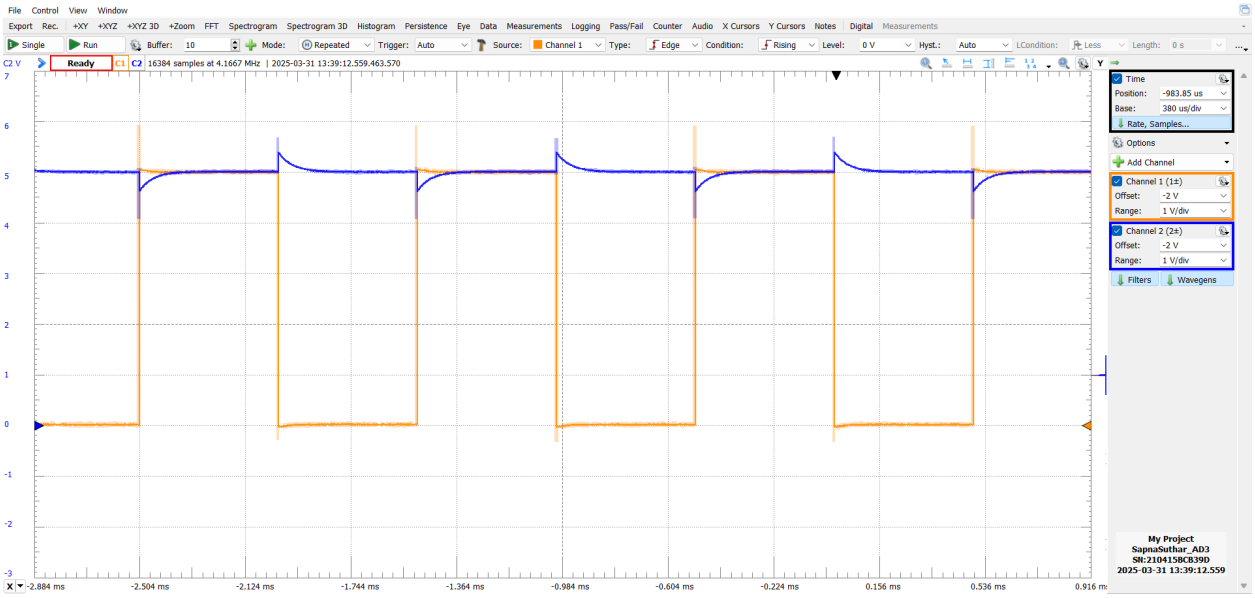

Figure 6: Waveform of Input 2 (B = 5V, A is square waveform 0-5V)

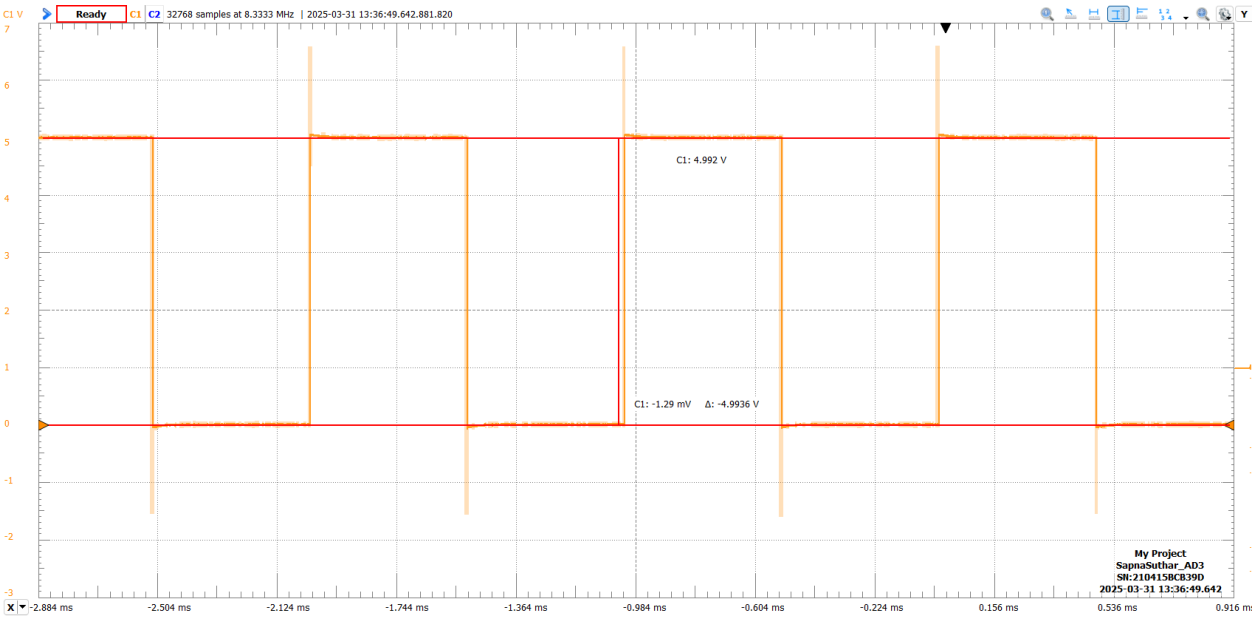

Figure 7: Waveform of Output 1

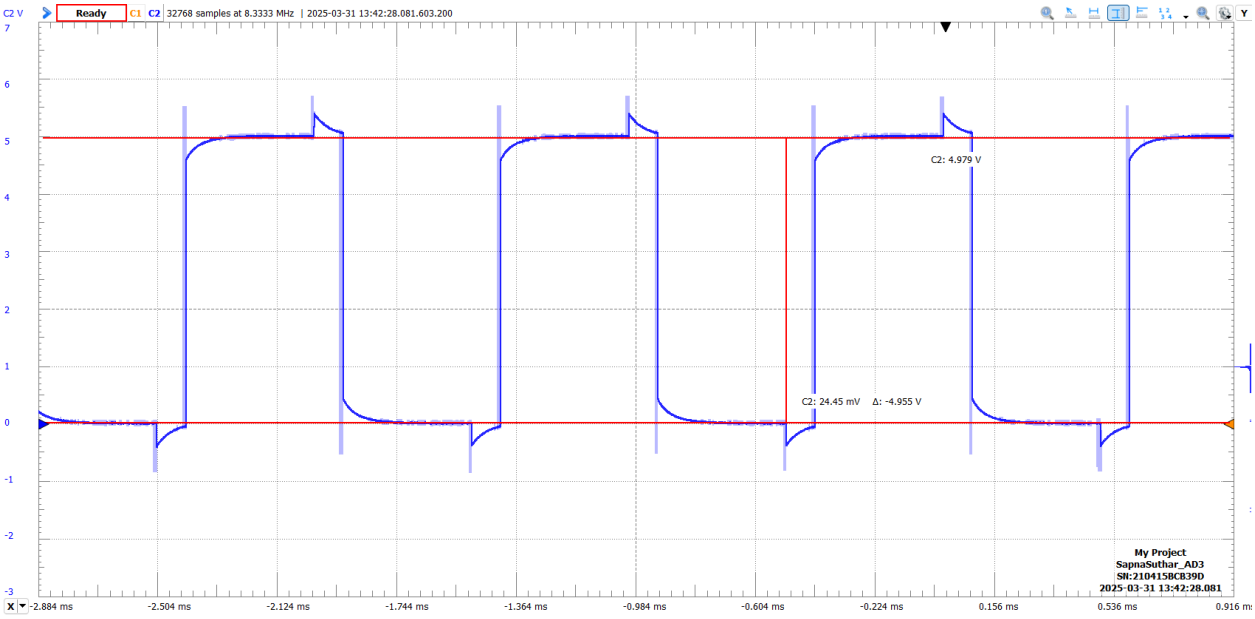

Figure 8: Waveform of Output 2

Timing

To evaluate the switching performance of the CMOS XOR gate, a timing analysis was conducted to measure the delays during transitions between logic states. The focus was on the transition from low-to-high and high-to-low. This was done by connecting a 100 nF capacitor (CM104) to the output and observing the voltage across it.

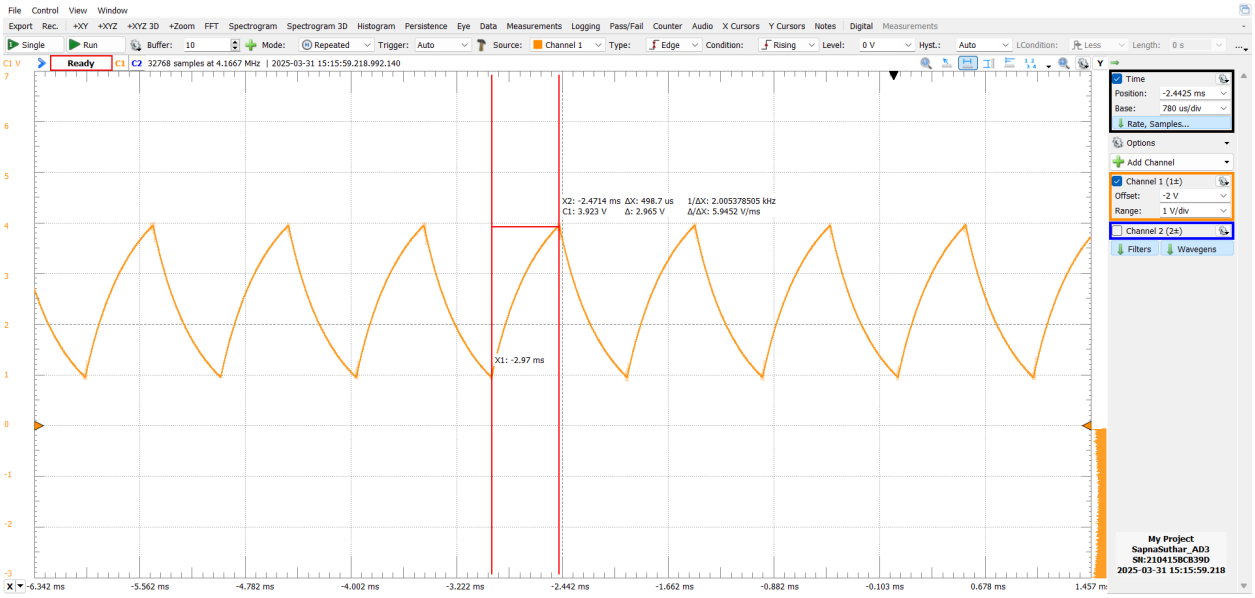

Figure 9: Output Waveform Showing Rising Time

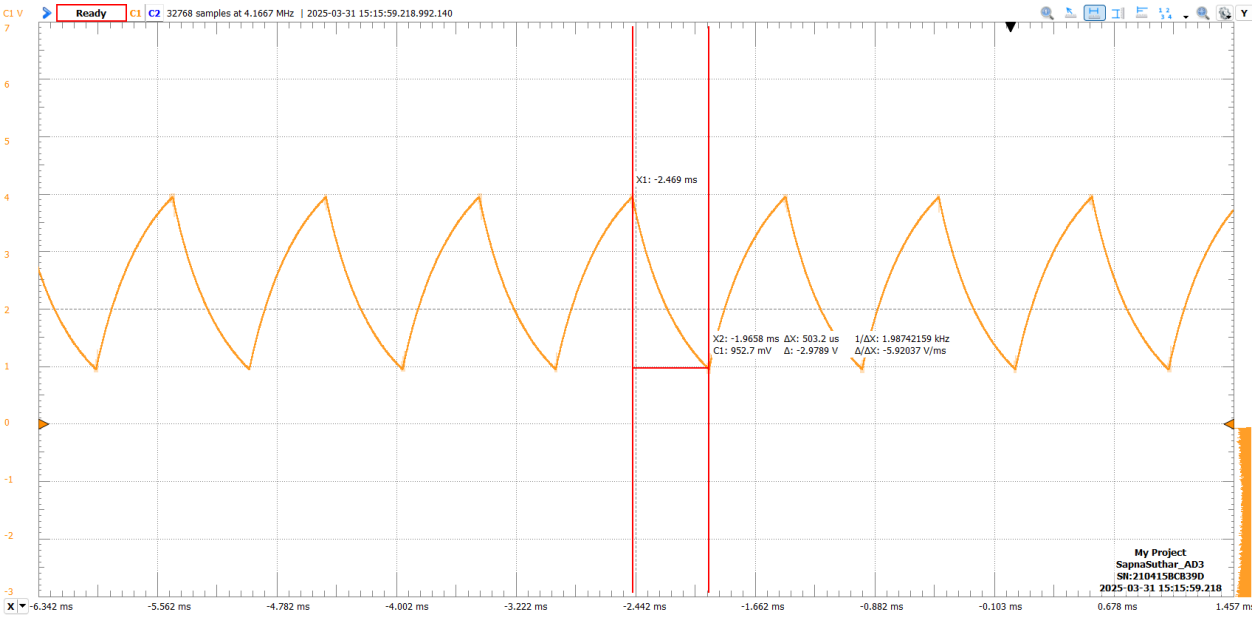

Figure 10: Output Waveform Showing Falling Time

In the setup, input B was held at a constant 5V DC, while input A was driven by a square wave with a 2.5 V amplitude, 2.5 V offset, and a frequency of 500 mHz. From the recorded waveform, the rise time was measured to be 498.7µs, while the fall time was 503.2µs.

To determine the high-to-low propagation delay (τ_{pHL}), we measured the time from the midpoint of the input's rising edge to the midpoint of the output's falling edge. This delay was found to be $\tau_{pHL} = 502.01\mu s$. A similar measurement was performed for the low-to-high transition, yielding a low-to-high propagation delay (τ_{pLH}) of $\tau_{pLH} = 489.49\mu s$.

$$\tau_{pLH}(low - high\ delay) = 244.745\mu s$$

$$\tau_{pHL}(high - low\ delay) = 251.005\mu s$$

Using these values, the average propagation delay (τ_p) was calculated as:

$$\tau_p = \frac{\tau_{pHL} + \tau_{pLH}}{2}$$

$$\tau_p = \frac{251.005 + 244.745}{2}$$

$$\tau_p = 247.875\mu s$$

References

[1] A. S. Sedra, K. C. Smith, T. C. Carusone, and V. Gaudet, Microelectronic circuits, 8th ed. New York, NY: Oxford University Press, 2019.

[2] "MC14007UB Datasheet," Digikey, https://www.digikey.ch/htmldatasheets/production/100087/0/0/1/mc14007ub.html?srsltid=AfmBOorKgJ8WIFsFtOI8Ptt6YHAYwE5BUXYKtxTXDS0_yM5ZEkDWCUhi [accessed Mar. 31, 2025].