

# **2EI4 – Electronic Devices and Circuits I**

## **Project 1 – DC Power Supply**

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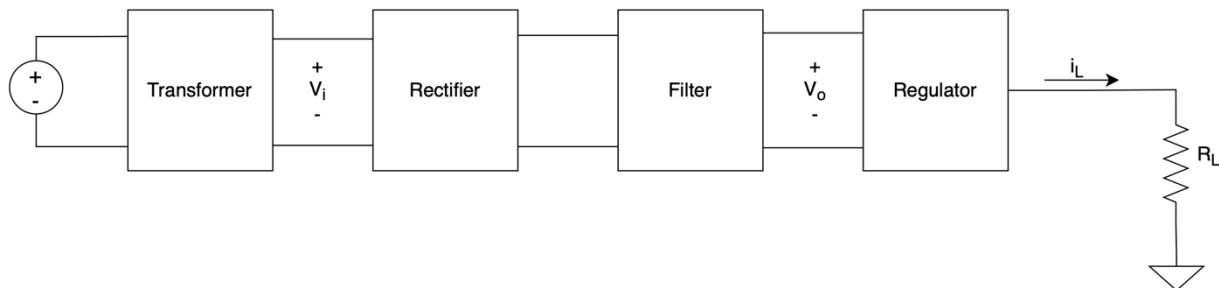
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## **Summary**

The goal of this project was to create a DC power supply that converts AC to DC current. This power supply consists of 4 main components. These include the transformer, rectifier, filter and regulator. However, a transformer will not be used, and instead an AD3 will create the transformer output. At the end of this project, the DC power supply should convert a 120V rms source with a frequency of 1kHz to a DC output of 10mA current at  $3V \pm 0.1V$ . The AC signal will be rectified of any negative cycles, filtered of any remaining noise, and regulated to deliver a DC signal.



*Figure 1: Block Diagram*

## **Design**

### **Part 1: Transformer**

Although the design does not include a physical transformer, the step-down process of the AC signal is simulated using the AD3. After the transformer steps down the 120V rms signal, an AC signal of approximately 5.45V is necessary. This occurs due to the 22:1 turn ratio used, reducing the 120V source to 4.45V with a peak to peak of 7.71V. This 7.71V input is generated by the AD3 waveforms tool. Despite the transformer not being built, it was designed as a center tapped transformer combined with a full wave rectifier circuit.

### **Part 2: Rectifier**

The chosen rectifier topology is a full wave rectifier with a centre tapped transformer. A full wave rectifier was chosen as it used both halves of the AC cycle. This is more efficient than a half wave rectifier as the negative half is used and not discarded. As well, it creates a smaller ripple in comparison to the half wave rectifier. A centre tapped rectifier was chosen to simplify the process, as it uses 2 diodes, while the bridge rectifier uses 4. Another key part of a full wave rectifier is due to its high rectified frequency, twice that of a half wave rectifier, a lower valued capacitor can be used to reduce the ripple in the DC output.

Based on the above, a centre tapped transformer with a turn ration of 22:1 will take the 120V rms, stepping it down to 5.45V. From there, the full wave rectifier will half the 5.45V received from the transformer, resulting in an output of 3.82V. This occurs because the peak voltage from the transformer is 7.71V and due to the full wave rectifier, the voltage will be halved.

### Part 3: Filter

The filter used in this design is a parallel RC filter. Some other options included an LC filter and other filters using capacitors. However, the RC filter was chosen as the components needed were more readily available in the provided lab kits. This filter acts to smooth the output of the DC power supply by reducing ripple voltage. After the voltage leaves the rectifier, it isn't a smooth line. The RC filter helps with this by storing and discharging charge to keep the voltage steady. The resistor in parallel to the capacitor works to control the rate at which the capacitor discharges, to better smooth any fluctuations. This filter works well for a low-power application, like this one. However, for a higher power application a LC filter may perform better. The built filter has a 25 microfarads capacitor to combat the voltage ripple of 0.2V. To achieve 25 microfarads, two 10 microfarad capacitors and five 1 microfarad capacitors were used. These seven capacitors were all connected in parallel to one another, to effectively create the desired capacitance of 25 microfarads.

### Part 4: Regulator

The purpose of a regulator is to help smooth out noise created by the peak-to-peak voltage. Although this is useful in some applications, it was not necessary for this design.

## Calculations

Theoretical Calculations	
Load Resistor	$R_L = \frac{V_L}{I_L} = \frac{3V \pm 0.1V}{10mA} = 300 \pm 10\Omega$ <p>The 2EI4 and 2CI4 kits do not contain a <math>300\Omega</math> resistor. Instead, two <math>150\Omega</math> were attached in series to create the necessary <math>300\Omega</math> resistance.</p>
Filter	$V_{ripple} = 3.1V - 2.9V = 0.2V$ <p>A small ripple was necessary to reduce the value of capacitors to ones that were available.</p> $I_L = 10mA$ $f_{in} = 1kHz$ $f_{out} = 2f_{in} = 2(1kHz) = 2kHz$ $C \geq \frac{I_L}{V_{ripple} \times f_{out}} \geq \frac{10mA}{0.2V \times 2kHz} \geq 25\mu F$ <p>The 2EI4 and 2CI4 kits do not contain a <math>25\mu F</math> capacitor. Instead, two <math>10\mu F</math> and five <math>1\mu F</math> were connected in parallel. This <math>25\mu F</math> is the minimum capacitance necessary for this circuit, however a higher capacitance can help produce and output voltage with less ripple.</p>
Diodes	$V_D = 0.72V$ <p>This is assuming a constant drop model.</p>

Rectifier	$V_{peak} = 3.2V$ $V_c = V_{peak} - \frac{V_{ripple}}{2} = 3.2 - \frac{0.2}{2} = 3.1V$ $V = V_D + V_C = 3.1V + 0.72V = 3.82V$ <p>This means the two rectified waveform inputs are:</p> $V_1 = 3.82 \sin(\omega t)$ $V_2 = -3.82 \sin(\omega t)$
Transformer	$V_o = 2V_1$ $V_o = 2(3.82 \sin(\omega t)) = 7.62 \sin(\omega t)$ <p>RMS Conversion:</p> $\frac{V_o}{\sqrt{2}} = \frac{7.64}{\sqrt{2}} = 5.40V RMS$ <p>Turns Ratio:</p> $\frac{N_1}{N_2} = \frac{V_{source}}{V_o} = \frac{120V}{5.40} \approx 22:1$ <p>Turns Ratio</p>

Table 1: Theoretical Calculations

## Expected Performance

After calculating and simulating my circuit, the design was finalised. The input signal had 3.82V amplitude at a frequency of 1kHz. However, since the design consisted of 2 diodes, two input waveforms would be used. The waves would be  $\pm 3.82 \sin(\omega t)$ . This occurs because the centre tapped rectifier chosen can use both the positive and negative cycles of the input voltage. When D1 conducts D2 will be in reverse bias and vice versa. As well, a 0.72V drop across the diodes has been accounted for, as the signal goes through only one diode at a time. At the end, the built circuit should produce a fully rectified wave with minimal ripple, showcasing a smooth DC output.

## Trade Offs

Although no major trade off were made in the construction of this circuit, limitations were put in place by the components available. Since all components had to come from either the 2CI4 or 2EI4 kit, certain values theoretically calculated either had to be made from multiple different components or components were switched for those of a higher value. These changes, although minimal, resulted in a less accurate result.

## Simulation

Before building the circuit using a breadboard and AD3, the circuit was simulated using LTSpice to ensure the desired results.

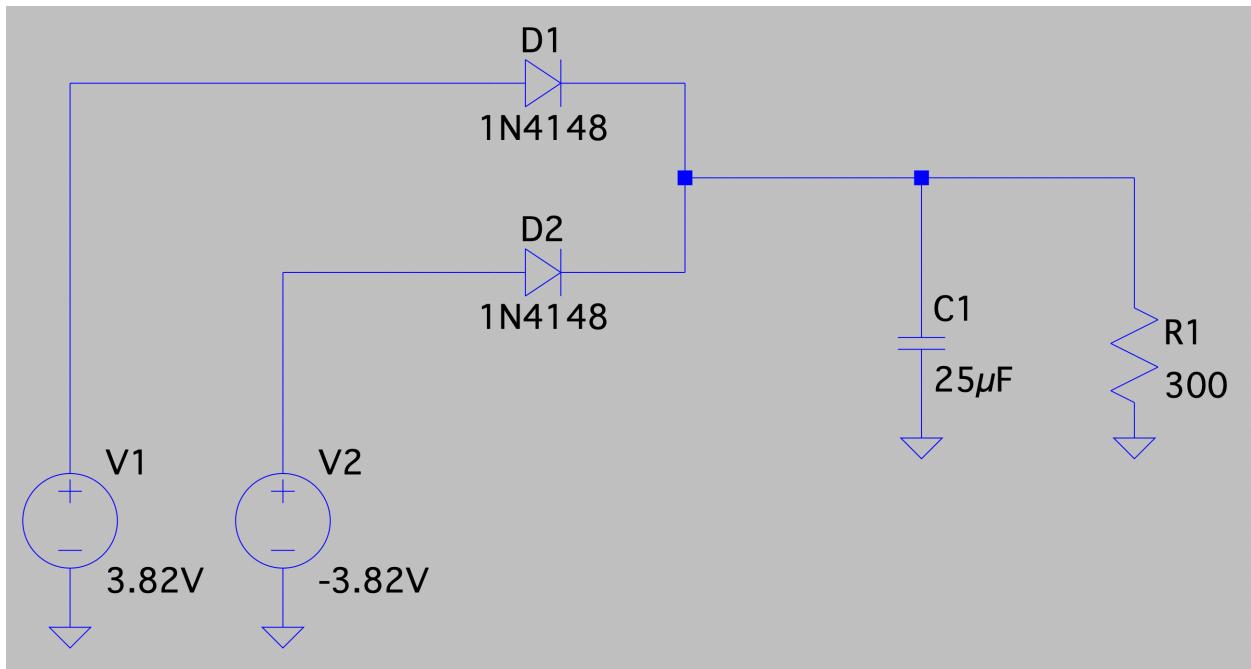


Figure 2: LTSpice Circuit Schematic

The screenshot shows the Draft1.net application window with the title "Draft1.net". The toolbar includes icons for zoom, selection, and search. A search bar at the top right contains the text "(normal)". The main area displays the LTSpice netlist:

```
*  
C1 N002 0 25μ  
V1 N001 0 SINE(0 3.82 1000)  
D1 N001 N002 1N4148  
D2 N003 N002 1N4148  
R1 N002 0 300  
V2 N003 0 SINE(0 -3.82 1000)  
.model D D  
.lib /Users/sapnasuthar/Library/Application Support/LTspice/lib/cmp/  
standard.dio  
.backanno  
.end
```

Figure 3: LTSpice Netlist

A transient simulation was performed, and data was recorded from 0ms to 10ms.

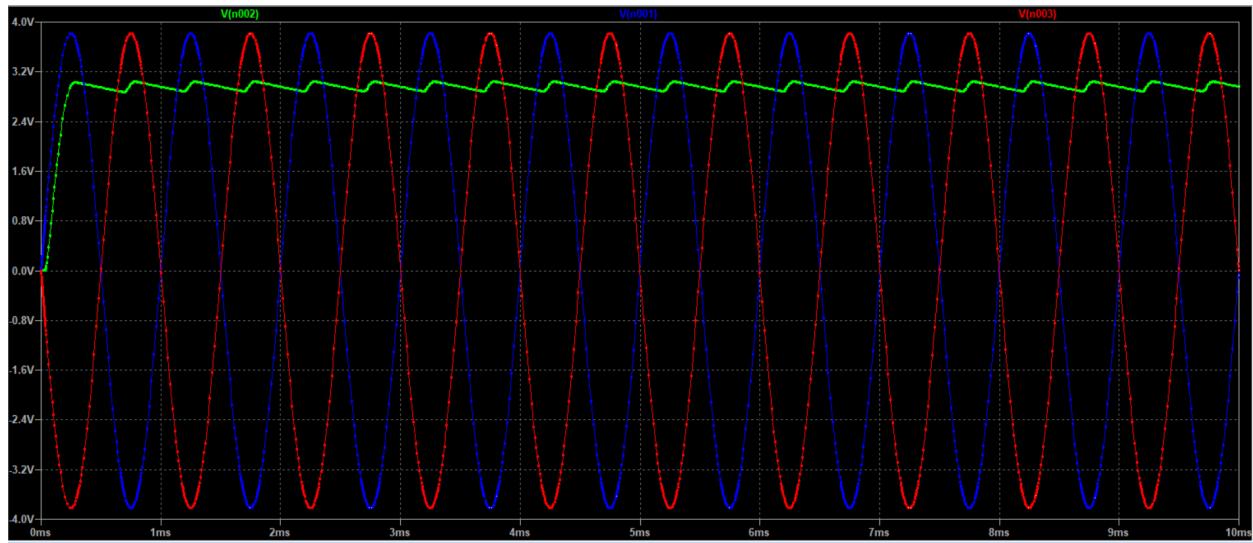


Figure 4: Graph of Input and Output Voltage

Based upon the graph of the output voltage, the output stays within the desired range of 2.9V to 3.1V. As seen in the graph, the input wave of 3.82V kept the output in range, however the ripple produced was larger than expected. To mitigate this a larger capacitance could be used.

## **Measurement and Analysis**

The circuit was built using components from the 2CI4 and 2EI4 kits.

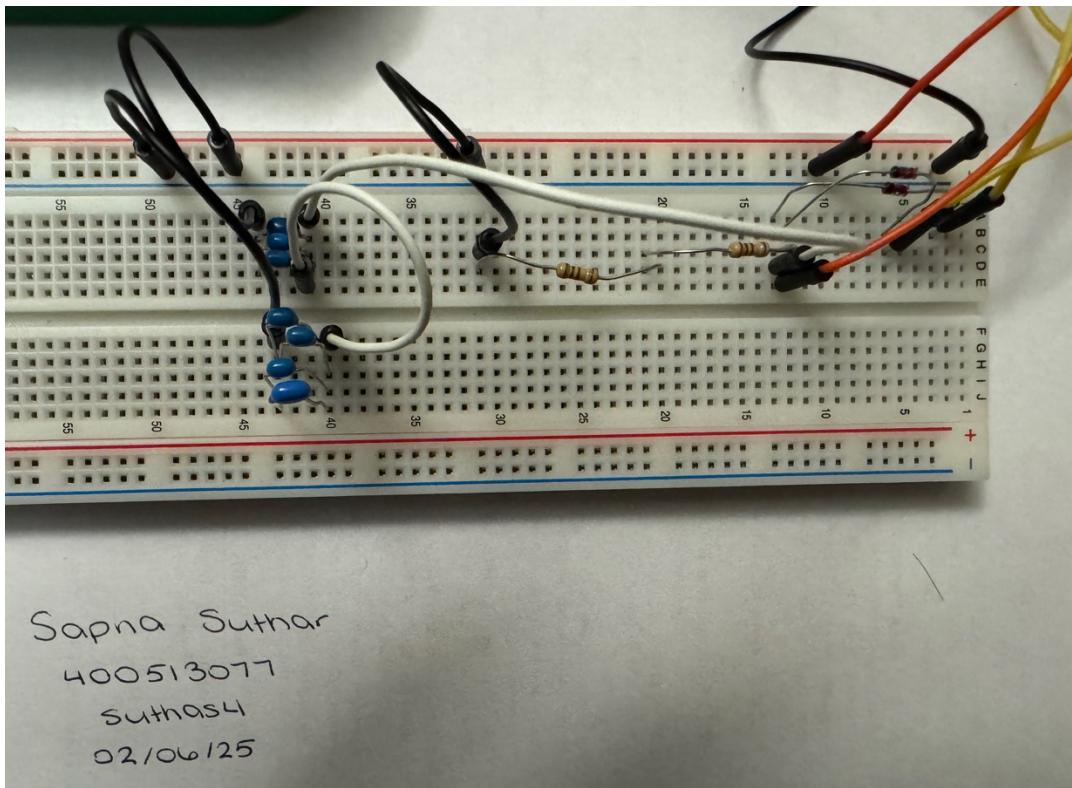
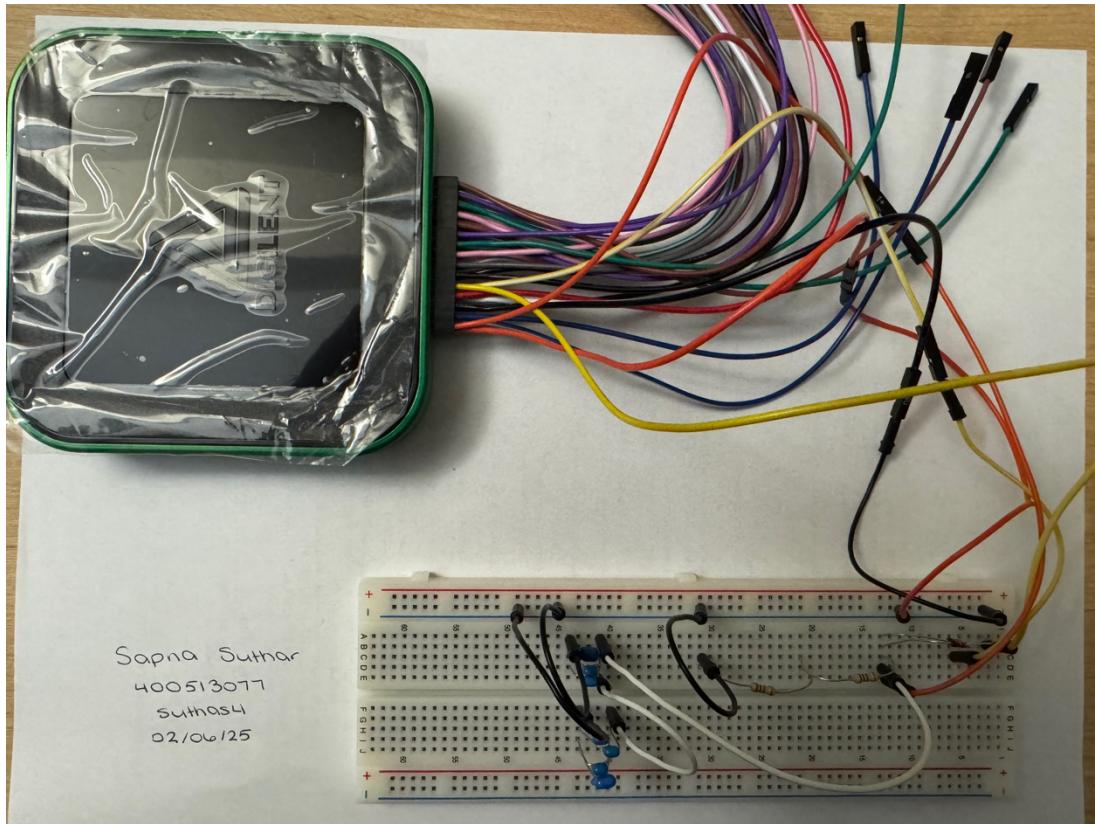


Figure 5: Built Circuit



*Figure 6: Built Circuit showing AD3 Connections*

To measure the performance of the circuit, the AD3 oscilloscope tool was used to graph the output voltage waveform. This was important to check for any errors in the circuit. The 1+ scope was attached to the breadboard at the node where the diodes, resistors and capacitors connect and the 1- scope was attached to ground. From there, the custom math function was used to display the current using Ohm's law.

When the circuit was graphed using the calculations from the above *Table 1*, there were some discrepancies from what was expected. For instance, the output voltage was not in the range of 2.9V to 3.1V. This could be caused by internal resistance in the wires and energy loss (became heat). As well, the chosen capacitance of 25uF was not enough to create a smooth voltage output. Instead, the outputted voltage had many large ripples.

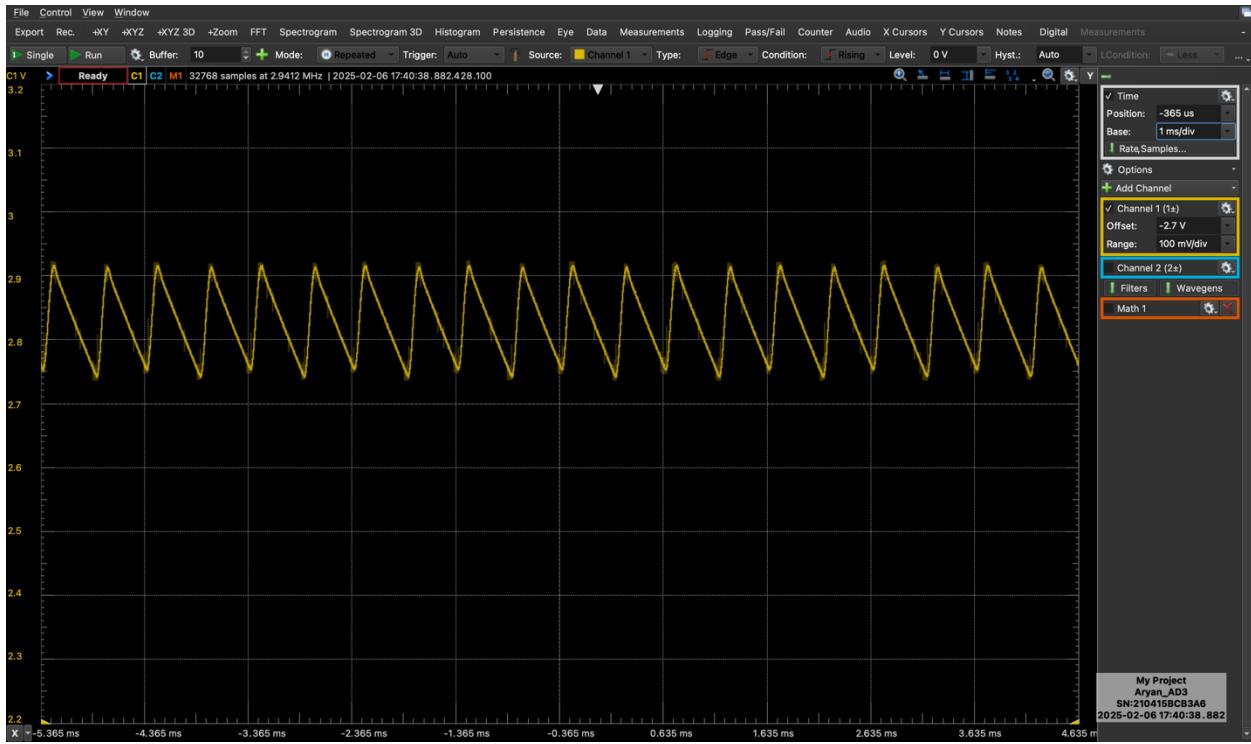


Figure 7: Output Voltage from Circuit Calculated Above

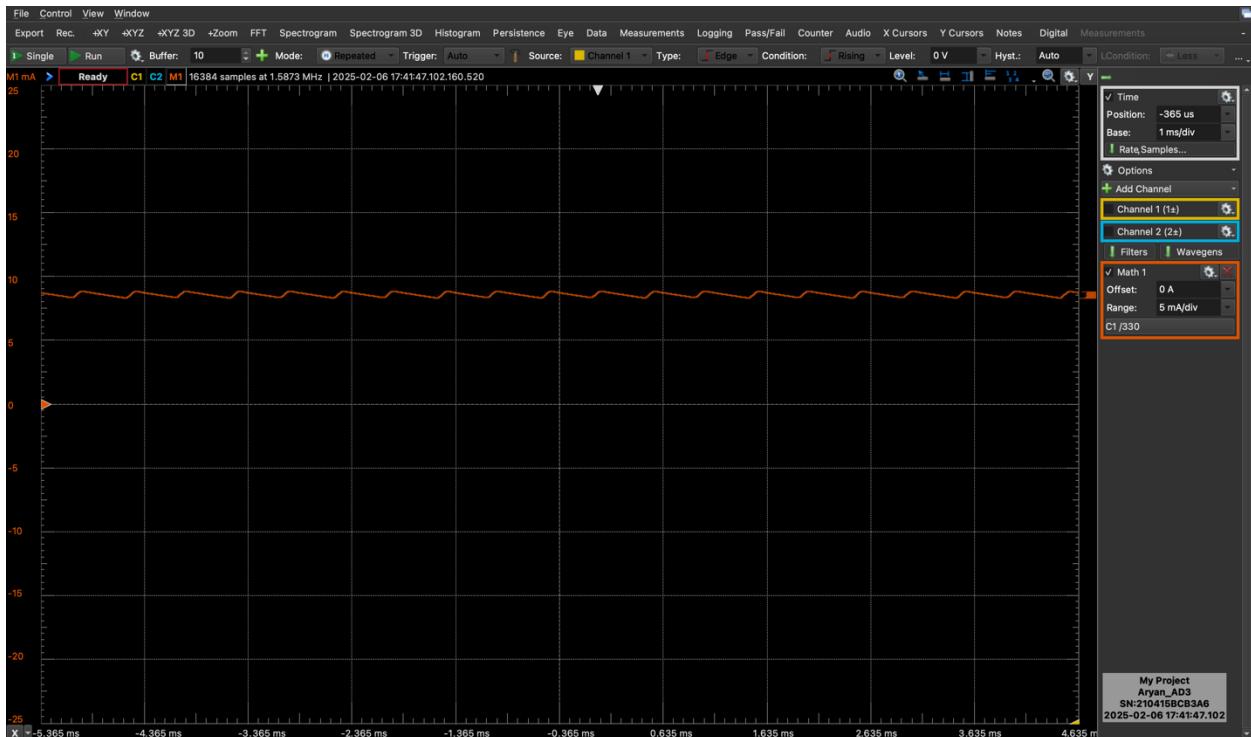


Figure 8: Output Current from Circuit Calculated Above

To mitigate the errors found in the initial circuit, some changes were made. Firstly, the input voltage was increased until it was within the specified bounds of 2.9V to 3.1V. In doing so, the

input voltage went from 3.82V to 3.94V. As well, the capacitance was increased from 25 $\mu$ F to 100 $\mu$ F to help mitigate the large ripple size. Lastly, the resistance was increased from 300 ohms to 330 ohms. This change in resistance helps to reduce the current draw, producing a higher output voltage. After making these changes, the graph of the output voltage and current fit within the parameters.

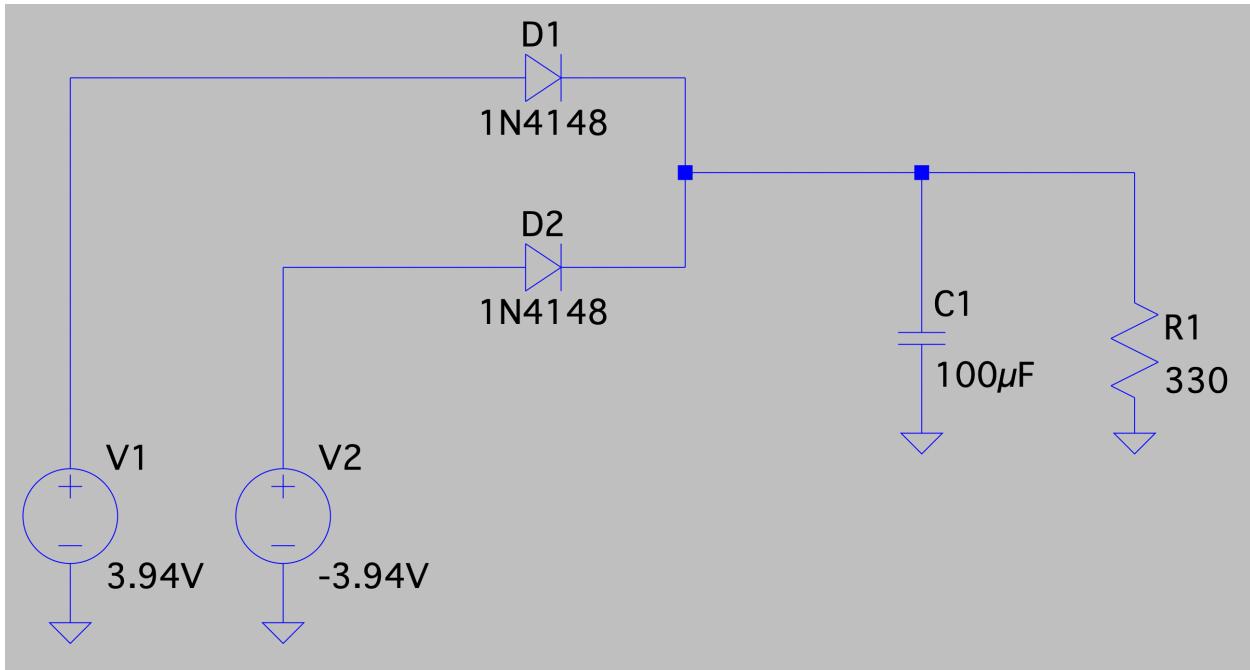


Figure 9: LTSpice Final Circuit Schematic

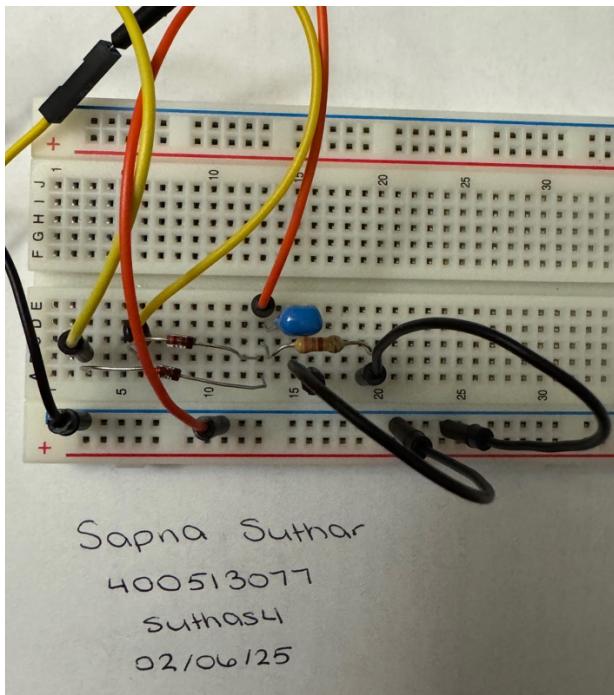


Figure 10: Final Built Circuit

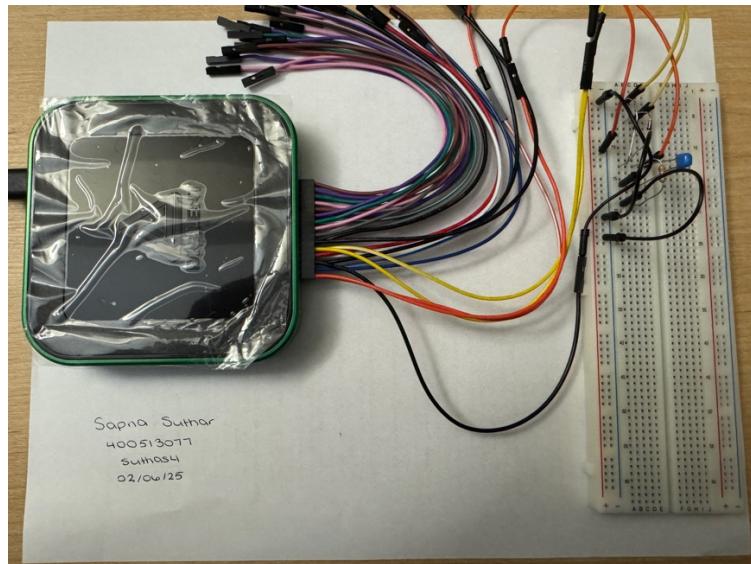


Figure 11: Final Built Circuit showing AD3 connections

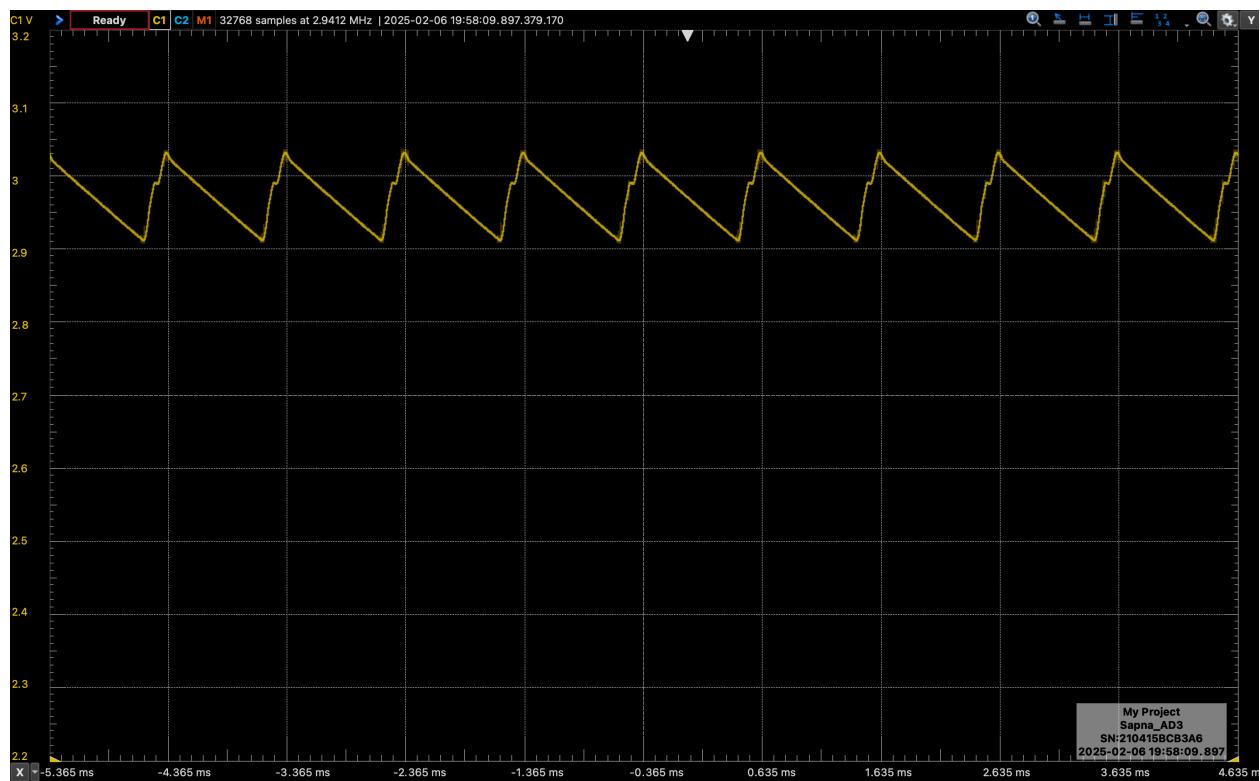


Figure 12: Final Circuit Output Voltage

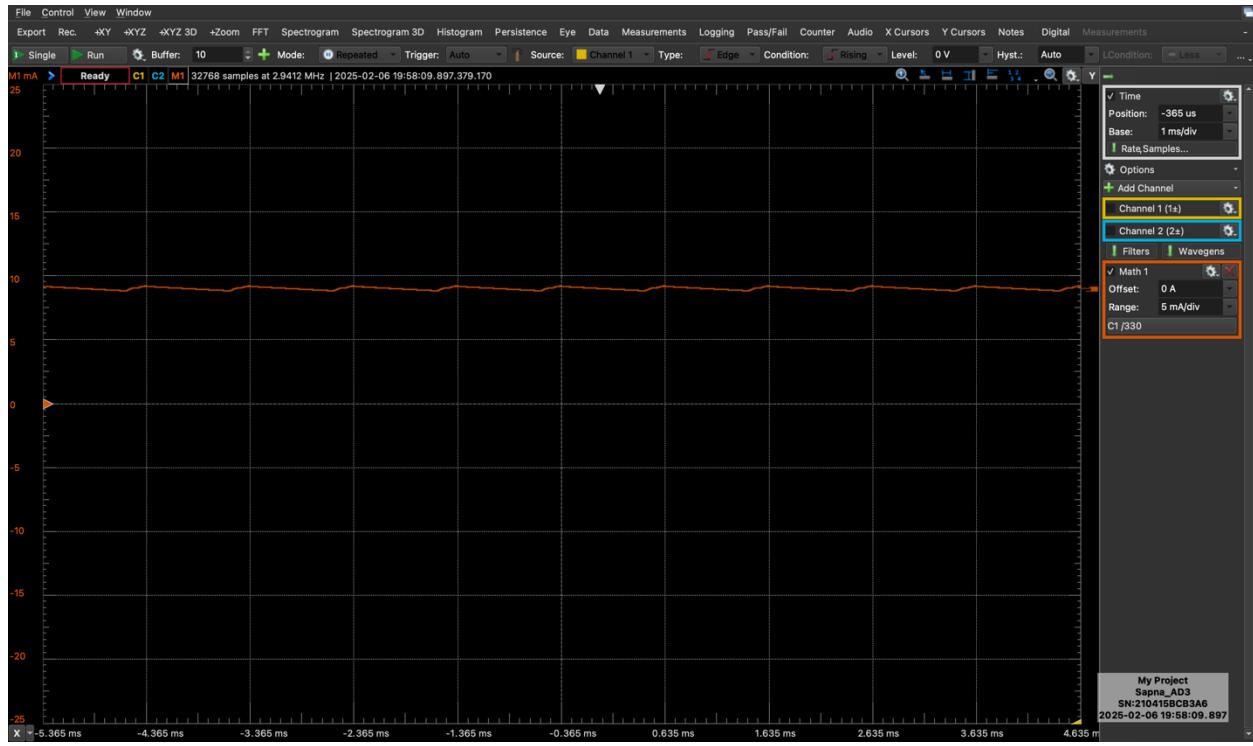


Figure 13: Final Circuit Output Current

## Discussion

### Results and Discrepancies

The largest discrepancy was found when comparing the LTSpice simulation graphs with the graphs produced by the AD3. The LTSpice simulation matched all calculations and fit within the range, as expected. However, the AD3 graphs were very different. Although the general shape of the output wave was similar, the expected range of the output voltage and size of the ripple were not as expected. This is because the simulation was done in an ideal scenario. Real-world factors were not considered, like internal resistance, component tolerances and energy loss. These discrepancies highlighted the importance of physically building circuits, as simulations are not always accurate.

Due to the discrepancies found between the simulating and AD3 graphs, the theoretical and actual values of all components were compared and adjusted. One of these discrepancies was the input waveform voltage. Based on the calculations, the input waveform was found to be 3.82V. However, the voltage had to be increased to 3.94V due to unaccounted for internal resistance from wires, components and the breadboard. Another discrepancy was found in the capacitors. When the circuit was simulated on LTSpice using a 25 $\mu$ F capacitor, a small ripple was shown. This was not the case when the physical circuit output voltage was graphed. Instead, a large ripple was seen, showing that the capacitance used was not enough to smooth the voltage output. Lastly, the resistance was increased from 300 ohms to 330 ohms. This change was necessary as it increased the current draw to create a greater voltage output. The two 150-ohm resistors were replaced with the 330-ohm resistor. After these changes were made, the circuit fit within the parameters of an output voltage of 2.9V to 3.1V.

## **Design Limitations**

The main limitation in this project was the components available were limited to those found in the 2CI4 and 2EI4 kits. To combat this, components were either put in series or parallel to create the necessary values.

## **Problems Encountered**

Many issues faced during the project were in relation to building the physical circuit. It took many components to equivilize to the calculated values. For example, to create the 25uF capacitor, two 10uF capacitors and five 1uF capacitors had to be used. Simply wiring this up became difficult as there were so many components that had to be put in parallel. Another issue encountered involved the AD3. Although the AD3 is very useful in creating the waveforms and measuring the output voltage, it is not the most accurate. When the circuit was first built, the expected waveform was incorrect. The input voltages were checked using the scope, before it was placed back at the node being measured. This seemed to fix the issue, and the expected waveform was outputted.

## **References**

- [1] A. S. Sedra, K. C. Smith, T. C. Carusone, and V. Gaudet, *Microelectronic circuits*, 8th ed. New York, NY: Oxford University Press, 2019.
- [2] YouTube, <https://www.youtube.com/watch?v=v6ZKVTdz07c> (accessed Feb. 9, 2025).
- [3] YouTube, <https://www.youtube.com/watch?v=Wq-QEDR3w0g> (accessed Feb. 9, 2025).