atom computing

ATOM COMPUTING FPGA CODING EXERCISE

Due: Two weeks after receipt of this document.

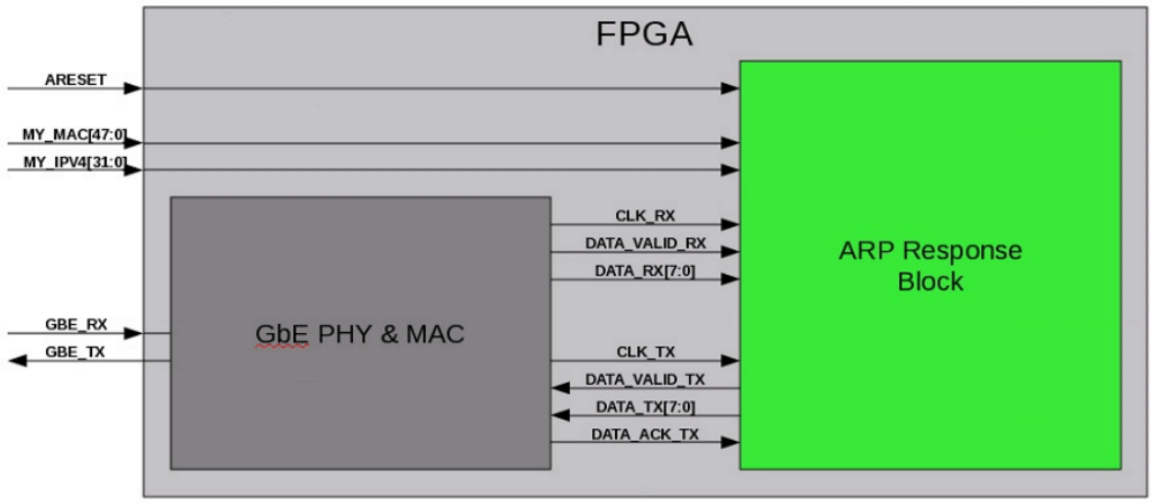
How to Submit: Create a merge request in the gitlab repo atom-fpga-<yourlastname>. You will receive a separate email with an invitation to access this repository. Write access will be revoked at midnight of the day following the due date of your submission.

You can download Vivado Web Edition here: https://www.xilinx.com/support/download.html Please use version Vivado 2020.1 or newer and be sure to specify which version you used in your submission.

Assignment: Design an ARP Response block in Verilog. Address Resolution Protocol (ARP) allows Layer 3 protocols such as IPv4 to discover the Layer 2 Ethernet MAC address of a networked device.

For example: PC A and PC B have Ethernet connections to the same IPv4 Local Area Network (LAN). PC A's IP address is 192.168.1.1 and PC B's IP address is 192.168.1.2. PC A must have PC B's Ethernet MAC address in order to route a data packet from PC A to PC B. PC A sends an ARP Request to PC B to 192.168.1.2. PC B will respond to the request with an ARP Response that contains its Ethernet MAC address.

For more details on the MAC interface, consult:
https://www.xilinx.com/support/documentation/user_guides/ug368.pdf



atom computing

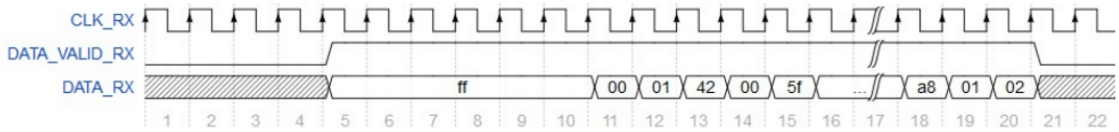
I/O Definitions

Port Name	Direction	Description
ARESET	Input	Active high, asynchronous reset
MY_MAC[47:0]	Input	MAC address for Ethernet port (static)
MY_IPV4[31:0]	Input	IPv4 address for Ethernet port (static)
CLK_RX	Input	Clock for DATA_RX and DATA_VALID_RX. This clock has a frequency of 125 MHz +/- 300 ppm and is recovered from GBE_RX input into the MAC
DATA_VALID_RX	Input	Ethernet frame data valid. Goes high when a valid Ethernet frame has been received and stays high for the entire duration of the received Ethernet frame (not including the Preamble, Start of Frame, or FCS bytes)
DATA_RX[7:0]	Input	Received Ethernet frame data (does not include Preamble, Start of Frame, and FCS bytes). Valid when RX_DATA_VALID is high.
CLK_TX	Input	Clock for DATA_VALID_TX, DATA_TX, and DATA_ACK_TX. Derived from an on-board oscillator. 125 MHz +/- 100 ppm
DATA_VALID_TX	Output	Ethernet frame data valid. Goes high when the first byte of the Ethernet frame begins to transmit. MAC responds with DATA_ACK_TX when it is ready to receive additional bytes.
DATA_TX[7:0]	Output	Transmit Ethernet frame data. Must be valid when DATA_VALID_TX is high.
DATA_ACK_TX	Output	Acknowledgement signal from the Ethernet MAC that goes high when MAC is ready to receive additional DATA_TX bytes. Stays high only for a single clock cycle.

Timing Diagram for ARP Request

ARP Request

0x00:	ff	ff	ff	ff	ff	ff	00	01	42	00	5f	68	08	06	00	01
0x10:	08	00	06	04	00	01	00	01	42	00	5f	68	c0	a8	01	01
0x20:	00	00	00	00	00	00	c0	a8	01	02						



Timing Diagram for ARP Response

ARP Response

0x00:	00	01	42	00	5f	68	00	02	23	01	02	03	08	06	00	01
0x10:	08	00	06	04	00	02	00	02	23	01	02	03	c0	a8	01	02
0x20:	00	01	42	00	5f	68	c0	a8	01	01