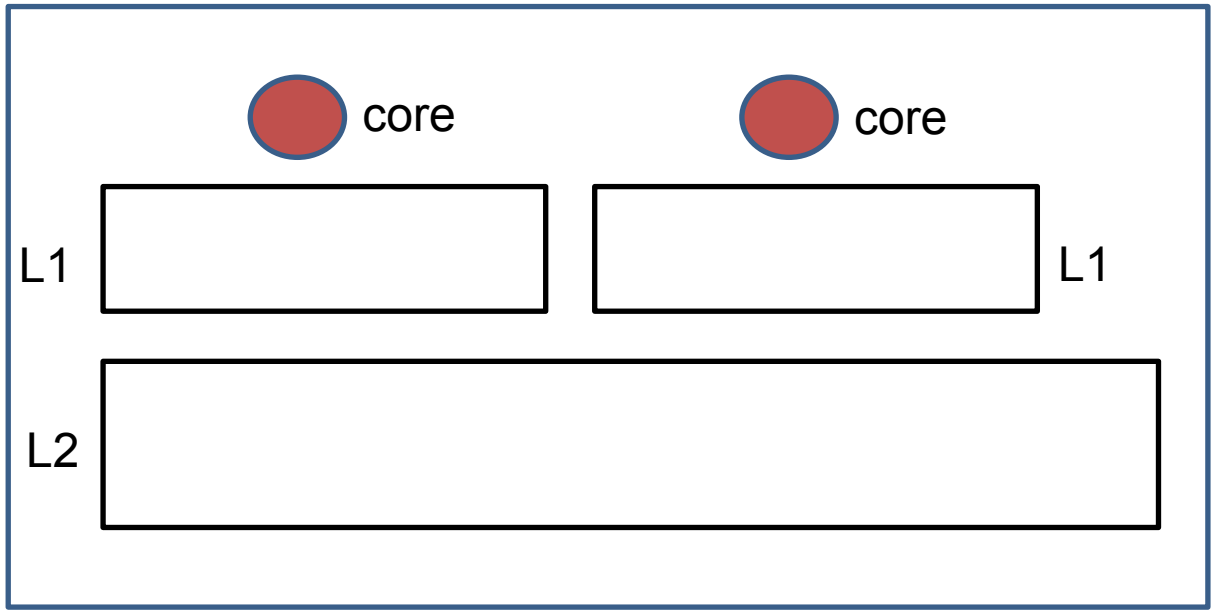
CS531: Memory Systems and Architecture
Jan-Apr 2022

Dr. Shirshendu Das
Assistant Professor,
Department of CSE
IIT Ropar.

Topic: Cache Coherence Protocols

Cache Coherence

- **Important Terms:**
  1. Cache Block.
  2. Private/Shared Cache
  3. Multiprogramed/Multithreaded Applications.
  4. Replacement Policies.
  5. Cache Structure



Multicore Processor

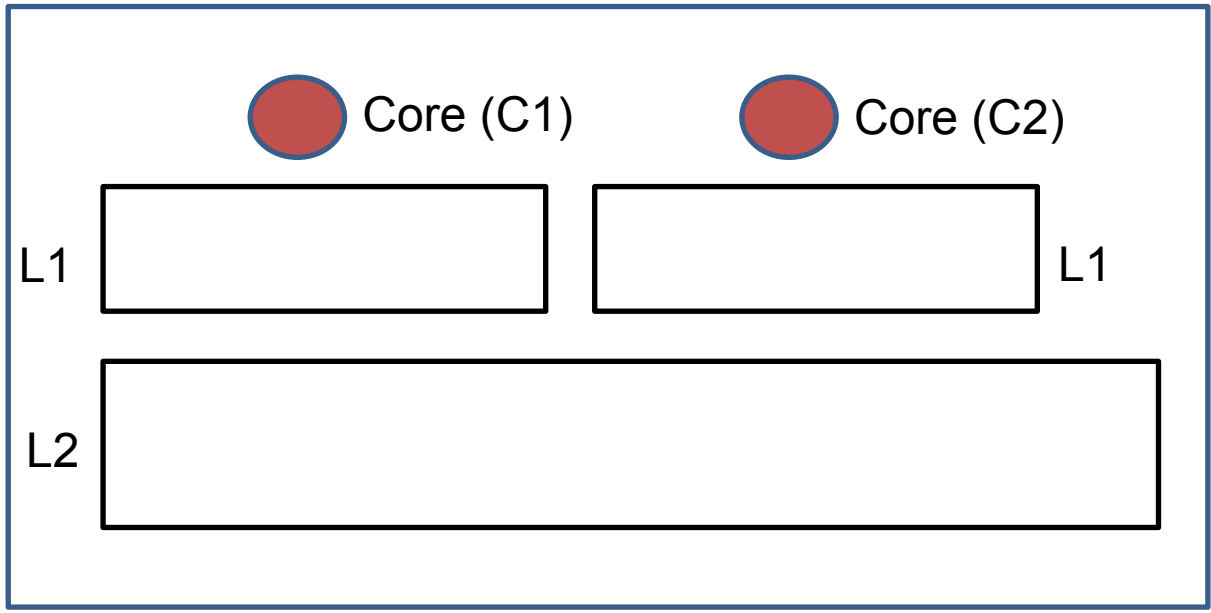
- **Important Assumptions:**
  1. The cache structure is set-associative.
  2. The replacement policy is LRU.
  3. There are two cores C1 and C2.
  4. Each core has private L1 cache.
  5. Both core share a common L2 cache.
  6. Both core runs a multithreaded application.

- **More Assumptions:**
  1. Let us assume that all the set-associative cache in this diagram have only one set.

Cache Coherence:
MSI Protocol

Cache Block State: M, S, and I

Events: GETS, GETX, UPGRADE, PUTX, REPLACE, REPLACE_CLEAN



Multicore Processor

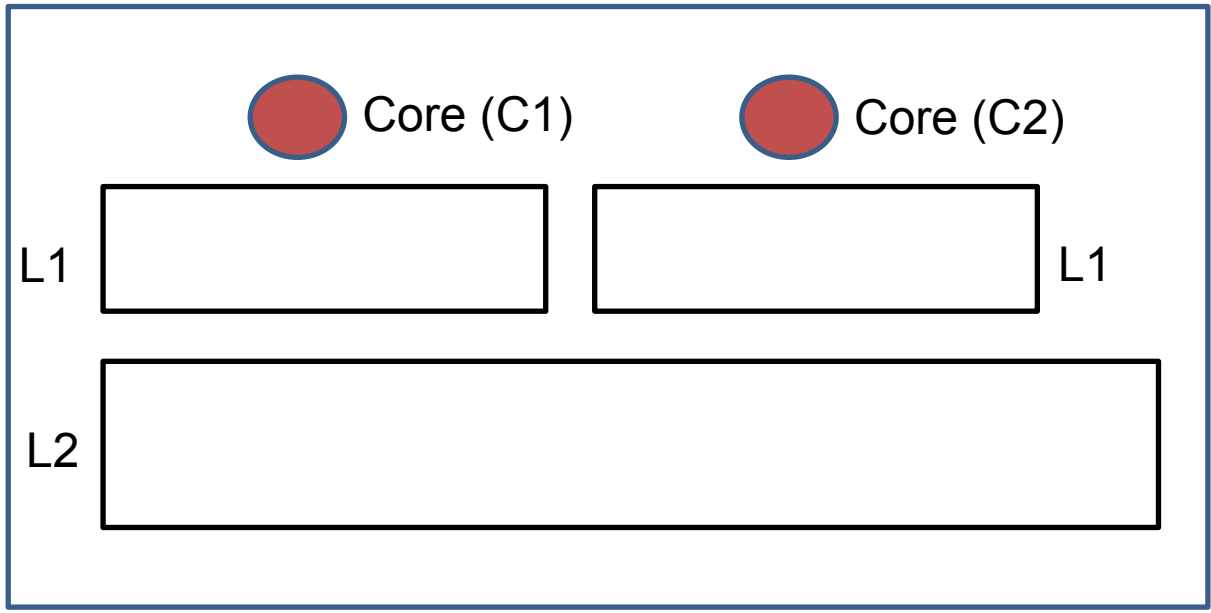
Inclusive vs Exclusive Cache setup.

Cache Coherence:
MSI Protocol

Cache Block State: M, S, and I

Events: GETS, GETX, UPGRADE, PUTX, REPLACE, REPLACE_CLEAN

Curr State	Event
I	GETS
I	GETX
I	Other
S	GETS
S	GETX
S	UPGRADE
S	PUTX
M	GETS
M	GETX
M	UPGRADE
M	PUTX



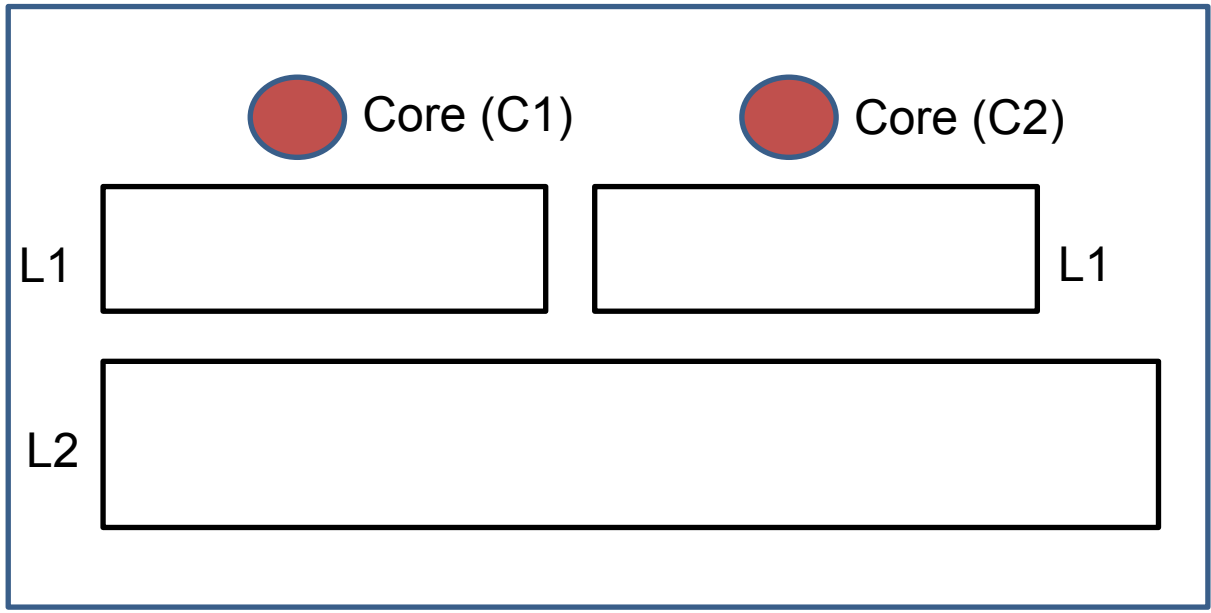
Multicore Processor

Cache Coherence:
MSI Protocol

Cache Block State: M, S, and I

Events: GETS, GETX, UPGRADE, PUTX, REPLACE, REPLACE_CLEAN

Curr State	Event
I	GETS
I	GETX
I	Other
S	GETS
S	GETX
S	UPGRADE
S	PUTX
M	GETS
M	GETX
M	UPGRADE
M	PUTX



Multicore Processor

Curr State	Event
S	REPLACE
S	REPLACE_CLEAN
M	REPLACE
M	REPLACE_CLEAN

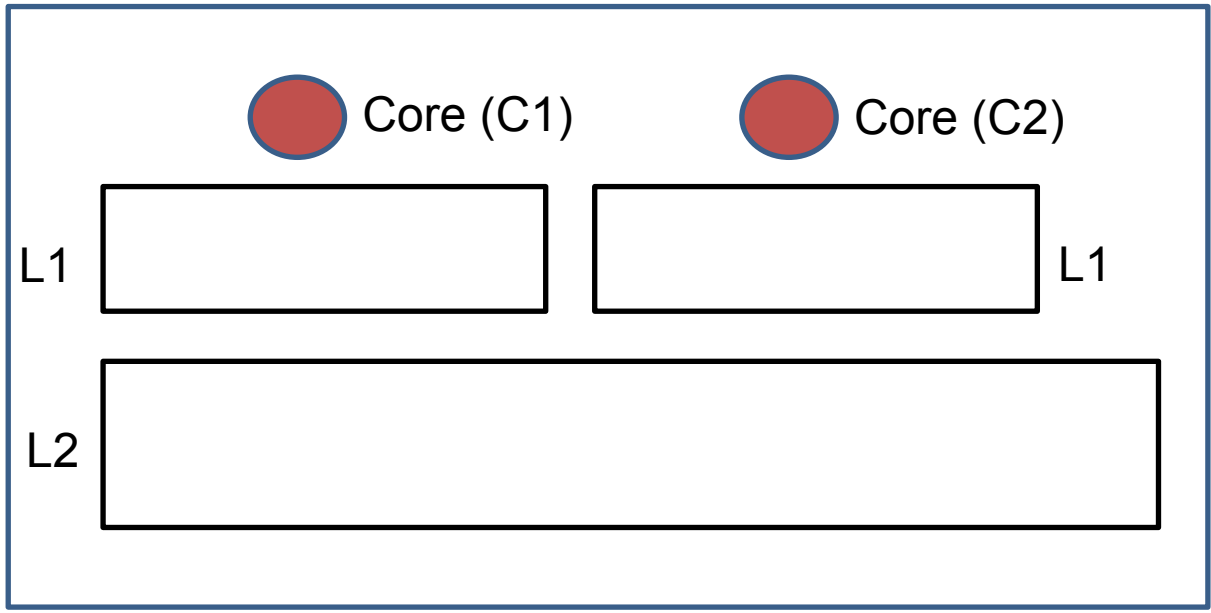
Cache Coherence: MSI Protocol

More states/event are required.

Cache Block State: M, S, and I

Events: GETS, GETX, UPGRADE, PUTX, REPLACE, REPLACE_CLEAN

Curr State	Event
I	GETS
I	GETX
I	Other
S	GETS
S	GETX
S	UPGRADE
S	PUTX
M	GETS
M	GETX
M	UPGRADE
M	PUTX



Multicore Processor

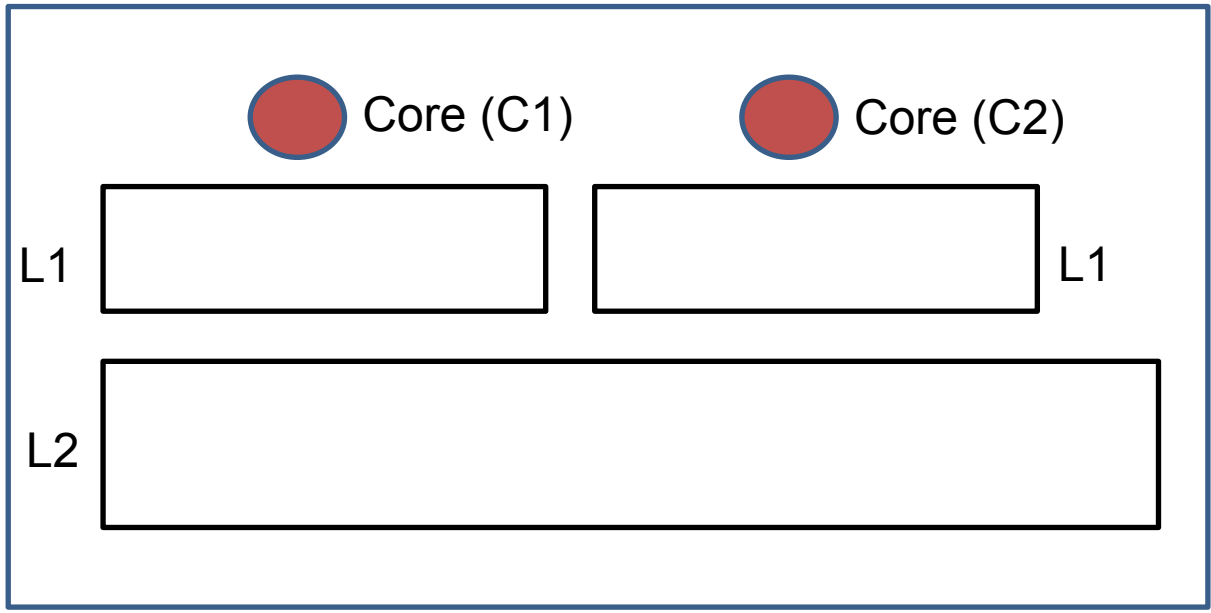
Cache Coherence: MSI Protocol

More states/event are required.

Cache Block State: M, S, and I

Events: GETS, GETX, UPGRADE, PUTX, REPLACE, REPLACE_CLEAN

Curr State	Event
S	REPLACE
S	REPLACE_CLEAN
M	REPLACE
M	REPLACE_CLEAN

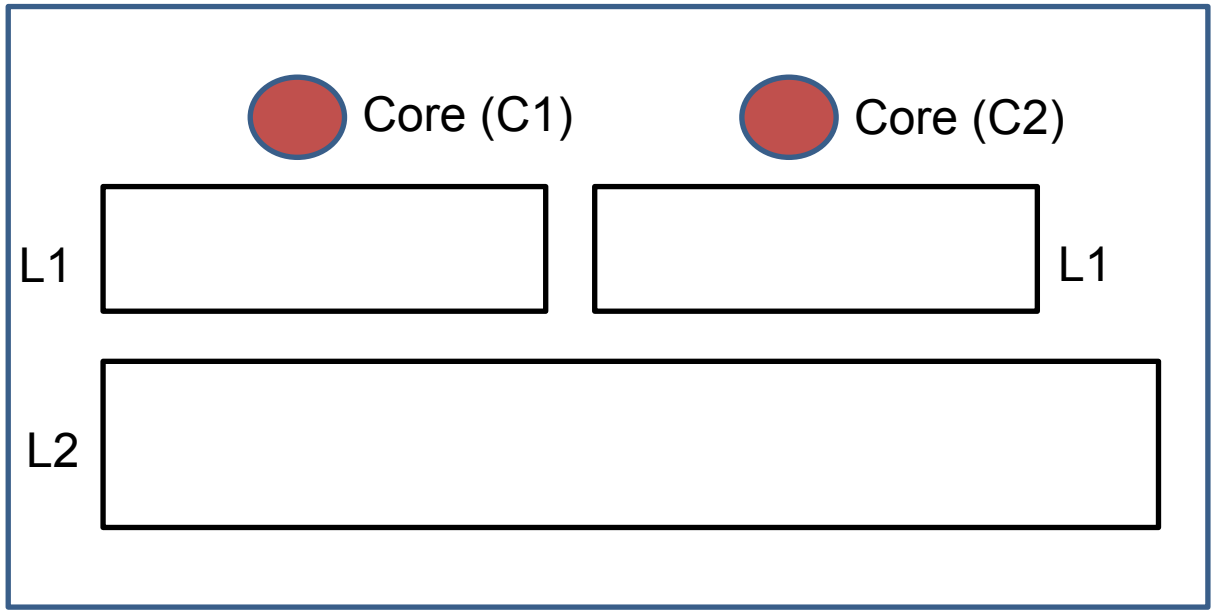


Multicore Processor

Cache Coherence:
MESI Protocol

Cache Block State: M, E, S, and I

Events: GETS, GETX, UPGRADE, PUTX, REPLACE, REPLACE_CLEAN



Multicore Processor

Important Resources for Cache Coherence

1. Hennessy and Patterson, "***Computer Architecture A Quantitative Approach***", Fourth edition, 2007.
2. Gem5 Documentation: https://www.gem5.org/documentation/general_docs/ruby/

Thank You