Compressive Sensing Architecture for Gray Scale Images

Link :- https://link.springer.com/content/pdf/10.1007%2F978-3-319-13647-9_32.pdf

Abstract:
The paper proposes a CS architecture implemented in an FPGA platform for 128 × 128 gray scale images. A Unit Control (UC) based on a Mealy type state machine directs operations in this architecture. First, the UC uses the Universal Asynchronous Receiver Transmitter (UART) to receive the sample image and store it in the corresponding RAM block. Second, the UC directs the matrix multiplication operation to the ALU and obtains the compressed image. Finally, the UART transmits the compressed image to a base station. The main characteristics of our architecture are the following: the maximum frequency of operation is 30 MHz, the power consumption is 37 mW, and the average time processing is 4.5 ms.

Equations:
Similar to CS theory studied in class
$y = \Gamma s$ where $\Gamma = \Phi\Psi$ is called random sensing matrix with size $K \times N$.
Usually, each entry for the matrix is a random variable with either uniform or normal distribution and variance 2/K.

The main building blocks of the architecture:

1. ALU to perform mathematical operations synthesized using look ahead kin VHDL to improve the speed.
2. Image Memory - to store the raw gray scale image where each pizel represented by 8 bit word
3. Frame Memory - to store the measurement matrix where the entries of random sensing matrix can be +1 or -1. In start, RAM memory is set to 1 and then random numbers are generated by random generator block using Linear Feedback Shift Register (LFSR) technique to specify the positions where value 1 should be substituted by -1.
4. Multiplication Block - consists of multiplier blocks and adders. Here each row of the matrix Φ is multiplied by the column vector x. Subsequently, the corresponding compressed coefficients are obtained by adding the resulting vector. The so generated compressed vector is then transmitted by UART.
5. UART - to receive and transmit data

ASM Chart:
Algorithmic State Machine for Compress Sensing :
Reset registers and memories and store the random matrix Φ.
The UART block receives the gray scale image x from a second device using serial protocol.The compressed samples are obtained by means of the product Φx and the compressed vector y is stored in RAM memory. Finally, the vector y is transmitted to the second device.

In this process, the original images with 2^14 samples is reduced to 1000 samples. This means, we have a compression ratio of 0.061

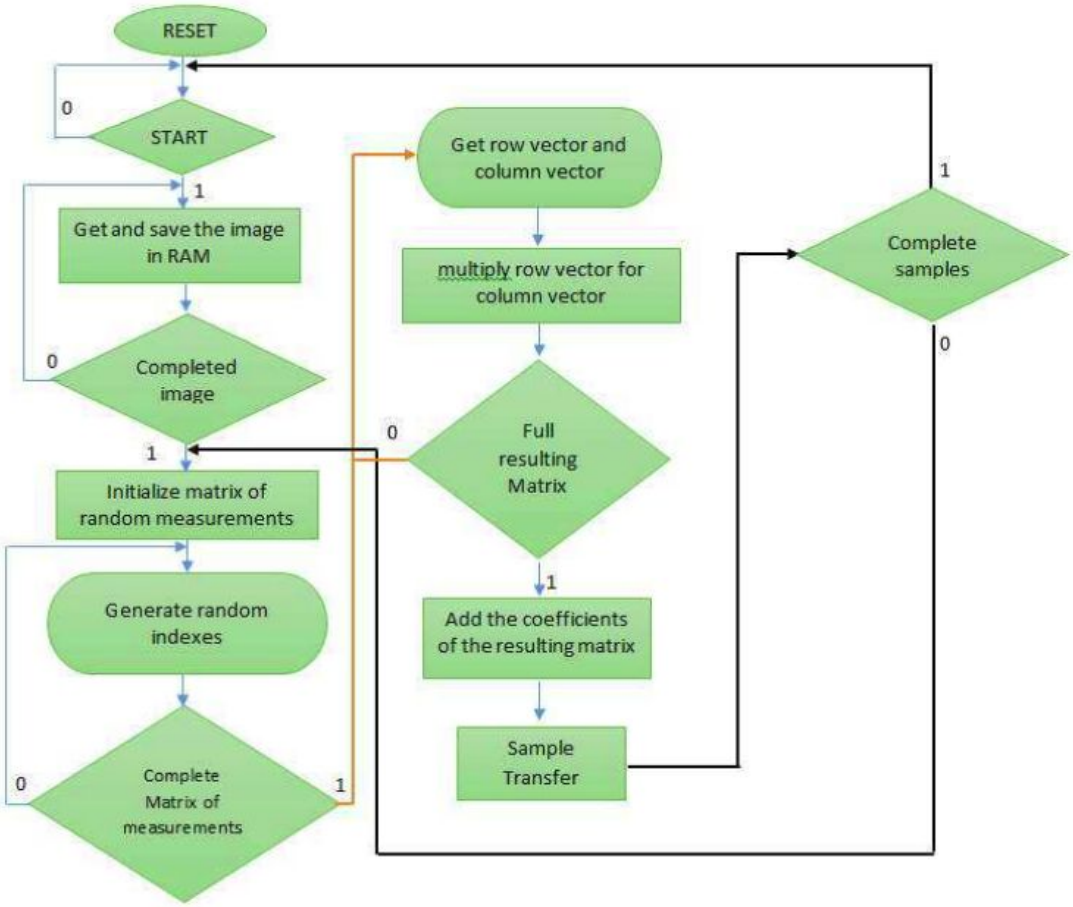

Fig. 3. ASM chart

Results:

Synthesis results of the proposed architecture and optimization analysis:

Total combinational functions - 13355 → It directly affects the total area.
Dedicated logic registers - 12014
Embedded Multiplier elements - 0
Maximum Frequency - 30 MHz
Core Static Thermal Power Dissipation - 102 mW
Thermal Power Dissipation - 37 mw
Execution time of the algorithm - 4.5 ms