Design flow for MultiCycle RISC-IITB

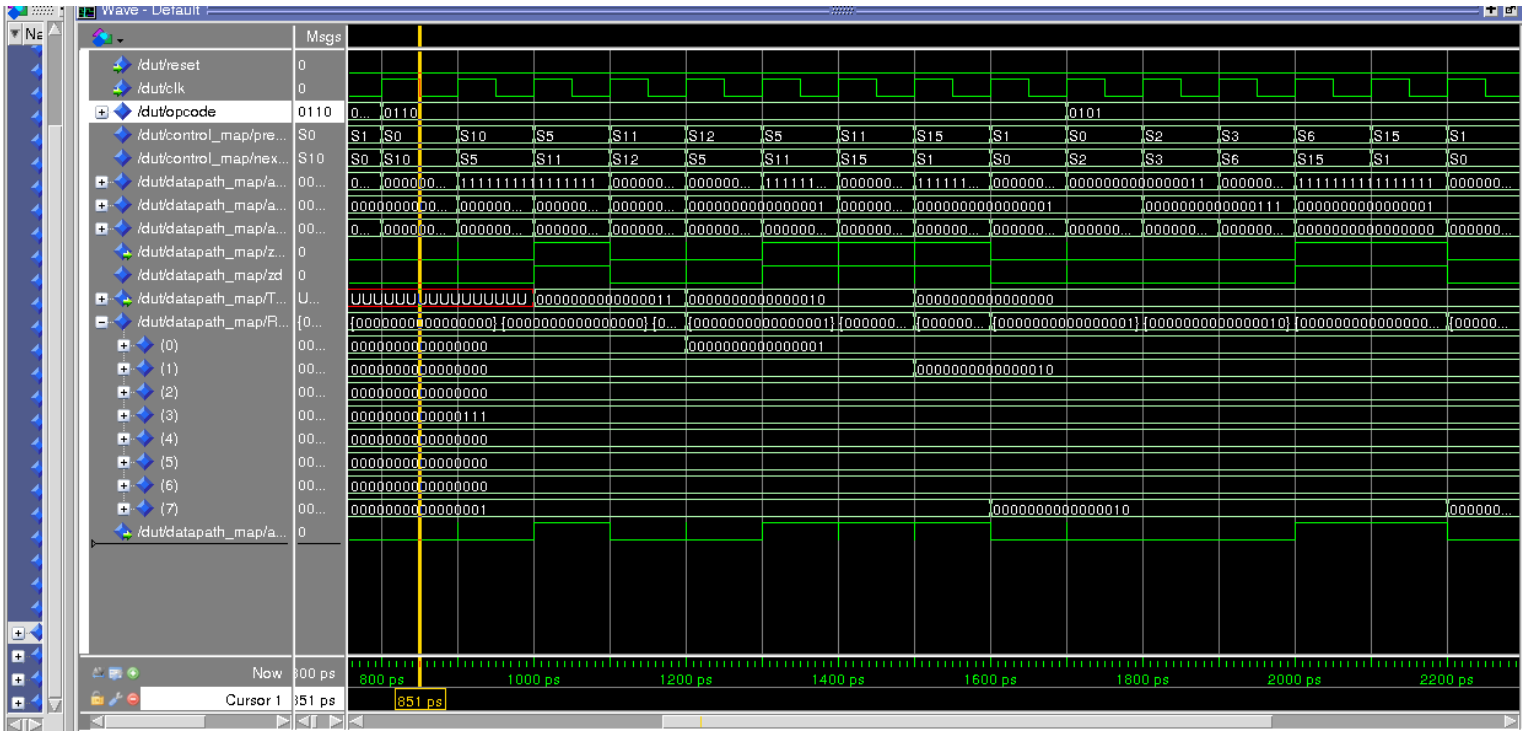
Our entire project includes four files:

1) datapath_components.vhd – This includes all of our entity components for example ALU, MUX, Register Files, registers, Memory, priority Encoder, zero decoder, Left Shifter, Extender etc. These entities are included in a library package which is further used in other files.

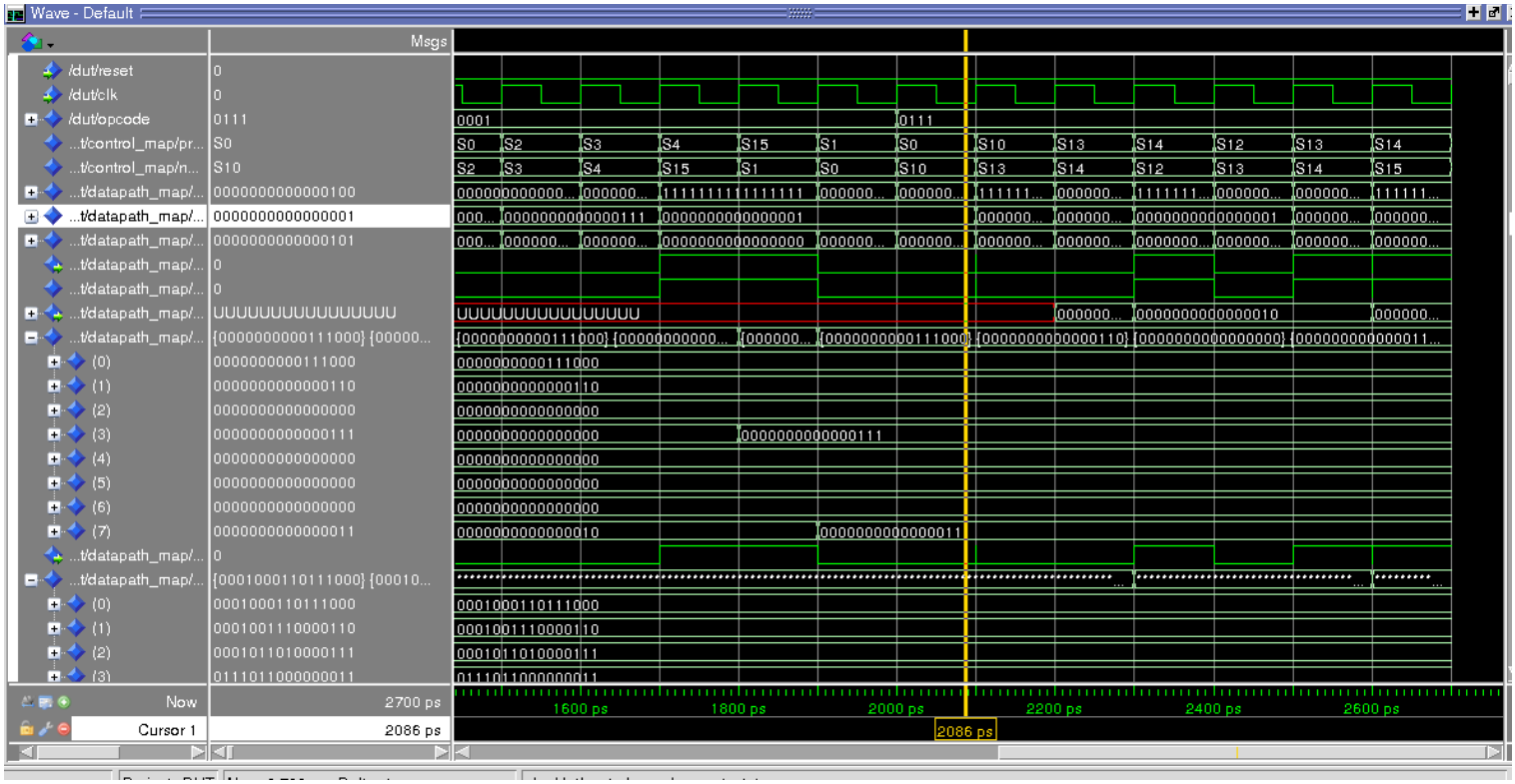
2) datapath.vhd – The datapath lays out the entire flowgraph of our RISC design. It includes all the connections between various instances of components.

3) controlpath_fsm.vhd – This file implements the FSM and the next state logic as well as generates the values of the control pins which are required by the datapath .

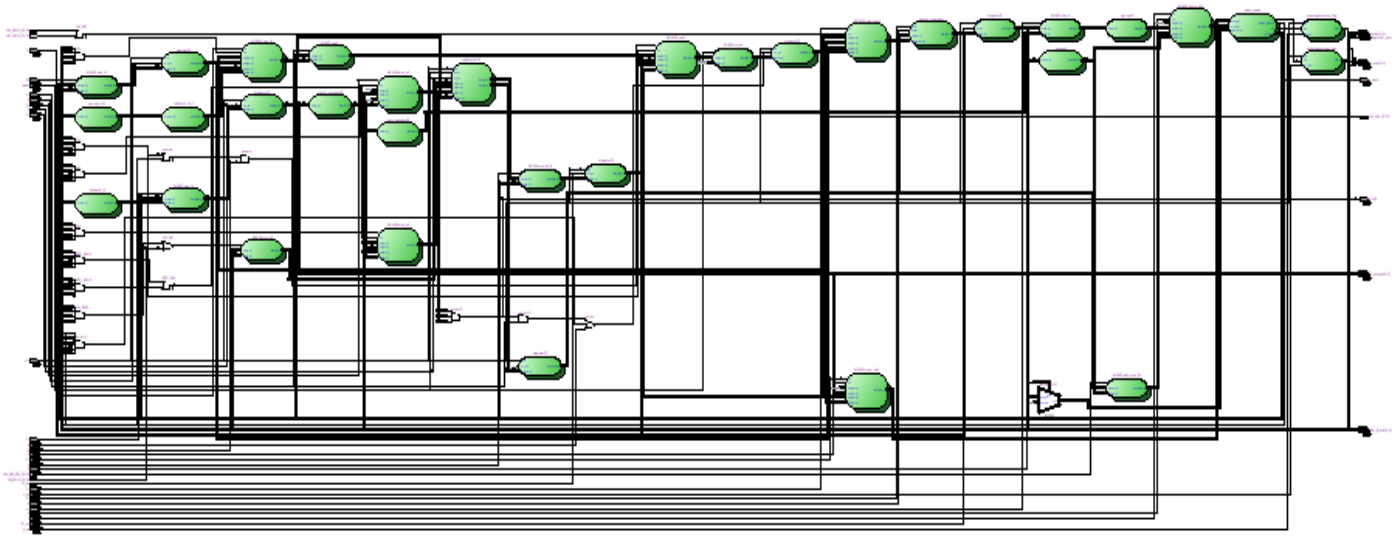
4) DUT.vhd – The DUT is the top-level entity which maps the pins of the control_path and the datapath.



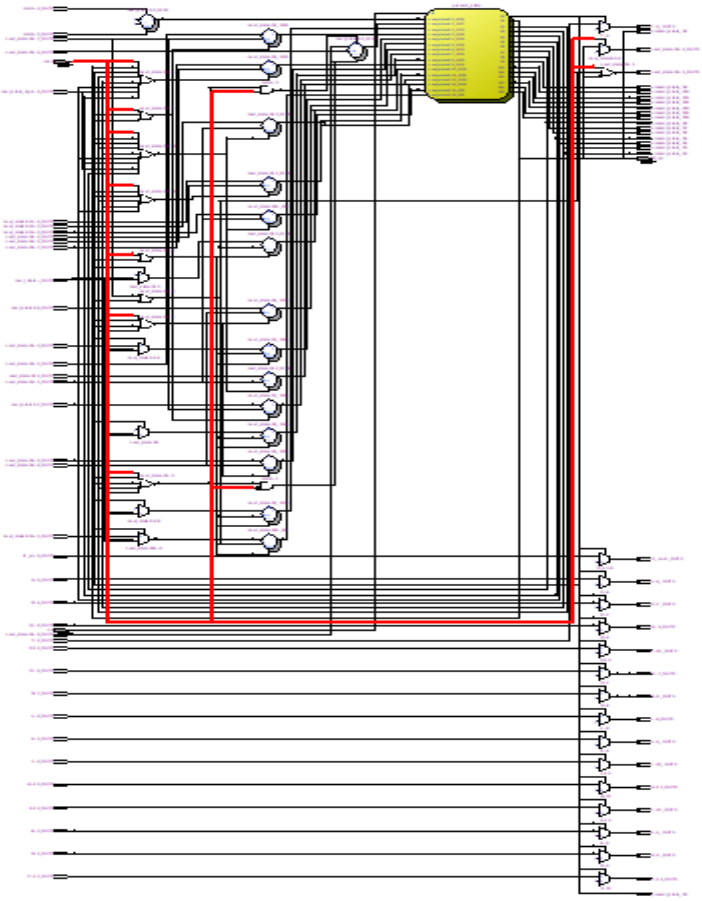
Simulation for LM



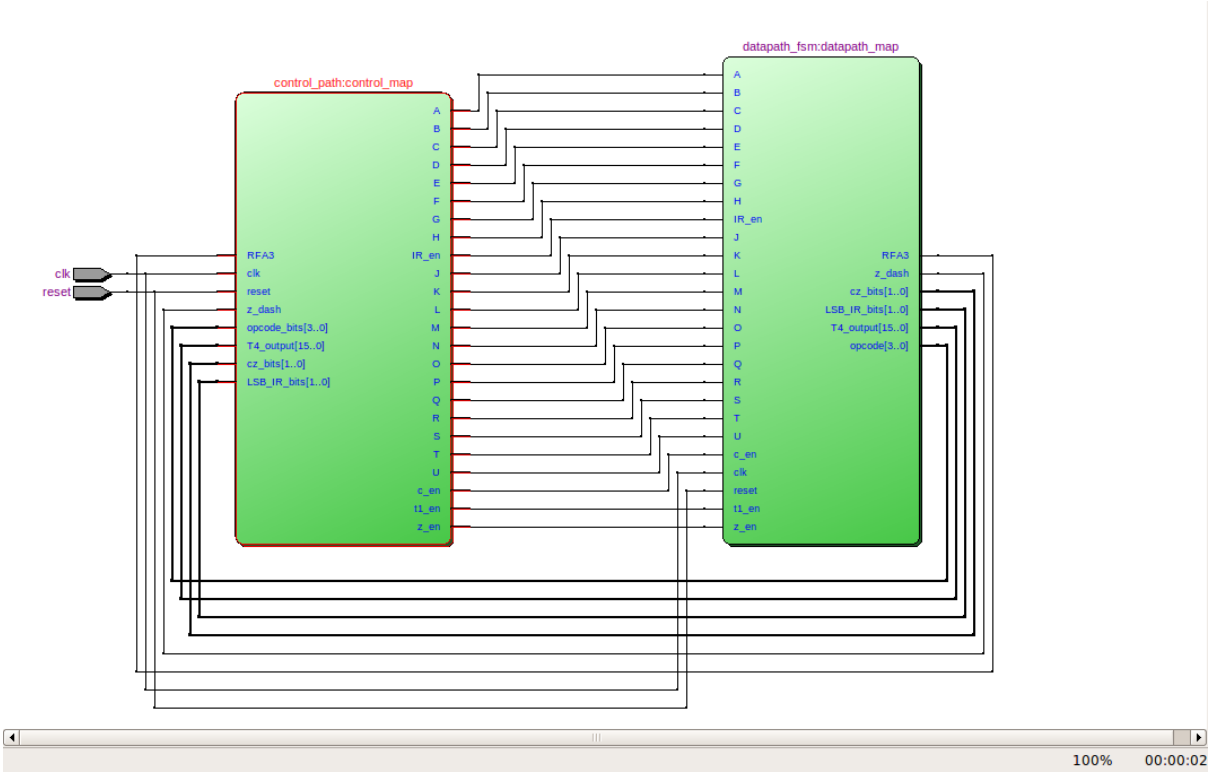
Simulation for SM



Datapath



Control Path



DUT

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Github Link:

Link to Github Repo

https://github.com/saqib1707/Sem-5/tree/master/Microprocessors-Lab/Multicycle-RISC-IITB