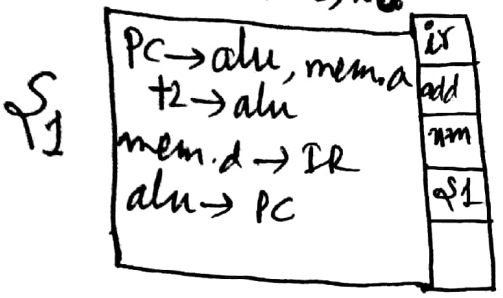
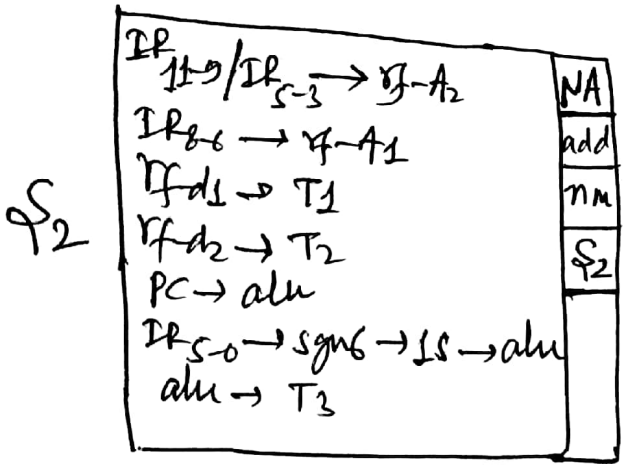
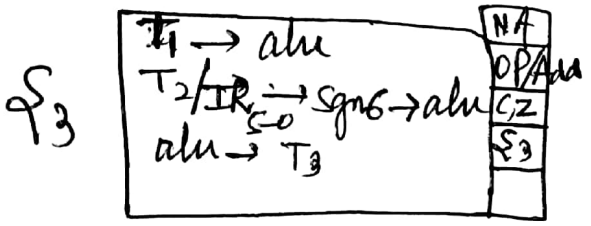
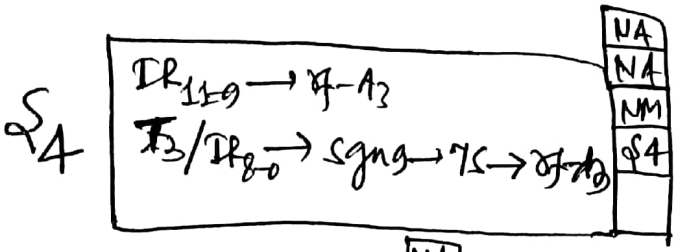
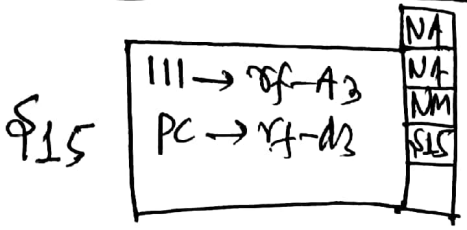
(1) ADD Rc, Ra, Rb



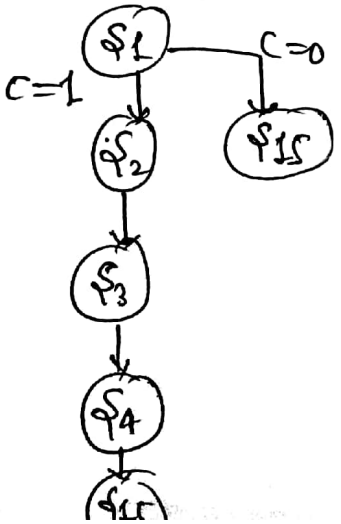




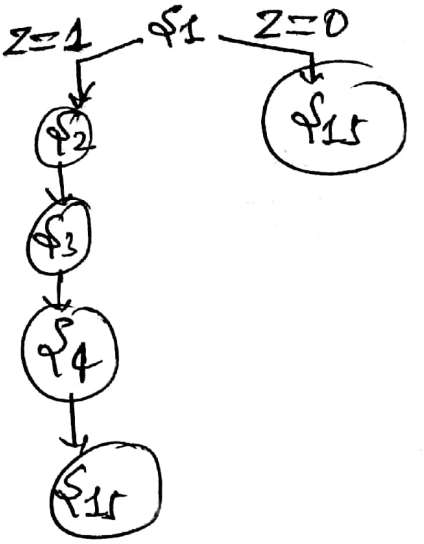




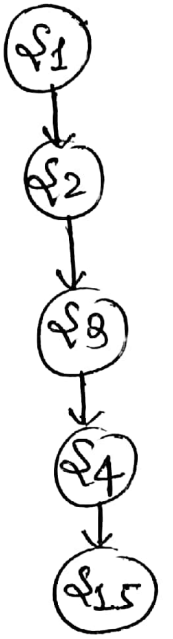
(2) ADC Rc, Ra, Rb



(3) ADZ Rc, Ra, Rb

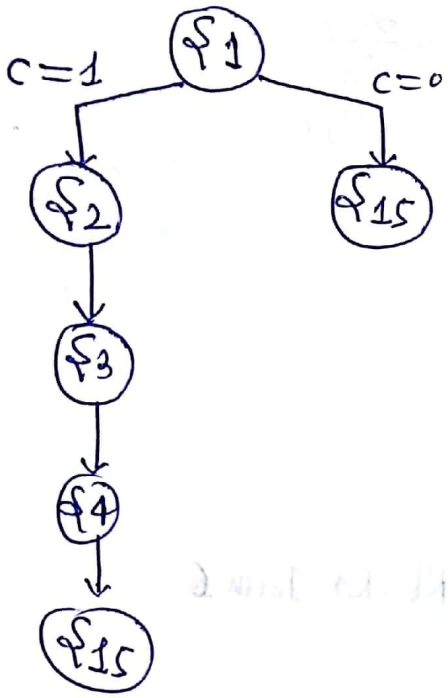


(4) ADI Rb, Ra, Imm6

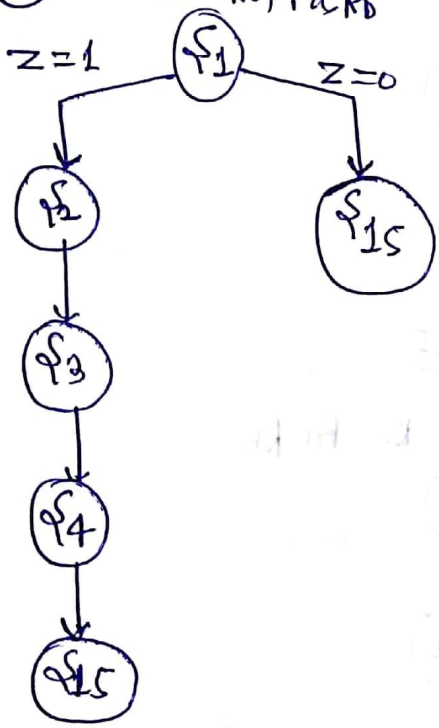


(5) NDU Rc, Ra, Rb

6. NDC Rc, Ra, Rb

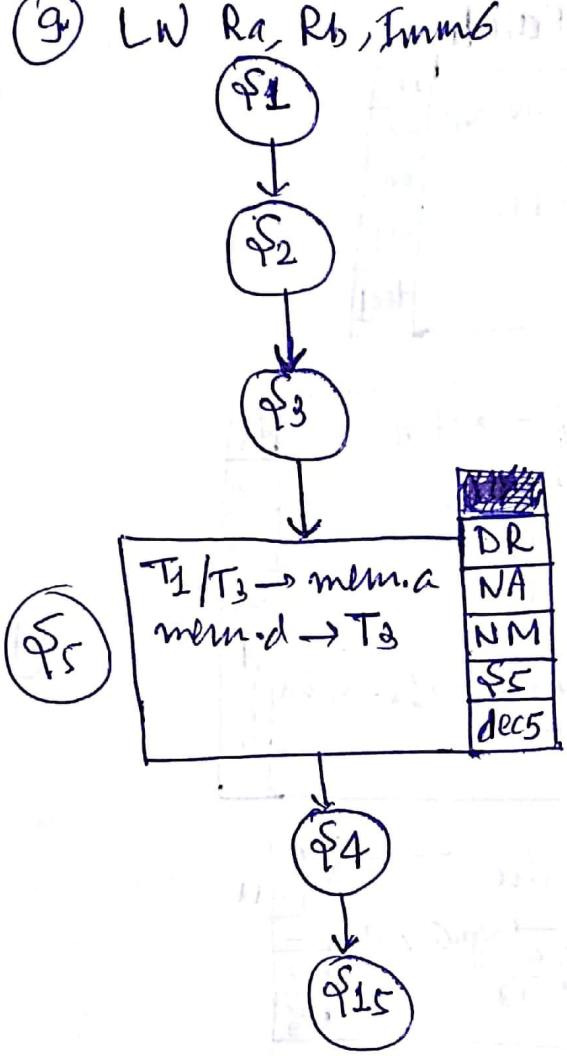


7. NDZ Rc, Ra Rb

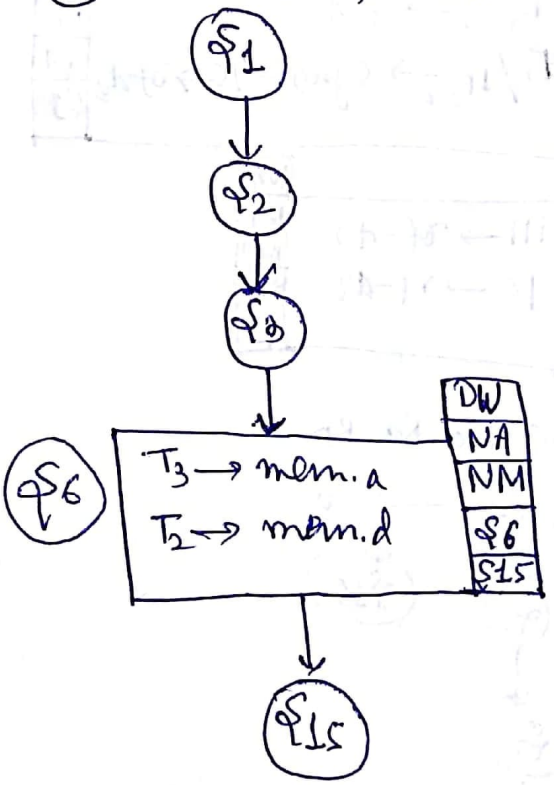


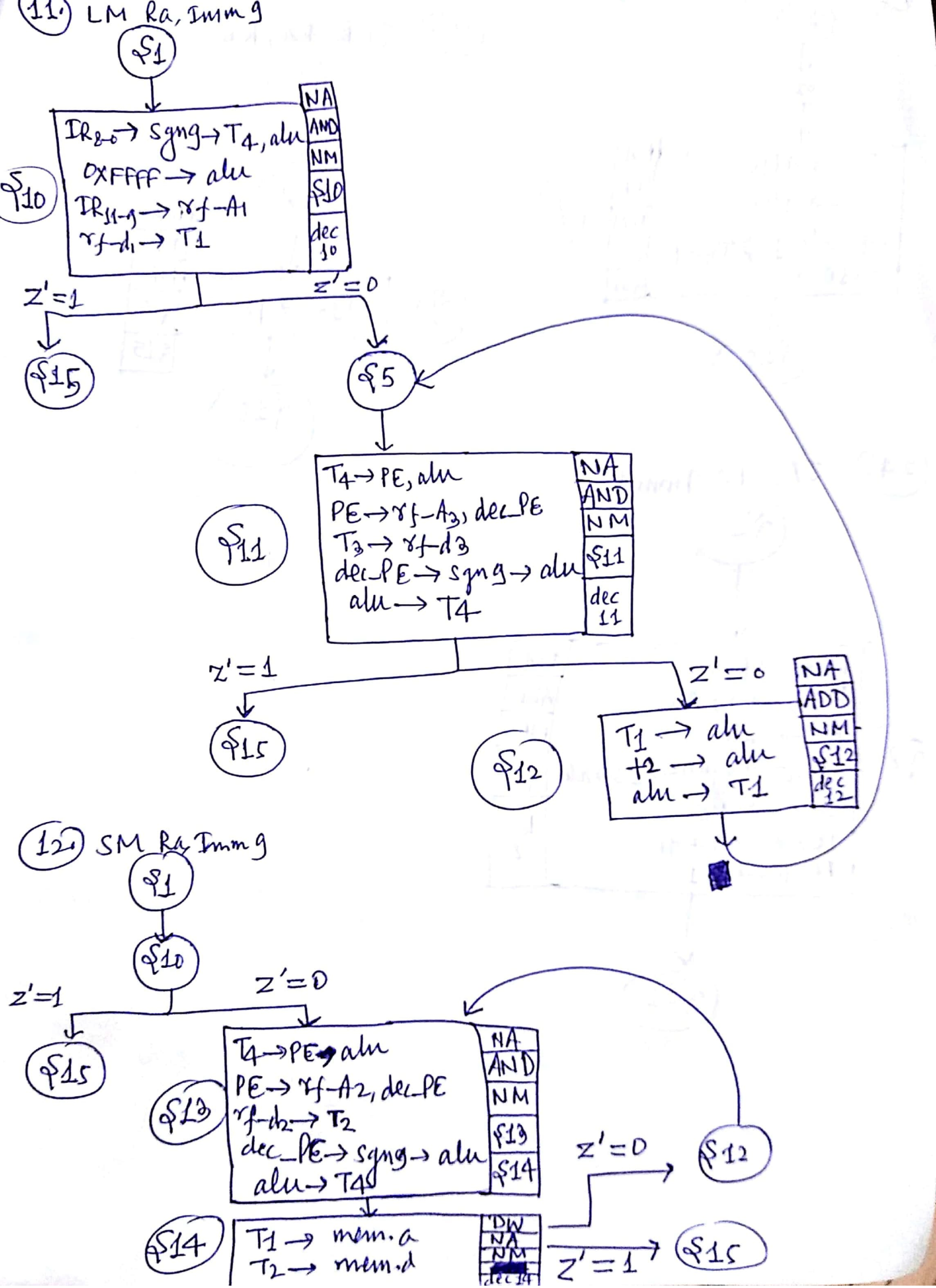
8. LHI Ra, Imm9

9. LW Ra, Rb, Imm6

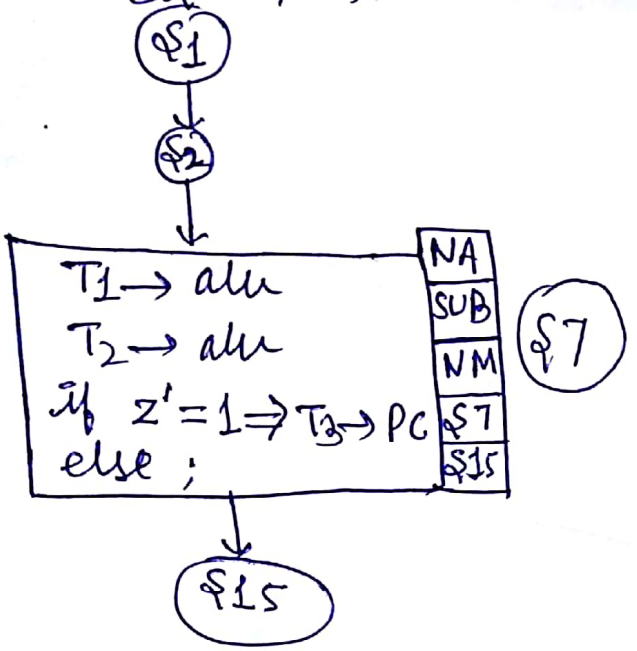


10. SW Ra, Rb, Imm6

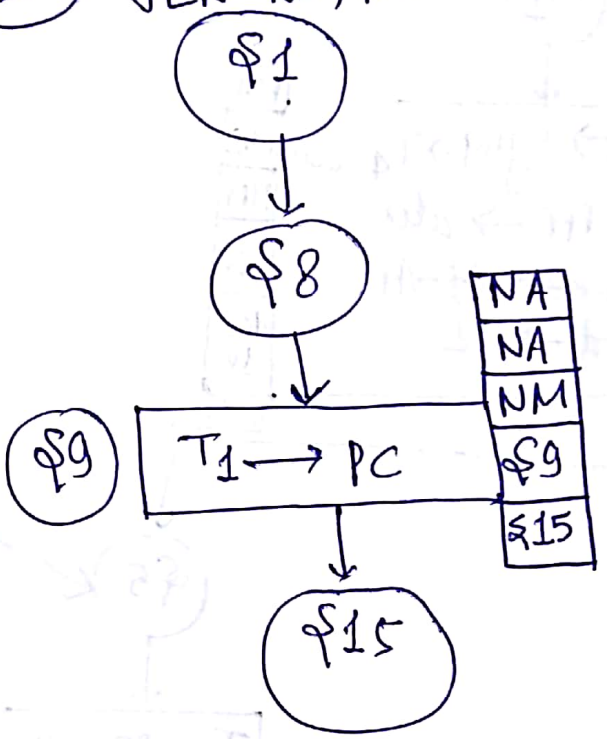




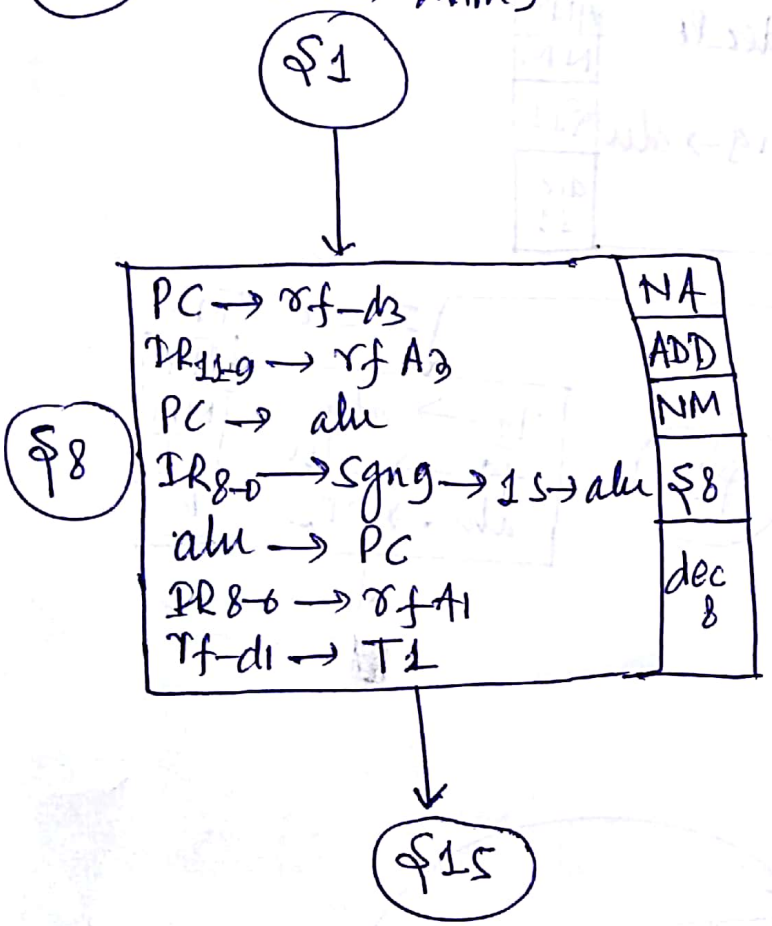
13. BEQ Ra, Rb, Imm6



15. JLR Ra, Rb



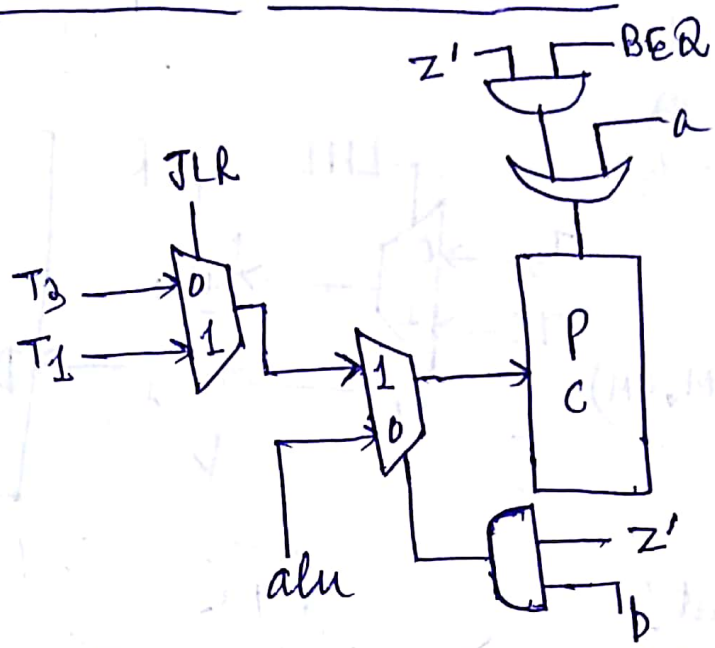
14. JAL Ra, Imm9



INDIVIDUAL COMPONENTS

① PC

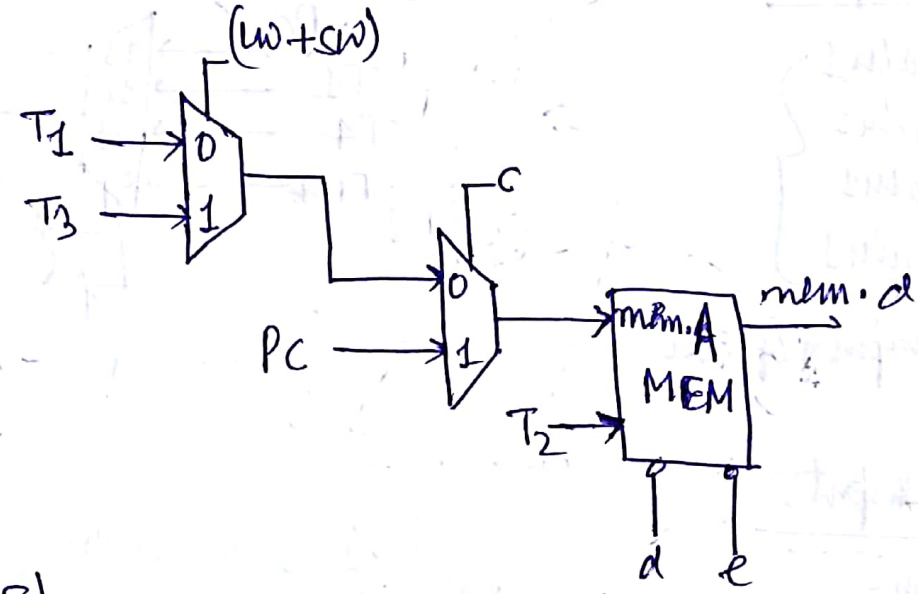
alu → PC
T3 → PC
T1 → PC



② Memory

PC → mem.a
T3 → mem.a
T1 → mem.a

T2 → mem.d

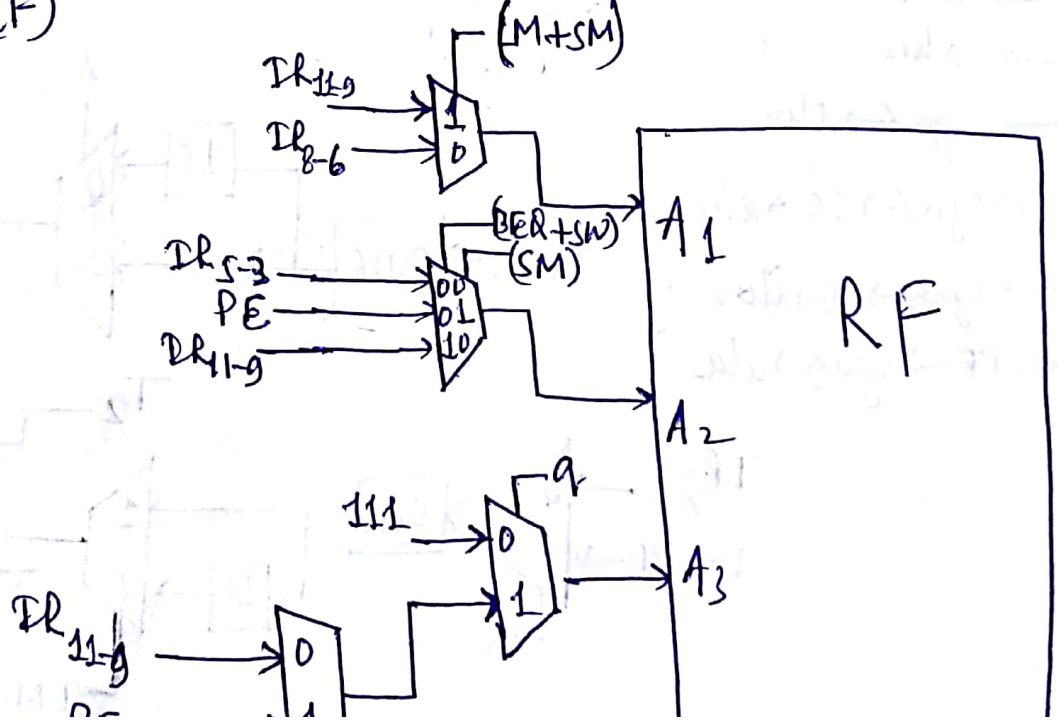


③ Register file (RF)

IR_{8-6} → rf-A1
IR_{11-9} → rf-A1

IR_{5-3} → rf-A2
IR_{11-9} → rf-A2
PE → rf-A2

IR_{11-9} → rf-A3
PE → rf-A3
111 → rf-A3



RF – D2

$t_3 \rightarrow$ rf – d3

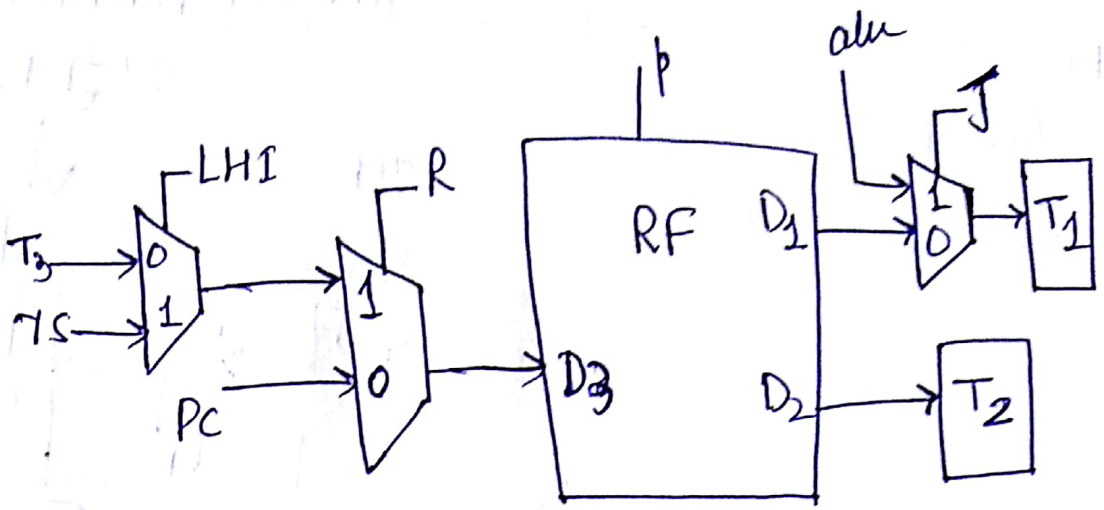
rs $\rightarrow$ rf – d3

PC $\rightarrow$ rf – d2

RF – d1 $\rightarrow T_1$

alu $\rightarrow t_1$ (LM, SM)

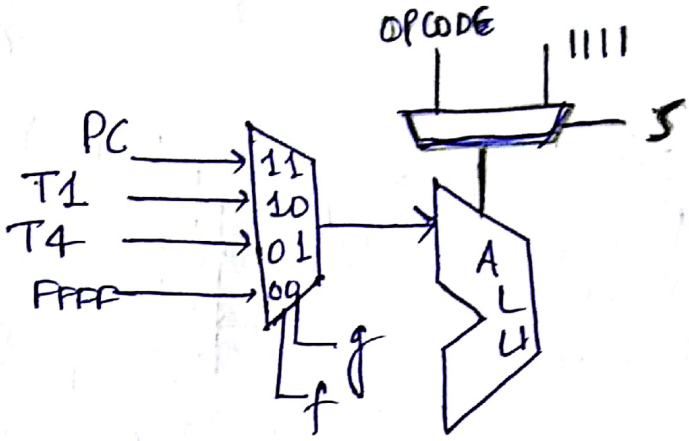
rf d2 $\rightarrow t_2$



ALU Input 1

- PC $\rightarrow$ alu1
- T1 $\rightarrow$ alu1
- T4 $\rightarrow$ alu1
- FFFF $\rightarrow$ alu1

alu1 : Input 1 of alu



ALU Input 2

+2 $\rightarrow$ alu2

$T_2 \rightarrow$ alu2

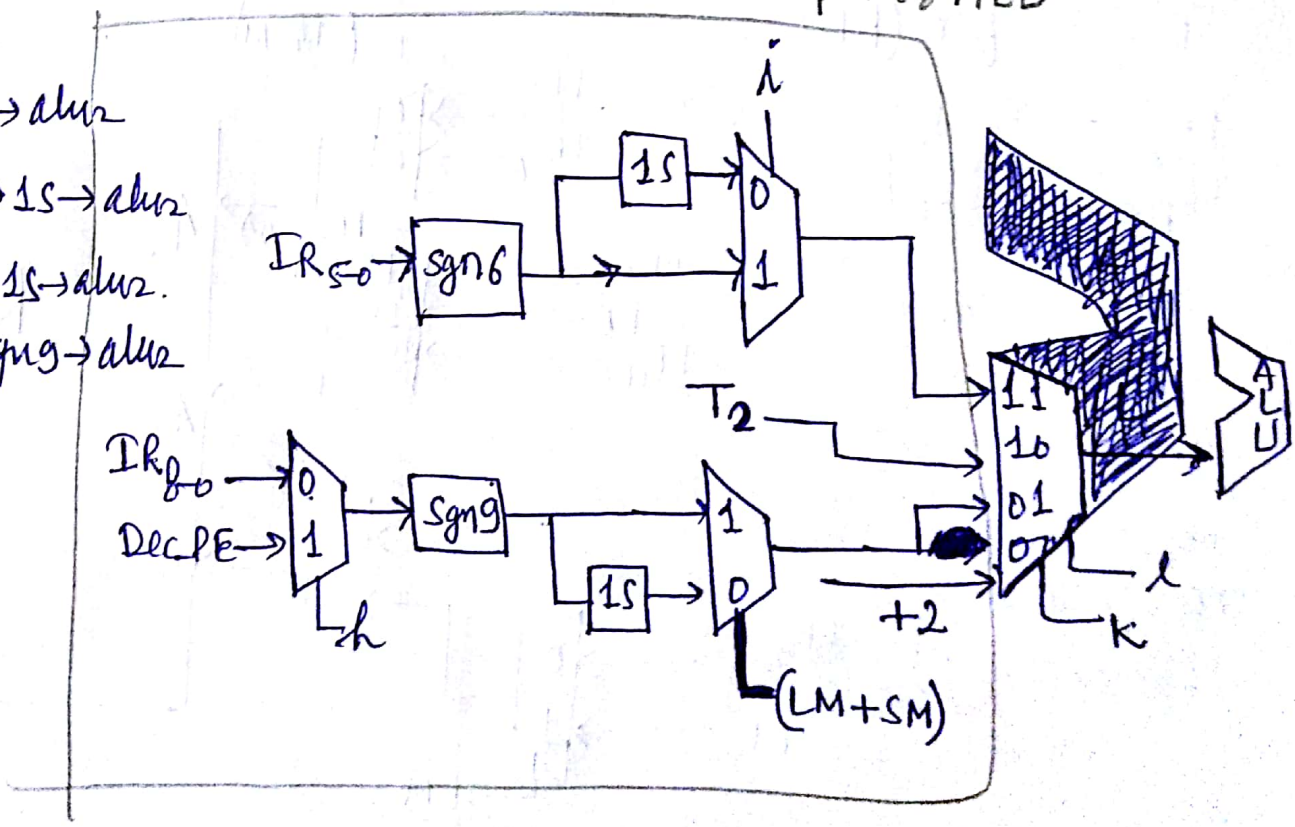
$IR_{5-0} \rightarrow$ sgn6 $\rightarrow$ alu2

$IR_{5-0} \rightarrow$ sgn6 $\rightarrow$ 1s $\rightarrow$ alu2

$IR_{8-0} \rightarrow$ sgn9 $\rightarrow$ 1s $\rightarrow$ alu2.

DecPE $\rightarrow$ sgn9 $\rightarrow$ alu2

Box for 2nd input of ALU



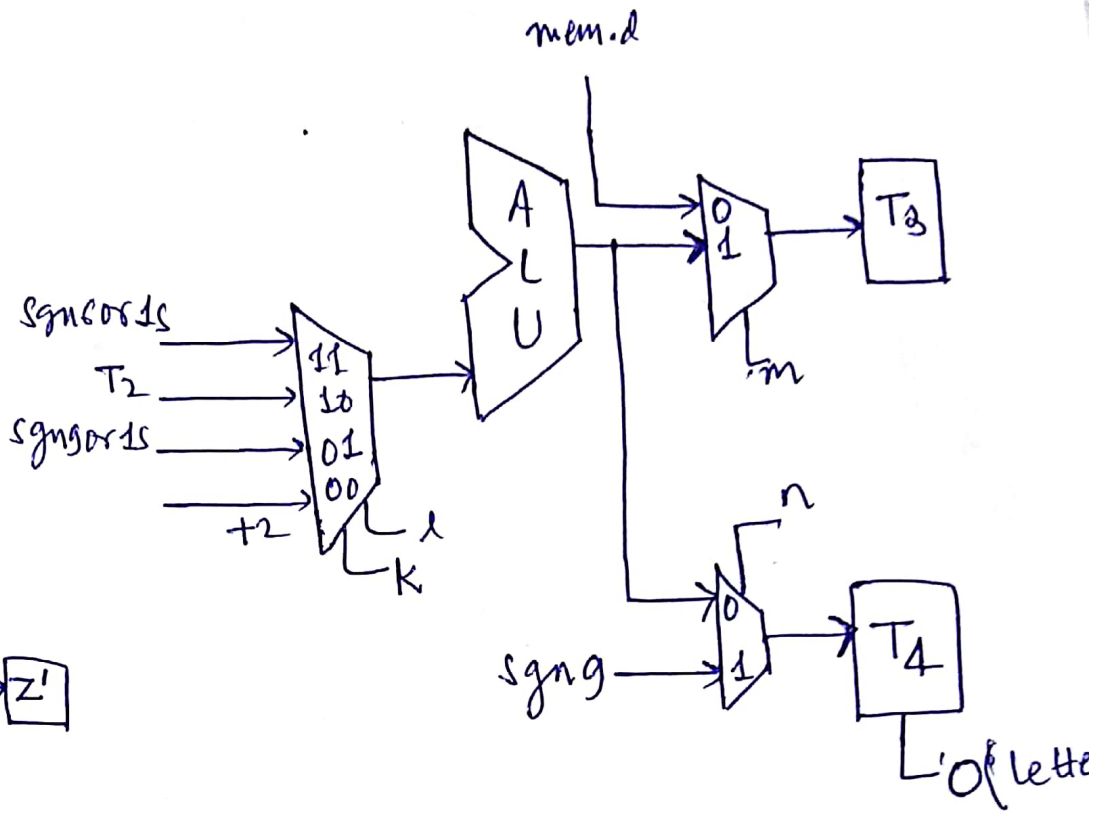
T3 and T4

alu → T3

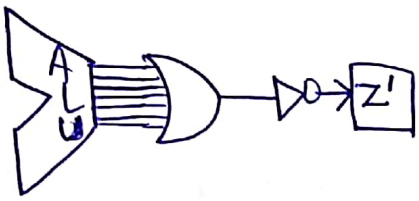
mem.d → T3

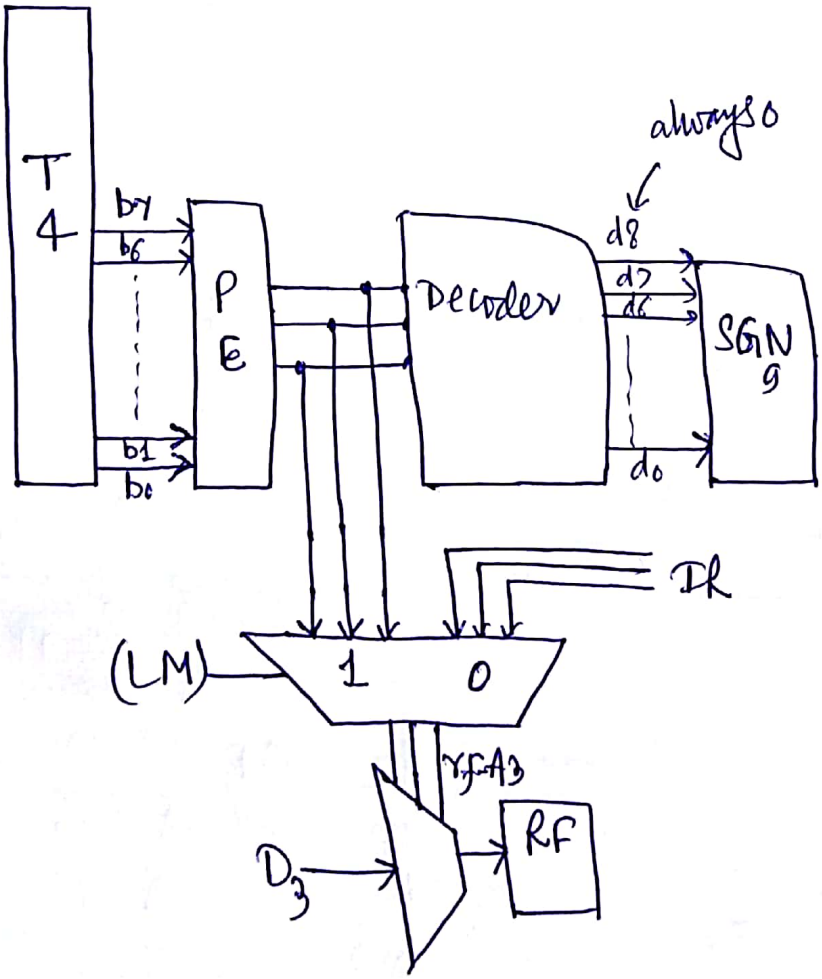
alu → T4

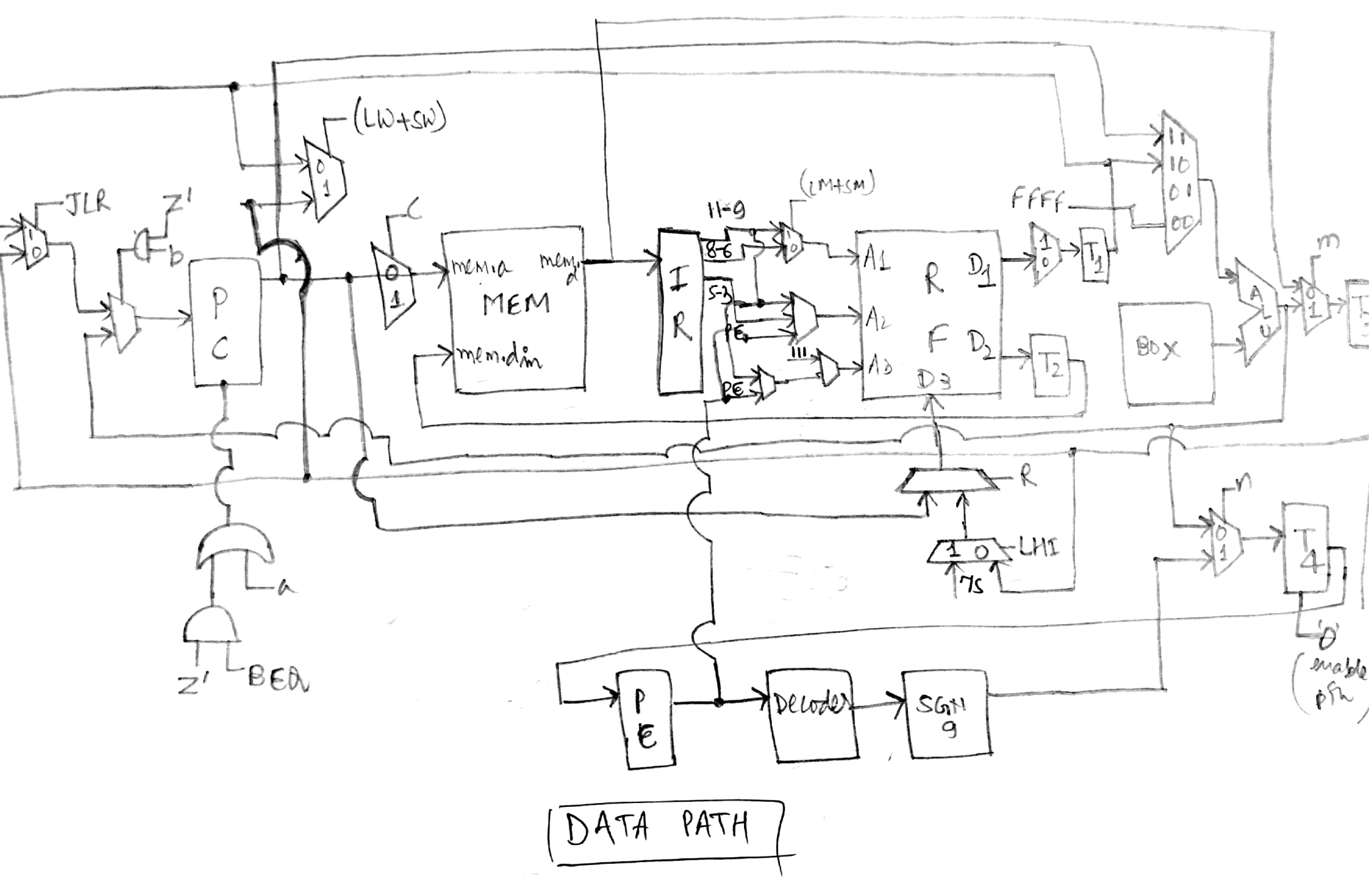
sgng → T4



'z' bit internal







DATA PATH

FSM