**Verification of OpenRISC 1200 Processor**

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This project will focus on implementing assertion-based verification (ABV) of the OpenRISC 1200 (OR1200) architecture using system Verilog assertions and RTL simulation. OR1200 is a 32-bit implementation of the open source OpenRISC 1000 architecture. Due to the limited time and OR1200 being a complex architecture, we will limit our verification efforts to certain key modules.

There exists an open source tool called ORPSoC (OpenRISC Reference Platform System on Chip) that includes several testbenches that we can use for testing OR1200. We can utilize these testbenches to build directed tests that triggers our assertions. Once the assertions are put in place, we will perform a code coverage to see how well the assertions perform. We will also generate random testcases to see how well they perform with the directed test cases in achieving maximum code coverage.

Code coverage is an important metric in the verification process as it measures the degree of which the source code (RTL) has been tested. It is a form of white box testing which finds the areas of program/design not exercised by a set of test cases. Major code coverage method includes:

1. Statement Coverage
2. Conditional Coverage
3. Branch Coverage
4. Toggle Coverage
5. FSM Coverage