

Design of PCB for Automated C_{OSS} Measurements

EE 391 Report

Sara Davidova, Prof. Juan M. Rivas

2023-06-14

Objective

C_{OSS} losses have become a focus of the Stanford University Power Electronics Research (SUPER) Lab for their importance in high voltage, high frequency MOSFETs and GaN HEMTs, potentially limiting their frequency applications. A measurement procedure using the Sawyer-Tower circuit was developed; however, it involved several time-consuming steps such as probe deskewing and it relied on the use of an expensive fridge-size power amplifier. Therefore, the SUPER lab proposed an automated and compact system for measuring C_{OSS} losses that could easily be adopted in industry. The system replaces the massive power amplifier with a small 25W power amplifier in conjunction with an impedance matching network which ensures that enough voltage is delivered to the device under test (DUT) to quantify the losses for the entirety of the frequency range of interests, 500kHz to 30MHz. The signal from the Sawyer-Tower circuit is then sensed using a capacitive-resistive voltage divider and read by a PicoScope, which is integrated with software needed to quantify the loss. The system diagram can be viewed on Figure 1. The power amplifier was already designed by Weston Braun and the software interface for the PicoScope was developed by Steven Abrego. This report is documenting the design and validation of the PCB that includes the impedance matching network, the Sawyer-Tower, and the voltage sensing circuitry.

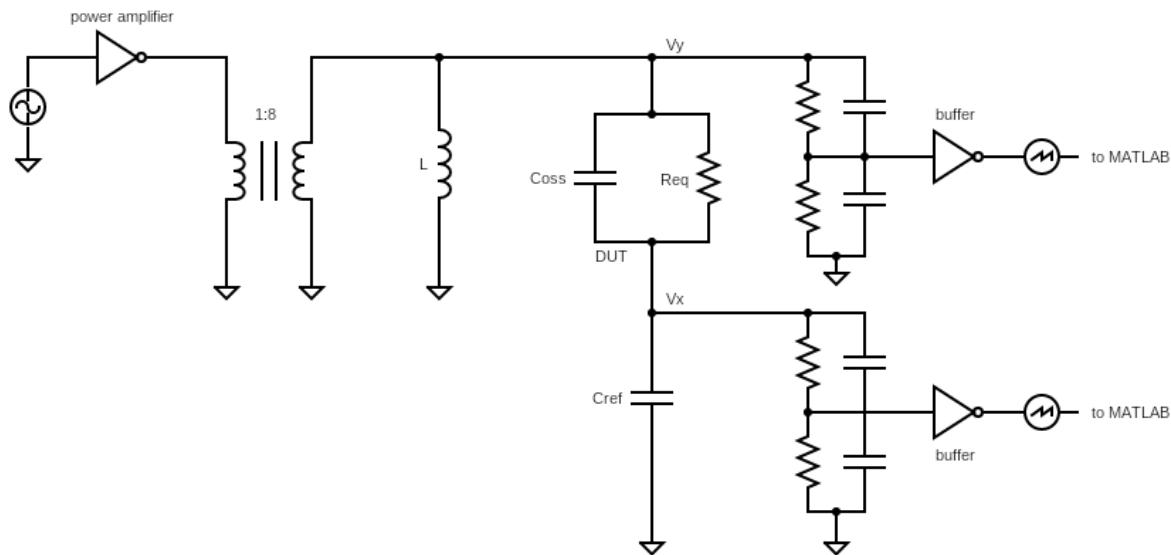


Figure 1: Schematic diagram of entire new Coss loss measurement system for a general device under test (DUT)

Chapter 1

Background

This chapter describing the original Coss loss measurement method had been written by Grayson Zulauf and is included here purely for completeness and as a contextual reference.

The Sawyer-Tower circuit was originally introduced in 1921 to measure new candidate ferroelectric materials for capacitors (Sawyer and Tower 1930). In 2014, Fedison reintroduced the circuit to the power electronics community by reporting COSS losses in silicon superjunction devices (J. Fedison et al. 2014). Two years later, he expanded on this study (J. B. Fedison and Harrison 2016). I also recommend Roig's papers on the loss mechanisms that cause the losses in these devices (Roig and Bauwens 2015), (Roig et al. 2018).

Although Fedison mentions that the convex V vs. Q curves in superjunction Si devices meet "*the conditions for ferroelectric behavior.*" This mislead me for some time into thinking that the superjunction devices, and silicon more broadly, was a ferroelectric material. I do not believe this to be the case. The convexity of the Q-V curves comes from the lossiness of the construction, where the charge added negative-going voltage goes only to recombine with regions of stored charge. For a fairly whimsical discussion of ferroelectrics, see (Scott 2007), which led me to many more sources on ferroelectrics.

We can use the Sawyer-Tower circuit to measure the intrinsic energy / C_{OSS} losses in switching devices of interest whether active (e.g. MOSFETs, GaN HEMTs) or rectifying (e.g. SiC Schottky diodes, Si PIN diodes) or capacitors that we might like to use in circuits. The capacitor measurements are important because many capacitor manufacturers do not include quality factors at the frequencies of interest, and the choice of capacitor can impact resonant converter efficiency quite dramatically at high powers and device losses under soft-switching. Importantly, while the capacitor losses are general because capacitors always swing a voltage across them, the device losses are only relevant under soft-switching conditions. Under hard-switching, all of the energy stored in the output capacitor is dissipated upon device turn-on, so these intrinsic losses can be ignored.

1.1 General Operating Equations

The Sawyer-Tower circuit works because the charge on series capacitors must be equal, and the charge on the non-linear device capacitor (Q_{OSS}) can be deduced from the voltage on the known capacitance, C_{REF} . In steady-state, C_{REF} also provides a DC offset to reverse-bias the DUT's body diode (see Figure 1.1).

The voltage across the device is $V_Y - V_X$, and Q_{OSS} is equal to the charge on C_{REF} [J. Fedison et al. (2014)](J. B. Fedison and Harrison 2016).

$$Q_{OSS} = V_X C_{REF}$$

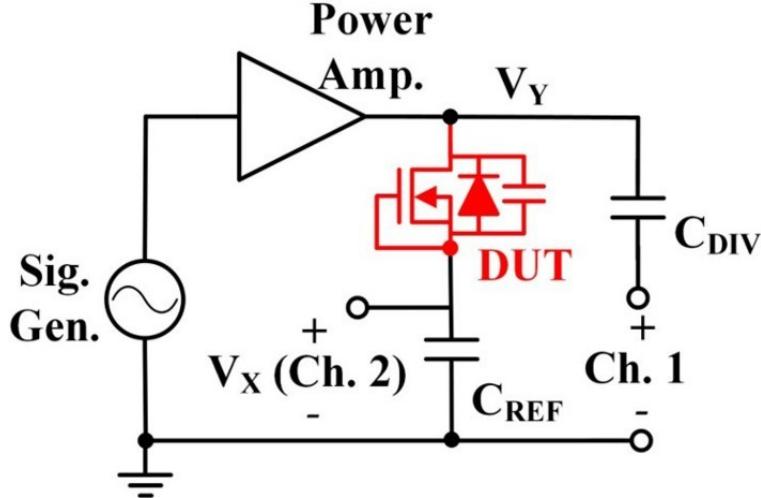


Figure 1.1: Modified Sawyer-Tower circuit, with CDIV added to attenuate high voltages at the VY probe.

The energy during a charge or discharge cycle is:

$$E_{OSS} = \int_{Q_1}^{Q_2} V_{DS}(Q)dQ$$

The energy dissipated in a cycle (E_{DISS}) is the sum of the energy to charge and the energy to discharge the capacitor. The key waveforms are shown in Figure 1.2, where subfigure a) shows the time-domain waveform of the voltage across the device, subfigure b) shows the charge (Q) vs. drain-source voltage waveform, and subfigure c) shows the large-signal capacitance deduced from this testing. In all three figures, the red waveform shows the “charging” portion of the curve and the green waveform is the “discharge” part of the cycle. Note that the difference between the two curves in subfigure b) is the energy dissipated per cycle.

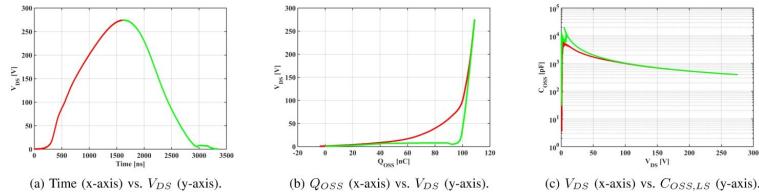


Figure 1.2: Figures showing one test point for the STL18N55M5 device.

1.2 Selecting C_{REF} value

The choice of value and part number for C_{REF} is critical to the test operating correctly. C_{REF} forms a voltage divider with the output capacitance of the DUT, so the value of C_{REF} should be large enough to provide a measurable voltage on Ch. 2 but small enough to keep most of the voltage on V_Y dropped across the DUT. I recommend reviewing the device datasheet and calculating the voltage on each using the provided small-signal C_{OSS} value (which, for most of the devices we consider, will be roughly constant at voltages above 100 V). Note the fundamental tradeoff here a larger C_{REF} will be easier to measure but will result in less voltage dropped across the DUT (this is generally not a problem with power amplifier inputs for 600V devices, but with the Φ_2 waveform generator, deserves more consideration). The self-resonant frequency of C_{REF} must be at least an order of magnitude higher than the maximum frequency that you will measure, which is not easy to attain for very-high-frequency input waves. C_{REF} should be a low-loss (see Section III-C xxx for

more detail on this point) and use a dielectric that does not change significantly across voltage or frequency. In a body-diode test setup, the voltage rating of CREF must be able to withstand the maximum input voltage ($V_{PP}/2$, see Figure 1.1), and, in a capacitor test setup, the voltage rating of C_{REF} must withstand the voltage experienced at the maximum input voltage and the appropriate divider ratio (see Figure 1.3).

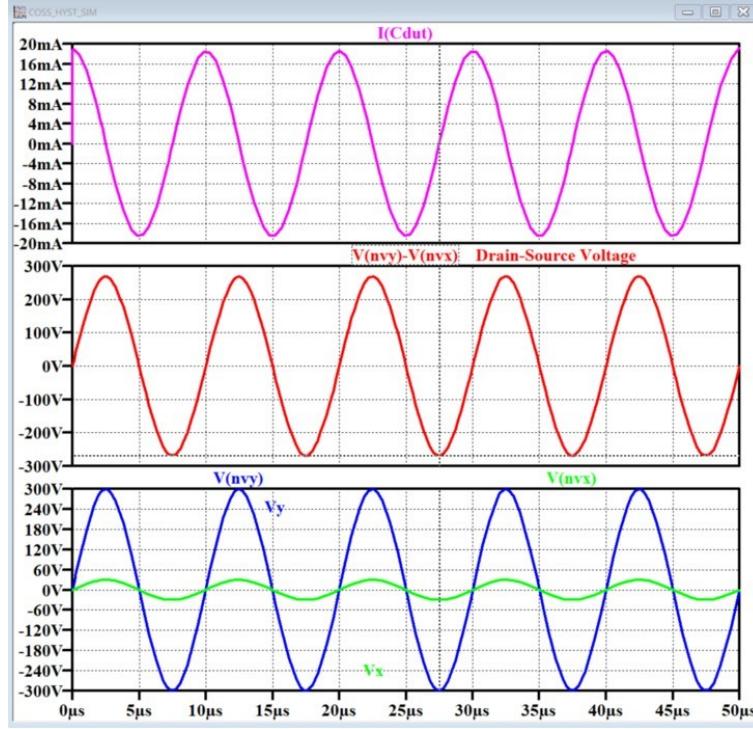


Figure 1.3: Simulated waveforms with 111 pF DUT and 1000 pF CREF operating at 100 kHz. Captured waveforms are from the first cycle. There is no settling time here.

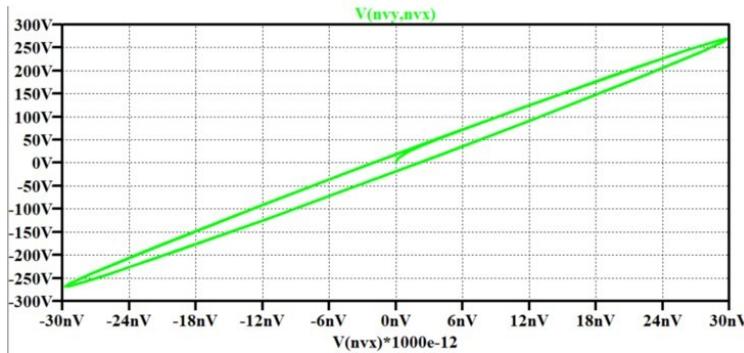


Figure 1.4: Eye diagram for a low-Q capacitor ($C=111\text{pF}$, $\text{ESR}=100\Omega$). $VY-VX$ (y-axis) plotted against $VX \cdot \text{CREF}$ (x-axis).

1.3 Expected Waveforms

1. *Capacitive D.U.T.:* With a capacitor under test - or a device with reverse conduction characteristics, the waveform will be a simple bipolar charge-discharge cycle. This is shown in Figure 1.3. There is no transient, and the voltage applied across the capacitor-under-test is a simple capacitor divider ratio from the input voltage. When the charge on the reference capacitor is plotted against the device

voltage, as shown in Fig. Figure 1.4, a low-Q capacitor will form the cigar-shaped eye-diagram characteristic of a lossy cycle. The area between the bands is the energy dissipated per cycle, and the quality factor is easily calculated from this energy dissipation value and the peak energy stored.

2. *D.U.T. with Reverse-Bias Diode:* In our testing, it is absolutely fundamental that the body diode inherent in all of these devices (including GaN HEMTs, which do not have a body diode but exhibit reverse conduction characteristics) does not conduct during the measurement. Fedison (J. B. Fedison and Harrison 2016) mentions in passing that C_{REF} provides a DC bias of $\frac{V_{PE}}{2}$ to ensure the body diode never conducts, but does not dive into the exact operation that ensures this is the case. Figure 1.5 plots the key waveforms in a circuit with the PGA26E19BA (Panasonic, GaN HEMT) device under test. On the first cycle, the body diode clamps the voltage across the device to zero (or a diode drop) when the power amplifier input reverses direction. When the current crosses through zero again, the diode must stop conducting, returning the device- under-test to a capacitor, and restoring the division of voltage across the the DUT and C_{REF} to a simple capacitor divider. The voltage across C_{REF} remains at this DC-biased value of $\frac{V_{PE}}{2}$ for the duration of the test.

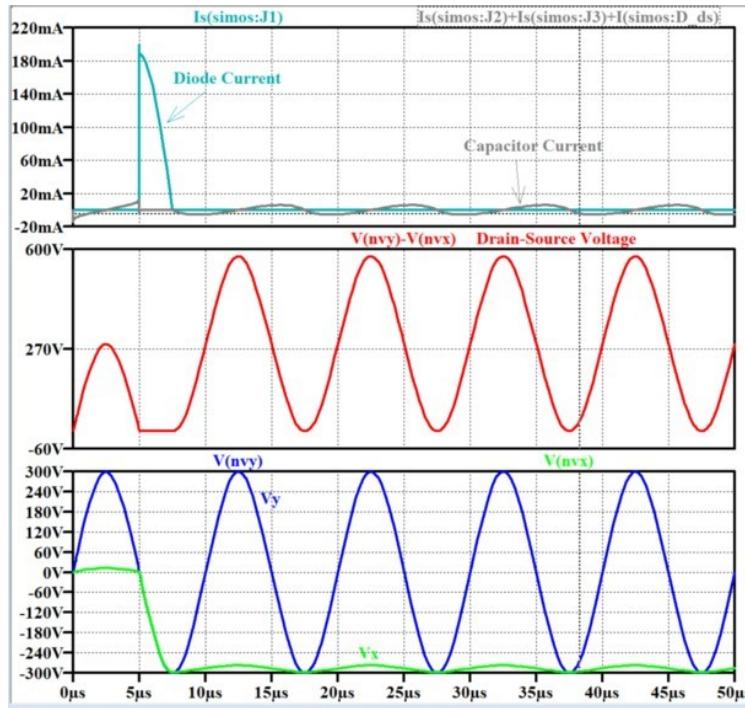


Figure 1.5: Transient simulated waveforms in the Sawyer-Tower circuit, with the PGA26E19BA device and 1000 pF CREF operating at 100 kHz. Initial condition is 0 V CREF and the captured waveforms are from the first cycle.

Devices with body diodes that have reverse-recovery charge take longer to settle to the steady-state operation where the body diode does not conduct. When gathering data, we must carefully examining the voltage waveforms to ensure that we have reached steady-state before taking the measurements. Figure 1.6 shows the operation in this silicon superjunction device after 10 cycles. It is clear primarily from the V_{DS} waveform that the diode is clamping the voltage, and we cannot take a measurement at this test point. The equilibrium operation is shown in Figure 1.7.

When testing a device with reverse-conduction characteristics, you must be sure to wait until the transient waveform has settled. This is not a concern when a simple capacitor is under test.

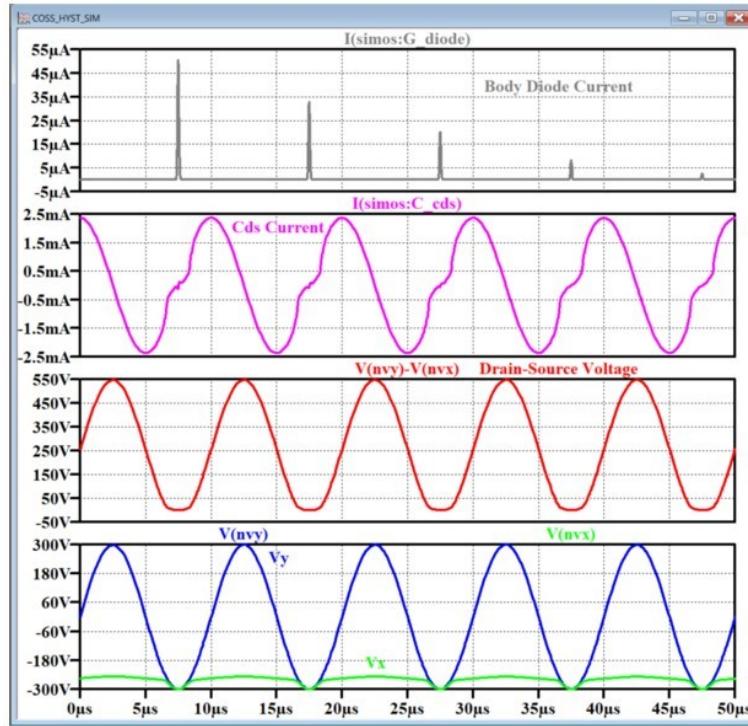


Figure 1.6: Transient simulated waveforms in the Sawyer-Tower circuit, with the STL15N65M5 device and 1000 pF CREF operating at 100 kHz. Initial condition is 0 V CREF and the captured waveforms are from the tenth cycle.

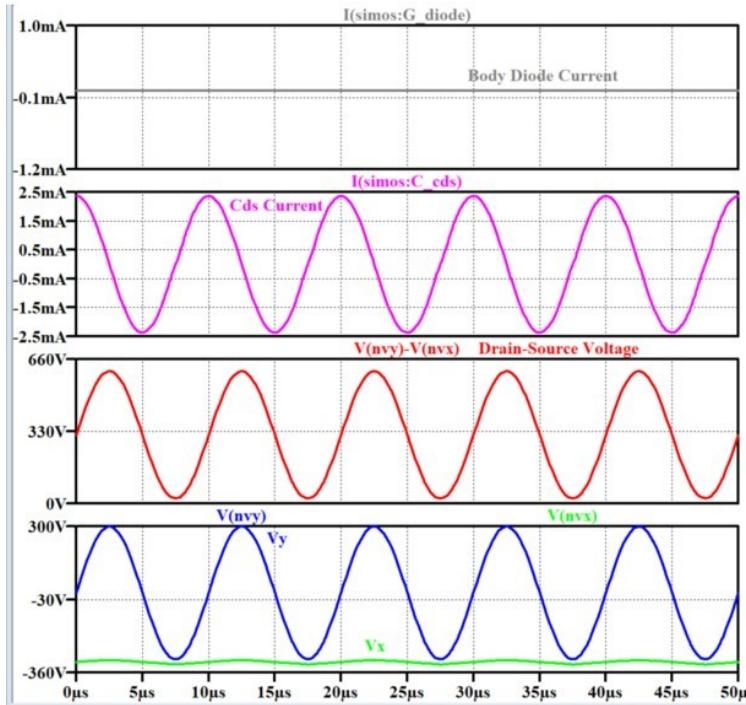


Figure 1.7: Equilibrium simulated waveforms in the Sawyer-Tower circuit, with the STL15N65M5 device and 1000 pF CREF operating at 100 kHz. Initial condition is 0 V CREF and the captured waveforms are from the 1000th cycle.

Chapter 2

Test Procedure

The current test procedure is as follows:

1. *Warm-up:* Connect the two probes to the oscilloscope (MSO9404A assumed) and wait 15 minutes for the probes to warm up before calibrating. Connect an N2873A probe to Ch. 1 and connect a N2875A probe to Ch. 2. Set each probe to the appropriate attenuation and DC coupling. Wait 15 minutes to allow the probes to reach their equilibrium temperature before proceeding.
2. *Manual calibration:* With the probe connected to Probe Cal, perform the manual probe compensation (capacitor adjustment) until the on-screen waveform appears as a square wave without under- or overdamping.
3. *Automatic calibration:* Perform the automatic attenuation and calibration on each probe, in turn, by connecting them to Probe Cal on the front of the oscilloscope. Follow the on-screen prompts to perform the automatic calibration.
4. *Capture settings:* Change both probes to AC coupling, 16 cycle averaging, and high-resolution time capture.
5. *Calibrate board:* Install test board with a low-loss capacitor of a similar size to C_{REF} in place of the DUT. Perform the following two steps at each frequency (or a reasonable subset) you plan to test, especially if testing will occur in the high- and very-high-frequency range.
 - a. *CDIV Ratio:* Connect the Ch. 2 probe directly at the output of the power amplifier (I recommend using a “T” SMA connector) and connect Ch. 1 between C_{DIV} and ground. Inject a signal at the appropriate frequency and measure V_{PP} on each channel. Record this voltage at three magnitudes, calculating the ratio at each point (*note: this should not vary significantly at these different magnitudes*). Ensure that the frequency-voltage setup is significantly below the derating curve for the probes. Add a Math function on the scope as Ch. 1 multiplied by this C_{DIV} attenuation, and a second Math function of this scaled function minus Ch. 2 to provide a measurement of the actual injected voltage.
 - b. *Deskew:* Carefully affix the probes to a “permanent” location and mark the board position. Connect Ch. 1 between C_{DIV} and ground and connect Ch. 2 across C_{REF} . Inject a reasonably-sized waveform (I typically aim for 1-10 V across each channel) and deskew the offset between Ch. 1 and Ch. 2. FR4 introduces approximately 150 ps/inch of delay, so we expect approx. 300 ps of skew, with Ch. 2 lagging. This skew calibration is especially important at tens-of-MHz frequencies, but can generally be ignored if measurements do not exceed hundreds-of-kHz.
6. *Install DUT:* Remove the board from the test setup, being careful to mark the location of the board and the probes that you just deskewed, as the skew will be slightly position-dependent. Remove the low-loss capacitor from the DUT position, and install the DUT. Be careful to make a low-inductance connection between the gate and source pins. I recommend locating the DUT as close to the power

amplifier input as possible, although the board is designed to appear low inductance for any DUT location.

7. *Thermal impedance:* Place the board in the existing test fixture location. (Note: be careful that this location does not have air blowing from the power amplifier while the power amplifier is running, as this will affect the thermal measurement results.) Do not connect the power amplifier or oscilloscope, as neither of these are isolated, and, depending on the configuration of your DC supply, may affect the grounding of the test setup. Connect a DC supply across the DUT (not across C_{REF}), forward-biasing the diode in the DUT, and set the current limit to the desired current level and the voltage limit to a value around 5V. Measure the temperature of the DUT case with the thermal camera. Measure 4 points with varying power (and temperature) with a constant soak time that allows the DUT to reach close to thermal equilibrium - keeping the device temperature well under its rated value - and fit a linear line between power and T_C with an intercept of (0,0) to find R_{TH} . Record this value and the ambient temperature.
8. *Operational testing:* Disconnect the DC supply used for the thermal impedance calibration. Connect the power amplifier and oscilloscope probes in the correct positions. For the provided Matlab script, this means you must have Ch. 1 connected to V_Y and Ch. 2 connected to V_X . The horizontal settings should capture approximately 3 cycles. Turn on the power amplifier, recording electrical measurements at the end of the thermal soak for 50 V_{DS} intervals (assuming you are testing 600 V devices) until the device voltage limit is reached or the device temperature reaches a level that is uncomfortable for testing. The thermal soak time should be similar to that used for the calibration in the previous step. Each channel should use the full resolution of the oscilloscope at each test point. Record the temperature of the device (I only use the thermal calibration if T_C exceeds 35°C) and the electrical measurements, carefully recording the frequency, C_{DIV} attenuation, and C_{REF} value for the testing performed (you might need this at some later date).
 - a. *Post-processing check:* Process the electrical data using the provided Matlab script, calculating the electrically-measured E_{DISS} and comparing it to the thermal measurements. These should be approximately equal. If they are not, you can repeat the previous calibration steps or minimally adjust the skew (50 ps maximum adjustment!) to achieve the correct matching. *Note that you may only adjust the skew once at each frequency do not adjust at each test point!!*
 - b. *Capture remaining data:* With confidence in the skew, attenuation, and capacitor values, repeat the rest of the desired measurements without moving the test setup or altering any of the key calibration methods. In between frequency setpoints, when the voltage is reset from the maximum to the minimum voltage, you absolutely must discharge both C_{REF} and C_{DIV} , both of which will have built up a DC voltage during the test time. This can be done with two DMM probes. **MAKE SURE THE TEST SETUP IS OFF WHEN YOU DO THIS. NEVER TOUCH A LIVE CIRCUIT.** Post-process the data and graph the electrical and thermal data at each voltage-frequency measurement point.

A couple of notes: we aim to detect sub- μ J differences across a 650 V swing at VHF, so the measurement setup is by far the most difficult part of gathering this data in the MHz range. The skew between V_X and V_Y , in particular, must be very carefully calibrated to compute the $V_{DS} \cdot dQ$ product, and has a major effect on the losses that are measured electrically. The 1 pF capacitor forms a capacitive divider with the probe to bring the V_Y measurement into the probe specification, but this introduces extra delay between the two probes and an additional complication in test setup. The thermometric estimation is performed to compare to the electrically-measured E_{DISS} . The power dissipated is estimated from the temperature rise of the device, as measured by an infrared camera (FLIR A655sc). The E_{DISS} per cycle is calculated from this thermometrically-measured value by dividing the power by the frequency. The thermal measurements are critical if there is any uncertainty about the electrically-measured values.



Chapter 3

Error Terms

3.1 Probe Skew

The accurate calculation of the energy dissipated per cycle depends on the term $V_{DS} = V_Y - V_X$ multiplied by the term $Q_{OSS} = V_X \cdot C_{REF}$, with V_Y and V_X measured on different probe channels. Unfortunately, automatic probe deskewing fixtures are designed for power calculations using current and voltage probes, so we must perform this deskewing manually. The delay between probes is due both to the propagation delay offset between the probes themselves and the finite delay through C_{DIV} . These must both be calibrated, and we expect the order to be in the hundreds of picoseconds. With measurement in the hundreds of kHz range, a cycle is μs , so these picoseconds are 10-6 percent of a captured a cycle and have no impact. At 10s of MHz, however, the probe skew is a major issue and must be carefully eliminated. To be precise, the probes should be deskewed at every frequency that you plan to measure at, but typically performing a deskew at a couple of intermediate frequencies should be okay. Check your deskew with the thermal measurement on the first few measurement cycles before gathering lots of data (*and wasting lots of time...*) with the probes offset incorrectly.

3.2 Probe Error

Very few oscilloscope probes are able to measure high-voltage and high-frequency effectively. For example, the rolloff in Agilent's N287x family of probes is shown in Figure 3.1. For this family of probes, for example, we cannot measure above $100V_{RMS}$ above around 10 MHz, complicating the measurement significantly. To get around this issue - which is present in nearly all probes - we have added C_{DIV} to the original Sawyer-Tower circuit. Of course, this automatically AC couples the V_Y measurement and adds an additional calibration step and error, but seems absolutely necessary to measure 600V and greater devices. For 100V (and lower) voltage-rated devices and capacitors, we may be able to exclude C_{DIV} .

The key takeaway here is that the probes must be carefully chosen to ensure they measure accurately at the applied frequency-voltage setpoint. Even if this operating point is within the datasheet specifications, proceed carefully, as many probes rolloff at high-frequency and introduce extra errors.

3.3 C_{REF} Losses

The test setup will inextricably combine the losses in the reference capacitor, C_{REF} , with the losses in the device-under-test. The peak AC energy stored during a cycle in the reference capacitor is the same as the energy in the device, or:

$$E_{C,REF} = \frac{1}{2}C_{REF} \cdot V_X^2$$

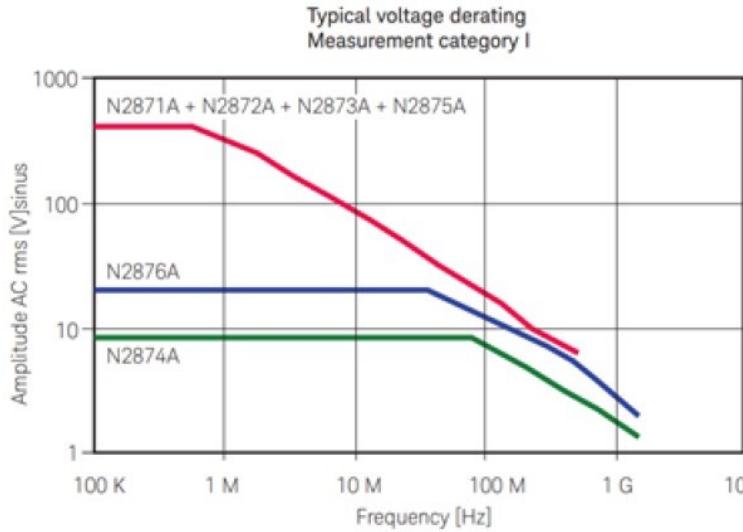


Figure 3.1: Agilent N287x family voltage rolloff with frequency.

where we have ignored the large DC bias present on C_{REF} and only considered the AC charge. And, beginning with the simple understanding that:

$$Q = \frac{\text{Peak Energy Stored}}{\text{Energy Dissipated Per cycle}}$$

which we can rearrange to find the energy dissipated per cycle in C_{REF} :

$$E_{DISS,CREF} = \frac{\text{Peak Energy Stored}}{Q} = \frac{C_{REF}V^2}{2 \cdot Q_{C,REF}}$$

Based on this equation, we see that the percent energy dissipation that we can measure is limited directly by the dissipation factor ($DF = \frac{1}{Q}$) of the reference capacitor we select. Typically, the dissipation factor is only affected by frequency, not by operating voltage. For example, the AVX 1812AA102KAT1A capacitor used in the GaN device study (Zulauf et al. 2017), (Zulauf et al. 2018) has a DF of 0.1% at 1 MHz. We certainly would be unable to measure energy dissipation in the DUT on the magnitude of 0.1% at 1 MHz, and, assuming a constant resistance, would not be able to measure dissipation under 1% of the energy stored at 10 MHz ($DF = 2\pi \cdot f_{SW}RC$). Achieving dissipation factors lower than around 1% at 10 MHz may require an RF capacitor, which will be difficult to connect to with low inductance and has not been tested. This may be necessary to measure extremely low losses in certain devices.

There are two primary takeaways: firstly, ensure that you select a capacitor with a low dissipation factor at the frequencies of interest. Secondly, I recommend either subtracting these losses from the final results for your device (these losses should be easy to calculate and a constant percentage across applied voltage) or reporting the losses and noting that they are negligible (we did not do this in the initial paper, but should have).

3.4 Overall Error Estimation

Estimating the overall error is a difficult exercise, but, empirically, I don't believe we can measure losses accurately under 10^{-2} micro Joules or less than around 2% of the total energy storage, due to C_{REF} quality factor limitations. Both of these can be improved at lower voltage or lower frequency. An accurate calculation of the overall error inherent in this test setup is certainly on the "to-do" list.

Chapter 4

Impedance Matching Network

The topological design behind the impedance matching network was developed by Steven Abrego and Zikang Tong in the SUPER Lab. I was responsible for its implementation.

4.1 Device model

When the source and gate of the device under test (DUT) are shorted, the device can be modeled as a parallel combination of capacitance and resistance. For maximum power transfer from the power amplifier, the device should appear purely resistive, whereby the exact resistance depends on the desired voltage amplitude. This impedance-matching circuit aims to resonate out the capacitor using a parallel inductor and adjust the resistance seen at the input by using a transformer, as shown on Figure 4.1.

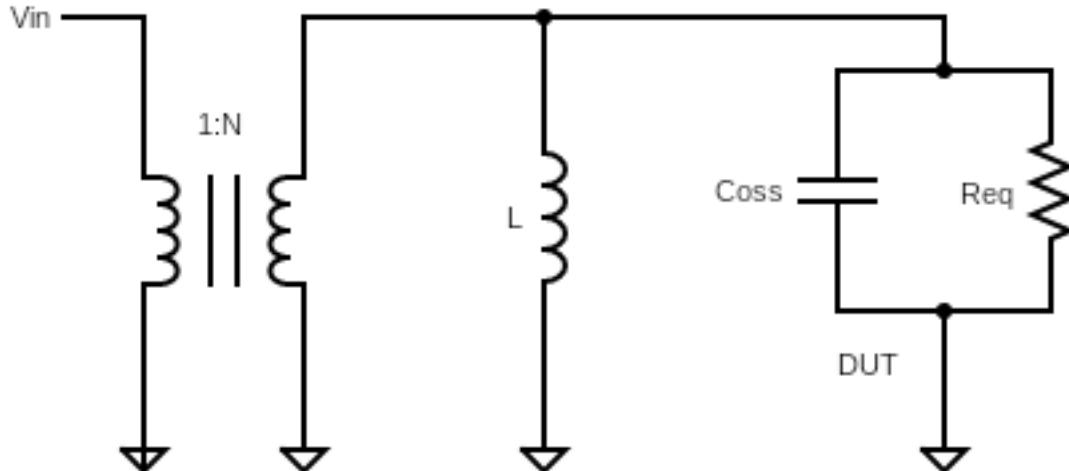


Figure 4.1: Impedance matching network topology

4.2 Parallel LC Resonant circuit

Since the Coss capacitance can range from $10s$ to $1000s$ of pF , an inductor bank is needed to create a variety of inductance values that can be used to resonate out the capacitor. Steven Abrego created an inductor network capable of producing between $0.46\mu H$ to $185\mu H$. The network, visible on Figure 4.2, utilizes three series inductors for big inductance steps and five parallel inductors for a variety of small inductance steps.

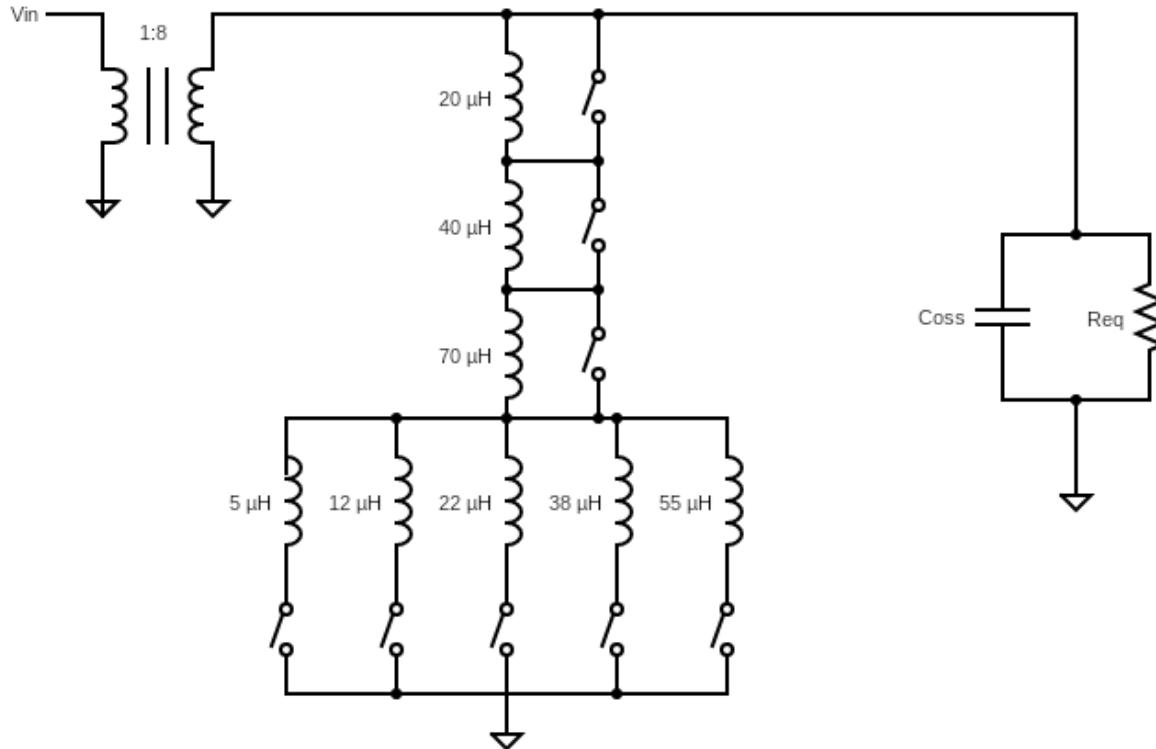


Figure 4.2: Impedance matching topology with detailed inductor-relay network

The switches were implemented with relays capable of passing over $2A$ of current, and withstanding $500VAC$. Relays were selected over MOSFETs because only low frequency switching was necessary (between each test point) and because they have lower parasitics despite their high current and voltage rating. Each relay were driven by the circuit shown on Figure 4.3 and digital input from an Arduino. The simple Arduino code is attached in Appendix A.

The inductors were hand-wound. For low inductance values, $18AWG$ magnet wire was used, and for inductor values above $30\mu H$, $20AWG$ wire was used because of their higher impedance which would lower the amount of current passing through. Initially, all but the two highest values were wound on ferrite pot cores which allowed for a creation of an air gap to lower the B-field the core was subject to. However, after measuring the impedance of those inductors, all but three lowest values had to be rewound on toroids to decrease the number of windings and to increase spacing between those windings for lower capacitance. Both the ferrite pot cores and the toroids were selected to be from materials whose reactive components of material permeability, μ' is stable until above $30MHz$, as can be seen on Figure 4.4. The resistive component of the permeability μ'' relates to the loss in the core, so even though it is still important that it does not increase too much, the linearity of it was not absolutely required.

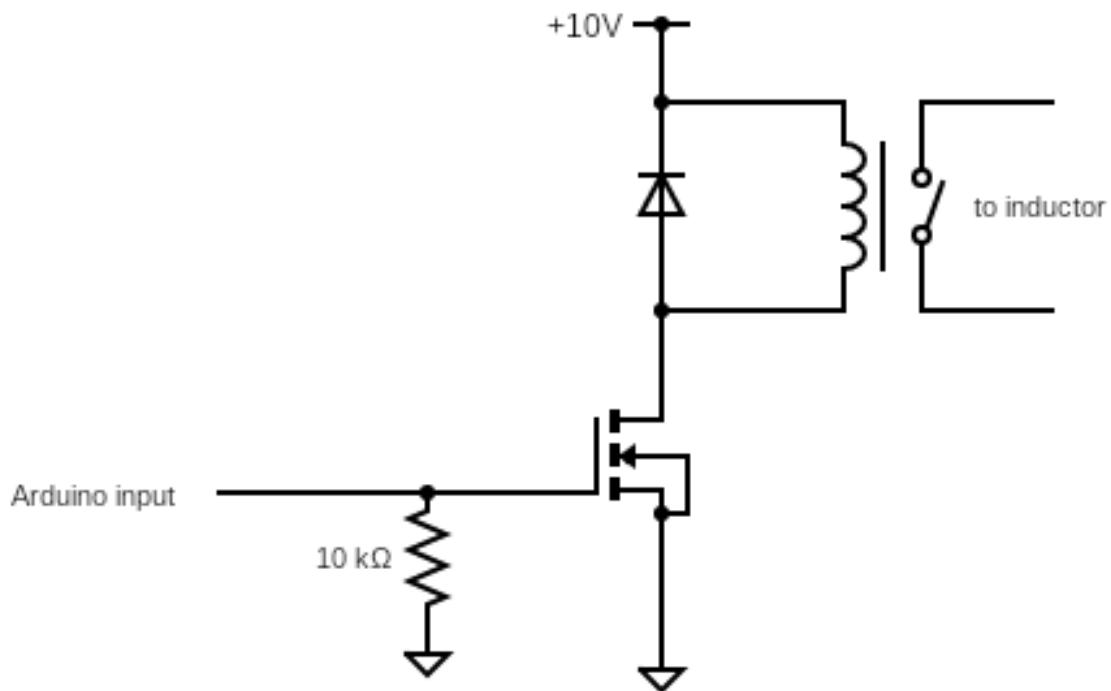
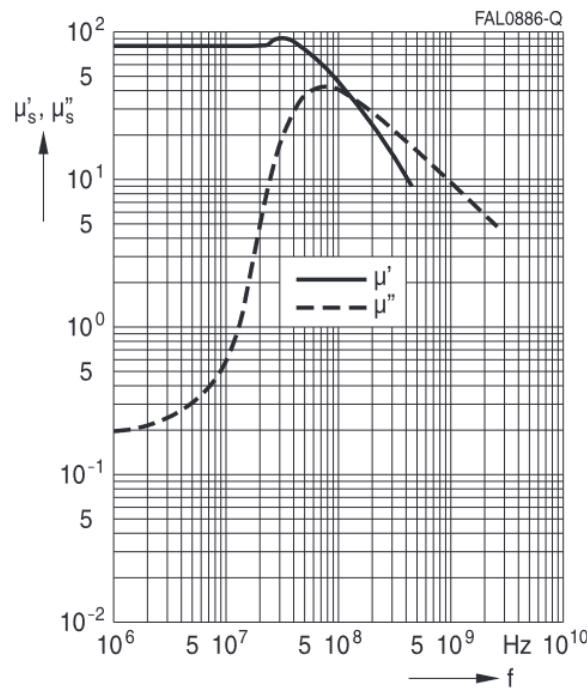


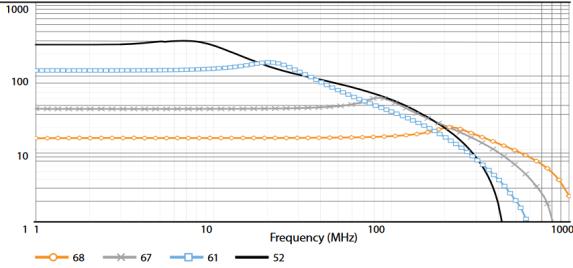
Figure 4.3: Relay drive circuit

Complex permeability

versus frequency

(measured on R10 toroids, $\hat{B} \leq 0.25$ mT)

(a) Ferrite pot core material "K1"

 μ' reactive component of material permeabilityFigure 4.4: μ' vs frequency for chosen inductor cores. Sources a; [Source b](#)

4.3 Transformer

The main requirement for the transformer was the turns ratio of roughly 1:8, which was determined by Steven Abrego based on experimental loss measurements. On the secondary, 18AWG wire was used because lower current would pass through it. On the primary, 14AWG wire was used (16AWG magnet wire was not available in lab at the time). Because cores capable of withstanding 30MHz have a very low permeability, the windings must be extremely tightly coupled. For example, it is not ideal for them to be on opposite legs of the core, instead, they should be wrapped around each other such that flux leakage is minimized. The number of windings on the secondary was determined based on the magnetizing inductance. In order not to affect the matching circuit significantly, an inductance much higher than $185\mu F$ would be necessary. However, this would mean that a huge number of winding would be needed, increasing the parasitic capacitance and causing self-resonance at much lower frequencies. For that reason, a temporary decision was taken to make the magnetizing inductance equal $185\mu F$, which amounted to 20 turns on the secondary. Since lower turns ratio was preferable to higher, the number of windings on the primary was rounded up to 3. The core used can be found [here](#).

The final board with the inductors and transformer can be seen on Figure 4.5.



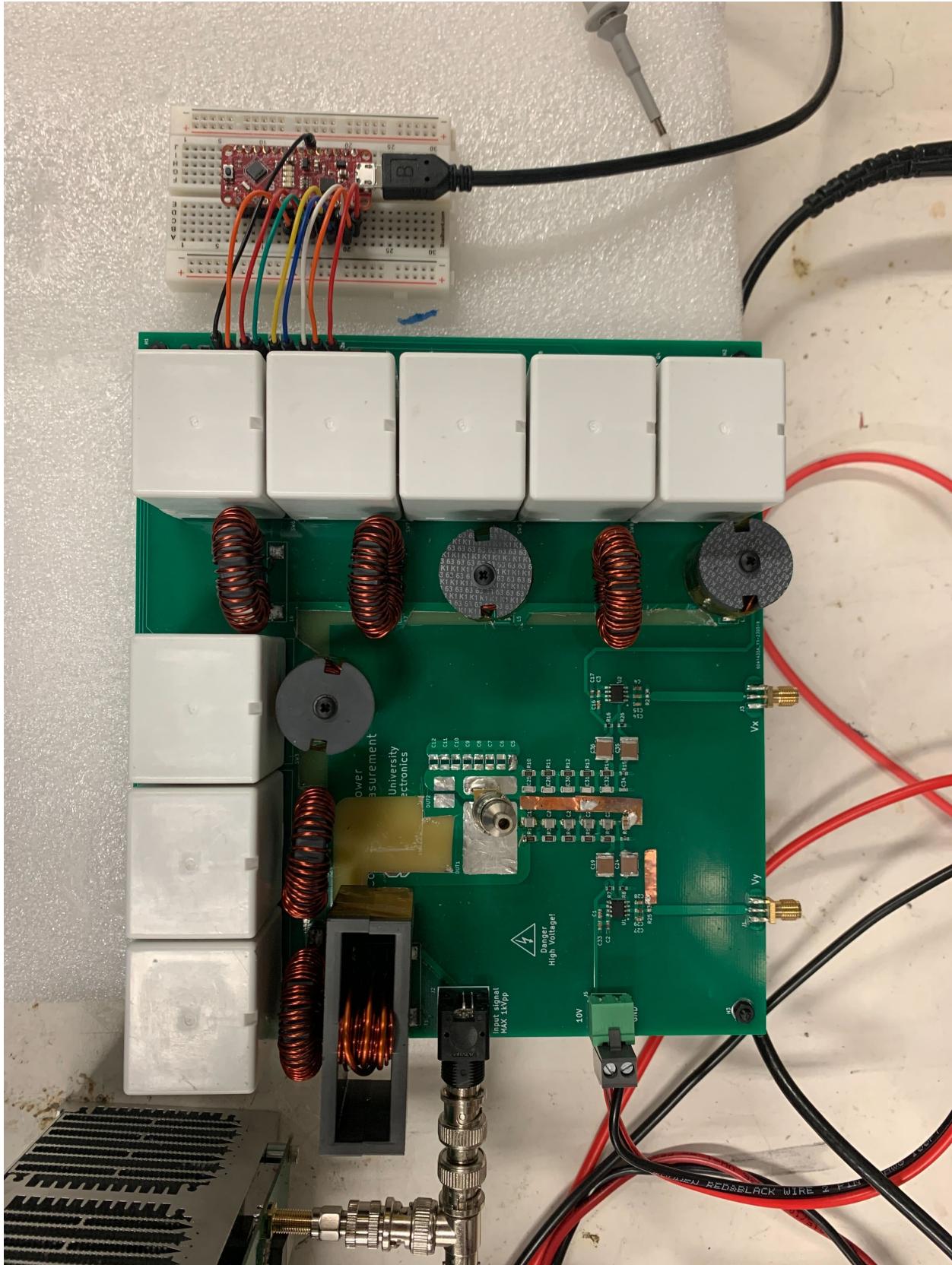


Figure 4.5: PCB with complete impedance matching network

Chapter 5

Voltage Sensing Circuit

The PicoScope has a maximum input voltage of $+/- 20V$. However, the measurement requires stressing the devices at high voltages, so AC waveforms up to $1000V_{PP}$ are expected. Therefore, it is necessary to scale down the voltage at the V_Y and V_X nodes. For this purpose, a parallel resistive-capacitive divider is used. Since there can be a DC bias to the AC waveform, the divider is followed by DC blocking capacitors and biasing resistors. The signal is then passed through a 50Ω buffer amplifier and another set of DC blocking capacitors to remove the bias, before it is sent using 50Ω microstrips to horizontal SMA connectors. This circuitry is displayed on Figure 5.1.

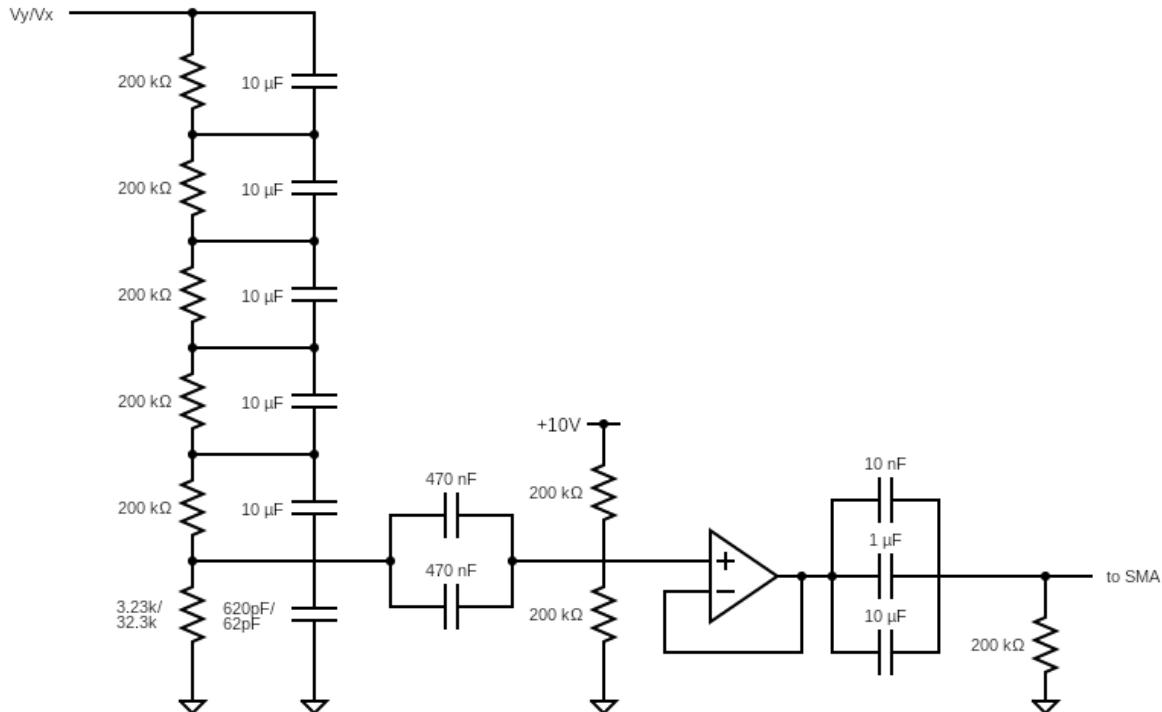


Figure 5.1: Voltage sensing circuitry

5.1 Resistive-capacitive divider

In DC and low frequency voltage dividers, a sequence of series resistors is used to divide voltage because it is much easier to get high-precision resistors (up to 0.01% tolerance) than capacitors (up to 1% tolerance) which could technically do the job too. However, at high frequencies, resistors are not enough because parasitic capacitances in the board could create a parasitic capacitive divider in parallel with the resistive one, affecting the division significantly especially during transients. Neither are capacitors enough, especially because of leakage currents, which is explained for example [here](#). Therefore, both capacitors and resistors were used. In order to minimize power dissipation, the resistors must be as large as possible without approaching parasitic resistances of the board, while capacitors must be as small as possible without approaching the parasitic capacitance. To divide 303:1 (for the V_Y node, where $1000V_{PP}$ must be divided to $3.3V_{PP}$), five $200k\Omega$ resistors and five $10pF$ capacitors were used, in series with a $3.23k\Omega$ and a $620pF$ capacitor respectively. To divide 30.3:1 (for the V_X node, where $100V_{PP}$ must be divided to $3.3V_{PP}$), five $200k\Omega$ resistors and five $10pF$ capacitors were used, in series with a $32.3k\Omega$ and a $62pF$ capacitor respectively. The choice of the capacitor values turned out to be problematic as discussed in depth in Chapter [7](#).

5.2 50Ω termination

Since the SMA cable carrying the signal to the PicoScope could load the voltage divider and change its division ratio, a voltage buffer is required. This buffer also minimizes the chance of reflection in the output transmission line, because if a 50Ω output buffer is used, followed by a 50Ω microstrip going straight into a 50Ω SMA connector and cable, there will be no impedance mismatch at this key part of the circuit which is ensuring that an accurate measurement is delivered to the PicoScope. However, because the buffer is ground-referenced through its negative supply rail, the potentially high DC voltage must be filtered out, which is done using two parallel $0.47\mu F$ capacitors. Although it would be ideal to get even higher capacitance, since the higher this capacitance the less it loads the capacitive divider in the circuit, anything larger than $0.47\mu F$ is extremely large and expensive given the large DC voltage rating necessary. The signal is then DC-biased at $5V$, halfway between the supply rails of the buffer. The choice of the buffer amplifier was itself quite difficult, since few amplifiers tolerate a large signal of a frequency up to $30MHz$ due to their low slew rate. For this reason, an ultra-high speed, open loop buffer with a $-3dB$ bandwidth at $780MHz$, a $4200V/\mu s$ slew rate, and an integrated 50Ω termination resistor was used, the [MAX4204](#). The opamp was verified in LTSpice using the manufacturer's device model.



Chapter 6

PCB Layout

The PCB design can be viewed in Figure 6.1. The following key considerations were made during its layout

1. A 2-layer 1.6mm board was selected, increasing the distance between signal and ground to minimize parasitic capacitance of the board.
2. Areas where the signal and ground plane overlap were minimized to minimize parasitic capacitance of the board. The area of V_y was overlooked in the original iteration, and had to be dealt with as explained in Chapter 7.
3. Particular focus was dedicated to making the current path through the inductors as direct as possible and thereby eliminating additional parasitic inductance from long current loops.
4. Reflections were avoided by minimizing the number of turns in the traces, where turns were inevitable, wider traces and small planes were used instead.
5. The two voltage dividers were laid out perfectly symmetrically, including the output buffers, which can each actually process two signals (including only one would create significant differences between the two paths). As the signal exits the buffer, it travels on a 50Ω microstrip straight into an SMA connector, which is positioned horizontally to minimize reflection. A ground plane was present below this entire segment of the circuit to minimize return path inductances and to enable the microstrip.
6. Relay drives were positioned at the perimeter of the board to prevent control signals from travelling near the Sawyer-Tower and the magnetic components.
7. The input from the Arduino was also positioned at the opposite side of the board from other inputs to make testing setup easier.

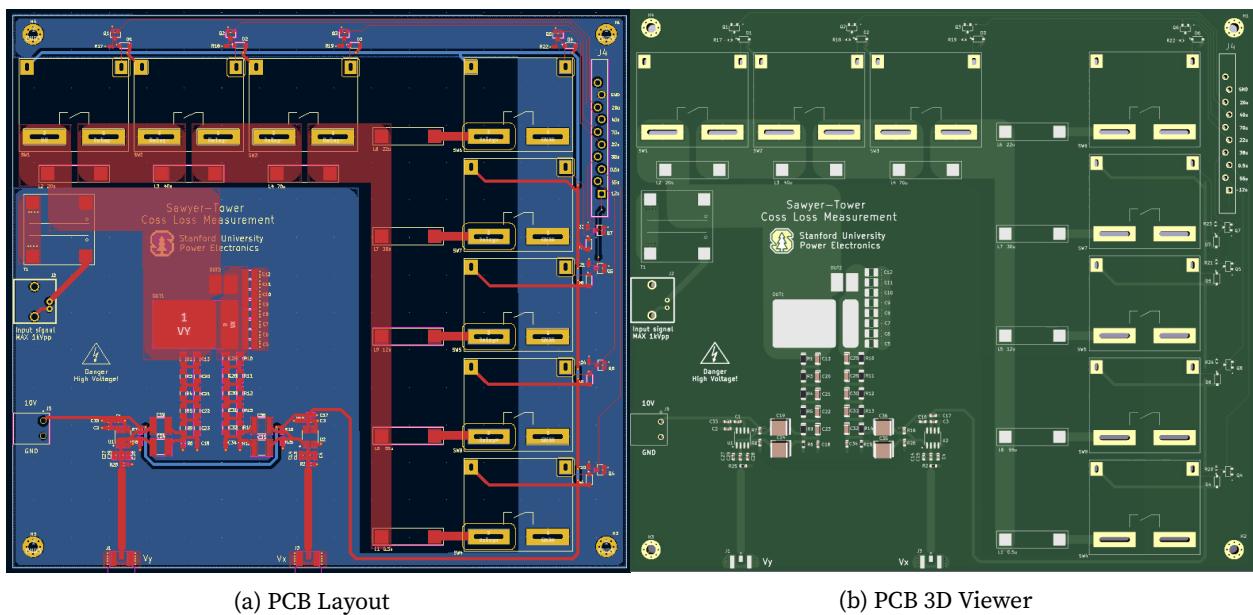


Figure 6.1: PCB Design



Chapter 7

Board Validation

The complete testing setup is documented on Figure 7.1.

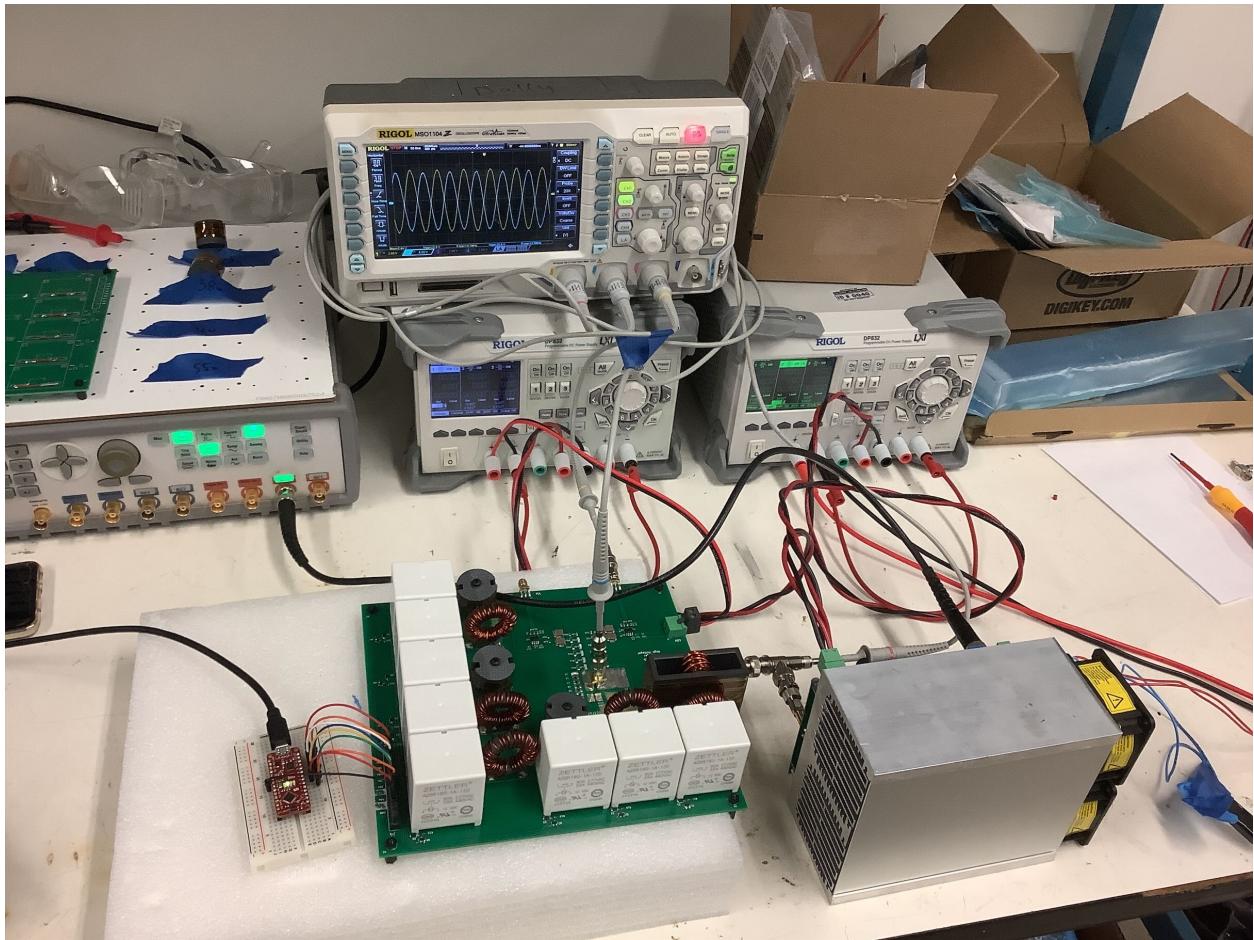


Figure 7.1: Complete setup with the power amplifier, signal input from a signal generator, and control input from an Arduino

In the sections below, I document how different parts of the circuit were tested and validated.

7.1 Inductor-Relay Network

After winding all the inductors and soldering them on the PCB, the setup was tested by shorting the transformer nodes and measuring the input impedance using a VNA for several different inductor combinations. At first, the circuit exhibited a lot of resonance in the frequency range of interest, which is up to $30MHz$ for the lowest inductance values and a couple MHz for the highest inductance values. In order to solve this, I first proceeded to rewind the inductors on toroids as described in Chapter 4 to lower the number of windings as well as increase spacing between the winding, thereby achieving lower parasitic capacitance. This helped minimally. However, as I was brainstorming where parasitic capacitance could come from, I realized that the V_y plane was unnecessarily large given that it was positioned directly over the ground plane. I proceeded to cut part of the V_y plane, which pushed the resonant peaks significantly. (Alternatively, the ground plane could be removed from under this segment of the circuit, although return path inductance loop must be avoided.)

By doing this, I was able to get the range of inductance demonstrated by the minimum and maximum value on Figure 7.4. The lowest inductance ($742nH$) now resonated at $27MHz$ and the highest inductance ($240\mu H$) now resonated at $2MHz$. Although the resonance was still very close to the applicable ranges, we decided to move on and test at frequencies below these boundaries for this iteration of the design.

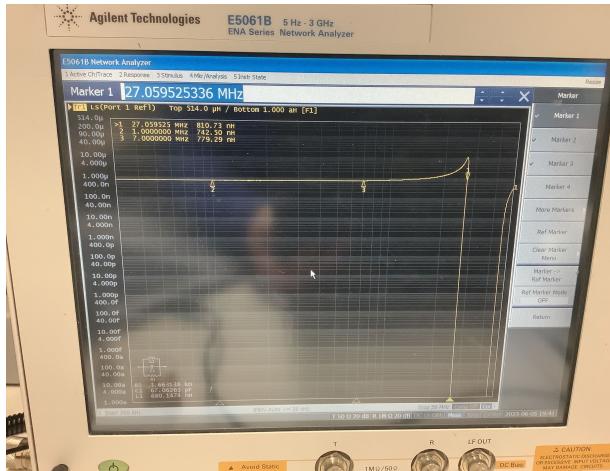


Figure 7.2: Minimum inductance combination



Figure 7.3: Maximum inductance combination

Figure 7.4: Range of inductance values achievable

The concerning part of the results is that the entire inductance range was shifted upwards from the expected range of $0.46\mu H$ to $185\mu H$. This could simply mean that we are too close to the resonant peak, but it could also suggest that there is parasitic inductance in the circuit. This made me realize that the effort not to overlap ground and signal planes in the matching network has inadvertently led to large return current loops, especially when it comes to the current returning from the five parallel inductor-relay sequences on the right side of the board. This could indeed be the culprit for the increased inductance, so for the next iteration, this should be solved by adding additional ground bridges under each of the five relays.

7.2 Transformer

Although the transformer operated well at open load conditions, when attached to the board, it exhibited highly non-linear behavior. Figure 7.5 shows a plot of the board's input impedance with the transformer.

As seen on the VNA plot in Figure 7.5, the board exhibits resonance at relatively low frequencies, deep in the range necessary for C_{OSS} loss measurements. Due to time constraints, this issue was not resolved yet. However, it poses important questions about the viability of the impedance matching network.





Figure 7.5: Input impedance of the board measured by a VNA with transformer in place.

7.3 Voltage divider

The V_Y divider was expected to divide a $1000V_{PP}$ waveform to a $3.3V_{PP}$ waveform, therefore its division ratio was roughly 303. However, during initial tests, the division ratio was much higher than expected (roughly 470 at $1MHz$) and behaved nonlinearly with frequency. Therefore, I proceeded to debug the circuit, first isolating that the issue lied in the divider itself rather than the buffer, and then probing each stage of the buffer to figure out a division relationship, as seen on Figure 7.6, using a very small ground loop on the pin so as to not add inductance to the measurement.

The probing showed that most of the AC amplitude dropped across the first level of the divider, and each subsequent level dropped less and less. Since most of the capacitors were $10pF$ capacitors, I realized that the problem might be that the parasitic capacitances are too similar in value. Using an LTSpice simulation, I confirmed that the parasitic trace capacitance (estimated based on the area) to ground at each node of the divider combined with the $5pF$ probe would produce very similar results. Therefore, I proceeded by multiplying all the capacitances by 10 and resoldering the divider with these new higher capacitors, which indeed minimized the effect of the parasitics, such that the division ratio was now much closer to the desired ratio as well as much more stable in frequency. In addition, I tuned the capacitor on the last level of the divider to match the ratio perfectly. The final value chosen for it was $5800pF$ (instead of the $6200pF$ gained by simply multiplying the original value by 10) in the V_y divider which I used for debugging. Although the divider now produced much more stable results, there was still some left over frequency drift to its division ratio - from 306 at $1MHz$ to 433 at $30MHz$.

Possible methods of improving the divider circuit include:

1. Decreasing the spacing between capacitors and resistors in the divider to minimize trace area and therefore minimize parasitic capacitances.
2. Changing the dielectric of the PCB from FR4 to other high-Q materials such as teflon to minimize nonlinearities in the parasitic capacitances.



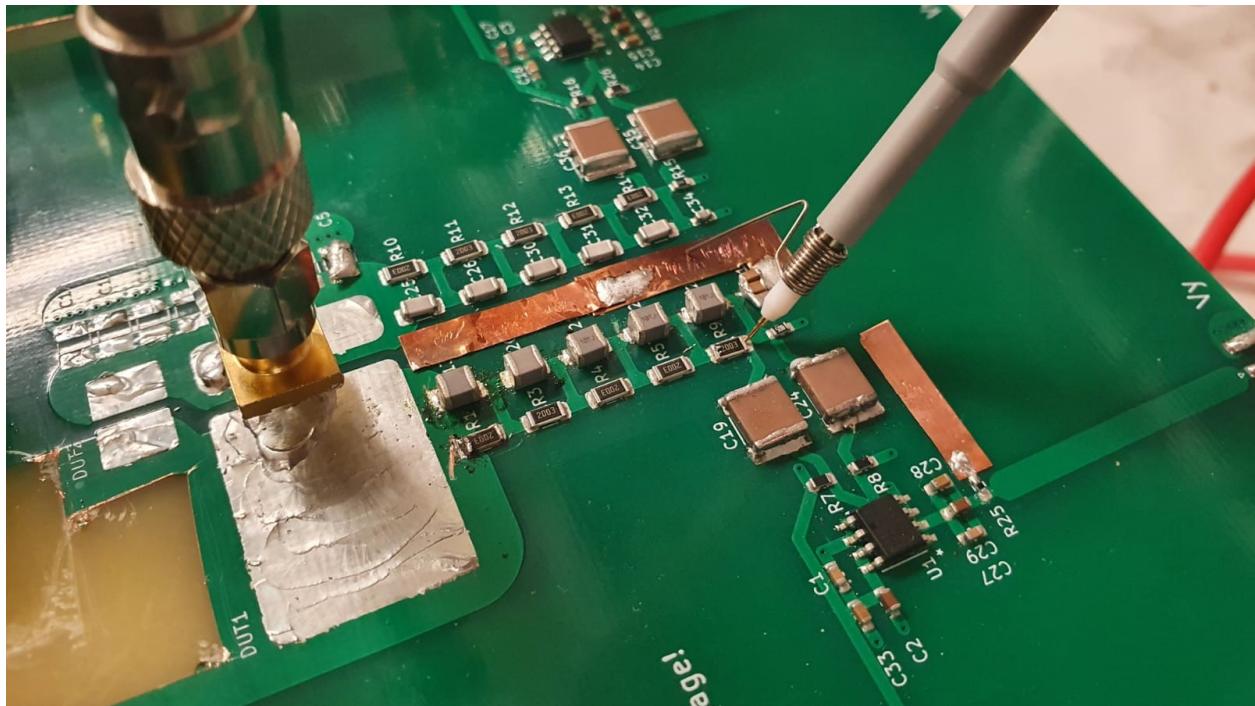


Figure 7.6: Debugging the voltage divider using a scope with a miniature ground loop and a copper tape to extend nearest ground within reach of the probe, in effort to maximize accuracy of the measurement.

Chapter 8

Next Steps

The biggest challenge going forward will be to push the resonance in the input impedance outside of the 500kHz to 30MHz frequency range of interest. This might be done by redesigning the transformer, or by rearranging the inductor bank to achieve the same inductance range with fewer large inductors (with significant capacitance). Alternative ideas mentioned during the project presentation could also be pursued: for example, instead of matching the device capacitance with a bank of inductors, a fixed inductor could be matched with a bank of capacitors in series/parallel with the device under test. This would be a much more spatially compact design and it would prevent significant parasitics coming from the large inductors. If all attempts at implementing a parallel LC match fail, a series LC match might need to be implemented instead.

Secondly, the voltage dividers were until now only verified on their own. A key step will be verifying that the division ratios do not change with respect to each other, and that the phase shift of the two dividers is the same. The cause of the slight frequency shift must also be debugged.

Finally, the board must be tested as a whole, and results for the C_{OSS} measurement must be compared to the original measurement method.

References

- Fedison, J. B., and M. J. Harrison. 2016. “COSS Hysteresis in Advanced Superjunction MOSFETs.” In *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 247–52. <https://doi.org/10.1109/APEC.2016.7467880>.
- Fedison, JB, M Fornage, MJ Harrison, and DR Zimmanck. 2014. “C OSS Related Energy Loss in Power MOSFETs Used in Zero-Voltage-Switched Applications.” In *2014 IEEE Applied Power Electronics Conference and Exposition-APEC 2014*, 150–56. IEEE.
- Roig, Jaume, and Filip Bauwens. 2015. “Origin of Anomalous C_{OSS} Hysteresis in Resonant Converters with Superjunction FETs.” *IEEE Transactions on Electron Devices* 62 (9): 3092–94. <https://doi.org/10.1109/TED.2015.2455072>.
- Roig, Jaume, German Gomez, Filip Bauwens, Basil Vlachakis, Maria R. Rogina, Alberto Rodriguez, and Diego G. Lamar. 2018. “High-Accuracy Modelling of ZVS Energy Loss in Advanced Power Transistors.” In *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 263–69. <https://doi.org/10.1109/APEC.2018.8341020>.
- Sawyer, Charles Baldwin, and CH Tower. 1930. “Rochelle Salt as a Dielectric.” *Physical Review* 35 (3): 269.
- Scott, JF. 2007. “Ferroelectrics Go Bananas.” *Journal of Physics: Condensed Matter* 20 (2): 021001.
- Zulauf, Grayson, Wei Liang, Kawin Surakitbovorn, and Juan Rivas-Davila. 2017. “Output Capacitance Losses in 600 v GaN Power Semiconductors with Large Voltage Swings at High- and Very-High-Frequencies.” In *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 352–59. <https://doi.org/10.1109/WiPDA.2017.8170572>.
- Zulauf, Grayson, Sanghyeon Park, Wei Liang, Kawin North Surakitbovorn, and Juan Rivas-Davila. 2018. “ C_{OSS} Losses in 600 v GaN Power Semiconductors in Soft-Switched, High- and Very-High-Frequency Power Converters.” *IEEE Transactions on Power Electronics* 33 (12): 10748–63. <https://doi.org/10.1109/TPEL.2018.2800533>.

Appendix A

Arduino Code

A.1 Relay drive

```
// Pin numbers driving each inductor (in order of layout on board)
const byte u70 = 6;
const byte u40 = 7;
const byte u20 = 8;
const byte u22 = 9;
const byte u38 = 10;
const byte u05 = 11;
const byte u55 = 12;
const byte u12 = 13;

void setup() {
    // configuration of pins to be low by default (relay open)
    for (byte i = 6; i < 14; i++) {
        pinMode(i, OUTPUT);
    }
    for (byte i = 6; i < 14; i++) {
        digitalWrite(i, LOW);
    }

    // Initialize serial communication
    Serial.begin(115200);
    Serial.println("Setup completed");
}

// set desired combination
void loop () {
    digitalWrite(u20, HIGH);
    digitalWrite(u40, HIGH);
    digitalWrite(u70, HIGH);
    digitalWrite(u22, LOW);
    digitalWrite(u38, LOW);
    digitalWrite(u05, LOW);
    digitalWrite(u55, LOW);
```

```
    digitalWrite(u12, LOW);
    delay(100000);
}
```

