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Design of a single-output DC-DC flyback converter for off-grid solar applications

Introduction

This paper outlines the design of a single-output DC-DC flyback converter intended for off-grid conversion of power from a solar panel for use by a water purification system as seen on Fig. 1.

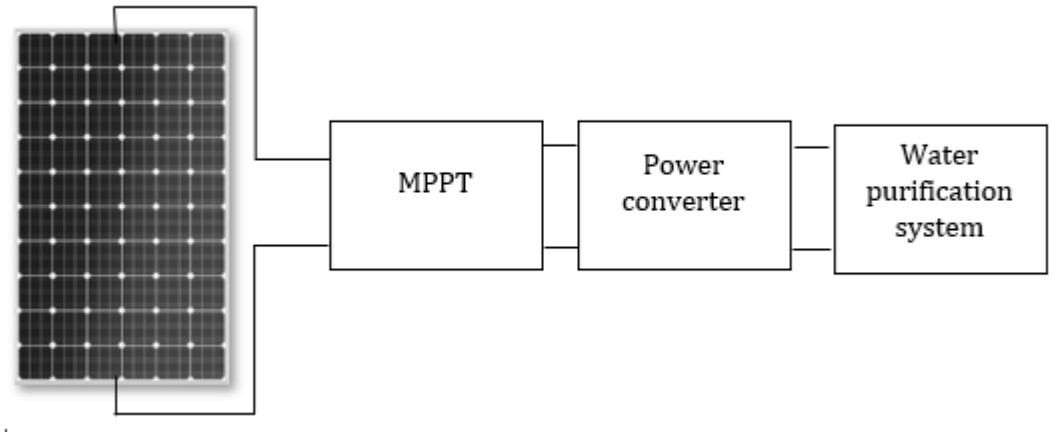

Figure 1: Block diagram of system setup

State of the art DC-DC off-grid power converters connected to solar panels implement direct power point tracking, using a digital processor to sense the current I-V curve of the module and setting output voltage and current to maximize the power drawn. Most common MPPT methods include 'perturb and observe', or 'incremental conductance method' [1]. It is also common for a power converter for a large PV installation to perform DC-AC conversion, so that the output of the system is comparable to an outlet from the electric grid. However, conversion to AC is not necessary for this design. This design is intended for remote applications, where the main factors are low price and durability of the design.

These considerations informed the choice of an isolated flyback converter. Galvanic isolation in off-grid solar converters is not very common, however, in our case it allows us to reduce stress on the semiconductor switches, extending their lifetime. In general, the low number of components and the fact that the core is reset automatically allows for desired simplicity and lower price. Additionally, if different nominal voltage is needed on the output because of different equipment chosen, the flyback can be easily reconfigured to either buck or boost the output voltage.

Specifications

The goal of this design is to:

1. Minimize the price of the converter. Similar 30W converters can be bought on DigiKey for a price between $20-50. The aim is therefore to stay within this range for our design.

2. Maximize the efficiency of the converter. Since the nominal output power of the solar panel is close to the operating power of both loads, the design will prioritize minimal power loss, aiming for an efficiency of 90%.
3. Since the off-grid is supposed to be operational on a daily basis over multiple years (at minimum 5 years - the lifetime of the water purification system before filter must be replaced). Therefore, the design will closely examine device stresses and leave wide margins in component ratings to prevent failure.

Nominal operating conditions have been chosen for interfacing NPA30S-12H solar panel with the S5Q-P/12VDC Viqua water purification system (see both datasheets attached).

	Nominal value
$\mathbf{V_{in}}$	16.77V
$\mathbf{V_{out}}$	12V
$\mathbf{I_{out}}$	1.8A
$\mathbf{P_{max}}$	21.8W
$\mathbf{R_{eq}}$	6.7Ω

Input ranges: The converter is designed to operate at input voltages spanning from 10V to 18V, accounting for temperature and irradiance changes, and spanning the approximate range over which the IV curve is able to supply the minimum power necessary for the appliance to function. In terms of current, the range translates to roughly 1-2A, which shows the device IV curve for the NPA30S-12H solar panel available in its datasheet.

Switching frequency: We will first choose the switching frequency. The industry standard for solar switching converters is between 100-250kHz. The higher the switching frequency, the lower the sizes of energy storage components, namely the magnetizing inductance and the capacitance. However, since the power supply is regulated by EU EN 61000-6-3 which has a tighter requirement above 150kHz, we will set the frequency right below that level $f_s = 140\text{kHz}$.

Output ripple specifications: The water purification system is essentially an LED lamp, and the manufacturer does not include its allowable voltage range or ripple in its datasheet. While we can assume that the appliance is quite insensitive to ripple in output voltage, we will start conservatively. We can assume the acceptable voltage range to be +/-3V volt from the maximum current and power specified in the datasheet. If we allow the ripple to cover a third of this range, according to the equation below, we get an output ripple specification of approximately 8%.

$$R_C = \frac{1}{2}\frac{\Delta V_{out}}{V_{nominal}}$$

Control bandwidth: We will try for the bandwidth to simply be as high as possible. We know that our average models will only be reliable up until 1/10th of the switching frequency, so we can set a goal of 14kHz.

Transient times: According to a study on grid-tied solar inverters, transient times are on the order of 1 millisecond. Since our system is not grid-tied, we can lower the requirements, but we shall aim for 1-10ms [2].

EMC standards: There seems to be a lack of clarity in the industry as to what EMC standards should be followed, as exemplified by a multitude of news reports on solar power equipment not following any standards. However, a consensus seems to point to the CISPR 14 standard for residential appliances [3], which prescribes the quasi peak to be 79dBµV for the range between 150kHz and 500kHz, and 73dBµV for the range between 500kHz and 30MHz.

Design

1. Switching converter

Figure 2 shows the circuit-level implementation of the design. The flyback converter is composed of one primary and one secondary winding, with a transformer separating the two.

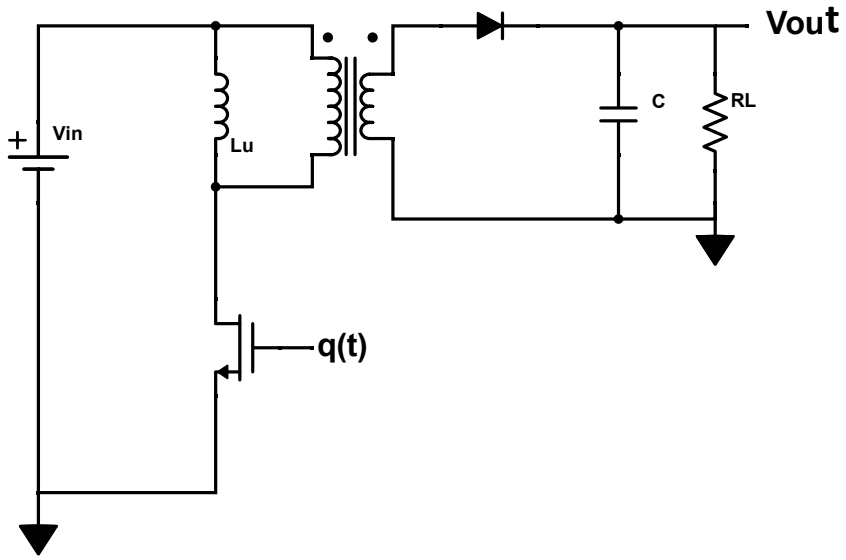

Figure 2: Basic converter topology

For sizing of individual components, we will use an average DC equivalent model.

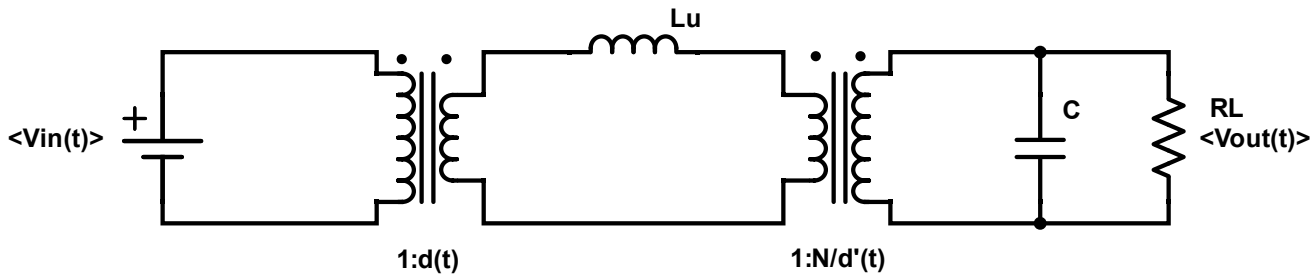

Figure 3: DC average equivalent circuit model

The conversion ratio of the ideal flyback in DCM is $\frac{V_{out}}{V_{in}} = \frac{DN_T}{D'}$. Notice that we have two degrees of freedom in setting the conversion ratio – we can vary both the turns ratio and the duty cycle. Because the design is meant to be durable and reliable, we will first select the duty cycle, which we will do by analyzing stress in the semiconductor (which happens to be the same as the stress in the diode). The analysis shows that the stress is expressed as:

$$S_q = P_{out}\left[\frac{1}{D(1-D)}\right]$$

which is minimized when D=0.5. With this chosen value, we can then calculate $n_T = \frac{N_2}{N_1}$, getting $n_T = 0.72$.

Since our design focuses on efficiency, we will operate the converter on the boundary of CCM and DCM where the switching losses are significantly decreased because of minimal voltage-current overlap on the MOSFET current's rising edge. Therefore, we set the ripple ratio in the magnetizing inductance to be equal to 1, i.e., $\mathcal{R}_L = 1$ and we can size the magnetizing inductance according to the following equation, getting:

$$L_\mu = \frac{RT(1-D)^2}{2(N_{T2})^2}$$

Similarly, we can derive the capacitor value. See summary of values below:

	Parameters
f_s	140kHz
D	0.5
n_T	0.72
L_μ	11.5µH
C	3.33µF

By simulating the switching operation of the converter in LTSpice, we see that our requirements on the nominal operation were met. Measurements suggest that 21.57W were delivered to load at 12V DC, with acceptable voltage ripple. Since we pulled only 21.57W from the source operating close to 100% efficiency (since no non-idealities were modelled), it only supplies 1.29A of current on average, which does not correspond exactly to the IV curve of the panel. This however is simply a lack of complexity of the LTSpice model. After we implement feedback control, the converter will be able to adapt the drawing voltage and current, which was not possible in this particular simulation. The model was however useful for measuring the maximum currents and voltages for both semiconductors to ensure their proper selection in the upcoming section.

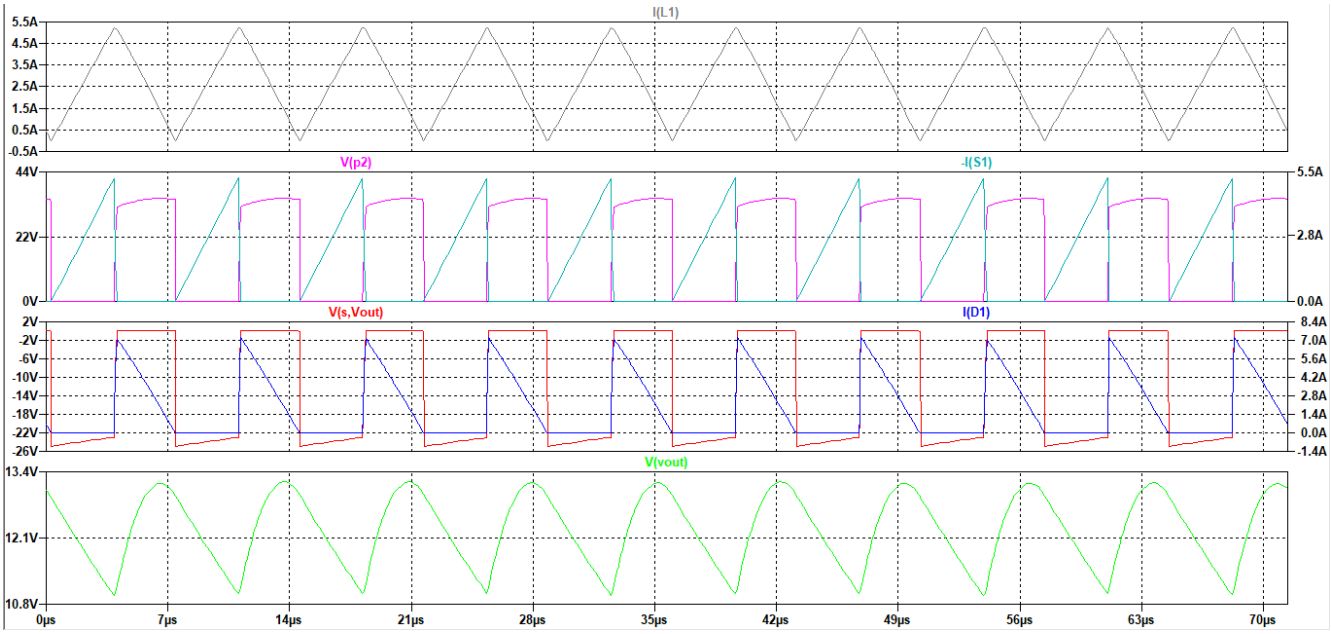

Figure 4: Nominal switching operation, plots include: 1) Magnetizing current, 2) MOSFET voltage and current, 3) Diode voltage and current, 4) Output voltage

We can now size all important components for the core converter topology:

Component	Requirements	Digi-Key ID	Specifications
Input connector	Max voltage 20V, Max current 2A, 3 inputs (GND, Vin, Vmpp)	796689-2 (well above needed rating)	300V, 17.5A, 2 pins (2 connectors will be used to accommodate all inputs)
Transformer	Magnetizing inductance 11.5uH, max current 5.5A, air gap, turns ratio 0.72	750311797	Magnetizing inductance 14uH, max current 11.5A, air gap, turns ratio 0.75
MOSFET	Avg current = 2.5, Max current = 5.5A, Max V_{dss}=36V, Lowest R_{dson} possible	IRFL024NPbF	Avg current = 2.8A, max pulsed current = 11.2A, V_{dss}=55V, R_{dson}=75mΩ

Diode	Max current =7A, Max V_r=25V, Lowest V_f possible (ideally Schottky)	SL23-E3/52T	V_{rmax}=30V, AVG current=2A, Vf@2A=0.42V, Vf@10A=0.6V
Capacitor	3.33uF, voltage rating >18V	C1608JB1E335M080AC	3.3uF, voltage rating = 25V
Output connector	Max voltage=15V, Max current=2A	796689-2 (well above needed rating)	300V, 17.5A

Feedback control

In this section, I will present the design of a PID controller, which was selected to enable a correction for the flyback's right half plane zero. The linearized equivalent circuit model that was used to derive the transfer functions of the controller can be seen on Fig. 5.

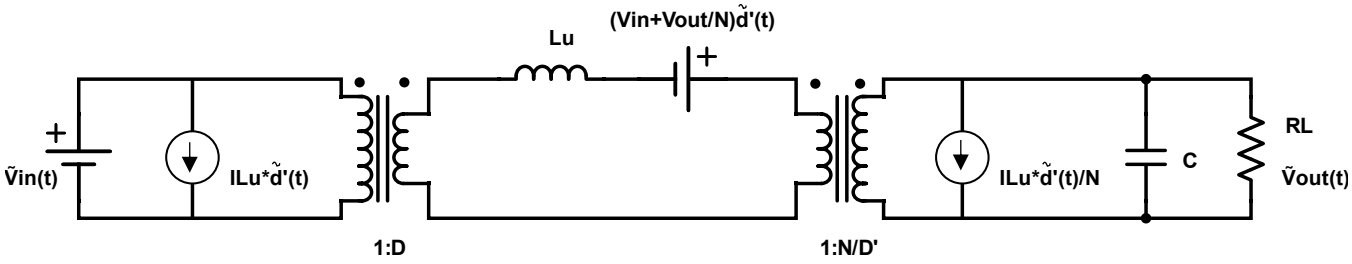

Figure 5: Linearized small signal equivalent model

For LTSpice simulations, the previously shown averaged circuit model was used. The transfer function from the duty cycle to the output voltage, $H_{od}(s)$ can be seen on Fig. 6.

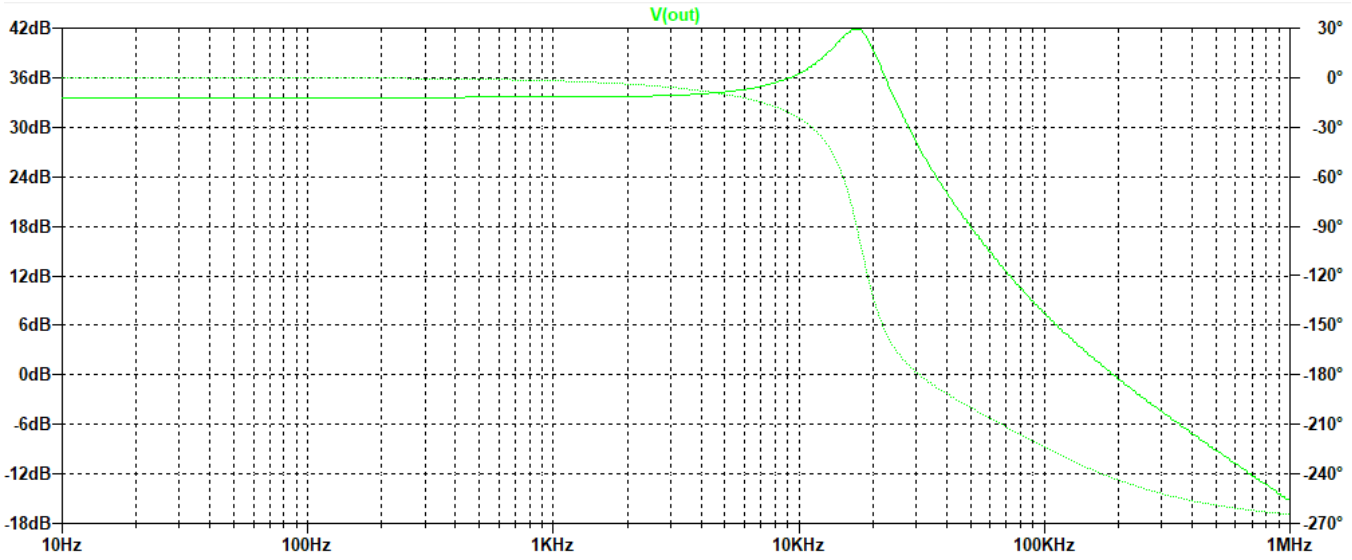

Figure 6: Hod(s) transfer function

To create a full feedback look, the output voltage must first be sensed, then passed through the PID compensator, and then fed through a pulse width modulator and a gate drive to determine the duty cycle needed for the correct output, as seen on Fig. 7. The unity buffer is provided to de-couple the sensor from the PID compensator.

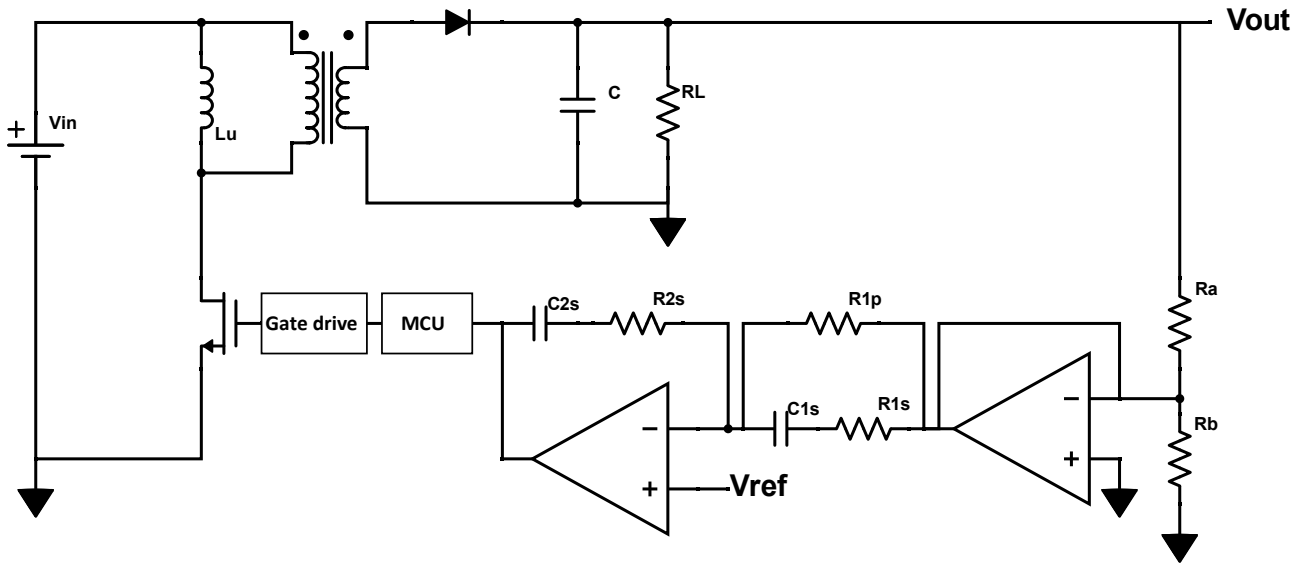

Figure 7: Circuit topology with feedback control

The equivalent block diagram below represents the loop, whose gain can be expressed as

$$L(s) = H(s) * I(s) * G(s) * \frac{1}{Vm} * Hod(s)$$

where H(s) is the sensor gain, I(s) the unity buffer gain (=1), G(s) is the compensator gain, V_m is the scalar of the pulse width modulation (in our case we can use V_m=1 because PWM will be implemented digitally using a microcontroller configured in analog comparator mode), and H_{od}(s) is the gain of the converter.

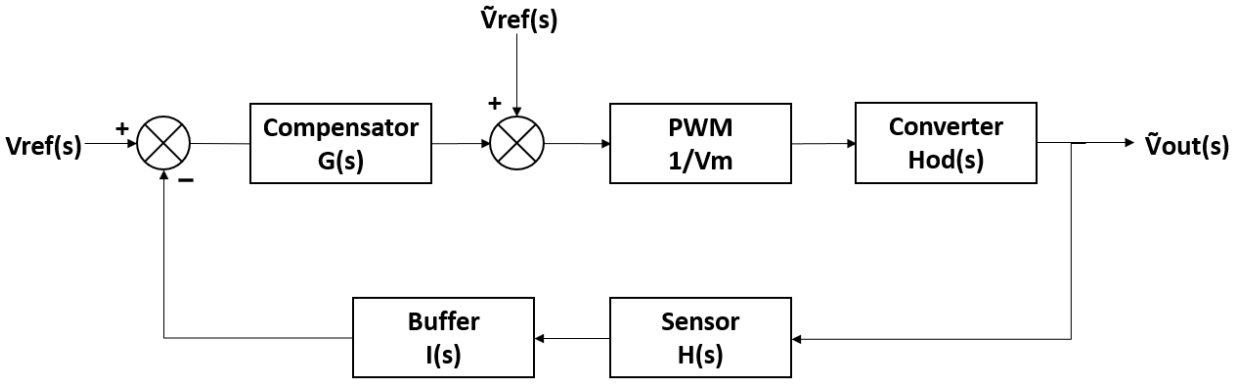

Figure 8: Feedback loop block diagram

Let's first discuss H(s). To maintain the load unaffected, we need the equivalent resistance of R_a and R_b to be significantly larger than the resistance of the load. R_a and R_b can be calculated from the equation of the voltage sensor gain, which we want to be equal to the inverse of the converters conversion ration so that we can use the maximum power point voltage as the voltage reference for which we are trying to control. However, this is not possible with a simple resistive divider, because R_a would have to be negative as seen from the equation below.

$$H(s) = \frac{R_b}{R_a + R_b} = \frac{1}{0.72}$$

Therefore, the MPPT must be designed to output the maximum power point voltage divided by four so that it lies within the operating range of the operational amplifier. We must now also divide H(s) by four:

$$H(s) = \frac{R_b}{R_a + R_b} = \frac{1}{4 * 0.72}$$

We choose R_a=150kΩ and R_b=80kΩ.

If we take G(s) = 1, we get the uncompensated loop gain of the system, which can be seen on Fig. 9.

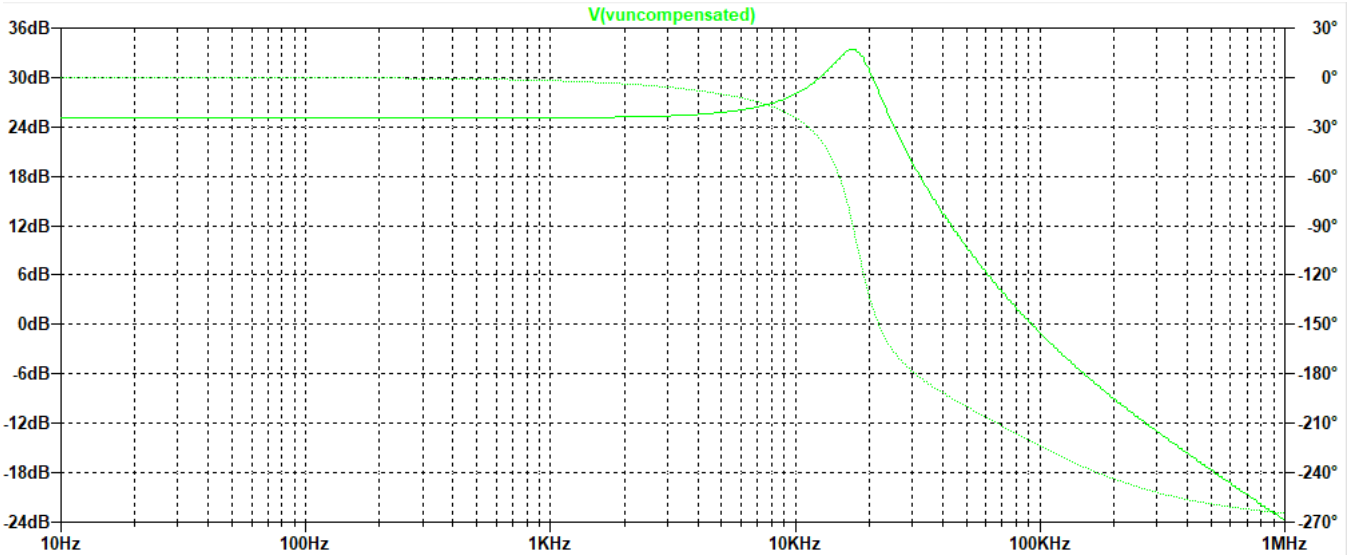

Figure 9: Uncompensated loop gain L(s)

It is clear that the uncompensated loop gain will lead to an unstable system, because the phase at the crossover frequency of 90kHz is -221°. Because our target crossover frequency is only 14kHz, we can 1. push the crossover frequency to the left which alone will decrease the phase and 2. design the PID's phase lead to be centered close to that frequency to achieve further gain increase at that point.

The selected components (see table at end of section) achieve precisely this. The compensated loop gain can be seen on Fig. 10. Phase margin 18° at 42kHz. Since the bandwidth is above 10th of switching frequency, we have reached our goal. The phase margin could be further increased by lowering the DC gain on the compensator, however, that would risk not satisfying the requirement for L(s) >> 1 for frequencies between 500Hz and 5kHz.

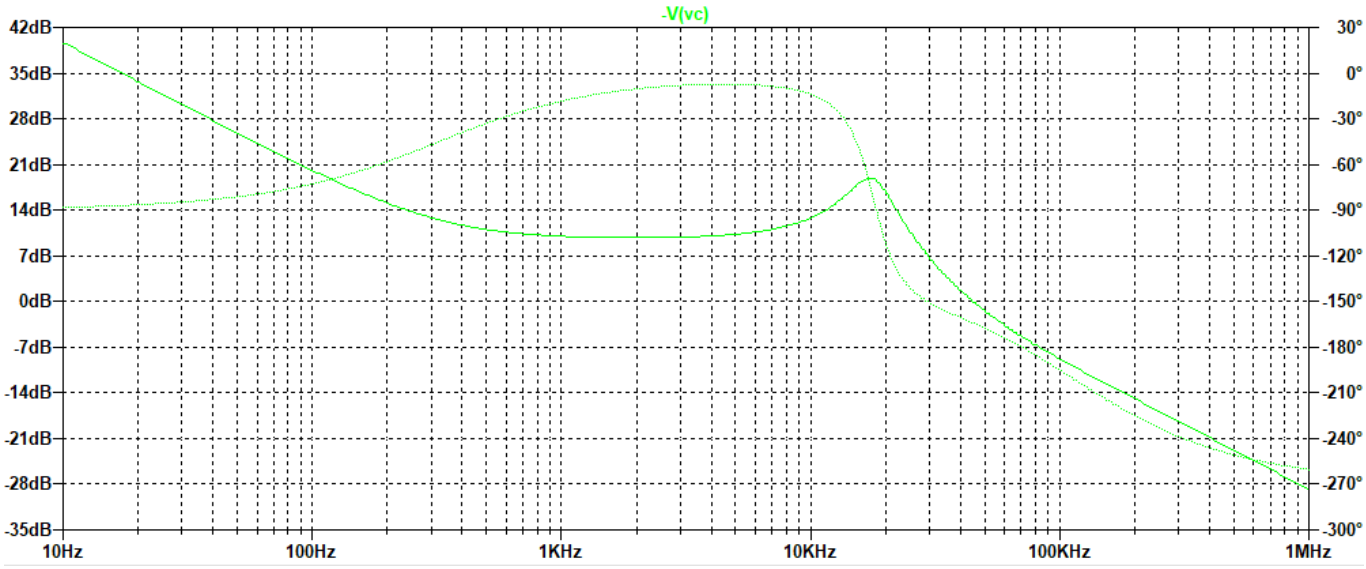

Figure 10: Compensated H(s)

From Fig. 11, we can also see that the crossover frequency falls correctly within 3° of the largest phase lead provided by the PID compensator.

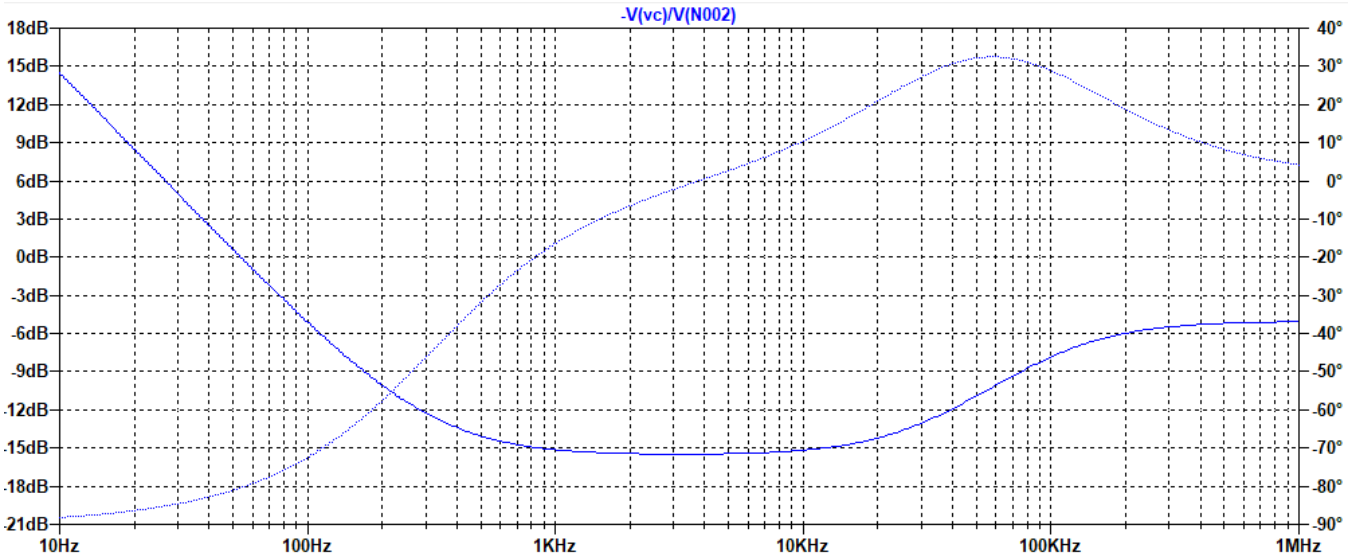

Figure 11: G(c)

In transient simulation of a step decrease of input voltage from 18 to 12V, the output voltage and current recover within 5ms, which fits perfectly within our target range of 1-10ms.

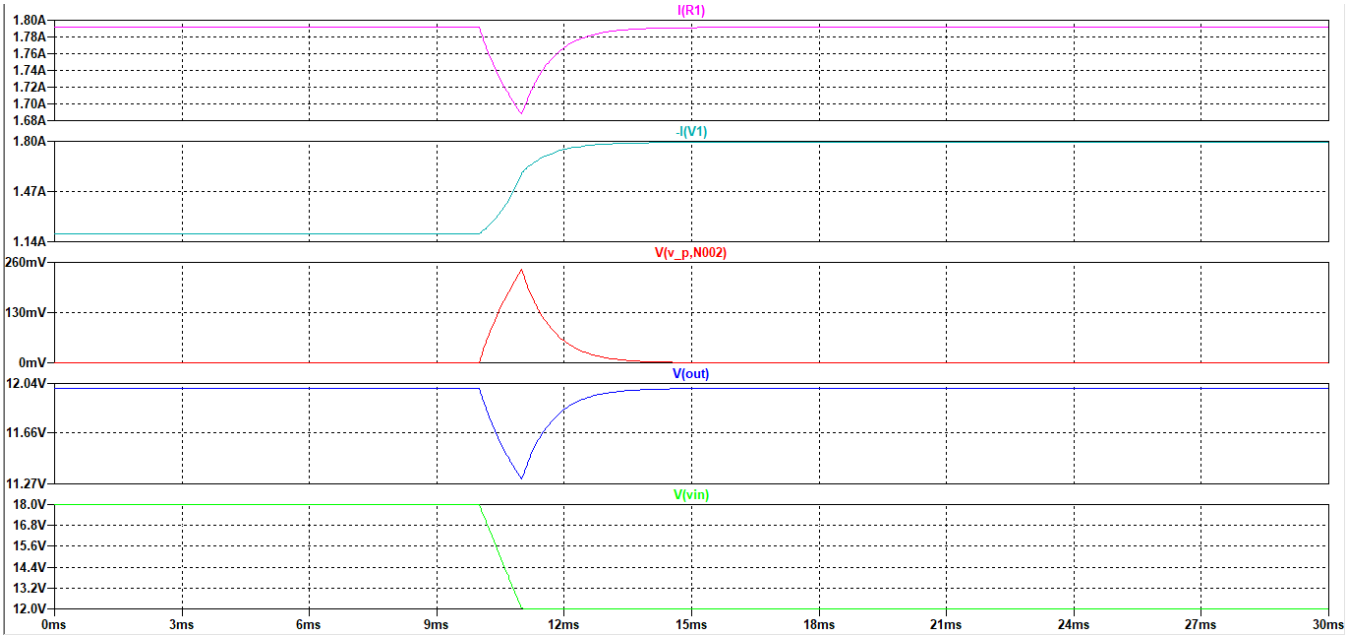

Figure 12: Transient simulation, 1) Output current, 2) Input current, 3) Error signal, 4) Output voltage, 5) Input voltage

The components selected for the control system are outlined below:

Component	**Requirements**	**Digi-Key ID**	**Specifications**
R_a	150kΩ, 0.4W, high precision	CR011503F	150kΩ, 1W, high precision (1%)
R_b	80kΩ, 0.2W, high precision	PTN1206Y8002BST1	80kΩ, 0.4W, 0.1%
Buffer operational amplifier	2.7V to 6.0V single supply	MCP601	Supply voltage: Vdd=2.7-6V, Vss=0
R_{1p}	300 Ω, 1/4W	RM12F3000CT	300Ω, 250mW, precision (1%)
R_{1s}	127 Ω, 1/4W	RM12F1270CT	127Ω, 250mW, precision (1%)
C_{1s}	12nF, >5V	GMC10CG122F50NT	12nF, 50V, 1%
C_{2s}	10µF, >5V	C2220C106J5RAC7800	10µF, 50V, 5%
R_{2s}	50 Ω, 1/4W	RW1S0BA50R0FE	50Ω, 1W, precision (1%)

Compensator operational amplifier	2.7V to 6.0V single supply	MCP601	Supply voltage: Vdd=2.7-6V, Vss=0
Microcontroller	frequency > 140kHz	MC9RS08KA2	Supply voltage: Vdd<5.8V (defined by max input voltage), Vss=0
Isolated gate driver	Galvanic isolation, drives 4V	ADUM6132	Supply voltage: Vdd= 4.5-5.5V, Vss=GND

Input filter

Fig. 13 shows the FFT of the voltage seen by a testing LISN in dBµV. It is clear that an unfiltered converter does not satisfy the standard. Therefore, and input filter must be designed. The complete topology with the filter can be seen on Fig. 14.

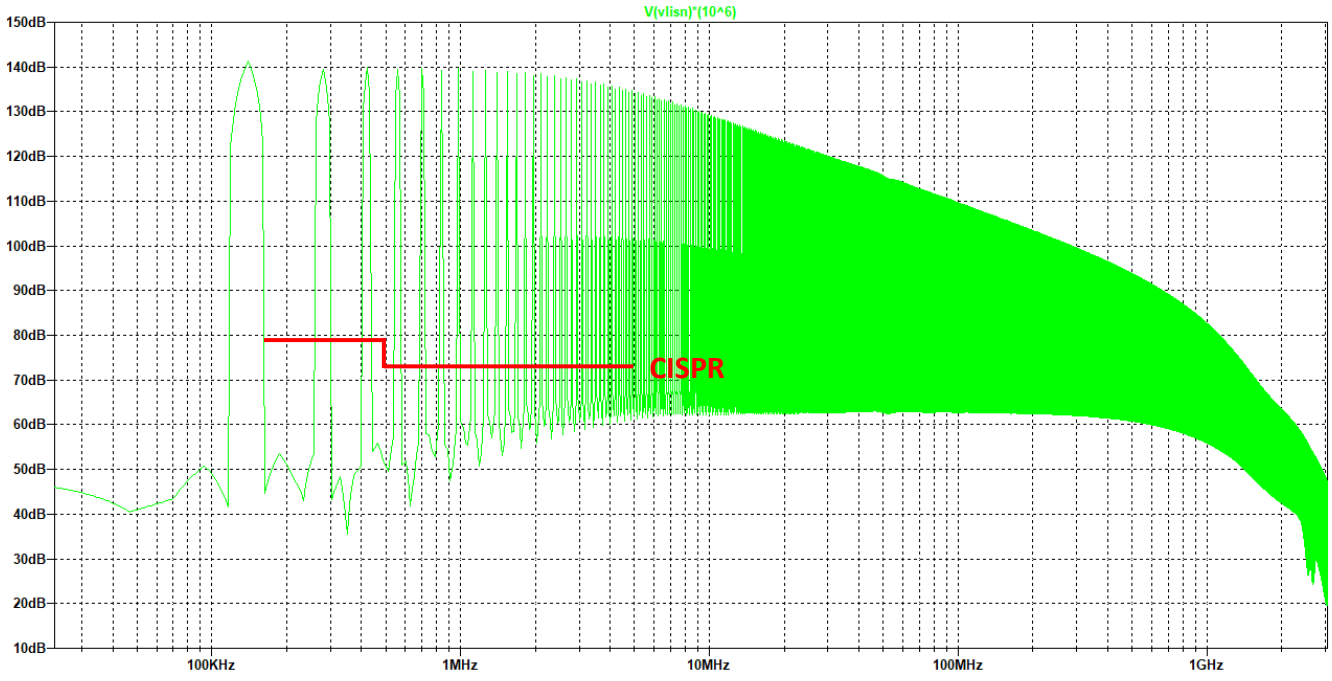

Figure 13: FFT without input filter

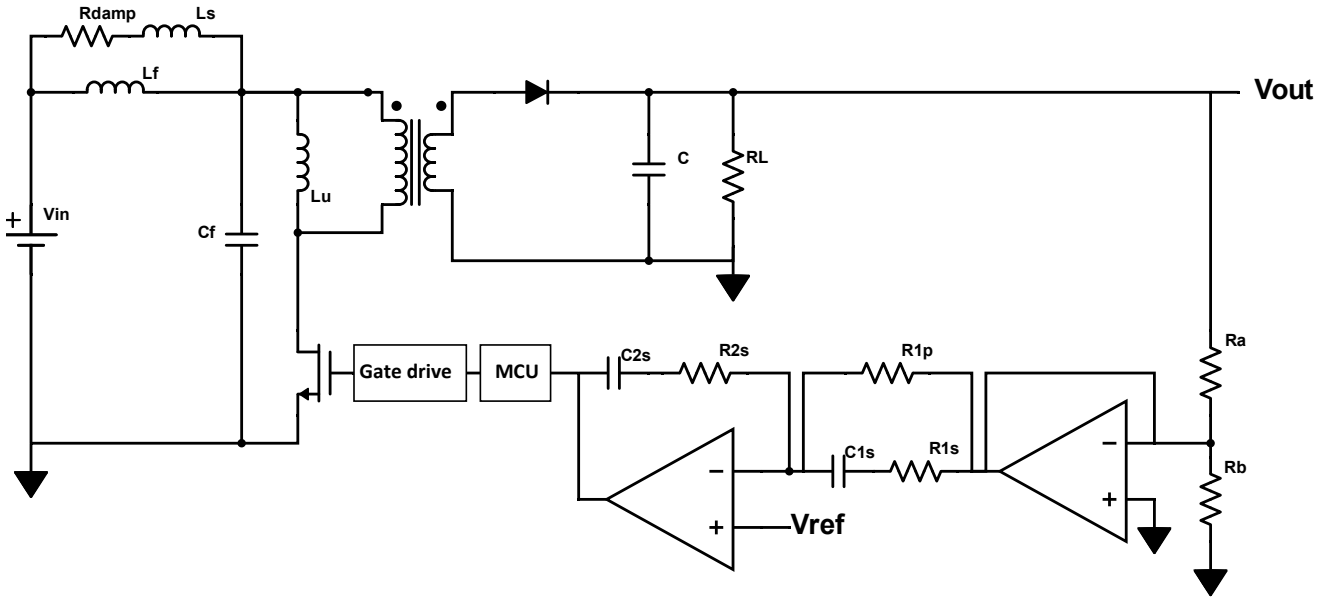

Figure 14: Circuit topology with input filter

To achieve the standard, we must make sure the second harmonic (first harmonic is outside the regulated range) is attenuated from 139dBµV to 79dBµV, requiring a 60dBµV attenuation at 280kHz, which means we must place the corner frequency of our LC filter 1.5 decades earlier, at 8.85kHz, informing our choice of inductance of 6.8 µH and capacitance of 47 µF (both commercially available values). To size the damping resistance, which will be placed in parallel to the inductor, Middlebrook's extra element theorem was used to ensure that the effective impedance of the filter is lower than the driving and null impedances, so that the Hod(s) transfer function of the converter remains unchanged. This led to a choice of resistance of 300mΩ and a small series inductance of 1pH. With this choice of components, we can achieve at least a 10dB separation between the impedances at all frequencies, as seen on Fig. 15.

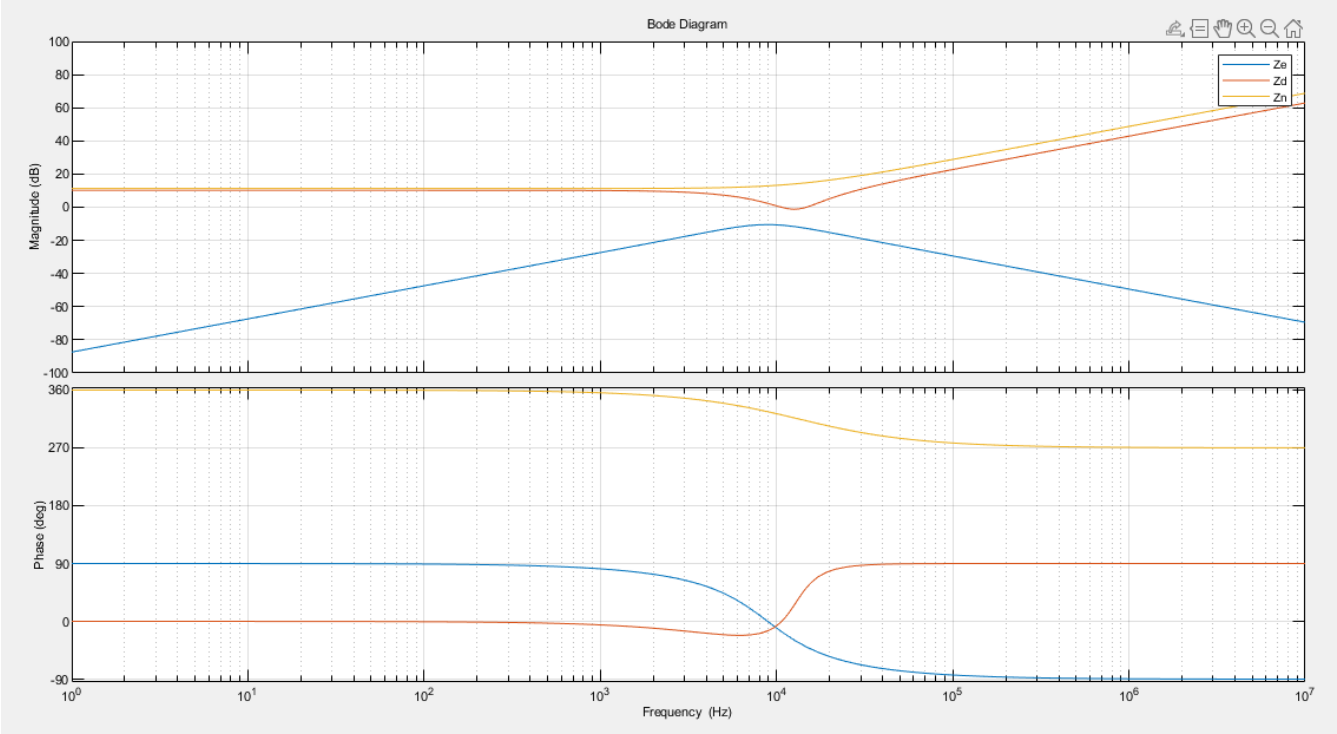

Figure 15: Comparison of Z_e - the filter impedance, Z_n - the null impedance, and Z_d - the driving impedance

The FFT of the voltage perceived by the LISN now perfectly satisfies the CISPR requirement as seen on Fig. 16. The fact that we used resistance in parallel to the inductor instead of the conductor made it possible to have small energy storage elements, decreasing overall dimensions of the filter.

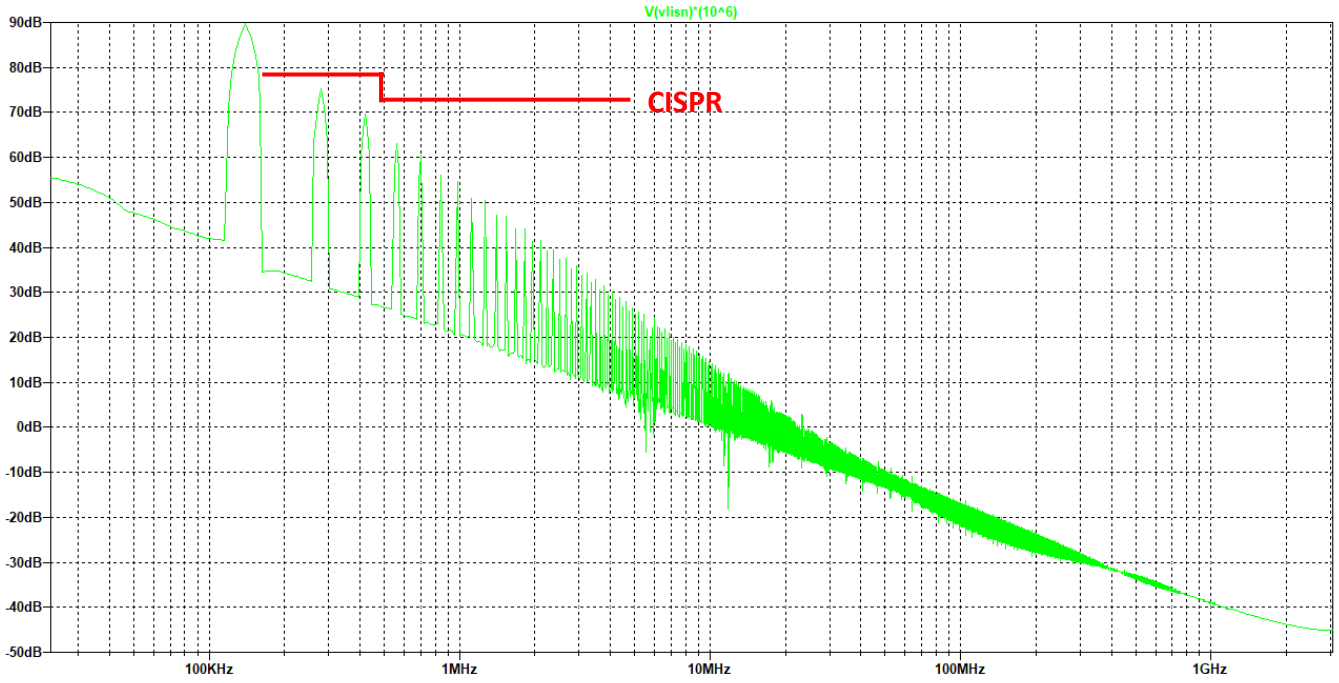

Figure 16: FFT with input filter

Components of the filter are summarized below:

Component	**Requirements**	**Digi-Key ID**	**Specifications**
C_f	47uF, voltage > 20V	KTJ500B476M76BFT00	47uF, voltage =50V
L_f	6.8uH, current > 5.5A	SRP1270-6R8M	6.8uH, current = 12A
L_s	1pH	ATFC-0201HQ-0N1B-T	100pH (smallest available), lowest DCR (50mΩ)
R_{damp}	300mΩ, 0.5W	RCWE1210R300FKEA	300mΩ, 1W

Isolation

Isolation of the converter was achieved by placing a transformer on the path from input to output voltage, and a galvanically isolated gate drive on the path from the feedback loop sensor to the MOSFET regulating the duty cycle.

Auxiliary power supplies

The microcontroller, both operational amplifiers, and the gate drive all use ground for V_{ss}, and have overlapping ranges for V_{dd} such that we can choose V_{dd}=5V. The simplest approach will be implemented by adding a parallel voltage divider at the output where we can ensure the voltage will be stable. Large

resistors will be chosen so that little power is dissipated. To get 5V from a 12V power supply, we choose R_{aux1}=120kΩ and R_{aux2}=50kΩ. This way, we lose only 0.8mW of power. Again, we install a unity buffer to prevent loading from the other components. The complete circuit diagram is below:

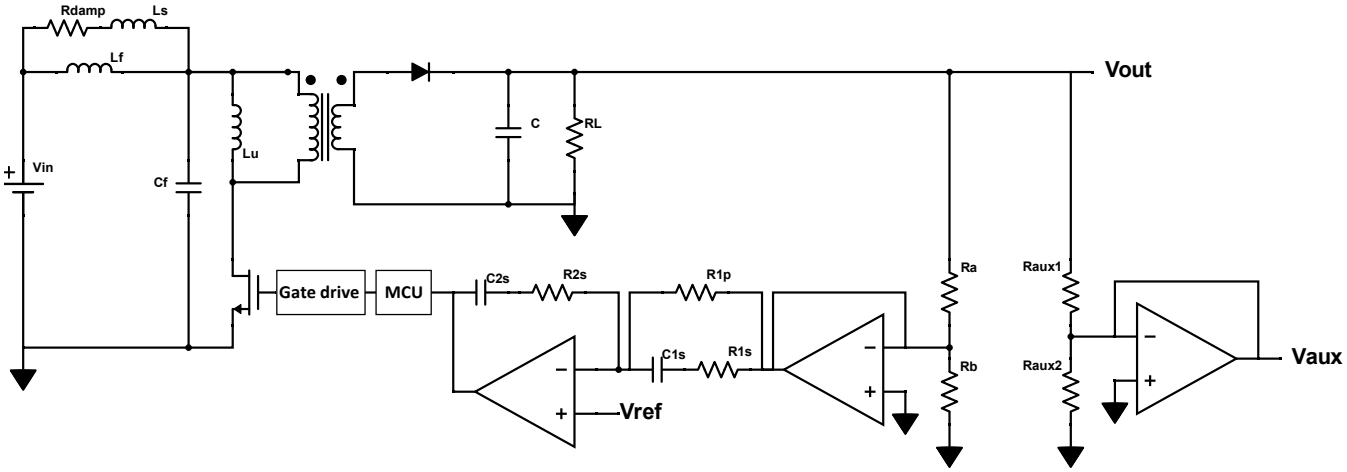

Figure 17: Complete circuit topology

Component	Requirements	Digi-Key ID	Specifications
Raux1	120kΩ, 0.5mW	RC1206FR-07120KL	120kΩ, 250mW
Raux2	50kΩ, 0.3mW	RT1206BRE0750KL	50kΩ, 250mW
Buffer opamp	2.7V to 6.0V single supply	MCP601	Supply voltage: Vdd=2.7-6V, Vss=0

KICAD Schematic and Layout

Circuit schematic and PCB layout were fully conducted in KICAD. The schematic is shown on Fig. 18.

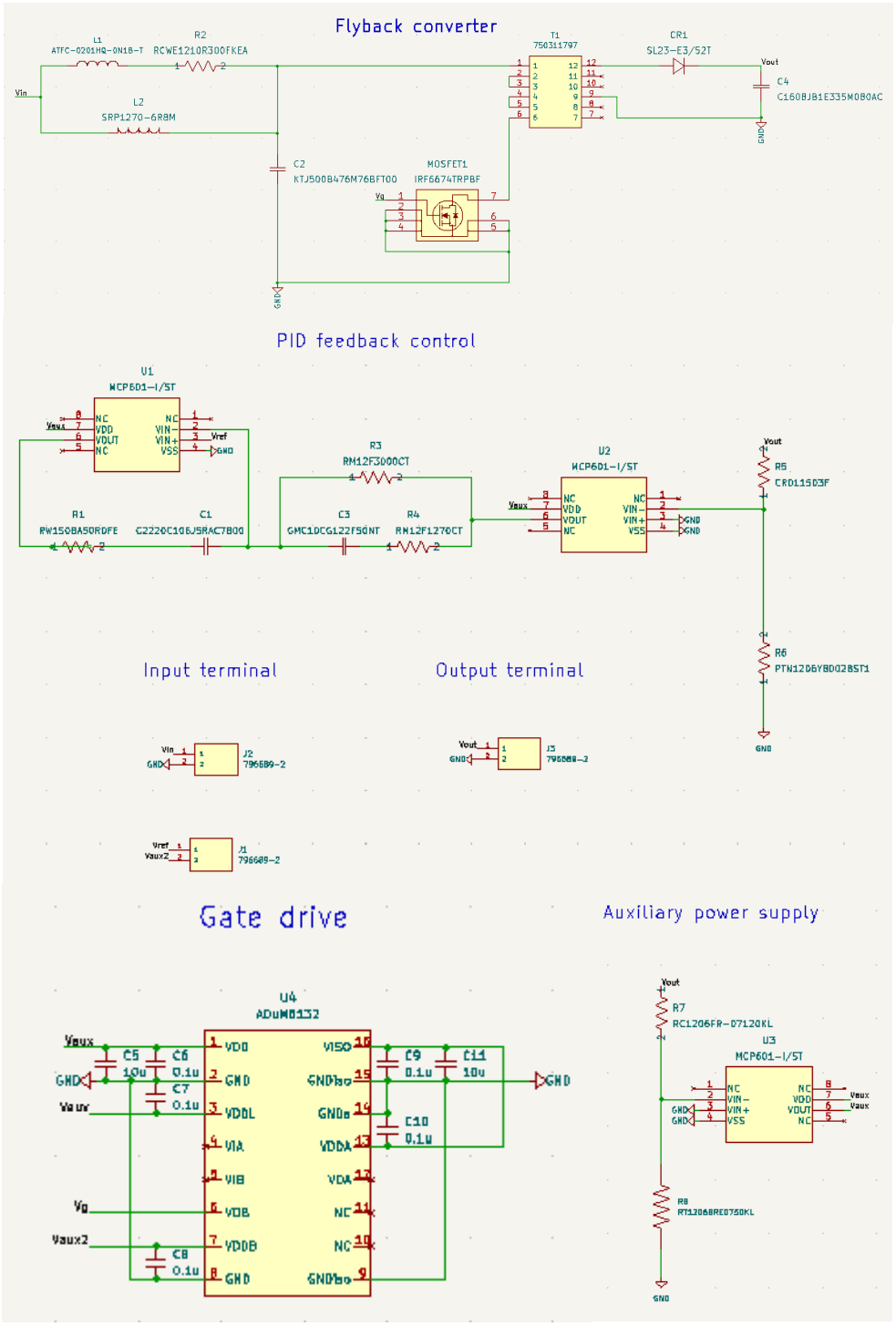

Figure 18: KICAD Schematic

The KICAD PCB layout can be seen on the following diagrams showing the different PCB layers separately. Traces were upsized to 0.42mm, so that they can accommodate a current of up to 10A, according to Advanced Circuit's online calculator [4].

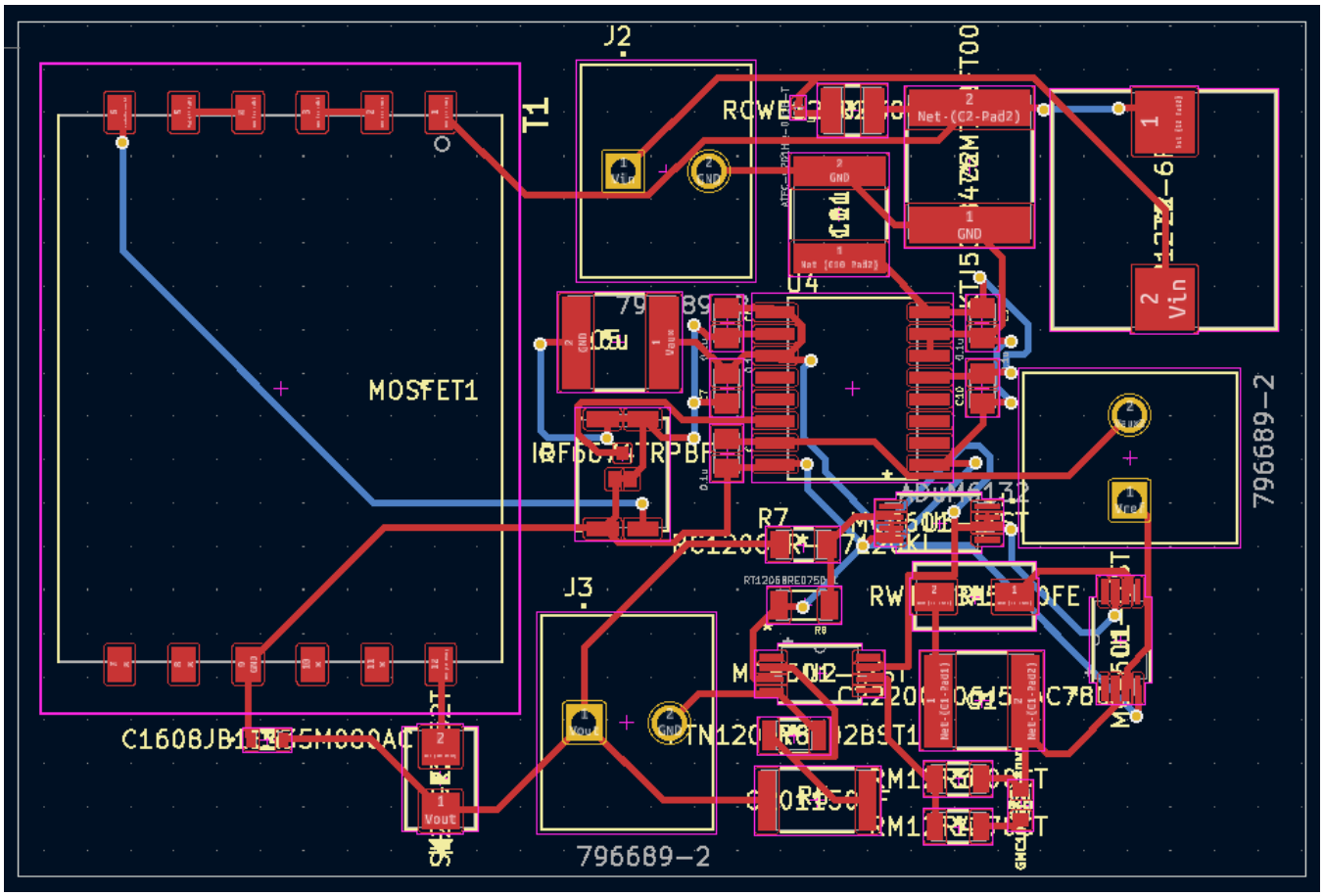

Figure 19: Complete view of PCB layout

Below, one can see the specific layers of the PCB.

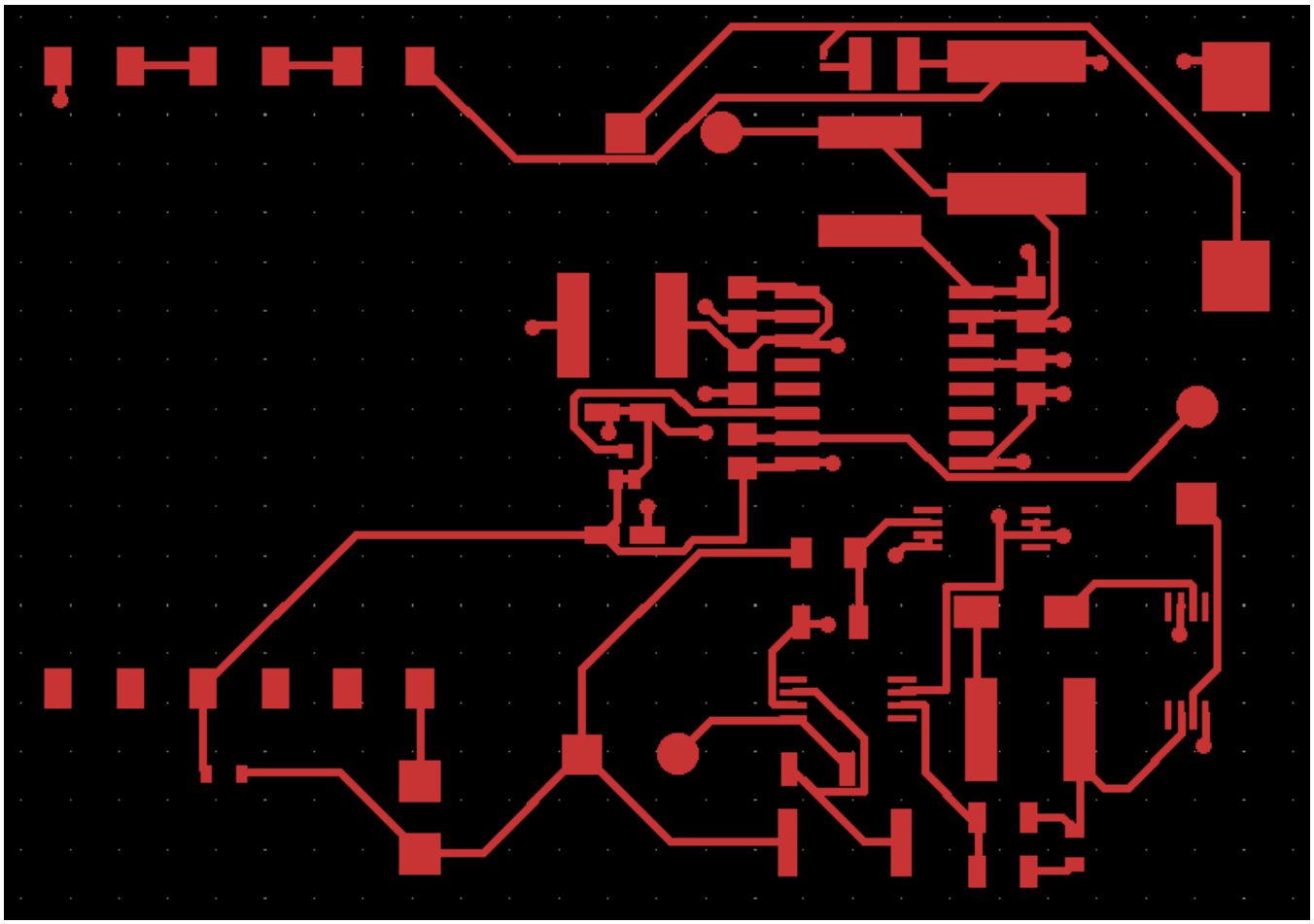

Figure 20: Front copper

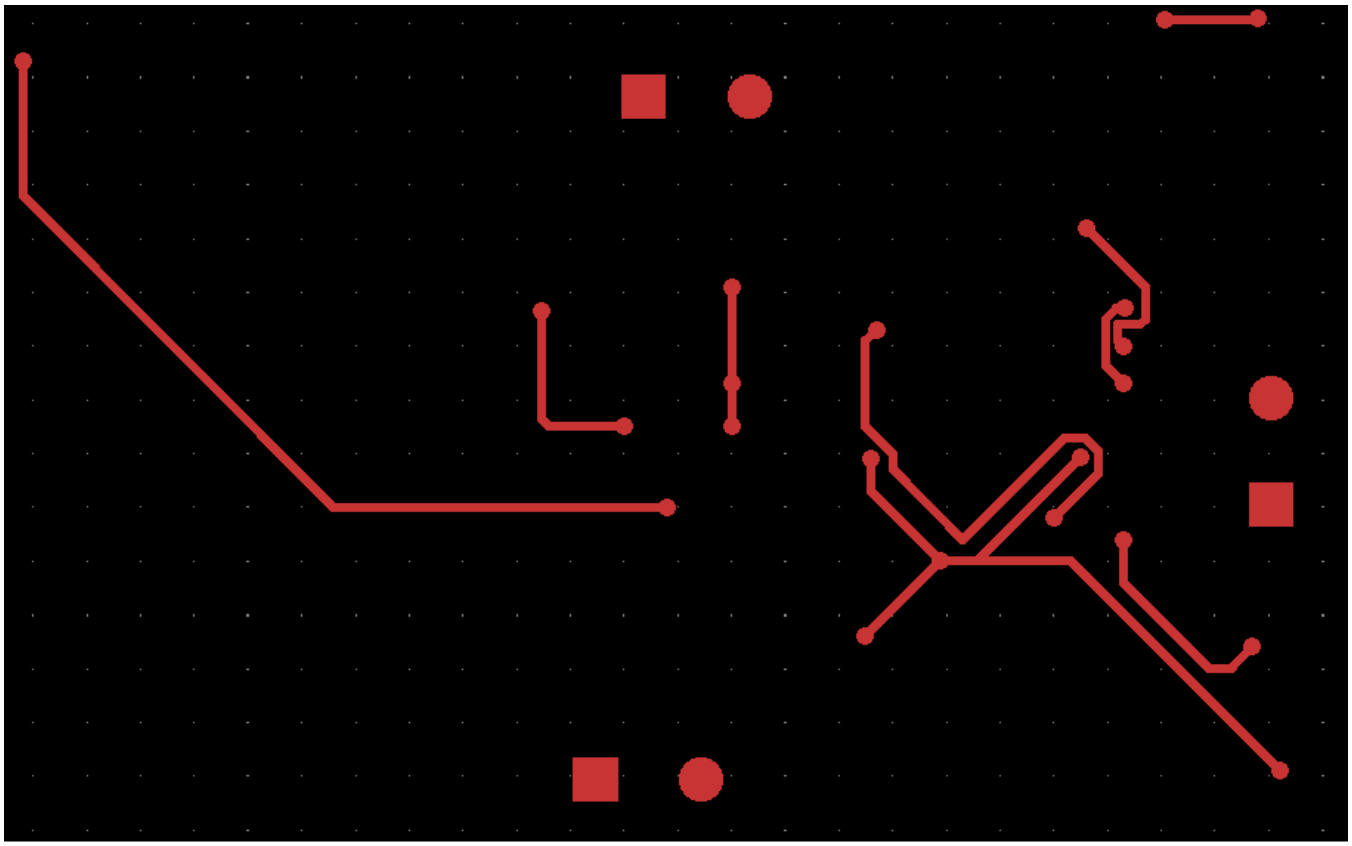

Figure 21: Bottom copper

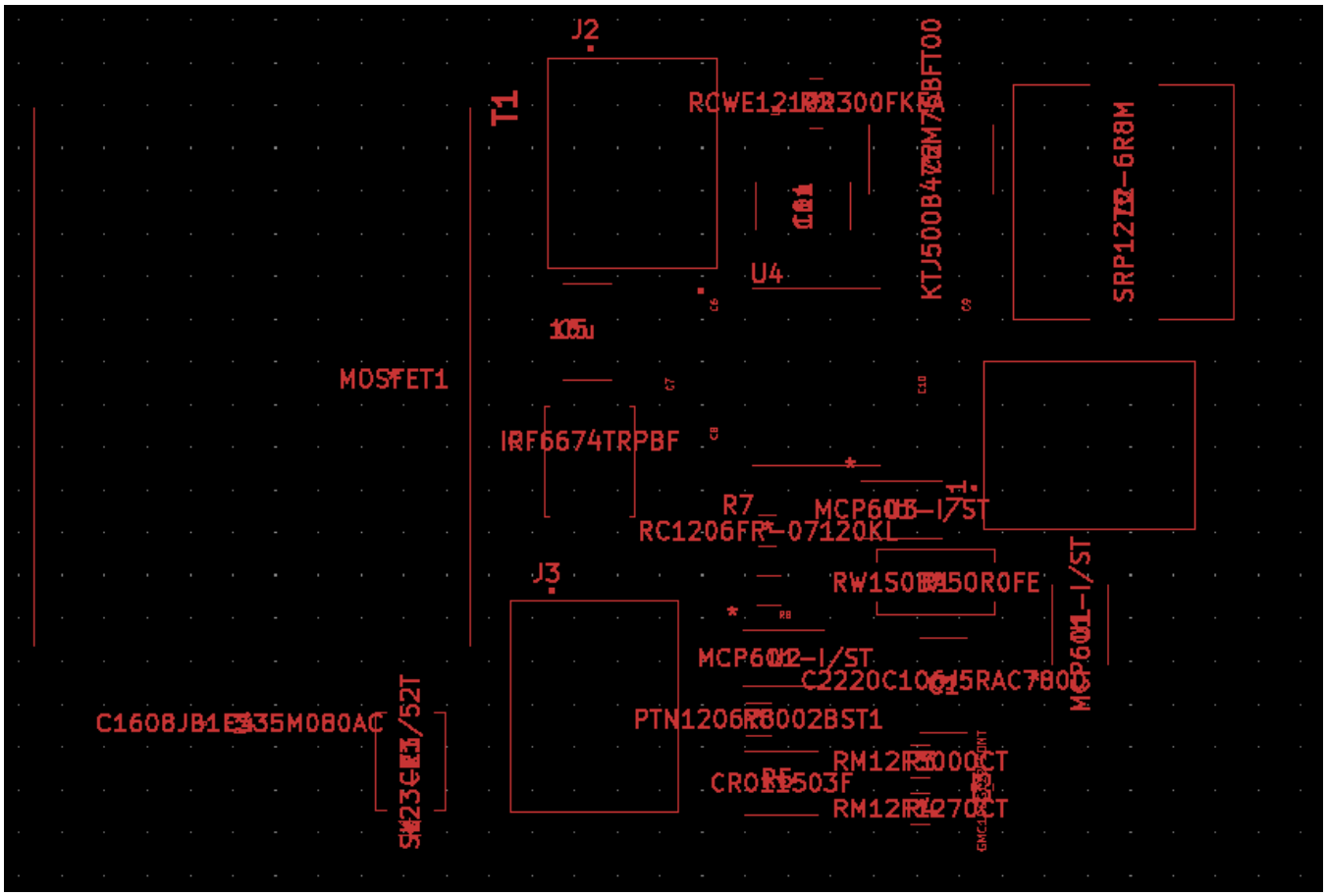

Figure 22: Front silkscreen

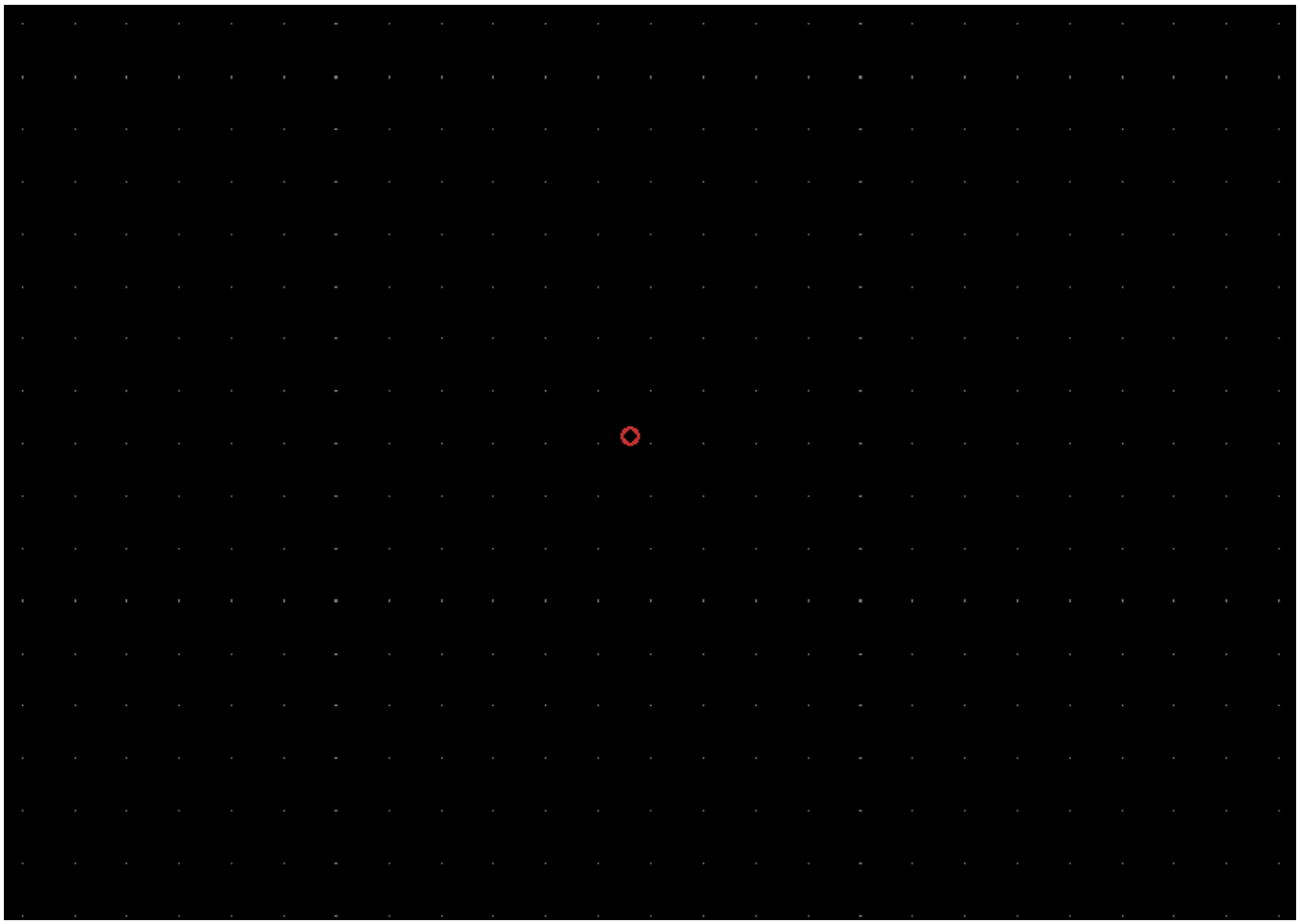

Figure 23: Bottom silkscreen

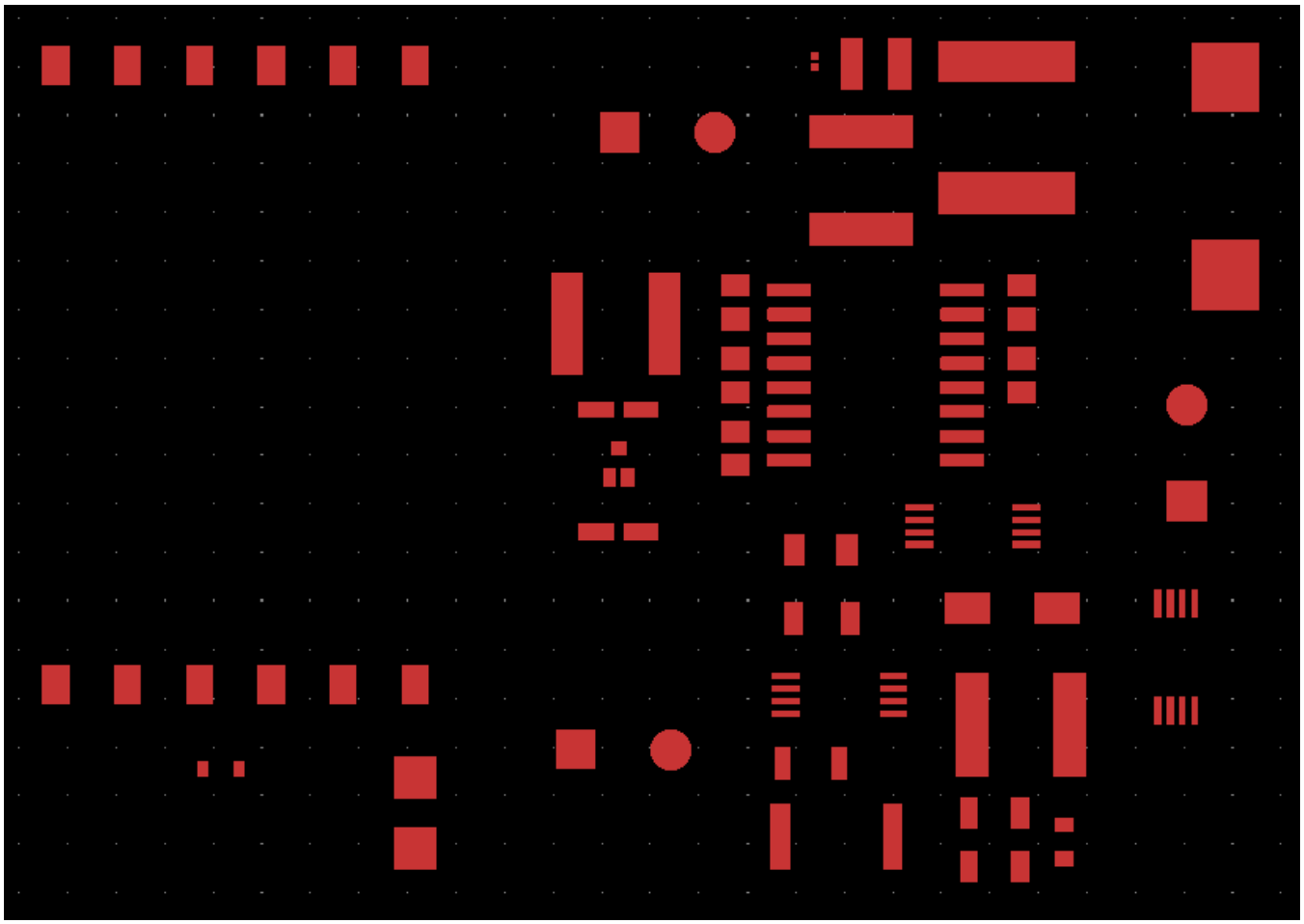

Figure 24: Front mask

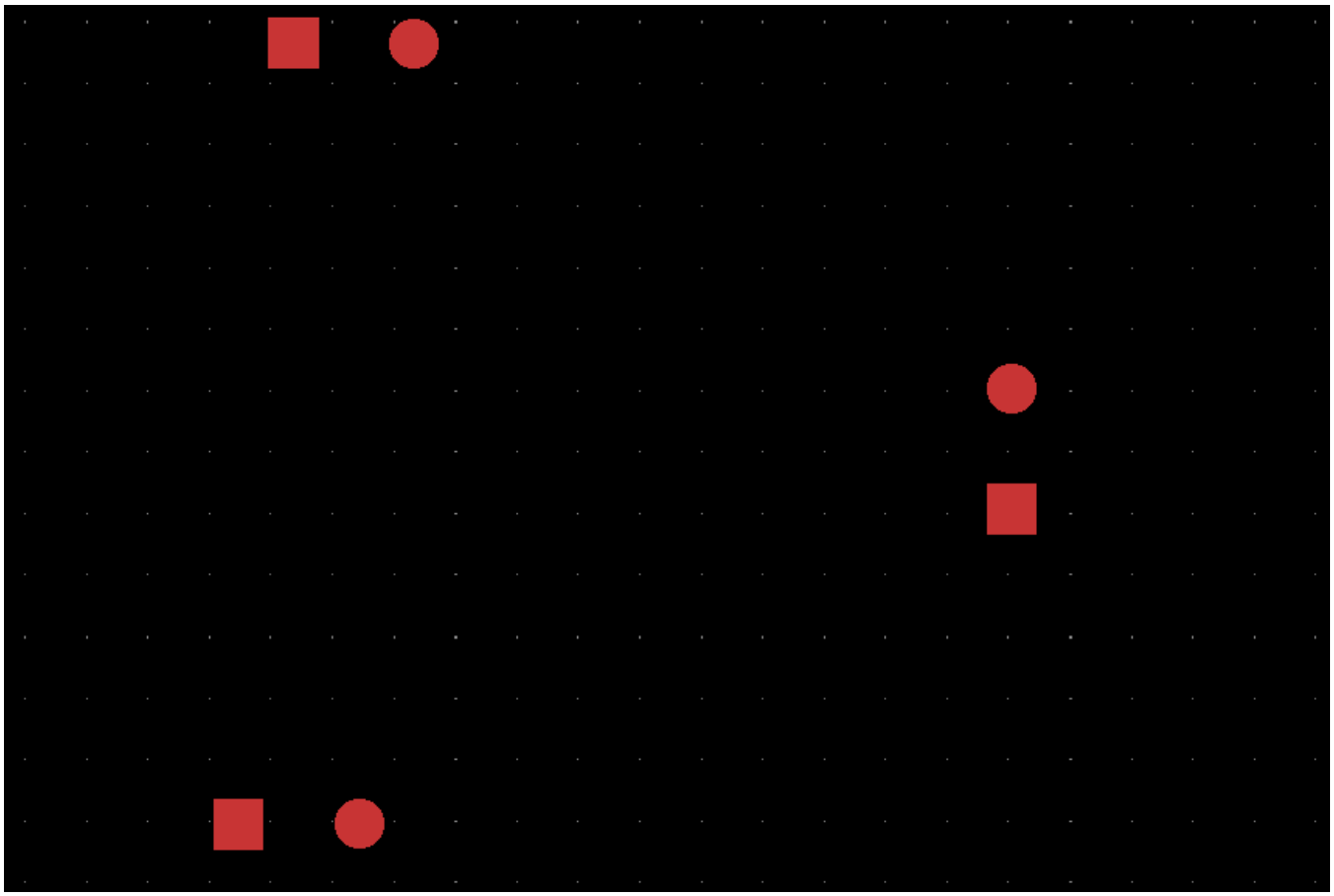

Figure 25: Bottom mask

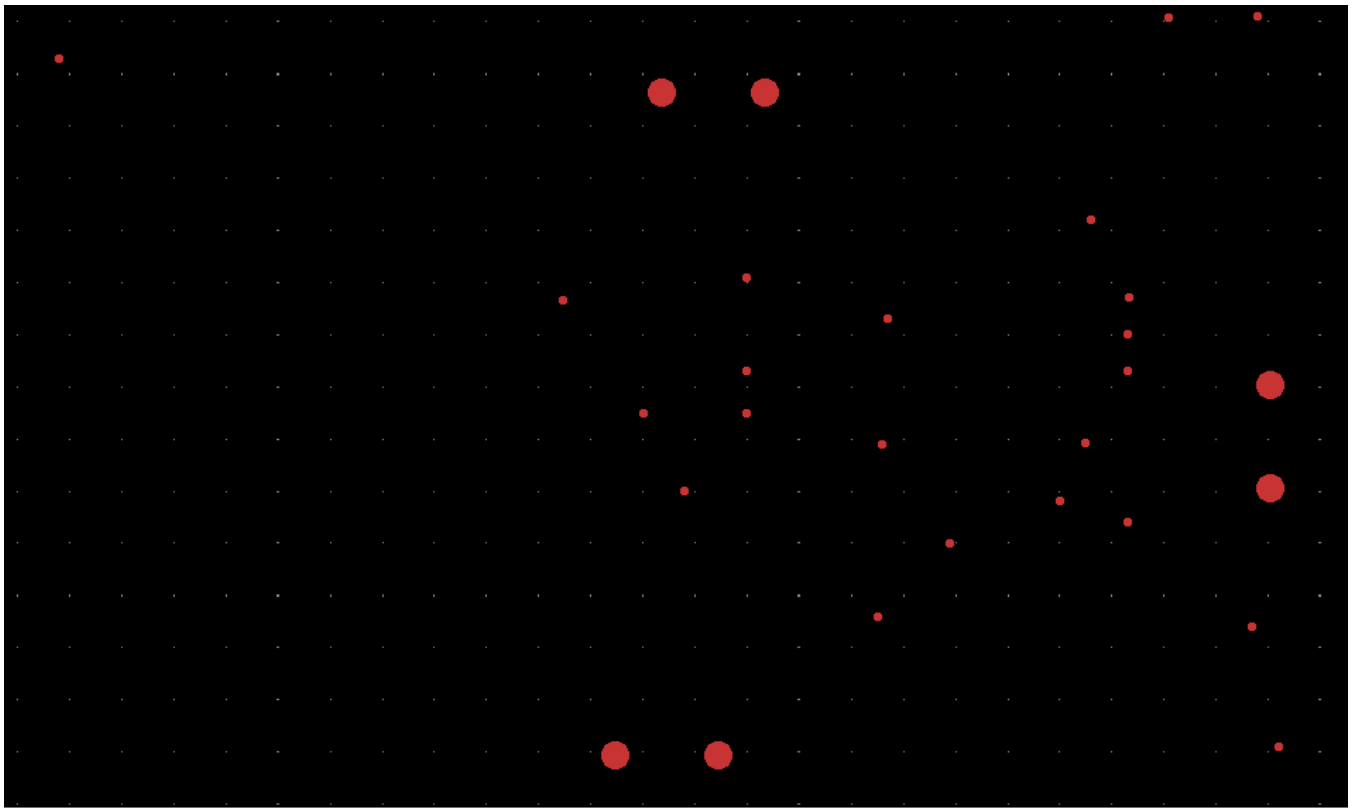

Figure 26: Drill mask

Layout checks

Below, the screenshots of ERC and DRC checks are provided. Both are essentially errorless; however, each screenshot shows one excluded error. In the ERC case, this was a problem with KICAD's interpretation of the ground pin. The error would jump from one ground pin to another based on random movement of the pin placement, suggesting that the error can be disregarded. In the case of the DRC, it was because the minimum clearance was set to a larger distance than what was fulfilled by the pads in the small inductor in the input filter. This is not a problem of the design; therefore, it can also be disregarded.

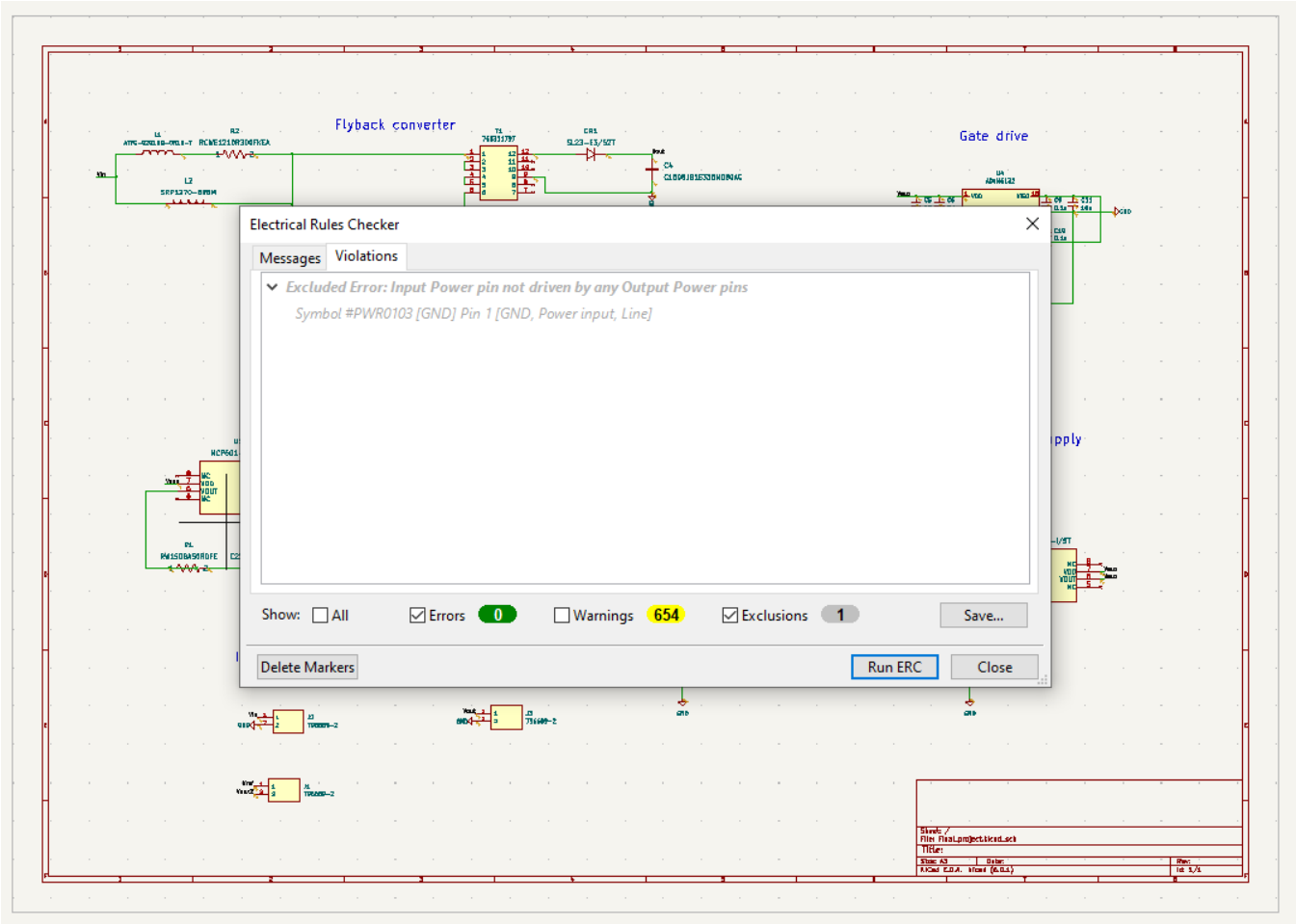

Figure 27: Electrical Rules Checker

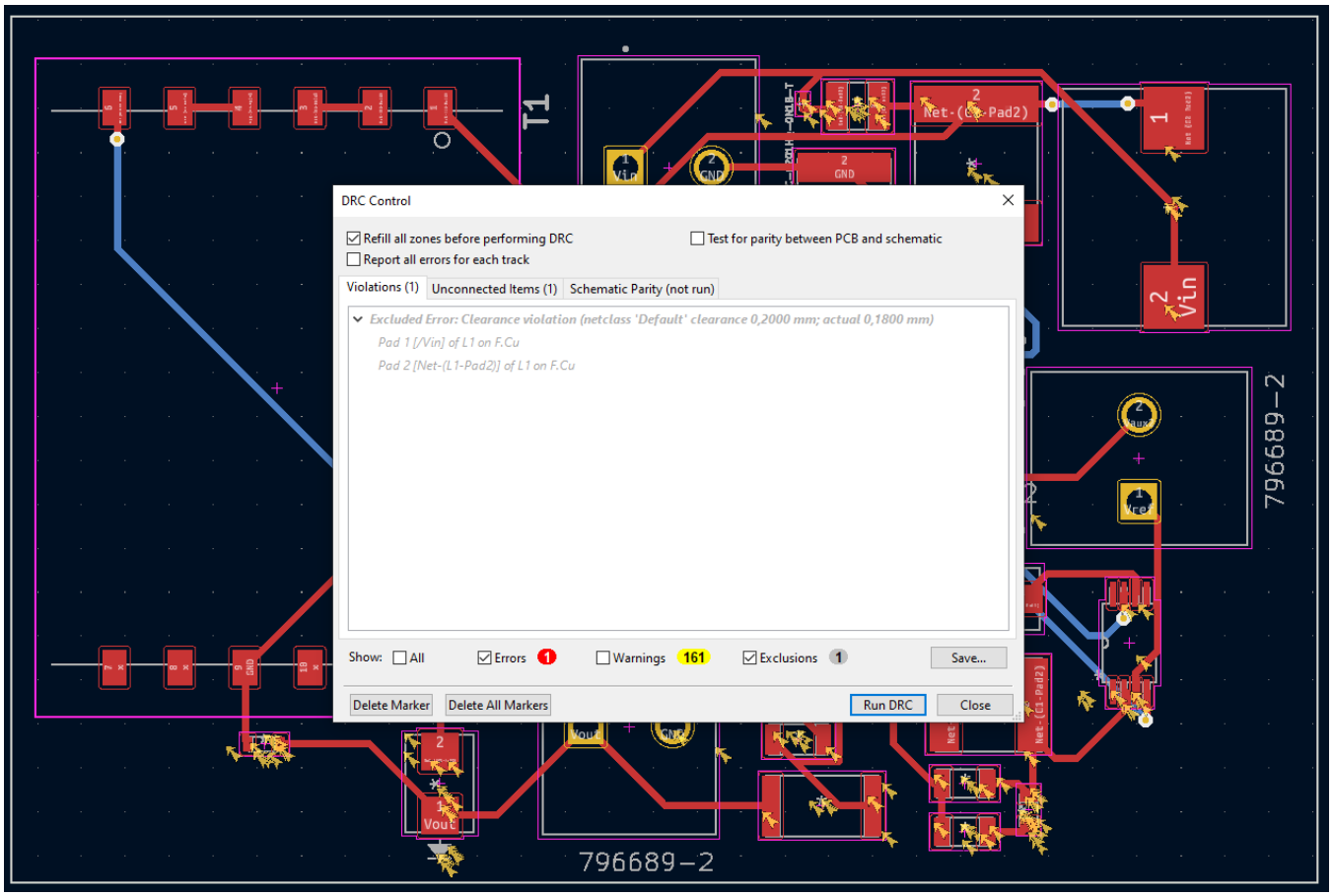

Figure 28: Design Rule Checker

Finally, Advanced Circuits' online tool at 4pcb.com was used to run the Design for Manufacturability test, which came out perfectly fine.

Figure 29: Design for Manufacturability Check

Quote

The cost of 5 copies of the PCB would be cost around $4 if purchased from JLC PCB.

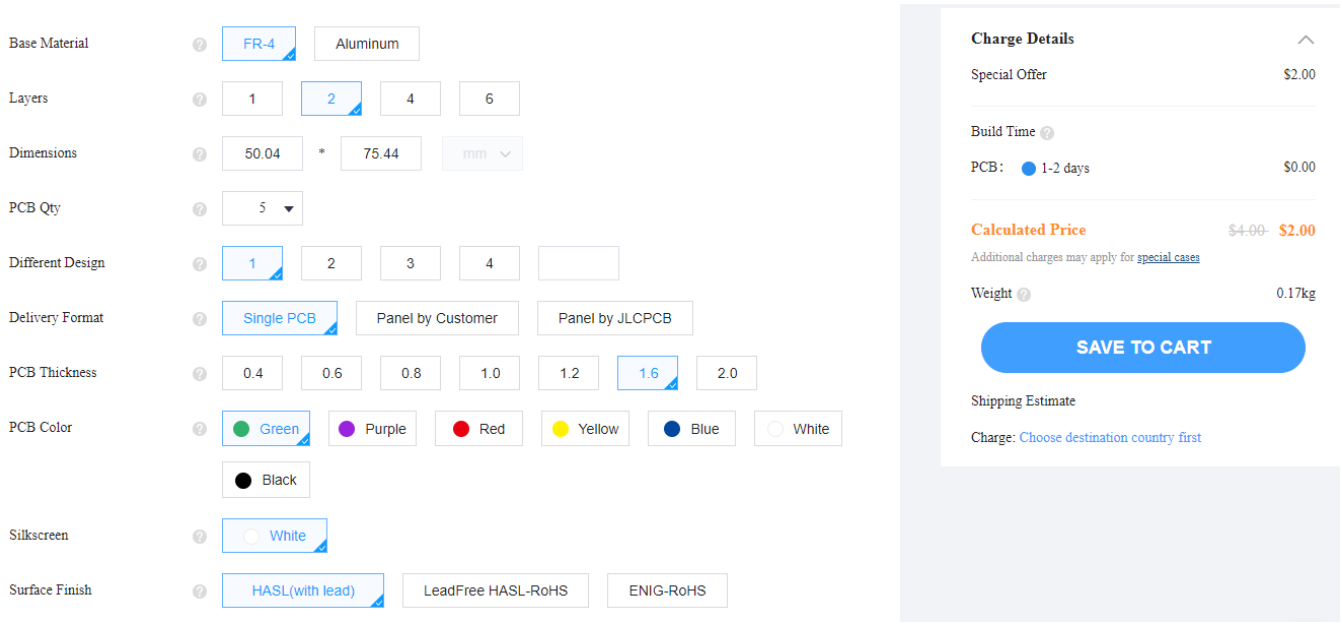

Figure 30: Quote for 5 PCBs

Summary

When looking back at the main goals of the design, it can be concluded that the design is a robust first iteration, that however has still many places for improvement. In terms of the price, the design comes up costing $57.86 per board if 5 boards were assembled. This exceeds the initial $50 goal; however, the price could be driven down by ordering more boards. In terms of efficiency and robustness, real testing would be necessary to assess both, but the design could be considered successful because the two criteria were key factor in decisions at various stages of the design process. All other specifications, including control bandwidth, transient time, and EMC standards have been fulfilled. The final board, with dimensions of 50.04mm x 75.44mm, converts 21.8W of power, and therefore achieves power density of 0.578 W/cm^2.

Additional work is required particularly in the following areas:

1. Three lines are lacking proper galvanic isolation needed to ensure the primary and secondary are truly isolated, these are the reference voltage from the MPPT V_{ref}, the auxiliary 5V power supply, and ground.
- The converter should include a comparator that would switch the system off when the solar panel isn't able to provide enough power for the load to operate.
- Both semiconductor switches are lacking proper heat sinks to prevent from overheating and failure.

- At last moment, I realized the gate drive also needs a second auxiliary supply with 12.5-17V. I have not provided that power supply, and instead left a space for it in the input terminal. Along with providing a start to the entire system, this is left to do on the side of auxiliary power supplies.

See attached files for complete BOM (including extra bypass capacitors for MCU and gate drive) generated from Digi-Key, key datasheets, KICAD files, simulation files and plots.

References

[1] N. Onat, "Recent Developments in Maximum Power Point Tracking Technologies for Photovoltaic Systems", *International Journal of Photoenergy*, vol. 2010, pp. 1-11, 2010. Available: 10.1155/2010/245316.

[2] E. Kaufhold, J. Meyer and P. Schegner, "Transient response of single-phase photovoltaic inverters to step changes in supply voltage distortion," *2020 19th International Conference on Harmonics and Quality of Power (ICHQP)*, 2020, pp. 1-6, doi: 10.1109/ICHQP46026.2020.9177918.

[3] EMC Compliance for Renewable Resource Power Systems. n.d. [online] Available at: <https://www.intertek.com/uploadedFiles/Intertek/Divisions/Commercial_and_Electrical/Media/PDF/EMC_Testing/EMC-Compliance-for-Renewable-Resource-Power-Systems.pdf> [Accessed 4 April 2022].

[4] "Printed Circuit Board Trace Width Tool | Advanced Circuits", *4pcb.com*, 2022. [Online]. Available: https://www.4pcb.com/trace-width-calculator.html. [Accessed: 11- Apr- 2022].