Design of a Fully Differential Optical Sensor

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EE 214A, Fall 2022

Parameter	Given Specifications	Achieved Specifications
Technology	1 μm CMOS	1 μm CMOS
Operating temperature	25$_\circ$C	25$_\circ$C
V_{dd}/V_{ss}	+/- 2.5 V	+/- 2.5 V
Output load resistance (differential), R_L	20kΩ	20kΩ
Output load capacitance (differential), C_L	150fF	150fF
Input load capacitance, C_{in}	100fF	100fF
Common-mode output voltage	$-0.5\text{ V} \leq VCM,out \leq +0.5\text{ V}$	VCM,out = +/-376.5mV
Power dissipation	≤ 2 mW	1.89mW
Small-signal transresistance gain ($A=v_{out}/i_{in}$)	≥ 40 kΩ	40,738Ω
Gain magnitude response (Bode plot)	Flat, then monotonically decreasing	Flat, then monotonically decreasing
-3dB bandwidth	≥ 50MHz	72.2MHz
Figure of merit (FOM) = (gain x BW) / (power)	≥1000 kΩ · MHz/mW	1556 kΩ · MHz/mW
Current mirror channel length	≥ 2 μm	≥ 2 μm
Gate overdrive for all devices	≥ 150 mV	≥ 150 mV
Width/length size increments	$\Delta Lmin$, $\Delta Wmin$ = 0.2 μm	$\Delta Lmin$, $\Delta Wmin$ = 0.2 μm
Maximum current mirror ratio	≤ 20	≤ 13.5

Table 1: Comparison of Given and Achieved Specifications

Annotated Schematic Diagram

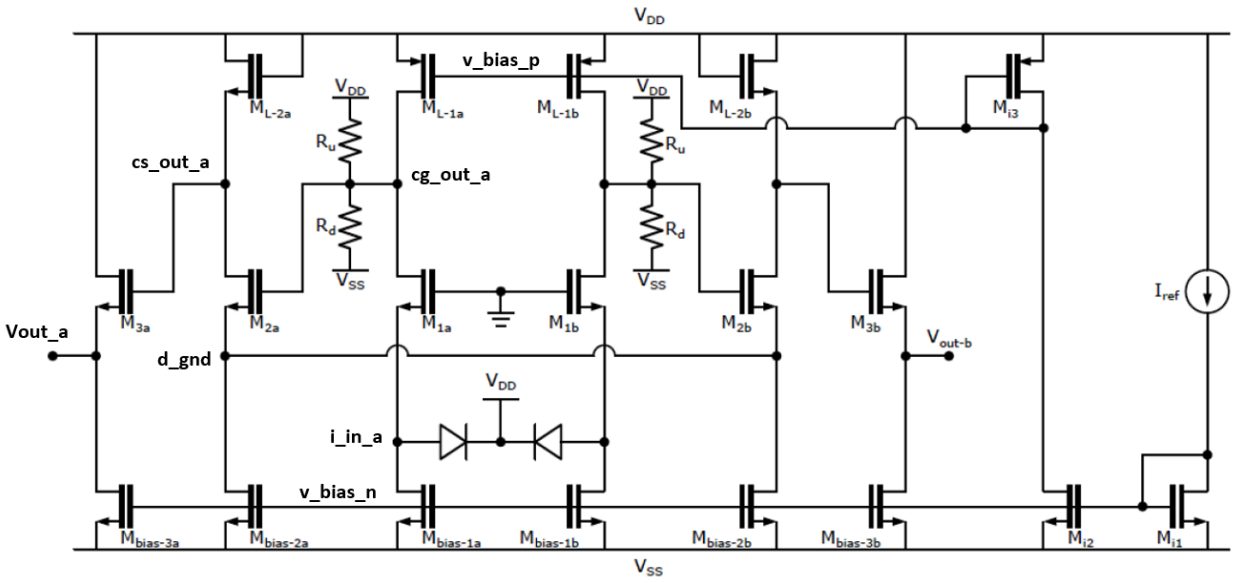

Figure 1: Circuit Schematic

Component Selections:

R_u = 110kΩ , R_d = 110kΩ

I_{ref} = 8.6μA

Transistor	**W (μm)**	**L (μm)**
$M_{i1,}$ M_{i2}	2	8
M_{i3}	3	5
$M_{bias-1a}$, $M_{bias-1b,}$ $M_{bias-2a}$, $M_{bias-2b}$	2	7
$M_{bias-3a}$, $M_{bias-3b}$	7.6	2
M_{l1a}, M_{l1b}	2.2	4
M_{l2a}, M_{l2b}	3	1
M_{1a}, M_{1b}	4	1
M_{2a}, M_{2b}	3.8	1
M_{3a}, M_{3b}	36.2	1

Table 2: Selected Transistor Dimensions

Node Voltages:

Vout_a/b = -376.5mV cs_out_a/b = 961.4mV d_gnd = -1.206V cg_out_a = -82.57mV i_in_a = -1.143V

v_bais_n = -839.0V v_bias_p = 934.2 V

Simulation Results

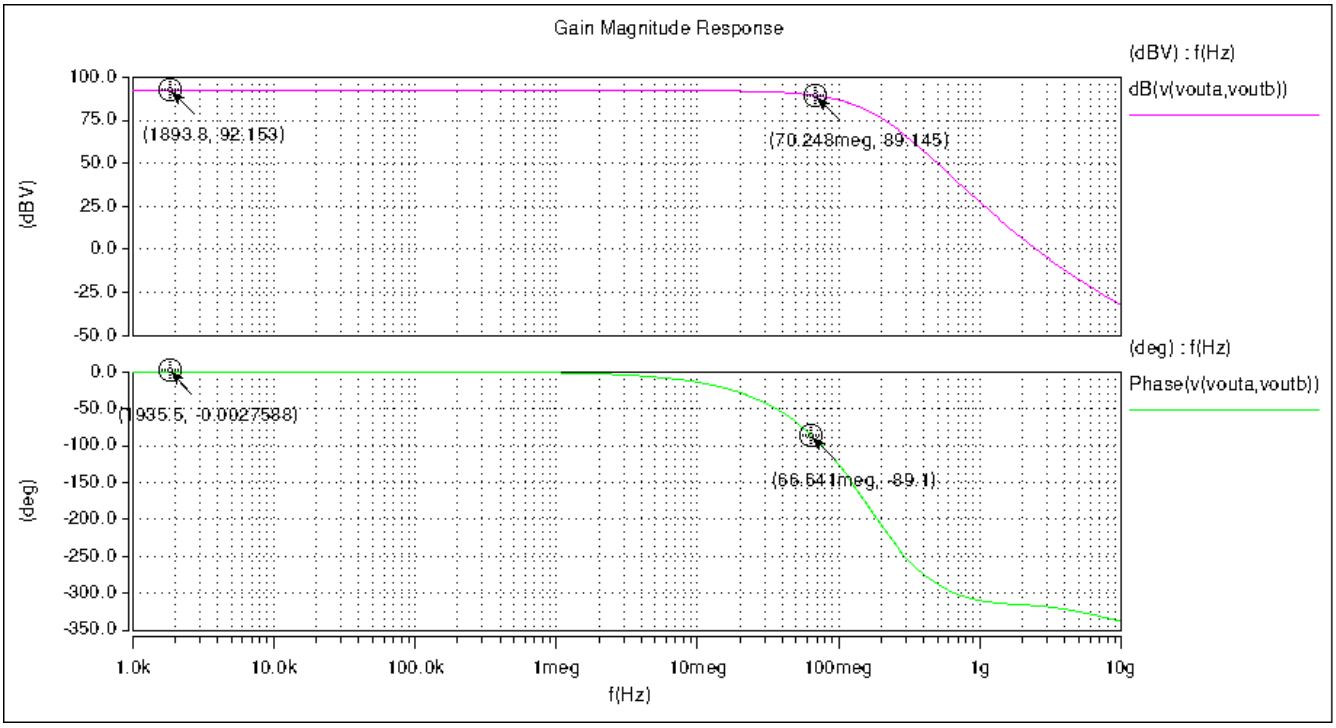

Figure 2: Gain Magnitude Response

Low frequency gain of 92.2dB (simulated) vs 95dB (calculated); -3dB bandwidth of 70.2MHz (simulated) vs 55MHz (calculated); *(Note: CSCOPE shows 70.2MHz, while .lis file measured 70.1MHz)*

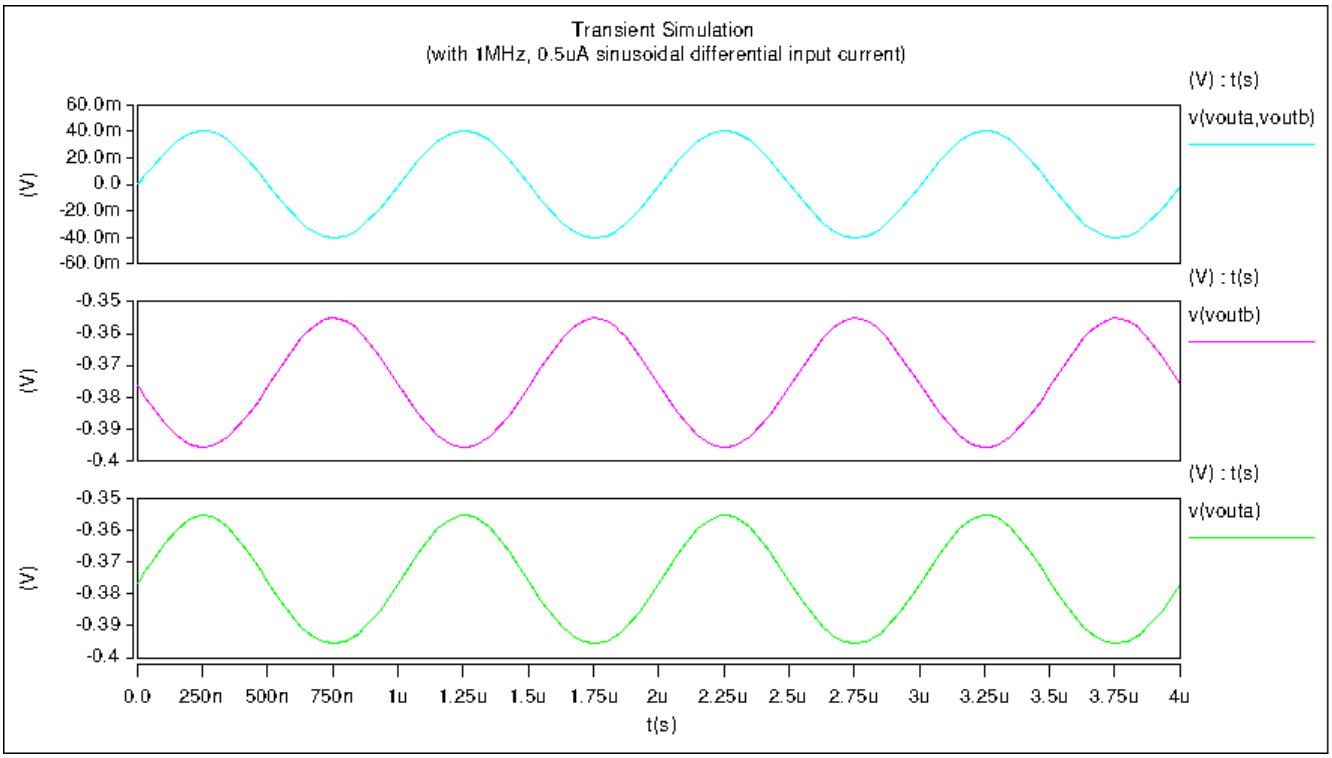

Figure 2: Transient Response

Design Process

We started the design process by restricting the solution space to all the combinations of main node voltages that would keep all the transistors in saturation. Then, we proceeded to identify the key aspects of the circuit that would affect the main specifications of the project—gain, bandwidth and power. For gain and power, we were able to formulate straightforward, simplistic equations. However, we realized that bandwidth was the one we were least certain of because of the many simplifications we had to make to get a reasonable equation. Specifically, we used the Miller approximation to separate the circuit into nodes, and then made the assumption that the circuit had a dominant nodal pole which would inform the -3dB bandwidth. Understanding that this was a gross simplification, we decided to include bandwidth not as a minimum requirement, but as a variable to maximize. We then constructed a MATLAB script that would help us with constraining our optimization space and performing the optimization.

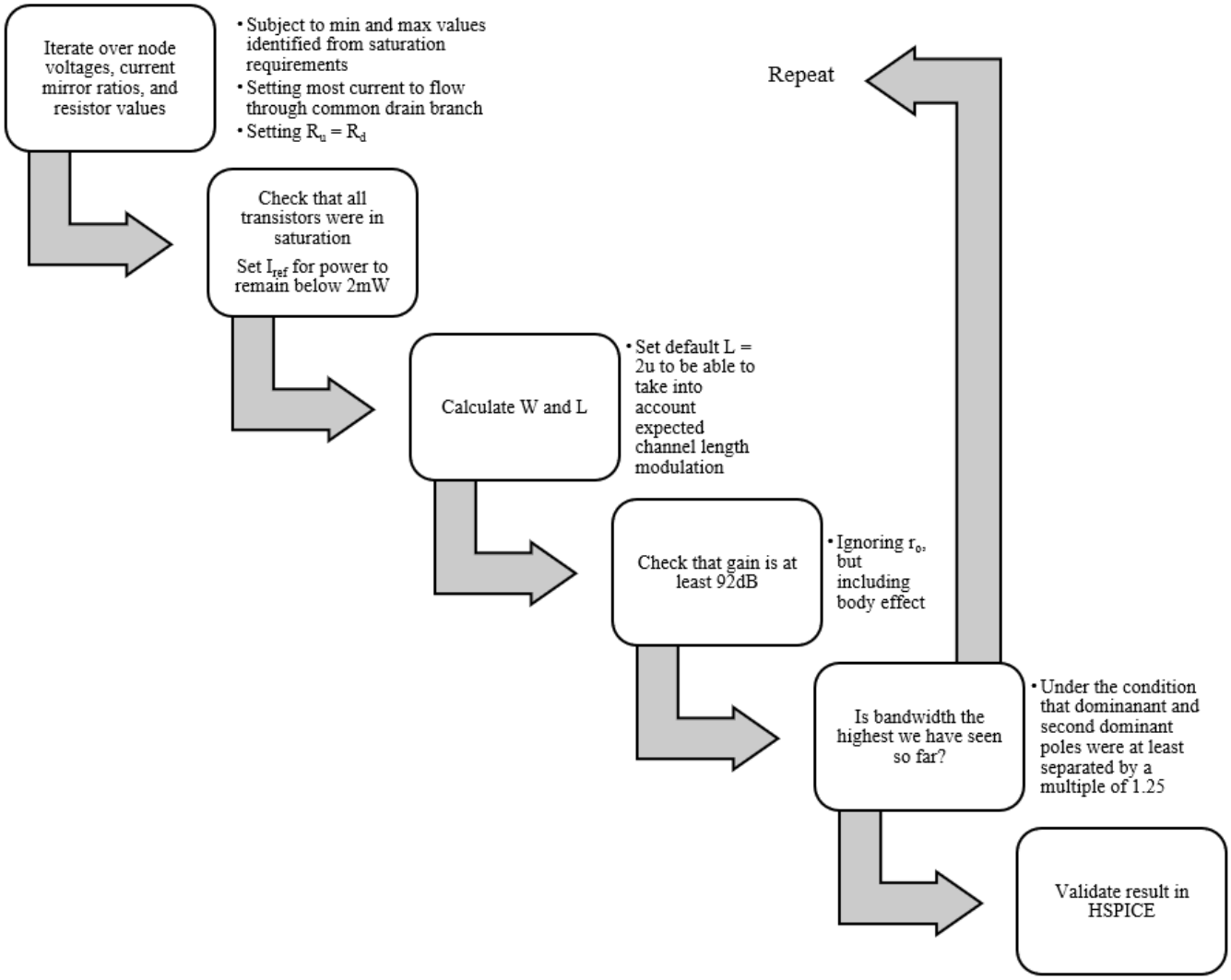

Figure 3: Optimization Flow Diagram

On the right of each optimization step is a description of the key insights and choices we used to constrain the process and to make use of our circuit intuition and the design knobs we identified. In particular, we decided to:

1. Maximize the current mirror ratio in the common drain (output) branch with respect to those in the common gate and common source branches, as it is the current most directly related to gain.
2. Set R_u and R_d to be the same, such that in small signal, their parallel combination is maximized. Again this choice was made to maximize gain.
3. Minimize each MOSFET's W and L within the constraints of the technology and the ratio W/L to minimize intrinsic and extrinsic capacitances and therefore maximize bandwidth.
4. Use the Miller approximation and a dominant pole assumption to get an estimate for bandwidth. To ensure that the dominant pole assumption is valid for the purposes of the -3dB frequency, a requirement is enforced that the second most dominant pole must be at least 1.25-times larger than the first one.
5. Set Vbias_n = -Vbias_p to reduce our option space, because the symmetry of the circuit suggests that the same values should work for both.

The initial set of calculations did not include a representation of an expected error; however, we were forced to add this as we analyzed the combinations our script suggested. Therefore, we added an extra 150 mV buffer on our minimal V_{ov}, a 3dB buffer on our gain, and a 10% buffer on our power. The final set of values was a combination of values suggested by the script and tweaks made based on real results.

Below, we describe how each key specification was calculated and modeled, which simplifications were made, and how insights were used. The related plots were generated after calculations were completed and the script was built. They were not used to produce insights about the problem we were solving, but instead were used to confirm them.

Design for Gain

The differential gain of the circuit was calculated by modeling the sensor with small-signal analysis (Equation 1). For simplicity, channel length modulation and bulk effect were ignored for all MOSFETs.

$$\frac{v_{out}}{i_{in}} = \frac{g_{m,2}}{g_{m,L2}} \cdot \frac{g_{m,3} \cdot \frac{R_L}{2}}{1 + g_{m,3} \cdot \frac{R_L}{2}} \cdot \frac{R_u \cdot R_d}{R_u + R_d}$$

Equation 1: Transresistance Gain

The last two terms of this equation were taken into account when sweeping variables in simulation to optimize for a high gain, as they suggest optimal relations between key design parameters. The middle term, which depends on $g_{m,3}$, can be maximized by maximizing $g_{m,3}$ itself (as it is << 1). Since the transconductance of an NMOS is directly proportional to its drain-source current, this suggests that we should size the current biasing MOSFET for the third branch to be high. This does not apply to $g_{m,2}$ and $g_{m,L2}$, because they share the same drain current, therefore it appears both in the numerator and in the denominator. In addition, the last term is equivalent to the parallel resistance of R_u and R_d; to maximize this value, both R_u and R_d should be equal, which further suggests that the gate voltage of M_2 should be exactly between V_{DD} and V_{SS}, at 0 V.

Design for Bandwidth

The bandwidth of this circuit was evaluated by calculating the pole locations via nodal analysis. At first, only intrinsic capacitances were included. The Miller approximation was used on the gate-drain capacitance of M_2 and gate-source capacitance of M_3 to form these nodes—gain values for the approximation were calculated quickly by ignoring channel length modulation. While the Miller approximation could also have been applied to the r_o of M_1, this resistance was ignored for the purpose of simplifying the nodal equations. After initial sweeps, in which we

looked for solutions spaces that maximized the dominant pole, our HSpice simulations constantly produced lower-bandwidth results than expected, and it appeared that our calculations were not detailed enough. We attempted two methods to fix this.

The first method was based on the hypothesis that the nondominant poles were close enough to the dominant pole that they were reducing the -3dB frequency. This would invalidate our simulation results, because we were effectively assuming that the dominant pole was the bandwidth frequency. Suspecting that our dominant pole assumption was the culprit behind our low bandwidth results, we attempted to construct a second way of estimating the bandwidth by using the zero value time constant method, and thereby see not just the effect of one node, but the combined effect of different nodes on the -3dB frequency. However, this method did not yield better bandwidth estimates. Therefore, we turned to making our equations more accurate. We added terms to also consider the bulk effect (on threshold voltages and transconductance), extrinsic capacitances, and a more sophisticated Miller gain calculation that included channel length modulation. For the purpose of simplicity, both source-body and drain-body capacitances were assumed to be equal to a third of the gate-source capacitance. The additional MOSFET transconductance due to the bulk effect was assumed to take a magnitude equal to 0.2 times the regular g_m. The following equations are our most accurate estimates of the time constants of the four nodes.

$$\tau_{in} = (R_{o,bias-1} || \frac{1}{g_{m,1}}) \cdot (C_{in} + C_{gd,bias-1} + C_{gs,1} + C_{sb,1} + C_{db,bias-1})$$

$$\tau_{cg,out} = (R_u || R_d || R_{o,L-1}) \cdot (C_{gd,1} + C_{gd,L-1} + C_{gs,2} + C_{gd,2} \cdot (1 - K_2) + C_{db,1} + C_{db,L-1}$$

$$\tau_{cs,out} = (\frac{1}{g_{m,L-2}} || R_{o,2} || R_{o,L-2}) \cdot (C_{sb,L-2} + C_{db,2} + C_{gd,3} + C_{gd,L-2} + C_{gd,2} \cdot (1 - \frac{1}{K_2}) + C_{gs,3} \cdot 1 - K_1)$$

$$\tau_{out} = (\frac{1}{g_{mb,3}} || R_{o,3} || R_{o,bias-3} || \frac{R_L}{2}) \cdot (2 \cdot C_L + C_{gd,bias-2} + C_{sb,3} + C_{db,bias-3} + C_{gs,3} \cdot (1 - \frac{1}{K_1}))$$

Equations 2-5: Time Constants Associated with Nodes

A final design consideration was made regarding the product of a MOSFET's width and length. Theoretically, extrinsic and intrinsic capacitance contributions decrease with smaller width and length, since C_{ov} is proportional to width, and intrinsic C_{gs} is proportional to the product of width and length. As a result, it would be expected that bandwidth increases with lower MOSFET width and length.

Gain and Bandwidth Simulation Results and Analysis

To investigate our assumption that a high I_{CD} should be beneficial to gain, a modified MATLAB script was written to plot gain and bandwidth for many possible design parameter combinations (Figure 4). Analysis of the graph shows that gain values above the 92 dB specification are generally associated with a ratio of I_{CD} to I_{REF} of 10 or greater. This would appear to confirm our initial assumption that gain is improved with high values of I_{CD}. In addition, the impact of I_{CD} in the range of 10 to 20 did not seem to have significant bearing on bandwidth for gain above 90 dB. There are a set of data points that appear to show lower I_{CD} associated with higher dominant pole frequencies, but these data points do not meet the gain specification. The results of this first simulation suggest that other variables are important in determining the bandwidth of the system.

To further explore bandwidth, another modified MATLAB script was written to plot gain and bandwidth for many values of R_u and R_d (Figure 5). Importantly, this script builds off of the previous analysis of I_{CD} by constraining the ratio of I_{CD}/I_{REF} to between 10 and 20. The plot of R_u and R_d values indicates that at the frequencies of interest, including directly above and below the bandwidth specification, higher R_u and R_d are associated with better gain. In particular, gain combinations exceeding 96 dB were reached using values of R_u that were more than 100 kΩ. This graph also gives insight into how to reach high bandwidth. There is a small sliver of data points that appear to result in bandwidth up to 30 MHz higher than the specification, and this grouping suggests that a similarity in certain design parameters creates this higher bandwidth. Indeed, probing the current through the branches of MOSFETs reveals a commonality in parameters; these points are associated with I_{CD} around 14 times the magnitude of the reference current. Our solution fits well into this observation, as it achieves >70 MHz of bandwidth with I_{CD} around 13.5 times the magnitude of the reference current.

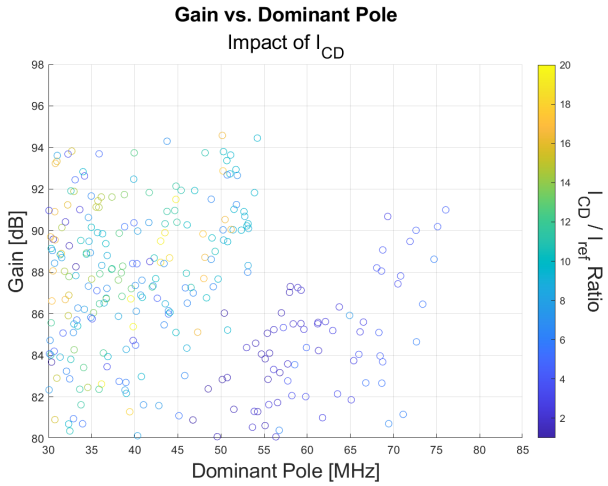

Figure 4: Impact of I_{CD} on Gain and Dominant Pole

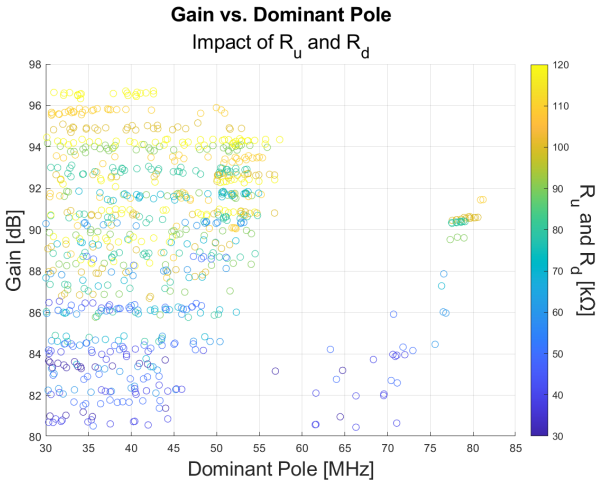

Figure 5: Impact of R_u, R_d on Gain and Dominant Pole

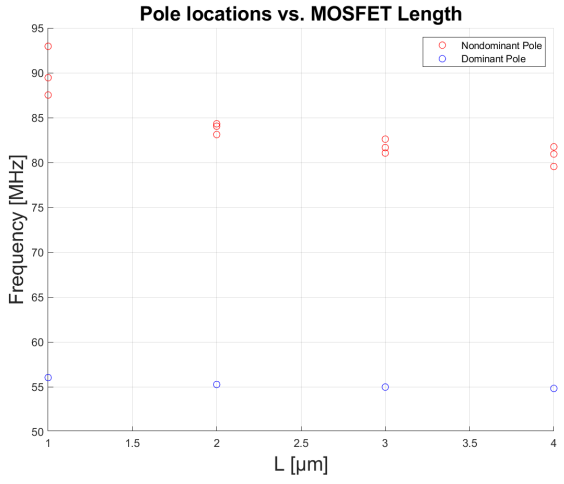

Figure 6: Impact of MOSFET Length on Dominant Pole

The third and final optimization that was verified for bandwidth was the impact of reducing the MOSFET sizes. It is not possible to use the same length for each MOSFET due to different desired W/L ratios, which necessitate that some MOSFETs are significantly larger than others. However, for simplicity, the theoretical pole locations were calculated for four common values of length (Figure 6). As expected, the dominant pole decreases as length of the MOSFET increases, likely a result of increased capacitance. In addition, a separate benefit to decreasing length can be determined: the nondominant poles move farther away from the dominant poles, and also farther away from each other. While the net effect on bandwidth is small, reducing width and length is also easily implementable, and this informed our final sensor design.

Design for Power

To calculate power, we simply summed currents flowing through all branches and multiplied that by the voltage drop from V_{DD} to V_{SS}. Doing that amounted to Equation 6.

$$W = (V_{DD} - V_{SS}) * \left[I_{REF} + I_{Mi1} + 2 * \left(I_{CG} + I_{CS} + I_{CD} + \frac{(V_{DD} - V_{SS})}{R_U + R_D} \right) \right]$$

Equation 6: Power Estimate

This equation is an accurate representation of power, with the only caveat that its accuracy depends on the accuracy of the current calculation. There were two possible sources of error for that: channel length modulation and accurate overvoltage. Channel length modulation was difficult to include in the script because it created a circular logic: we used target current levels defined by the current mirror ratios and I_{REF} to calculate W/L ratios, but knowing L beforehand was necessary to include channel length modulation. We fixed this by setting default L to 2µm, which was the smallest value that usually allowed us to create a ratio with an acceptable width. In cases where W and L were both divisible by 2, we halved each in our simulation, thereby improving effect on bandwidth but increasing error in current, though this seemed inconsequential. When L had to be increased above L=2µm, we concluded that calculating current with channel length modulation with L=2µm was inaccurate, but still better than including no channel length modulation at all. All in all, it was an approximation, but certainly a useful one that got the equation closer to real values. After this alteration, our power calculations were so close to the simulated values that there was no need to address the V_{OV} error separately.

Below is a comparison of our calculations of the three key specifications with HSPICE results, along with suggestions about the source of discrepancy.

	Hand Calculation	**HSPICE Result**	**% Error**	**Source of |Error**
Gain	57,678 Ω	40,738Ω	41.6%	- Bulk effect was considered in a very simplistic manner, assuming that $g_m' = 1.2g_m$ - Channel length modulation was ignored
Bandwidth	79.78 MHz	72.2 MHz	10.5%	- Miller approximation was used on gate-drain capacitance of M_2 and gate-source capacitance of M_3 - Simplifying assumptions were made about capacitances Csb = Cdb = (1/3)*Cgs - R_o values were calculated assuming L=2µm
Power	1.74 mW	1.89mW	7.9%	- Channel length modulation applied on current calculations assumed L=2µm - Errors in nodal voltages caused errors in V_{OV} and thereby errors in current calculations - Leakage current in mosfet gates were ignored

Table 3: Error Between Calculated and Simulated Specifications

Comments and Conclusions

Our biggest struggle during the design of the optical amplifier was achieving enough gain. This was due to two key factors. First, we only ever used a relatively simplistic gain equation (ignoring channel length modulation and bulk effect), mainly to understand the circuit intuitively and to focus our attention only on the key design knobs. Second, the way our script was structured was not optimizing for gain; instead, it simply made sure our design satisfied a certain threshold, leaving space for optimizing bandwidth, which we expected to be a much more difficult specification to hit. However, that meant that although we had already reached our bandwidth requirements by the checkpoint submission, we were struggling to meet the gain requirements. What helped us was the key insight that the resistances R_u and R_d should be kept the same, which our code was struggling to figure out itself. From this, we learned again that relying on the computer code alone was not enough, and creative, intuitive insights were key for completing the project.

A second issue we ran into during a couple final iterations of our design was that our bias transistors were going into linear mode of operation, suggesting that our operating point was very close to the boundary of linear and saturation mode. This occurred despite a constraint of $V_{OV} \geq 150$ mV. To prevent this from occurring, we had to increase this constraint in our calculations up to $V_{OV} \geq 300$ mV. We learned two things from this. First, that to make things work as expected, we had to represent the expected error of our calculations in our constraints, and second, that our design was still not entirely conceived for practical applications, where noise or a transient in the circuit could potentially compromise our saturation requirement.

Finally, although we were really trying to constrain the solution space by making creative design choices and by intuitively understanding what result to expect, there were still some small issues we encountered because of using the script. One example is that, at the very end, when we finally got a set of values that satisfied all the specifications, we noticed that there was some space to increase power, so we tried increasing the reference current, a method which had previously worked to maximize both gain and bandwidth. However, with this particular case, decreasing the current led to increased bandwidth, which surprised us, meaning that our intuition was simply not that complete, given the leap that the script made for us into a solution space whose behavior we did not know how to fully predict.