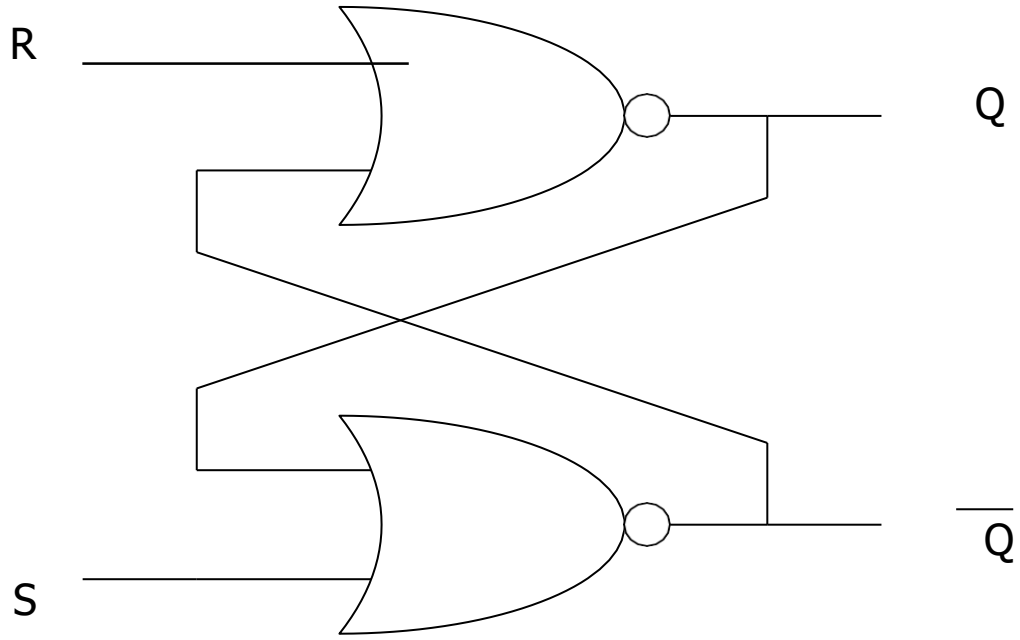
Sequential Logic Circuit

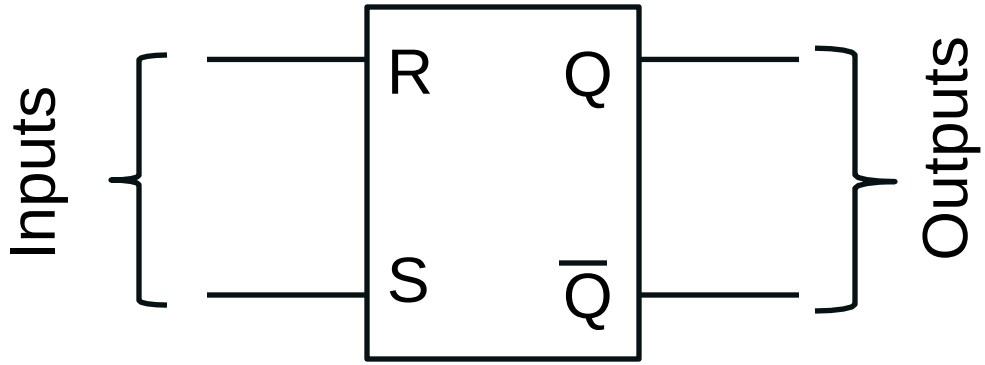
- ✓ **SR Flip Flops:** SR Flip Flop, Clocked SR FF with preset & clear, Drawbacks of SR FF
- ✓ **JK Flip Flops:** Clocked JK FF with preset & clear, Race around condition in JK FF, Master Slave JK FF, D and T type Flip Flop, Excitation Tables of Flip Flops, Block schematic and function table of IC 7474, IC 7475.

Sequential Logic Circuits

RS Latch using NOR



Circuit Diagram



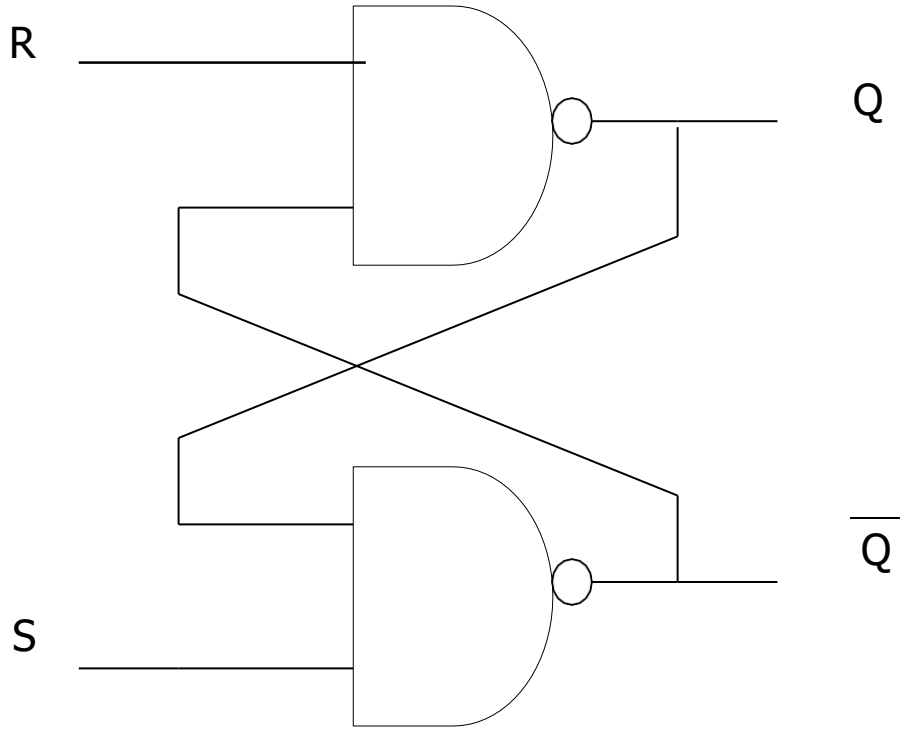
Symbol

RS Latch using NOR

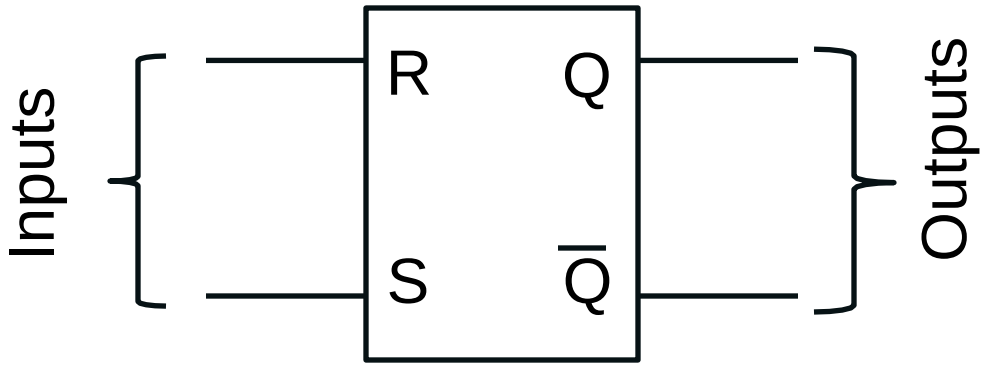
Logic Table

S	R	Q_n	Q_{n+1}	State
0	0	0	0	No Change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	X	Indetermine
1	1	1	X	

RS Latch using NAND



Circuit Diagram



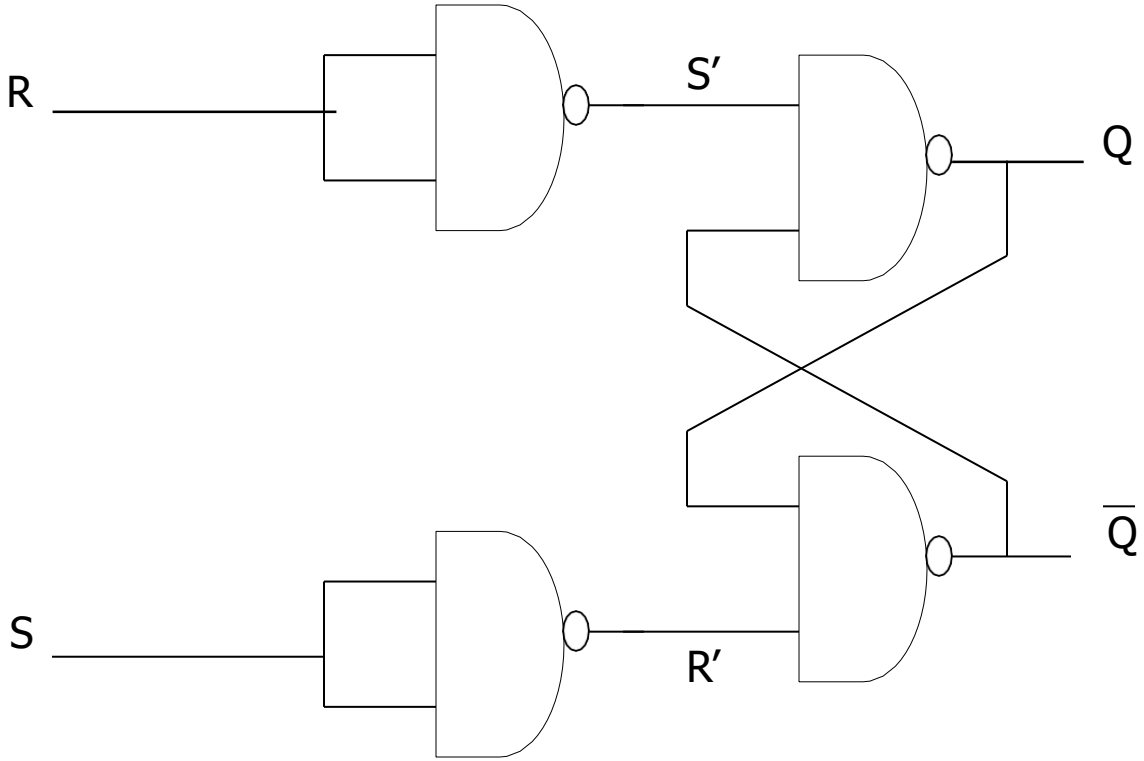
Symbol

RS Latch using NAND

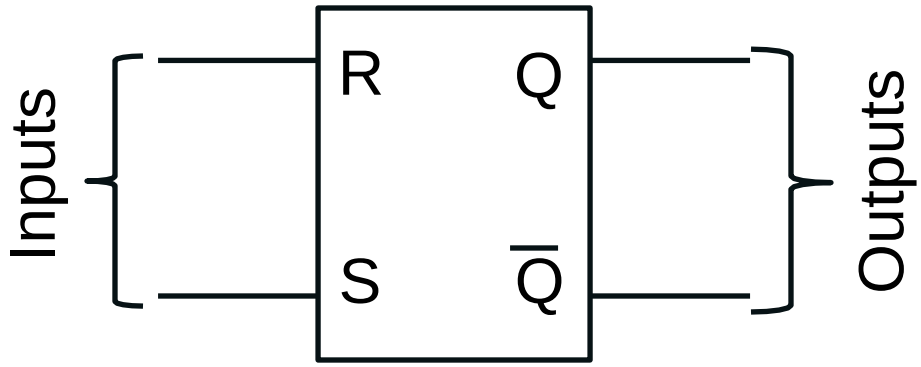
Logic Table

S	R	Q_n	Q_{n+1}	State
0	0	0	X	Indetermine
0	0	1	X	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	0	No Change
1	1	1	1	

RS Latch using NAND with additional circuitry



Circuit Diagram



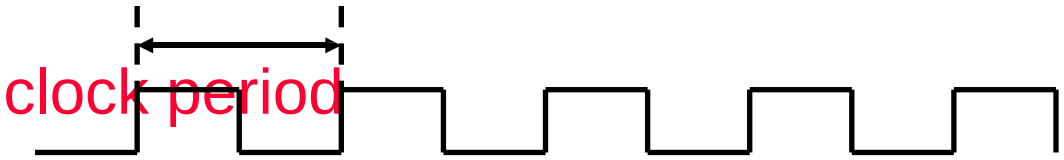
Symbol

RS Latch using NAND with additional circuitry

S	R	Q_n	Q_{n+1}	State
0	0	0	0	No Change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	X	Indetermine
1	1	1	X	

Clock

- ✓ A clock is a special device that whose output continuously alternates between 0 and 1.
- ✓ The time it takes the clock to change from 1 to 0 and back to 1 is called the clock period, or clock cycle time.
- ✓ Clocks are often used to synchronize circuits.



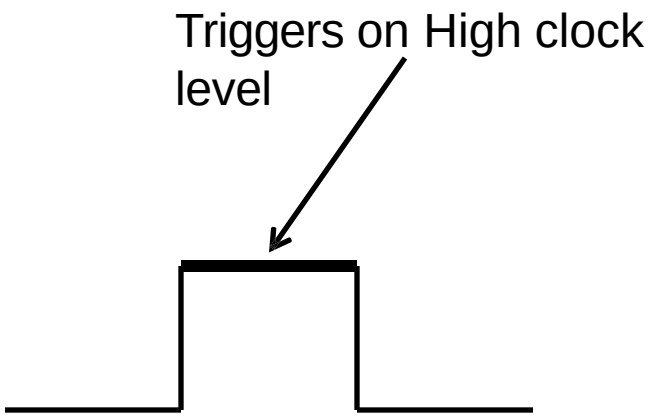
Triggering

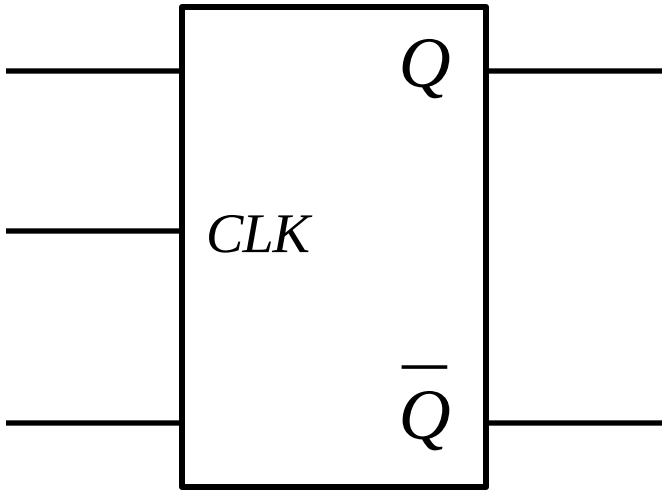
- ✓ Sequential circuits are dependent on clock pulses applies to their inputs.
- ✓ The result of flip-flop responding to a clock input is called **clock pulse triggering**, of which there are four types. Each type responds to a clock pulse in one of four ways:-

  - High level triggering
  - Low level triggering
  - Positive edge triggering
  - Negative edge triggering

High Level Triggering

- ✓ A flip flop who responds to a clock signal during the time at which it is in the logic High state.

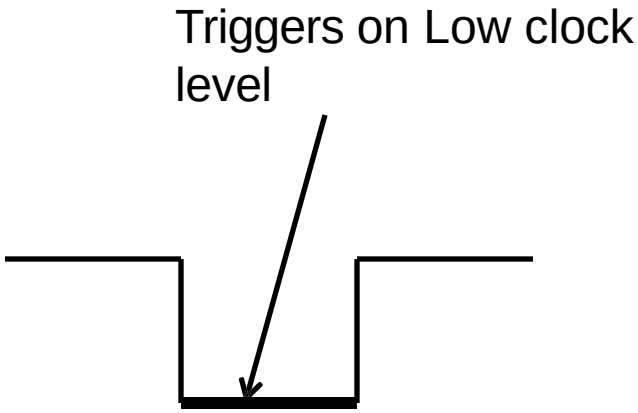


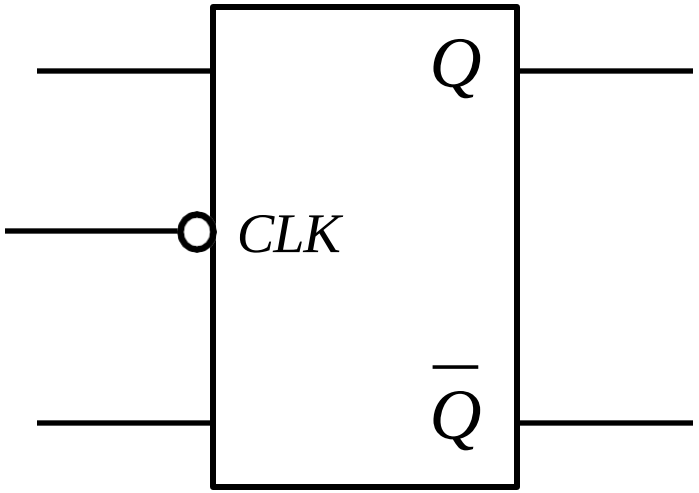


Symbol

Low Level Triggering

- ✓ A flip flop who responds to a clock signal during the time at which it is in the logic Low state.

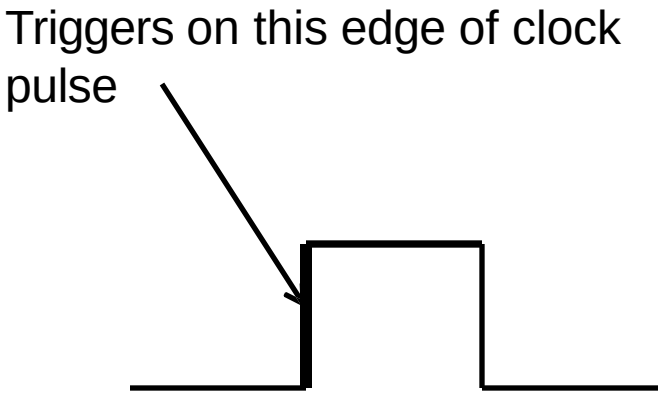


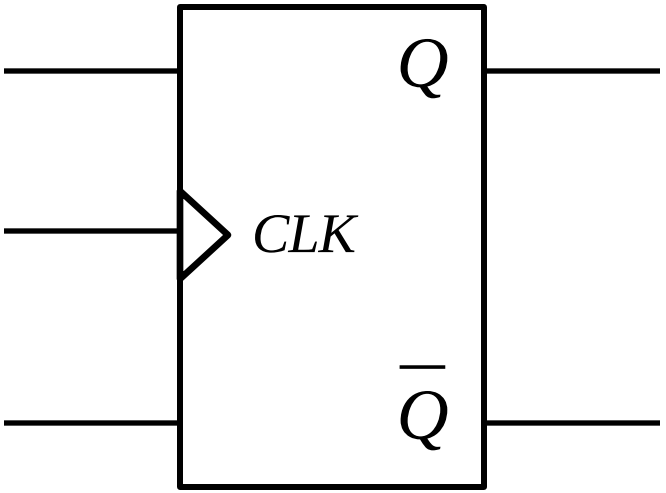


Symbol

Positive Edge Triggering

- ✓A flip flop who responds to a clock signal during Low to High transition of clock pulse.

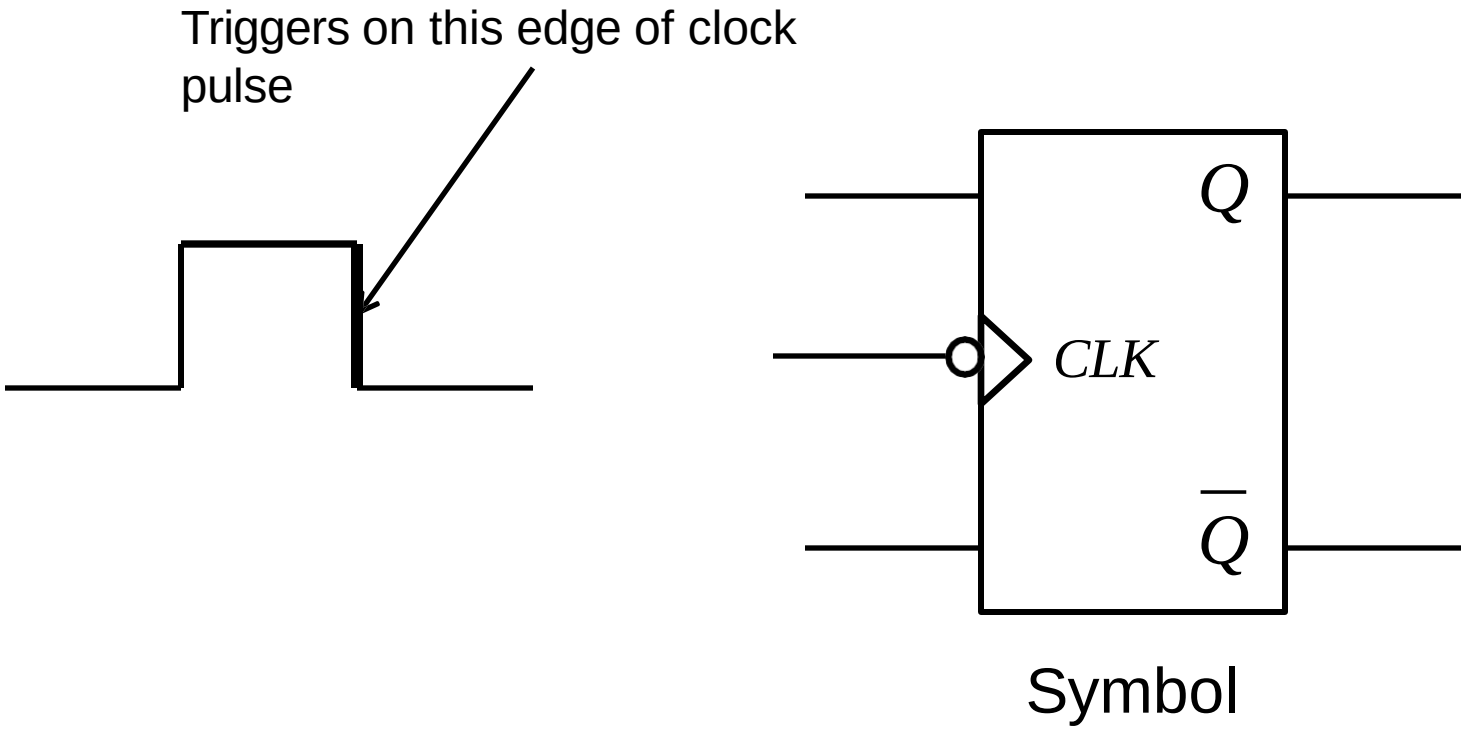




Symbol

Negative Edge Triggering

- ✓A flip flop who responds to a clock signal during High to Low transition of clock pulse.



Symbol

Gates Vs Flip Flops

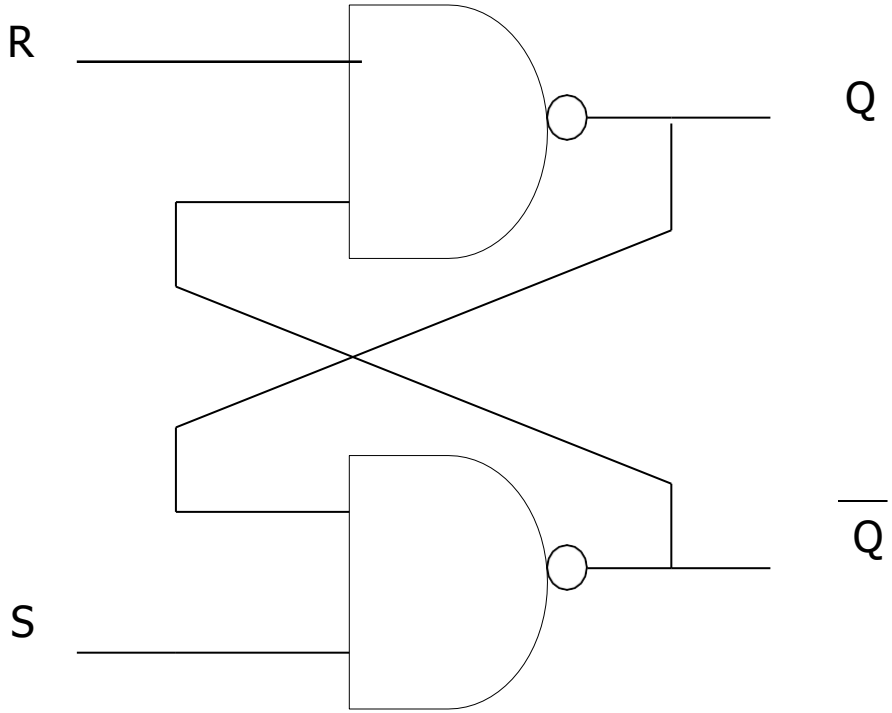
- ✓ **Gates** are the building block of the **logic circuits**. Their primary function is to perform decision making operations.

- ✓ **Flip-flops** are the building blocks of the **digital circuits**. Their primary function is to store the binary bits.

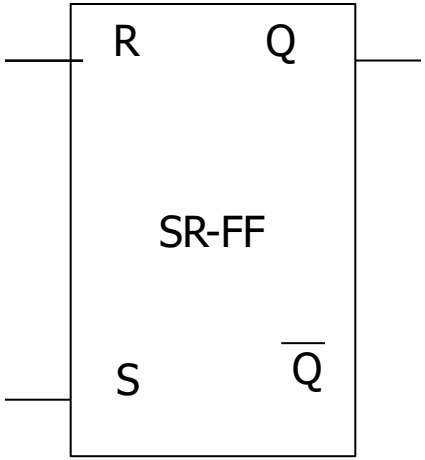
Flip Flops

- ✓ A flip-flop is a bi-stable device, with inputs, that remains in a given state as long as power is applied and until input signals are applied to cause its output to change.
- ✓ There are four basic different types of flip-flops:
  - SR Flip Flop
  - D Flip Flop
  - JK Flip Flop
  - T Flip Flop

SR Flip Flop



Circuit Diagram



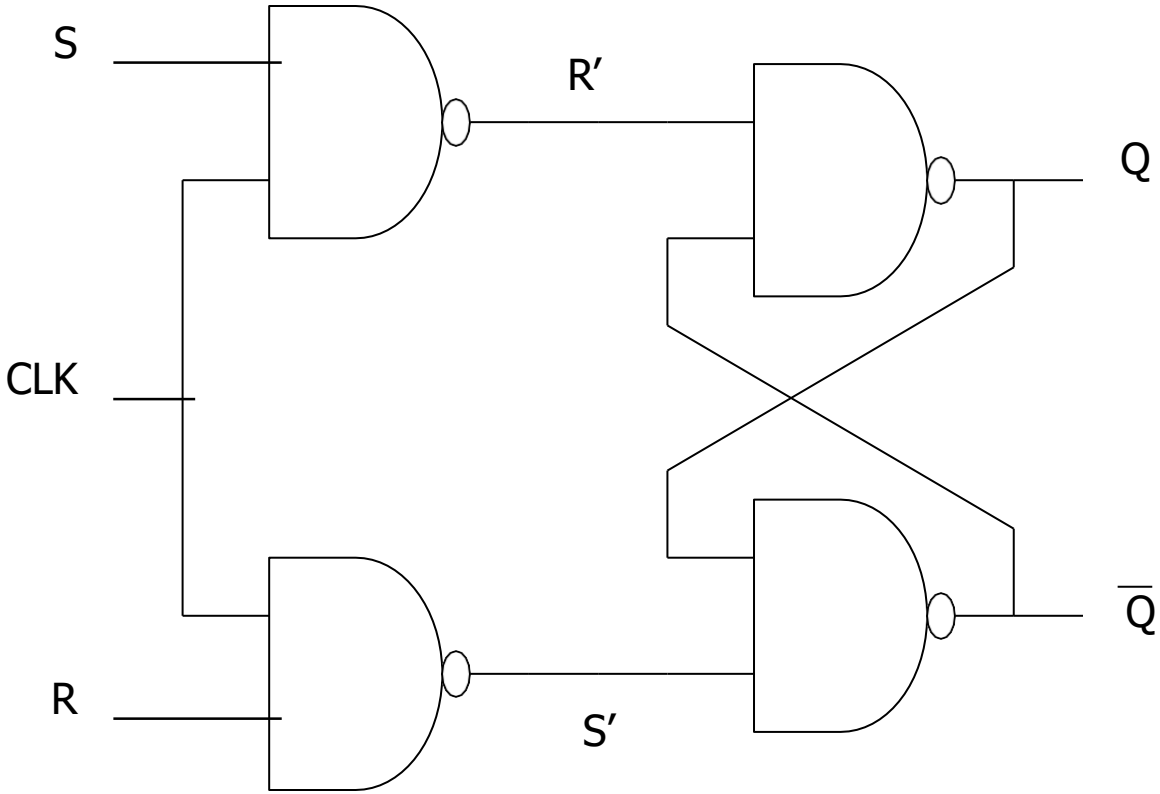
Symbol

SR Flip Flop

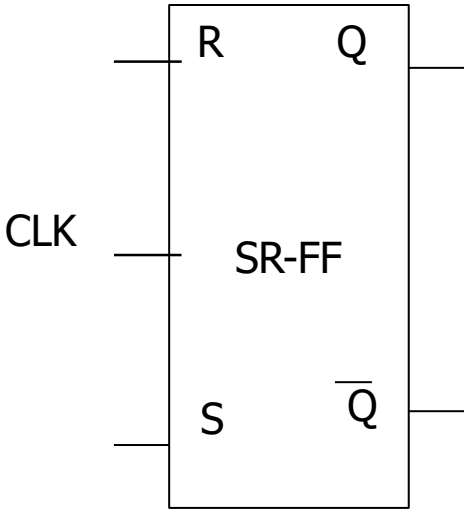
Logic Table

S	R	Q_n	Q_{n+1}	State
0	0	1	1	Indetermine
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	1	No Change
1	1	1	0	

Clocked SR Flip Flop



Circuit Diagram



Symbol

Clocked SR Flip Flop

Logic Table

CLK	S	R	Q	$\overline{Q}$	State
	0	0	Q	$\overline{Q}$	No Change
	0	1	0	1	Reset
	1	0	1	0	Set
	1	1	X	X	Prohibited
	X	X	Q	$\overline{Q}$	No Change

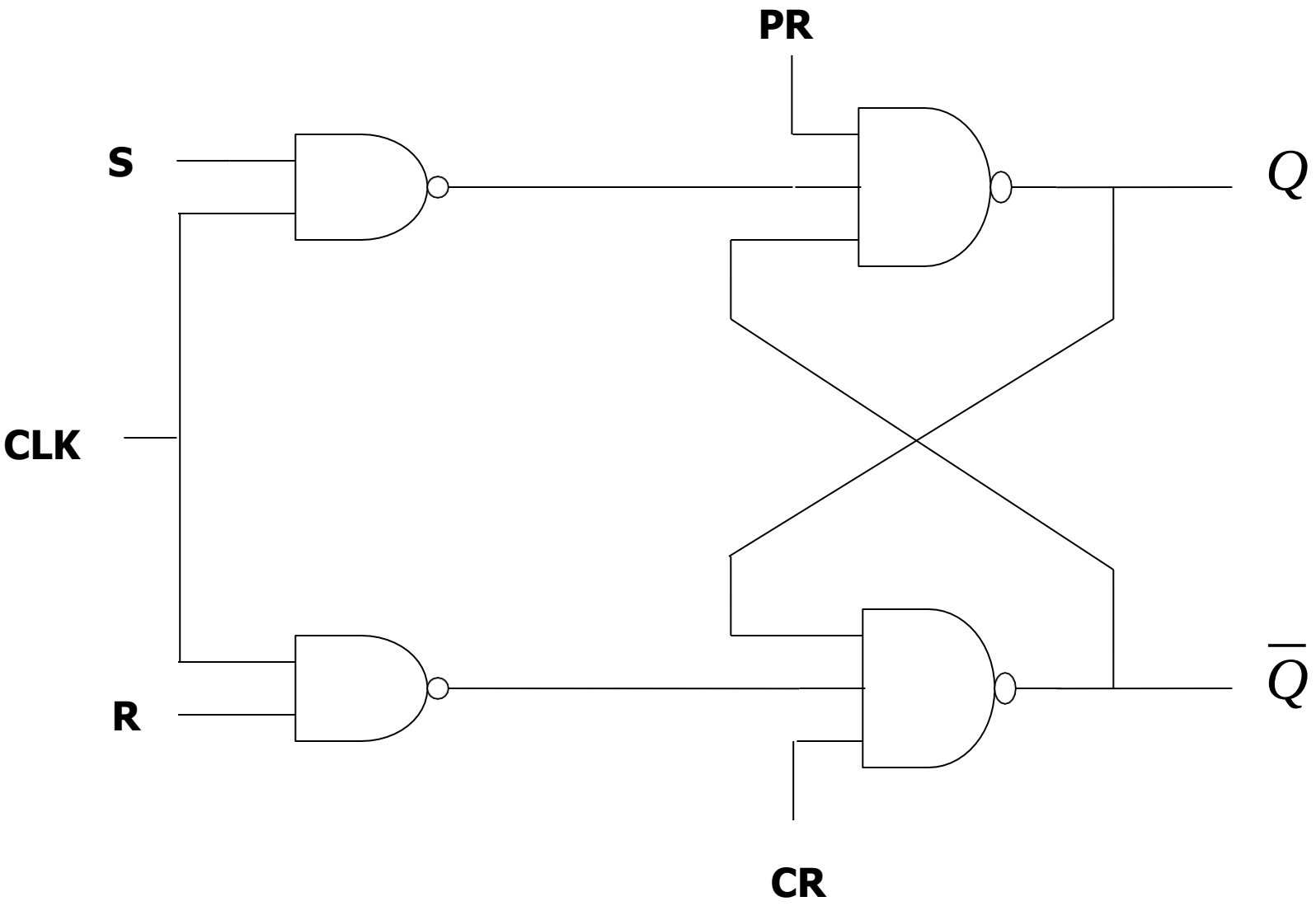
Synchronous Inputs

- ✓ The S and R (for SR FF), D (for D FF), J and K (JK FF), and so on….,inputs are control inputs.
- ✓ These inputs are also called “Synchronous Inputs” because the action of these inputs are synchronized with the action of clock.
- ✓ The flip flop changes state only on the application of clock signal.

Asynchronous Inputs

- ✓ In addition to synchronousinputs the flip flops have one or more asynchronous inputs .
- ✓ These asynchronous inputs operate independently of control and clock input.
- ✓ Two asynchronous inputs are $\overline{PRESET}$ and $\overline{CLEAR}$
- ✓ These are mostly active LOW inputs.

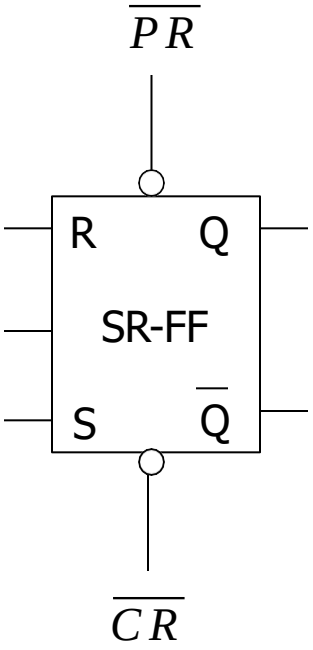
Clocked SR Flip Flop with Clear and Preset Inputs



Asynchronous Inputs: $\overline{PRESET}$ and $\overline{CLEAR}$

Sr. No.	Action	Function/Operation
1	$\overline{PRESET} = 1$ $\overline{CLEAR} = 1$	Both these asynchronous inputs are inactive. The flip flop responds to synchronous inputs.
2	$\overline{PRESET} = 0$ $\overline{CLEAR} = 1$	The PRESET is activated and Q is immediately set to 1 irrespective of synchronous inputs. The clock input cannot affect the flip flop when PR=0.
3	$\overline{PRESET} = 1$ $\overline{CLEAR} = 0$	The CLEAR is activated and Q is immediately cleared to 0 irrespective of synchronous inputs. The clock input cannot affect the flip flop when CR=0.
4	$\overline{PRESET} = 0$ $\overline{CLEAR} = 0$	This condition should not be used as it leads to race condition

Clocked SR Flip Flop with Clear and Preset Inputs



Inputs					O/P		Comment
CLK	$\overline{CR}$	$\overline{PR}$	**S**	**R**	Q	$\overline{Q}$	
	1	1	0	0	Q	Q	No Change
	1	1	0	1	0	1	Reset
	1	1	1	0	1	0	Set
	1	1	1	1	X	X	Invalid
X	0	1	X	X	0	1	Clear
X	1	0	X	X	1	0	Preset
X	0	0	X	X	X	X	Invalid

Synchronous Sequential Circuits Vs Asynchronous Sequential Circuits

Synchronous Seq Circuits	Asynchronous Seq Circuits
✓ In Synchronous circuits, memory elements are clocked FFs.	✓ In Asynchronous circuits, memory elements are either unclocked FFs or time delay elements.
✓ In Synchronous circuits, the change in input signals can affect memory elements upon activation of clock signals.	✓ In Asynchronous circuits, the change in input signals Can affect memory elements at any instant of time.

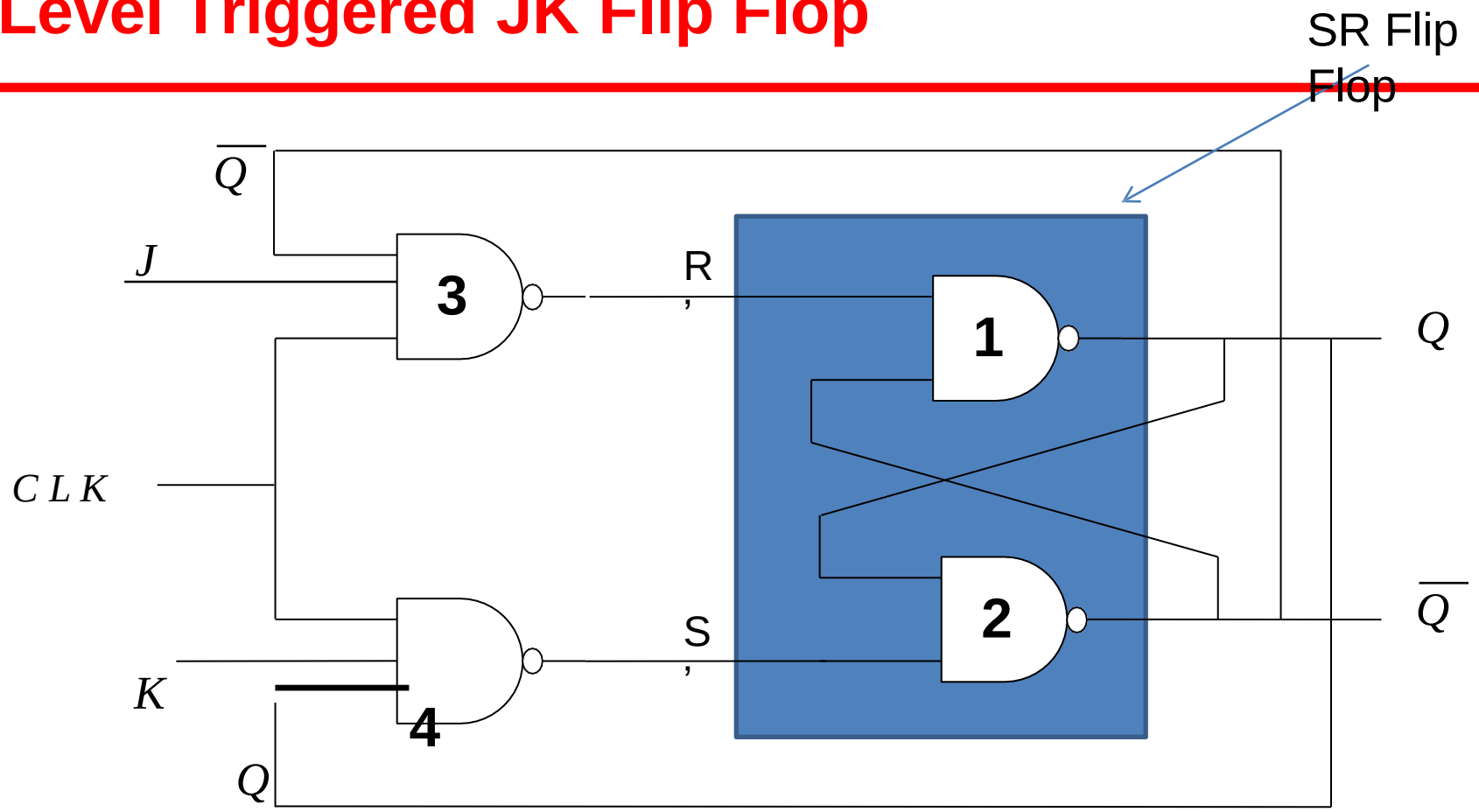
Synchronous Sequential Circuits Vs Asynchronous Sequential Circuits

Synchronous Seq Circuits	Asynchronous Seq Circuits
✓ The maximum operating speed of the clock depends on time delays involved	✓ Becauseof the absenceof the clock, asynchronous circuits can operate faster than synchronous circuits.
✓ Easier to design	✓ More difficult to design

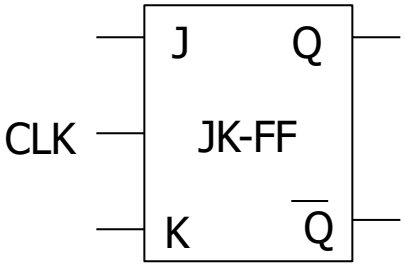
Drawbacks of SR Flip Flop

- ✓ If both inputs are pulled down to logic level 0, both outputs will be at logic level 1. This state should not be allowed to occur in flip-flops.

Level Triggered JK Flip Flop



Circuit Diagram of Level Triggered JK Flip Flop

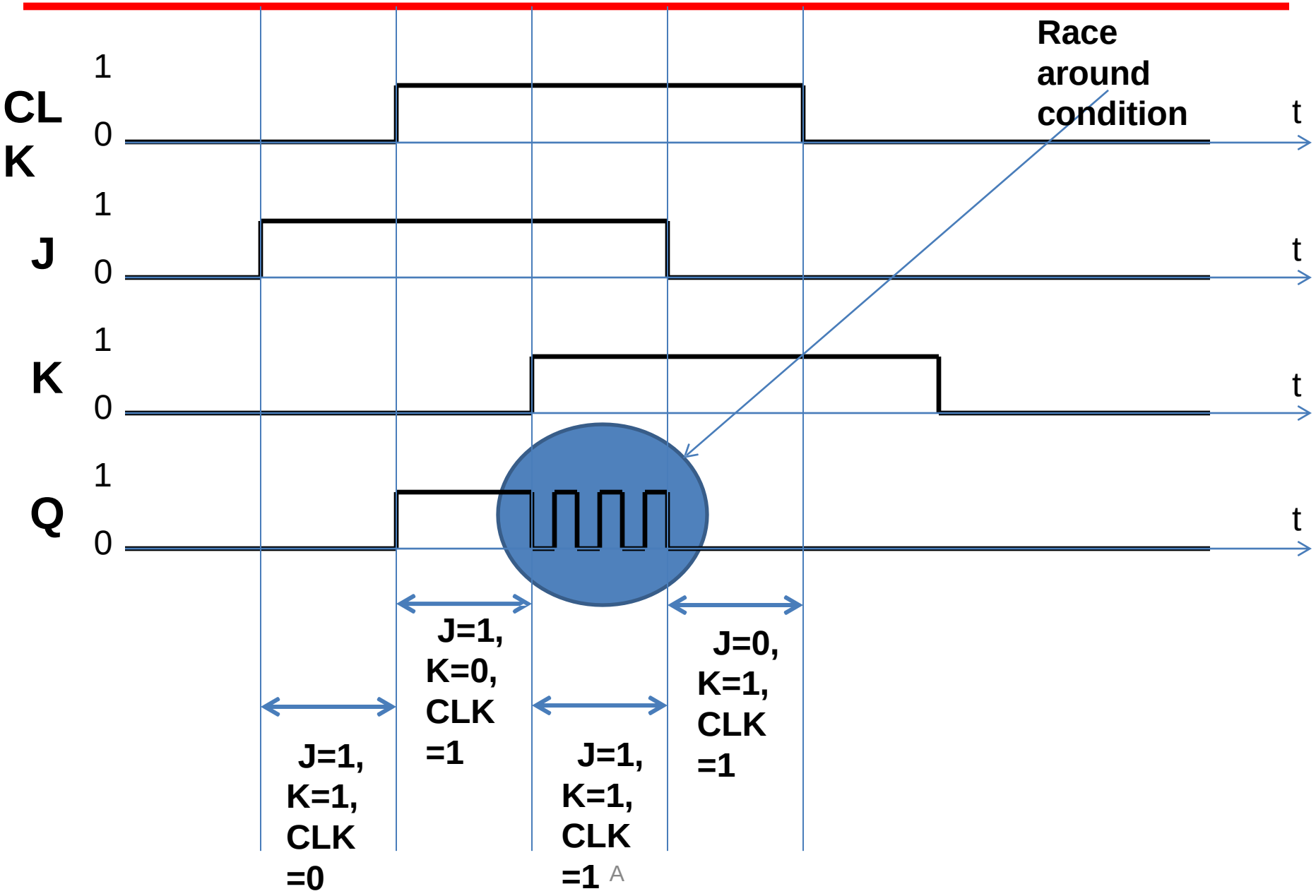


Symbol

Level Triggered JK Flip Flop

Inputs			Outputs		State
CLK	J	K	Q_{n+1}	$\overline{Q_{n+1}}$	
0	X	X	Q_n	$\overline{Q_n}$	Flip Flop is Disabled (No Change)
1	0	0	Q_n	$\overline{Q_n}$	
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	$\overline{Q_n}$	Q_n	Toggle

Timing Diagram of Level Triggered JK Flip Flop



Race Around Condition in JK Flip Flop

- ✓ The “Race Around Condition” that we are going to explain occurs J=K=1 i.e. when the flip flop is in the toggle mode.
- ✓ When J=1, K=1 and CLK=1, hence the JK flip flop is in the toggle mode and Q becomes low & $\overline{Q}$ becomes high.
- ✓ These changed outputs get applied at the inputs of NAND gates 3 and 4 of the JK FF. thus the new inputs to gates 3 and 4 are:

  NAND – 3 : J=1, CLK=1, $\overline{Q}$

  = 1 NAND – 4 : K=1,

  CLK=1, Q = 0

- ✓ Hence R’ will become 0 and S’ will become 1.

Race Around Condition in JK Flip Flop

- ✓ Therefore after a time period corresponding to the propagation delay, the Q and $\bar{Q}$ outputs will change to,

  Q = 1 and $\bar{Q}$ =0

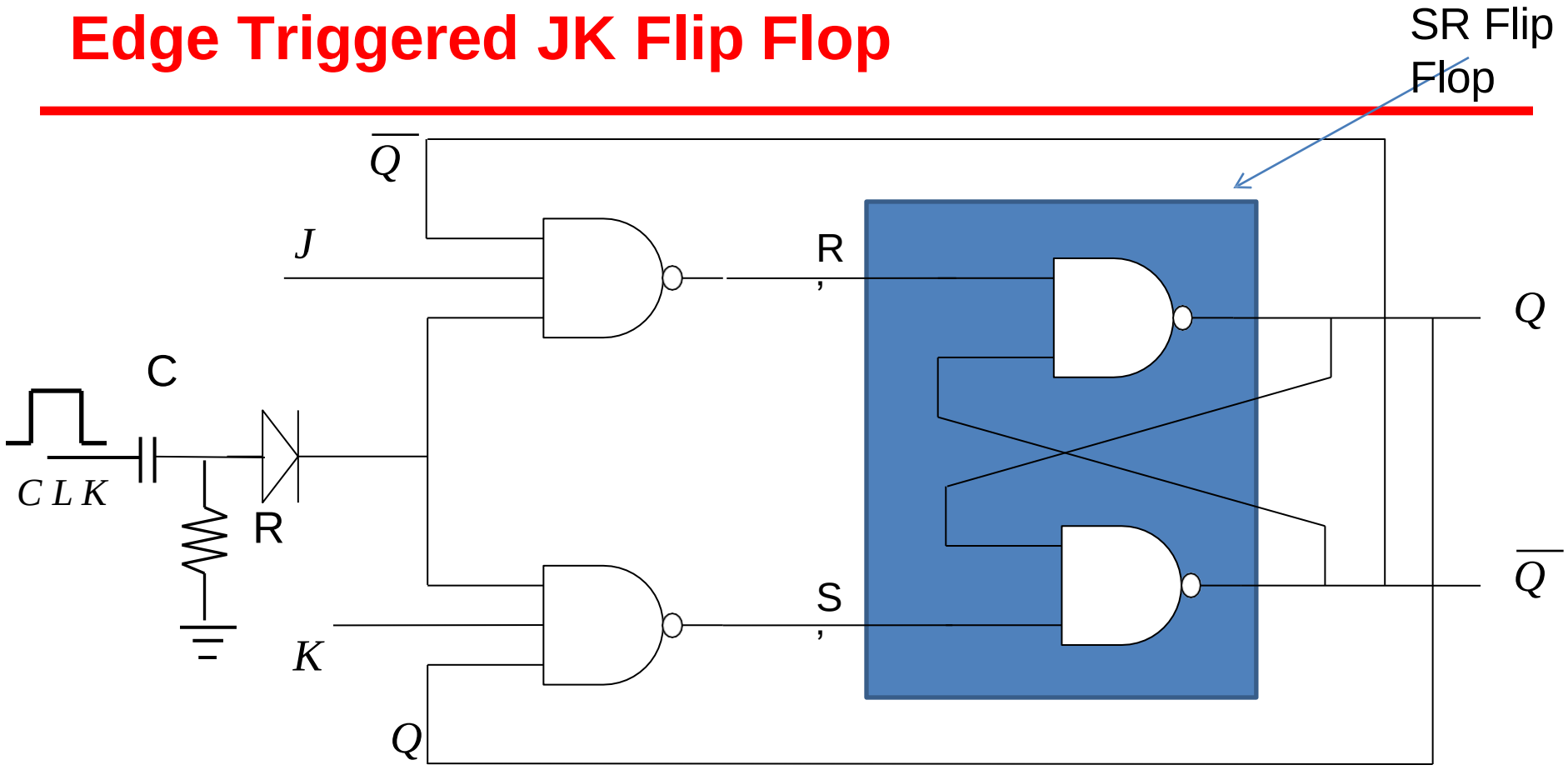
- ✓ These changed output again get applied to the inputs of NAND-3 and 4 and the outputs will toggle again.
- ✓ Thus as long as J=K=1 and CLK=1, the outputs will keep toggling indefinitely as shown in figure. This multiple, toggling in the JK Flip flop is called as **"Race Around Condition"**. It must be avoided

How to Avoid Race Around Condition in JK Flip Flop

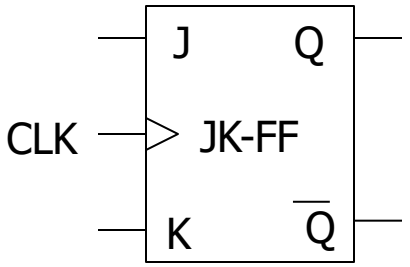
✓ The race around condition in JK flip flop can be avoided by

1. Using Edge Triggered JK Flip Flop
2. Using Master Slave JK Flip Flop

Edge Triggered JK Flip Flop



Circuit Diagram of Edge Triggered JK Flip Flop



Symbol

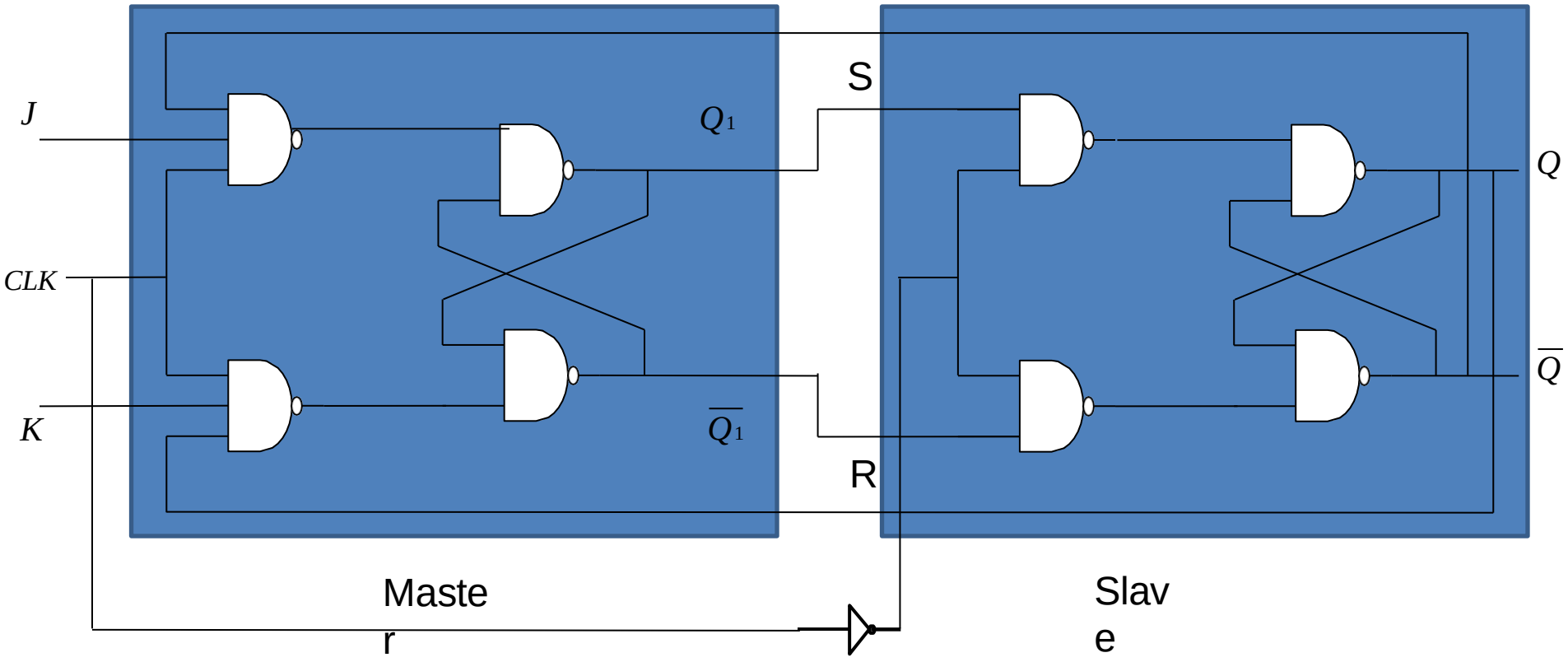
Positive Edge Triggered JK Flip Flop

Inputs			Outputs		State
CLK	J	K	Q_{n+1}	$\overline{Q_{n+1}}$	
0 or 1	X	X	Q_n	$\overline{Q_n}$	Flip Flop is Disabled (No Change)
↓	X	X	Q_n	$\overline{Q_n}$	
↑	0	0	Q_n	$\overline{Q_n}$	
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	$\overline{Q_n}$	Q_n	Toggle

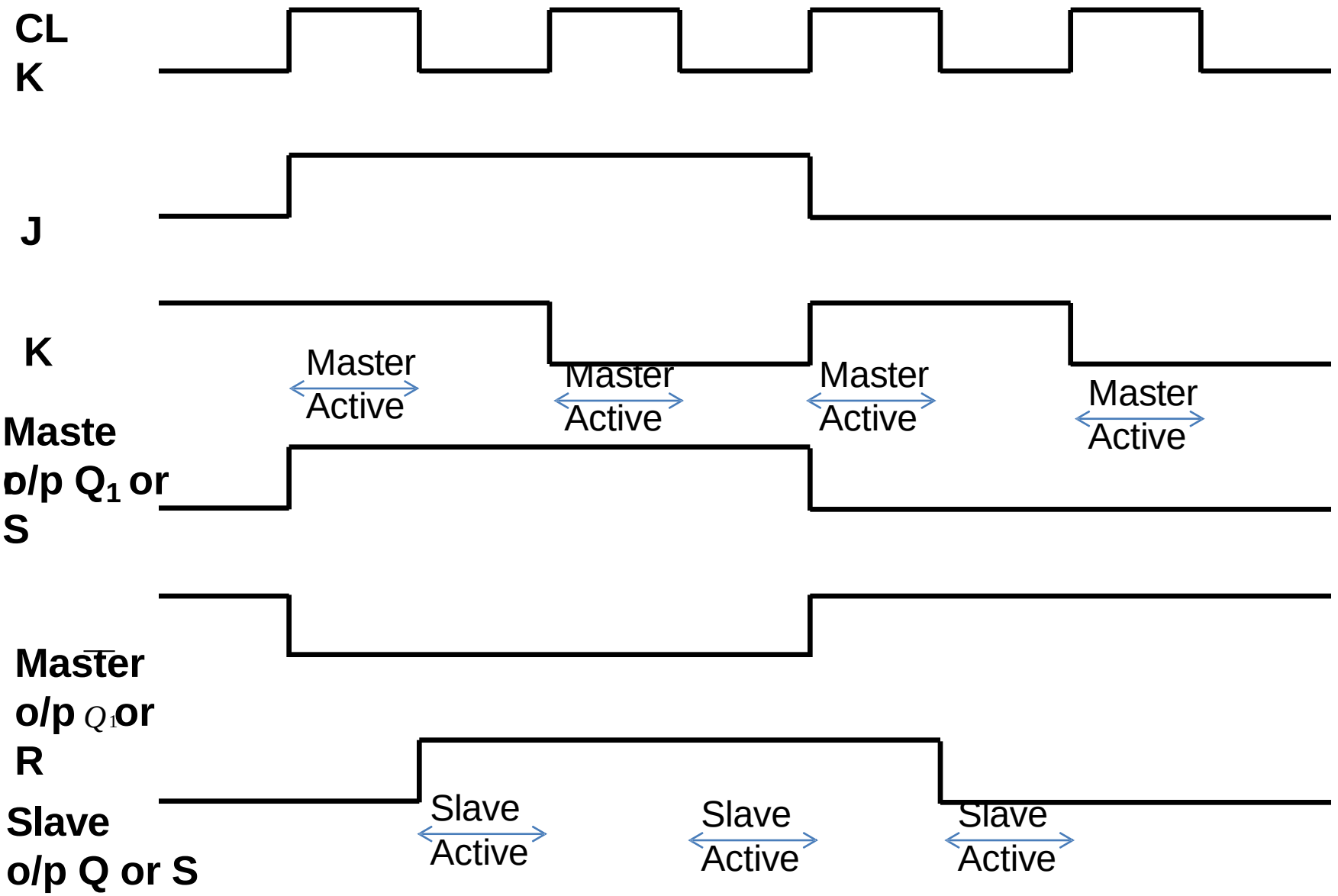
How to Avoid Race Around Condition in JK Flip Flop using Edge Triggered JK Flip Flops?

- ✓ For the racing around to take place, it is necessary to have the enable input high along with J=K=1.
- ✓ As the enable input remains high for a long time in a JK Flip Flop, the problem of multiple toggling arises.
- ✓ But in edge triggered JK Flip Flop, the positive clock pulse is present only for a very short time.
- ✓ Hence by the time changed outputs return back to the inputs of NAND gates 3 and 4, the clock pulse has died down to zero. Hence the multiple toggling can not take place.
- ✓ Thus the edge triggering avoids the race around condition.

Master Slave JK Flip Flop



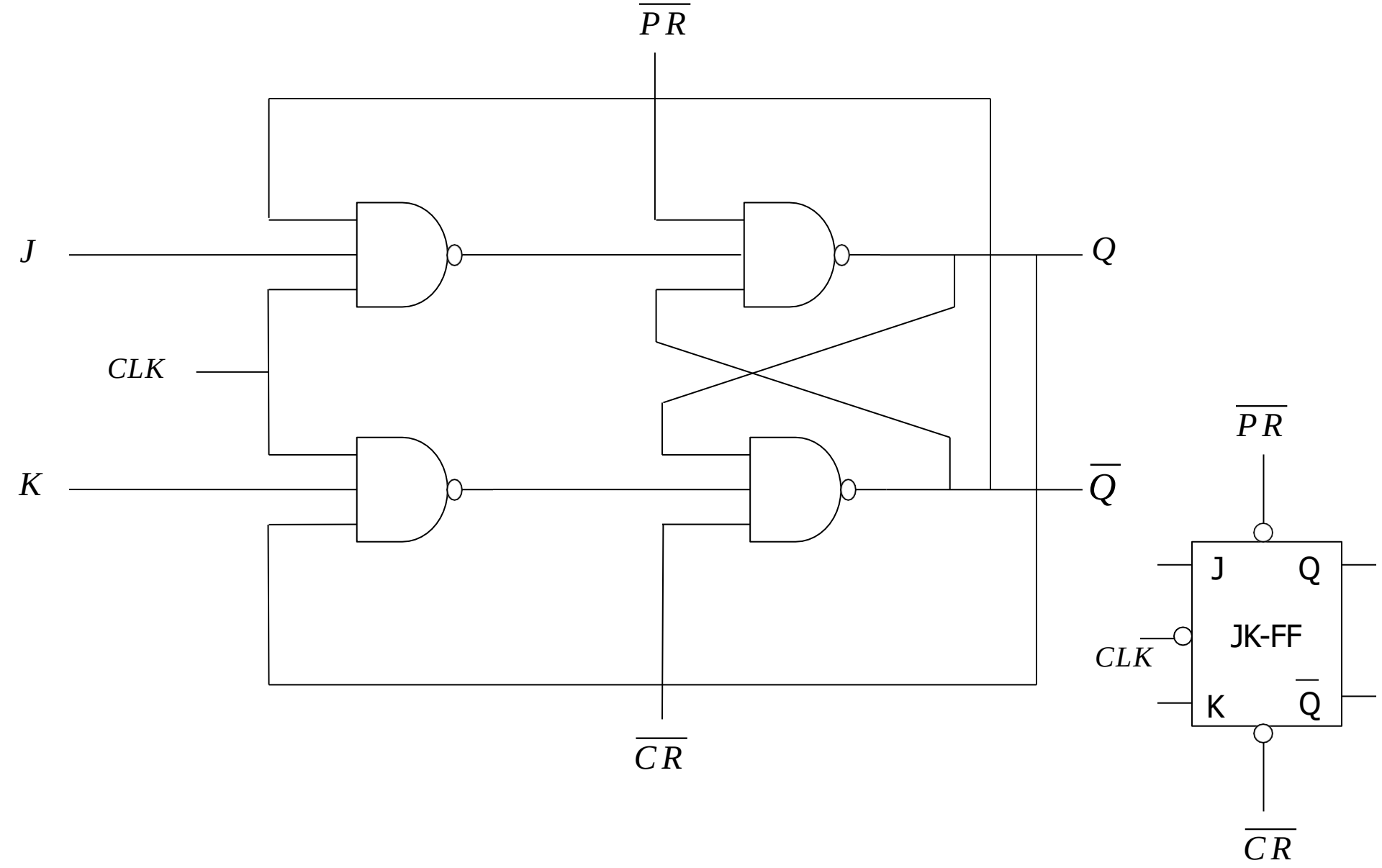
Timing Diagram of Master Slave JK Flip Flop



How to Avoid Race Around Condition in JK Flip Flop using MS JK Flip Flops?

- ✓ When Clock=1, J=1, K=1, Master Active and slave becomes inactive. Outputs of master will toggle. So S and R also will be inverted.
- ✓ When clock = 0: Master inactive, slave active. Outputs of the slave will toggle.
- ✓ These changed output are returned back to the master inputs.
- ✓ But since clock=0, the master is still inactive. So it does not respond to these changed outputs.
- ✓ This avoids the multiple toggling which leads to the race around condition. Thus Master Slave JK Flip Flop will avoid the race around condition.

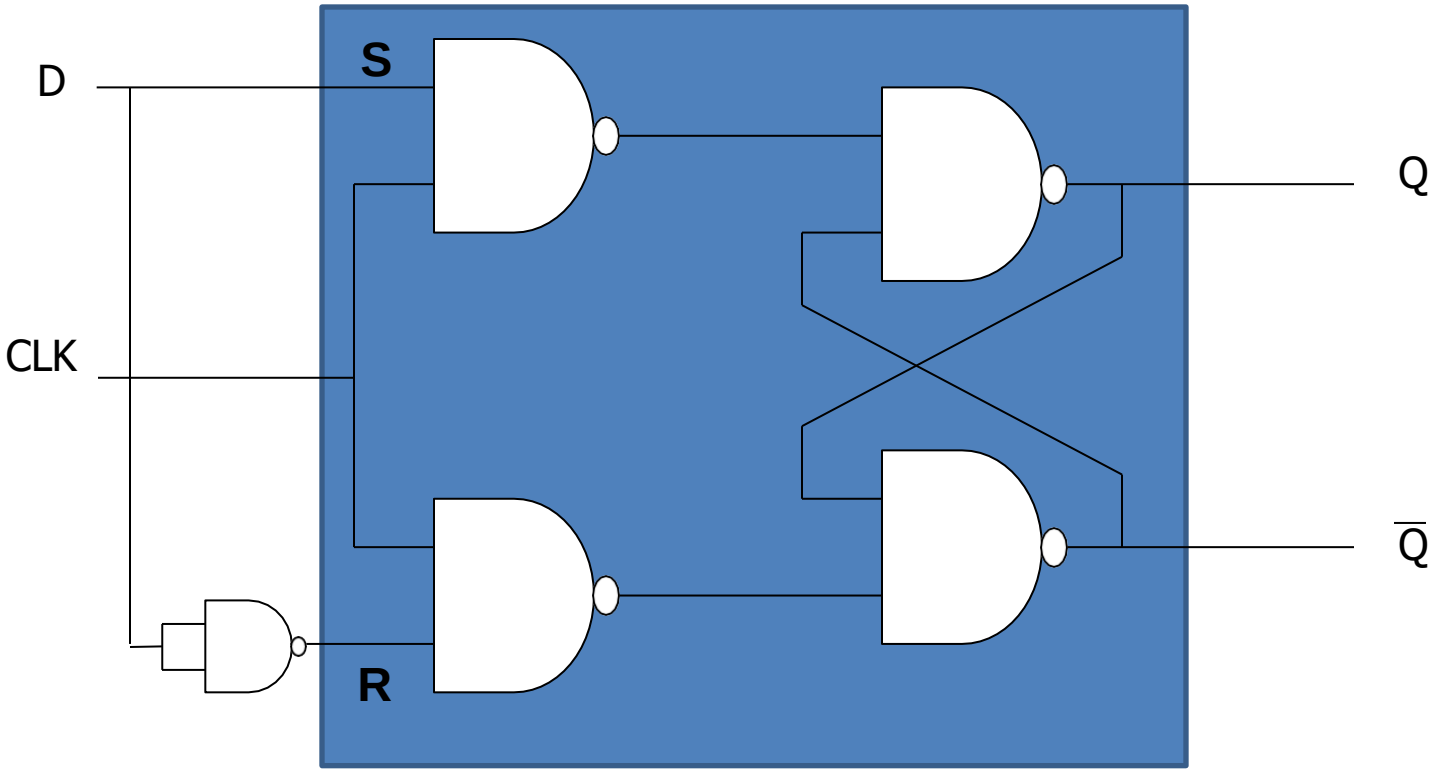
Clocked JK Flip Flop with Clear and Preset Inputs



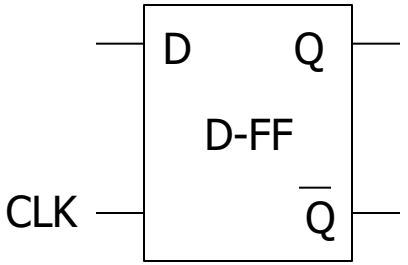
Clocked JK Flip Flop with Clear and Preset Inputs

Inputs					Outputs		Comment
Asynchronous		Synchronous					
PR	CR	CLK	J	K	Q	$\overline{Q}$	
0	0	X	X	X	1	1	Prohibited
0	1	0	X	X	1	0	Preset
1	0	0	X	X	0	1	Clear
1	1	↓	0	0	Q	$\overline{Q}$	No Change
1	1	↓	0	1	0	1	Reset
1	1	↓	1	0	1	0	Set
1	1	↓	1	1	$\overline{Q}$	Q	Toggle

D Flip Flop



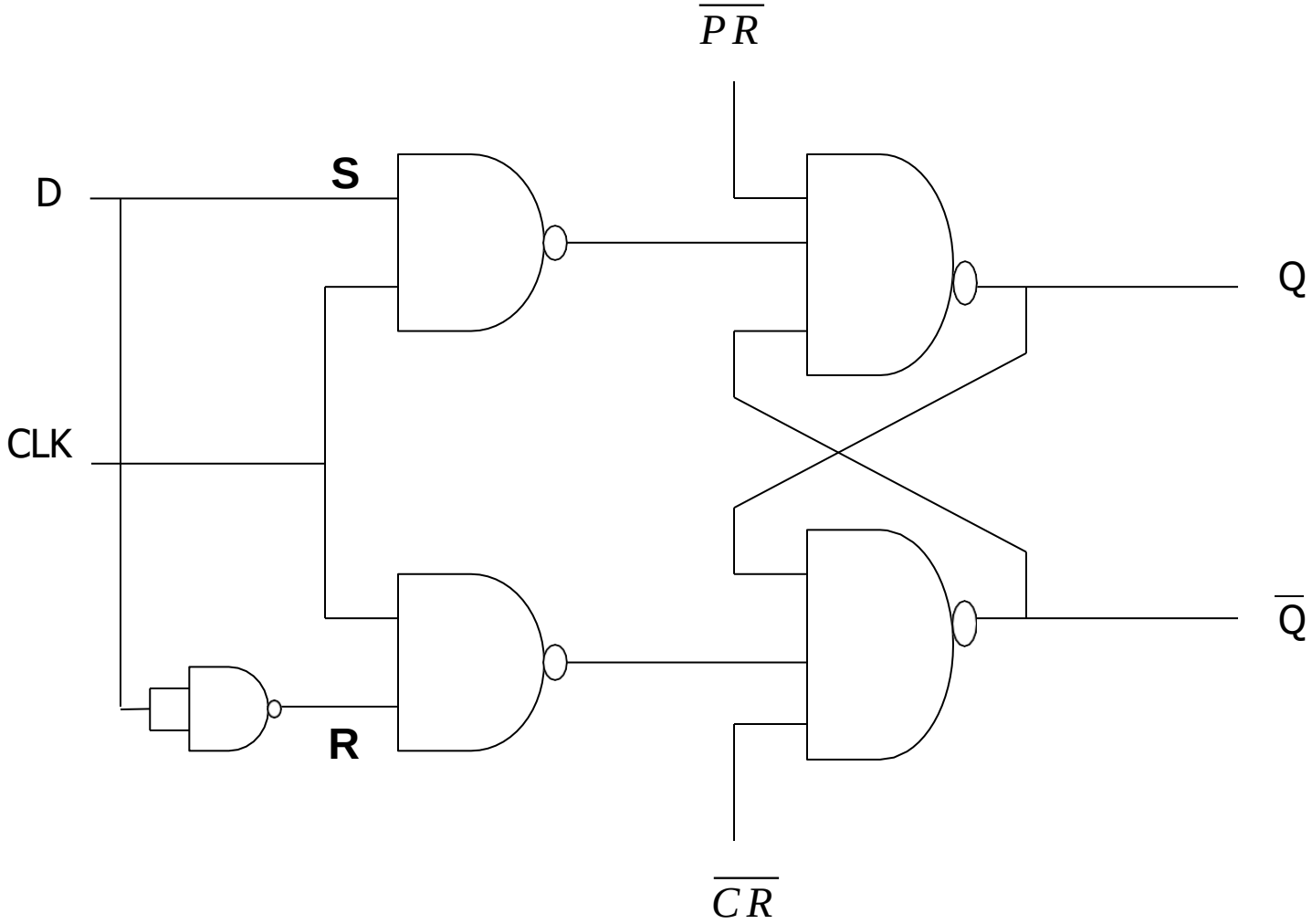
Clocked SR Flip Flop

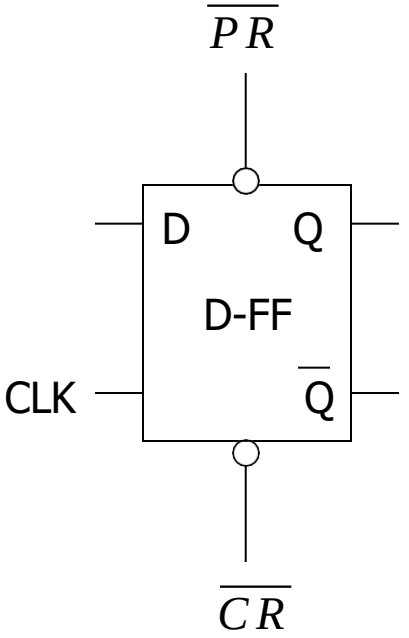


D Flip Flop

Inputs		Output		Comment
CLK	D	Q_{n+1}	$\overline{Q_{n+1}}$	
0	X	Q_n	$\overline{Q_n}$	Last Value or No Change
1	0	0	1	Reset
1	1	1	0	Set

D Flip Flop with Preset and Clear Inputs

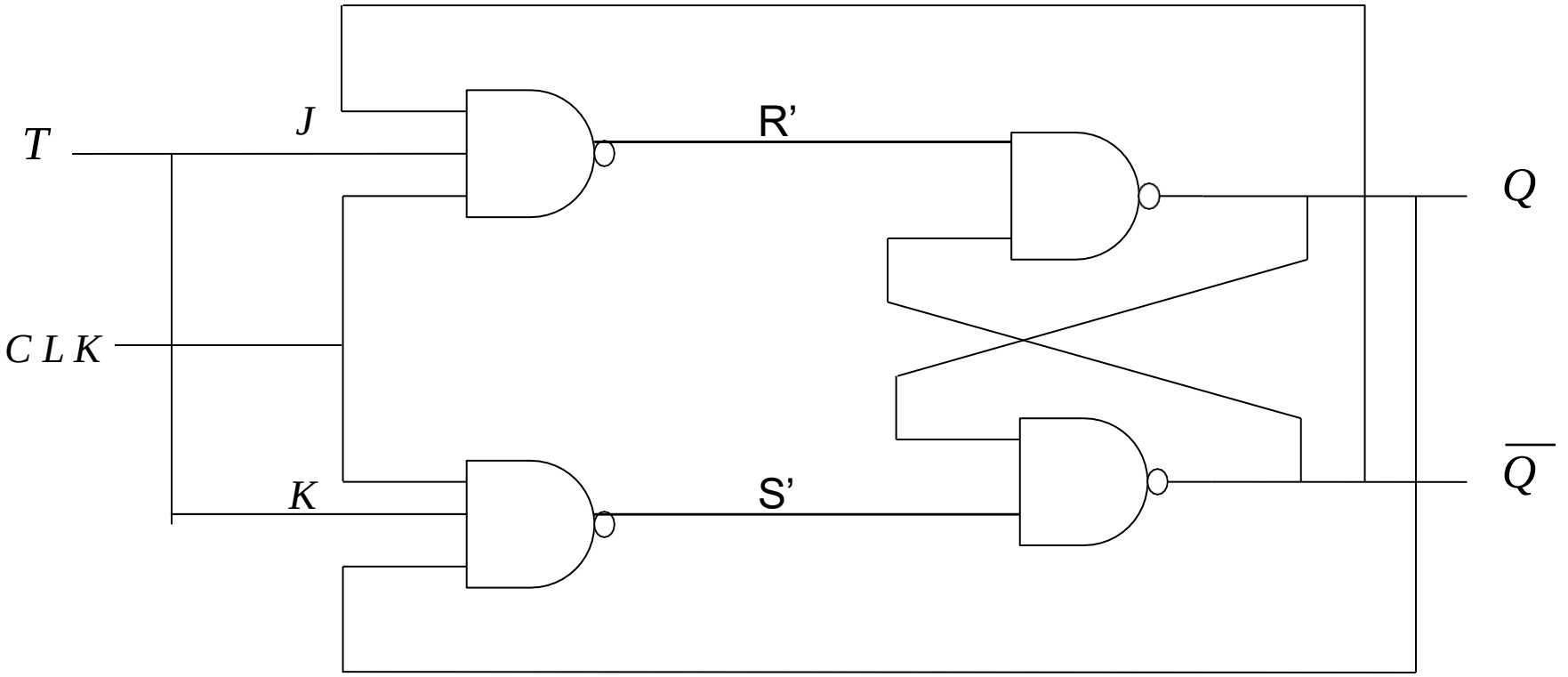


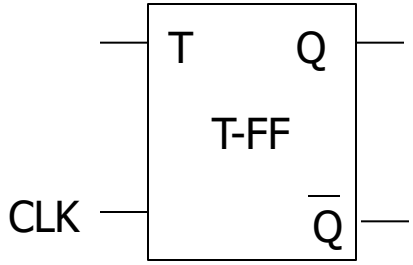


D Flip Flop with Preset and Clear Inputs

Inputs				Output		Comment
$\overline{PR}$	$\overline{CR}$	CLK	D	Q_{n+1}	$\overline{Q_{n+1}}$	
0	0	X	X	$\overline{Q_n}$	Q_n	Avoid
0	1	X	X	1	0	Preset
1	0	X	X	0	1	Clear
1	1	0	X	Q_n	$\overline{Q_n}$	No Change
1	1	1	0	0	1	Reset
1	1	1	1	1	0	Set

T Flip Flop

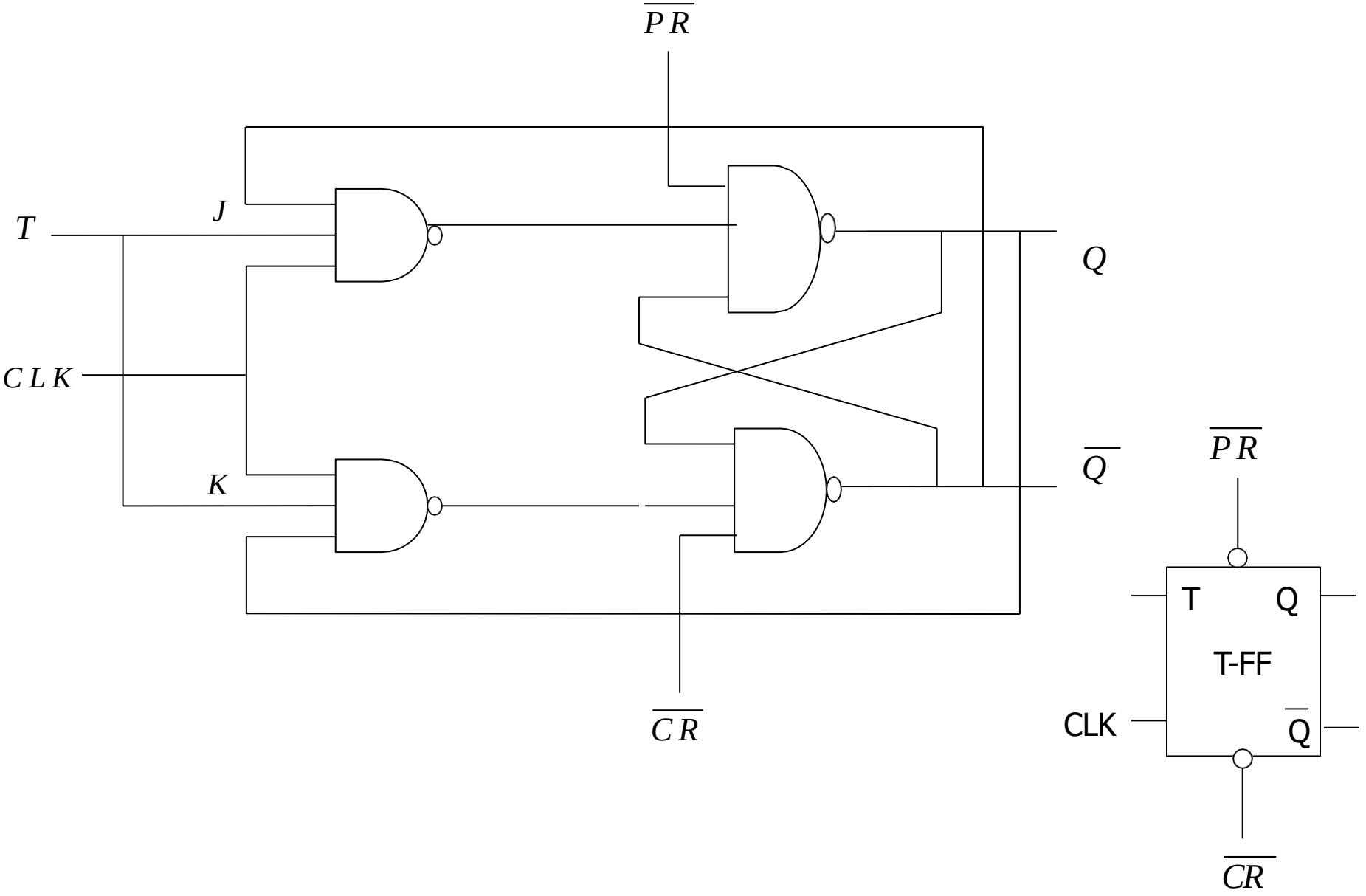




T Flip Flop

Inputs		Output		Comment
CLK	T	Q_{n+1}	$\overline{Q_{n+1}}$	
0	X	Q_n	$\overline{Q_n}$	No Change
1	0	Q_n	$\overline{Q_n}$	No Change
1	1	$\overline{Q_n}$	Q_n	Toggle

T Flip Flop with Preset and Clear Inputs



T Flip Flop with Preset and Clear Inputs

Inputs				Output		Comment
$\overline{PR}$	$\overline{CR}$	CLK	T	Q_{n+1}	$\overline{Q_{n+1}}$	
0	0	X	X	$\overline{Q_n}$	Q_n	Avoid
0	1	X	X	1	0	Preset
1	0	X	X	0	1	Clear
1	1	0	X	Q_n	$\overline{Q_n}$	No Change
1	1	1	0	Q_n	$\overline{Q_n}$	No Change
1	1	1	1	$\overline{Q_n}$	Q_n	Toggle

Applications of Flip Flops

- ✓ Elimination of Keyboard Debounce
- ✓ As a memory element
- ✓ In various types of registers
- ✓ In counters
- ✓ As delay element
- ✓ Parallel Data storage
- ✓ Serial Data Storage
- ✓ Serial to Parallel Conversion
- ✓ Parallel to Serial Conversion
- ✓ Frequency Division

Excitation Tables of Flip Flops

- ✓ Logic tables show the state of the output(s) of a logic circuit as a function of its inputs **at the same time**.
- ✓ Since, clocked digital systems have **memory**, their behavior depends on inputs **in the past** as well as the present values of the inputs.

Excitation Tables of Flip Flops

- Thus, flip-flops cannot be described by simple truth tables. Instead, we use excitation or transition tables. These show:

  - ✓ output before the clock transition — often labelled Q_n
  - ✓ inputs at the clock transition — such as *S* and *R*
  - ✓ occasionally the type of clock transition – positive/negative edge-triggered
  - ✓ the resulting output after the clock transition — often labelled Q_{n+1}

- It is important to remember that Q_n and Q_{n+1} describe the same signal but at different times. The notation can vary, e.g. Q_0 and Q instead.

Excitation Table of SR Flip Flop

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	?

Truth Table

Excitation Table

Present State O/P	Next State O/P	Required Inputs	
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Excitation Table of SR Flip Flop

- ✓ **$0 \rightarrow 0$ transition:** If the present state of the FF is 0 and if it has to remain 0 when a clock pulse is applied, the inputs can be either S=0, R=0 (no change condition) or S=0, R=1 (Reset condition). Thus, S has to be 0 but R can be either 0 or 1. So SR=0X for this transition.
- ✓ **$0 \rightarrow 1$ transition:** If the present state of the FF is 0 and if it has to go 1 state when a clock pulse is applied, the inputs have to be S=1 and R=0 (set condition). So SR=10 for this transition.

Excitation Table of SR Flip Flop

- ✓ $1 \rightarrow 0$ **transition:** If the present state of the FF is 1 and if it has to go to 0 state when a clock pulse is applied, the inputs have to be S=0 and R=1 (Reset condition). So SR=01 for this transition.
- ✓ $1 \rightarrow 1$ **transition:** If the present state of the FF is 1 and if it has to remain 1 when a clock pulse is applied, the inputs can be either S=0, R=0 (no change condition) or S=1, R=0 (set condition). Thus, R has to be 0 but S can be either 0 or 1. So SR=X0 for this transition.

Excitation Table of JK Flip Flop

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Truth Table

Excitation Table

Present State O/P	Next State O/P	Required Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table of JK Flip Flop

- ✓ $0 \rightarrow 0$ **transition:** The present state of the FF is 0 and it has to remain 0 after the clock pulse. This can happen with either J=0, K=0 (no change condition) or J=0, K=1 (reset condition). Thus, J has to be 0 but K can be either 0 or 1. So JK=0X for this transition.
- ✓ $0 \rightarrow 1$ **transition:** The present state of the FF is 0 and it has to go 1 state after the clock pulse. This can happen with either J=1, K=0 (set condition) or J=1, K=1 (toggle condition). Thus, J has to be 1 but K can be either 0 or 1. So JK=1X for this transition.

Excitation Table of JK Flip Flop

- ✓ $1 \rightarrow 0$ **transition:** The present state of the FF is 1 and it has to go to 0 after the clock pulse. This can happen with either J=0, K=1 (reset condition) or J=1, K=1 (toggle condition). Thus, K has to be 1 but J can be either 0 or 1. So JK=X1 for this transition.
- ✓ $1 \rightarrow 1$ **transition:** The present state of the FF is 1 and it has to remain in 1 state after the clock pulse. This can happen with either J=0, K=0 (no change condition) or J=1, K=0 (set condition). Thus, K has to be 0 but J can be either 0 or 1. So JK=X0 for this transition.

Excitation Table of D Flip Flop

D	Q_{n+1}
0	0
1	1

Truth Table

Excitation Table

Present State O/P	Next State O/P	Required Inputs
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Excitation Table of D Flip Flop

- ✓ For a D Flip Flop, the next state is always equal to the D input and it is independent of the present state. Therefore, D must be 0 if Q_{n+1} has to be 1 regardless of the value of Q_n.

Excitation Table of T Flip Flop

T	Q_{n+1}
0	Q_n
1	$\overline{Q}_n$

Truth Table

Excitation Table

Present State O/P	Next State O/P	Required Inputs
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	1

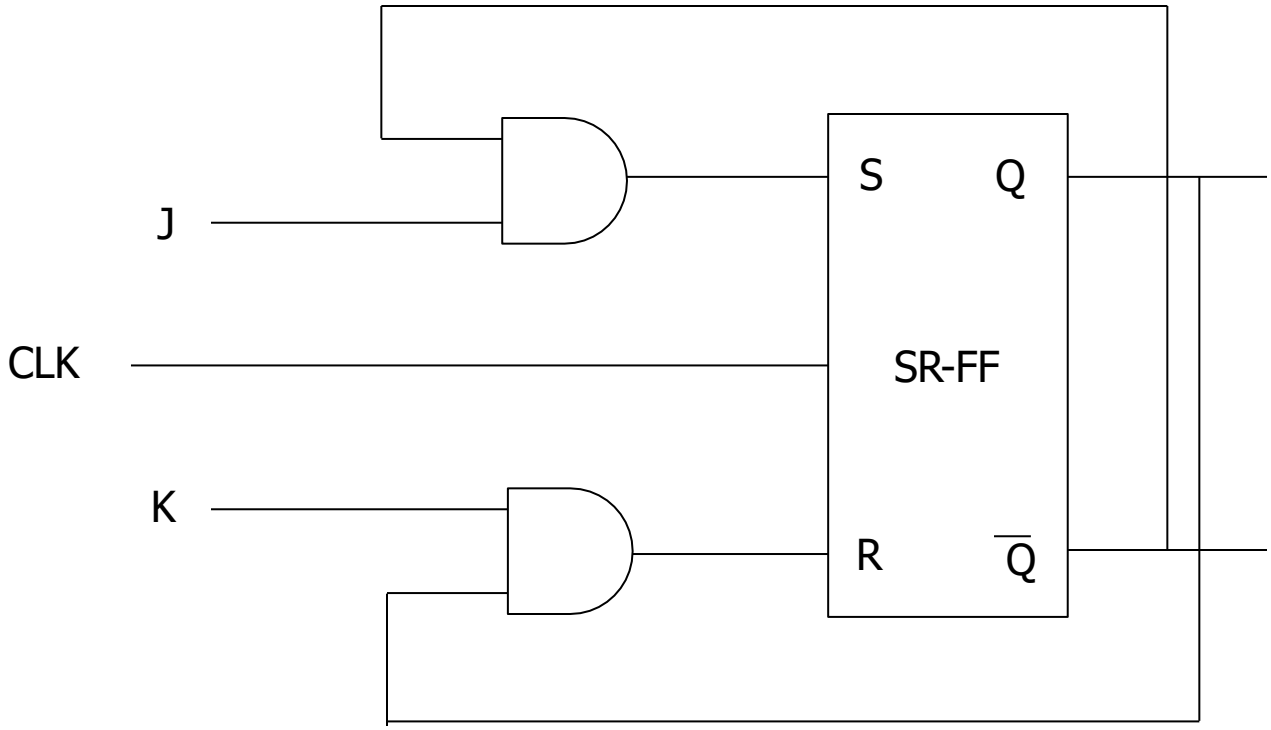
Excitation Table of T Flip Flop

- For a T Flip Flop, when the input T=1, the state of the Flip flop is complemented and when T=0, the state of the Flip Flop remains unchanged.

  Thus, for $0 \rightarrow 0$ and $1 \rightarrow 1$ transitions must T be 0 and for $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions T must be 1.

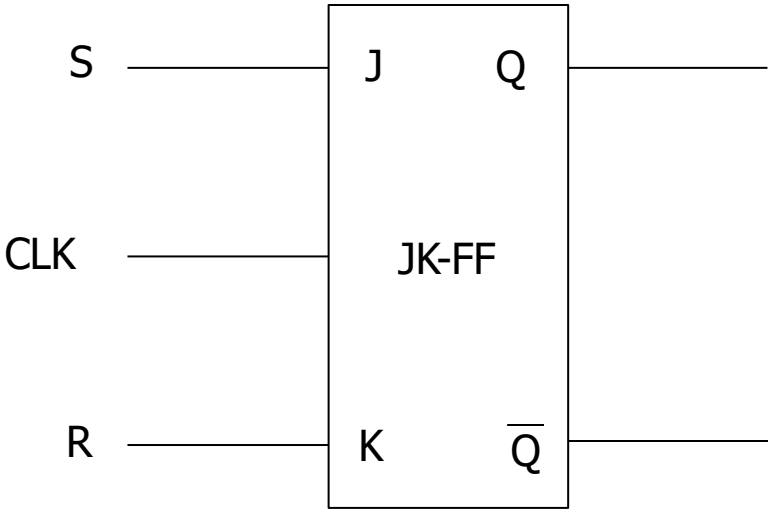
Conversion of Flip Flop

S R Flip to J K Flip Flop:



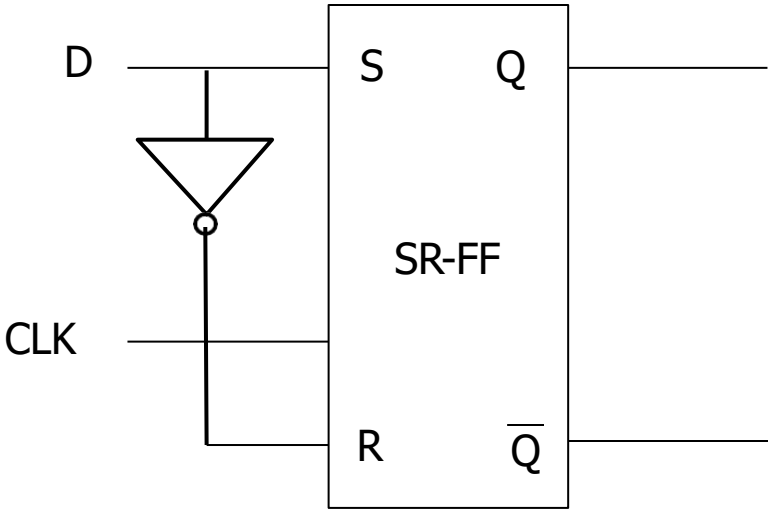
Conversion of Flip Flop

J K Flip to S R Flip Flop:



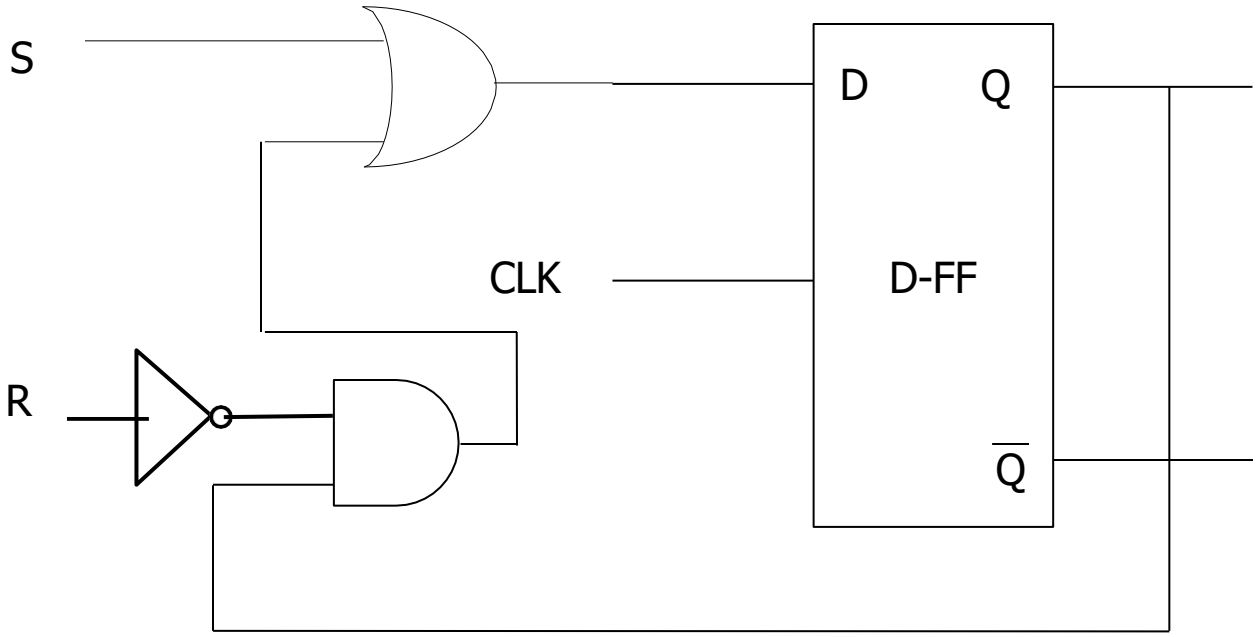
Conversion of Flip Flop

S R Flip to D Flip Flop:



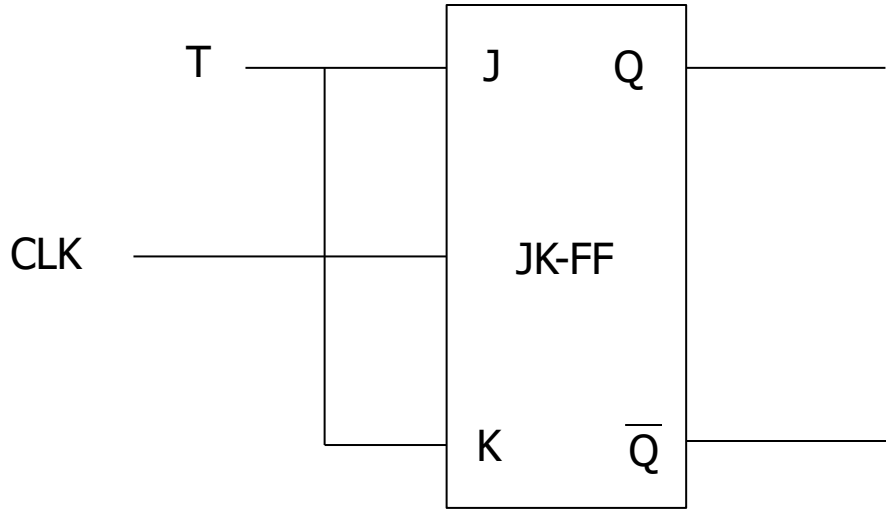
Conversion of Flip Flop

D Flip to S R Flip Flop:



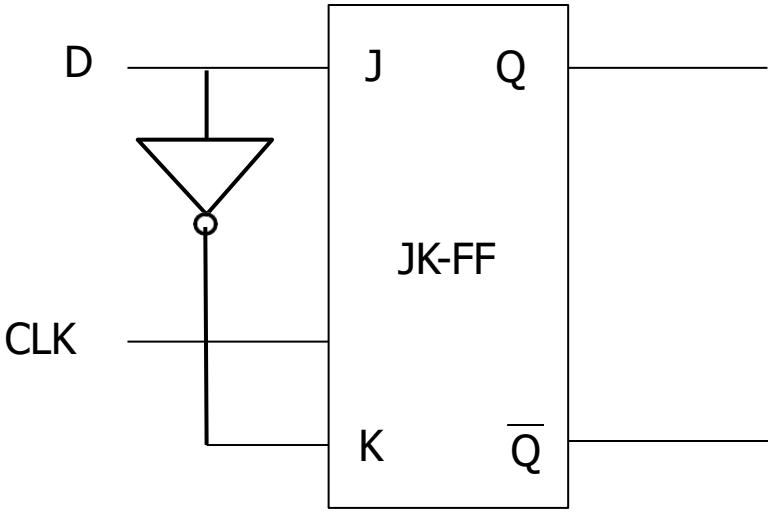
Conversion of Flip Flop

J K Flip to T Flip Flop:



Conversion of Flip Flop

J K Flip to D Flip Flop:



Conversion of Flip Flop

D Flip to J K Flip Flop: