CompArch Midterm

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1 Specification Document

The system in question is the LED controller in a bike light.

The system's input is a single button, and its output is a single LED.

The LED controller has four operational modes, enumerated and explained below. Pushing the button causes a change in state (see Figure 1).

1. Off: the LED is consistently off.
2. On: the LED is consistently on.
3. Dim: the LED pulses at 128Hz with a pulse width of 50% to simulate 50% brightness. Most humans don't detect flicker above 75Hz, so the LED doesn't look like it's blinking in the Dim state. [1]
4. Blink: the LED pulses at 1Hz with a pulse width of 50%. At 1Hz, the LED completes one on/off cycle per second.

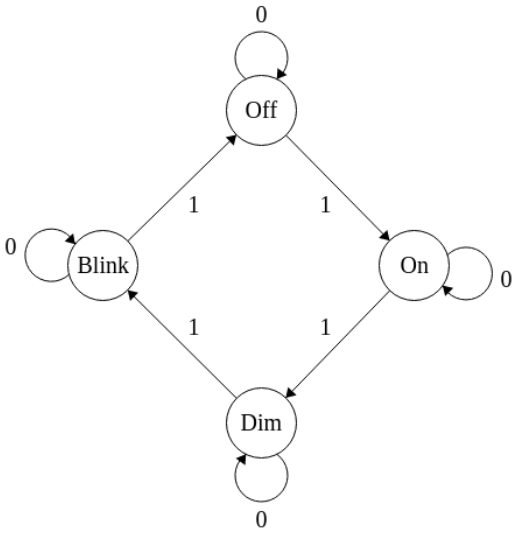


Figure 1: Finite state machine representation of the LED controller's operational modes. The arrows coming out of each state represent the position of the button – when the button is pressed down (1), the finite state machine transitions to the next state in the cycle. When it is not pressed down (0), the finite state machine stays in its current state.

[1] https://en.wikipedia.org/wiki/Flicker_fusion_threshold

2 Block Diagram

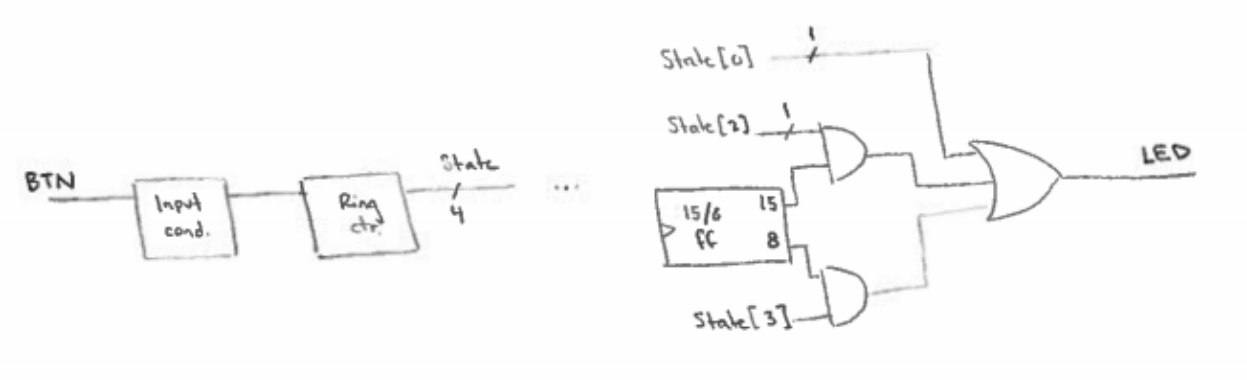


Figure 2: Caption

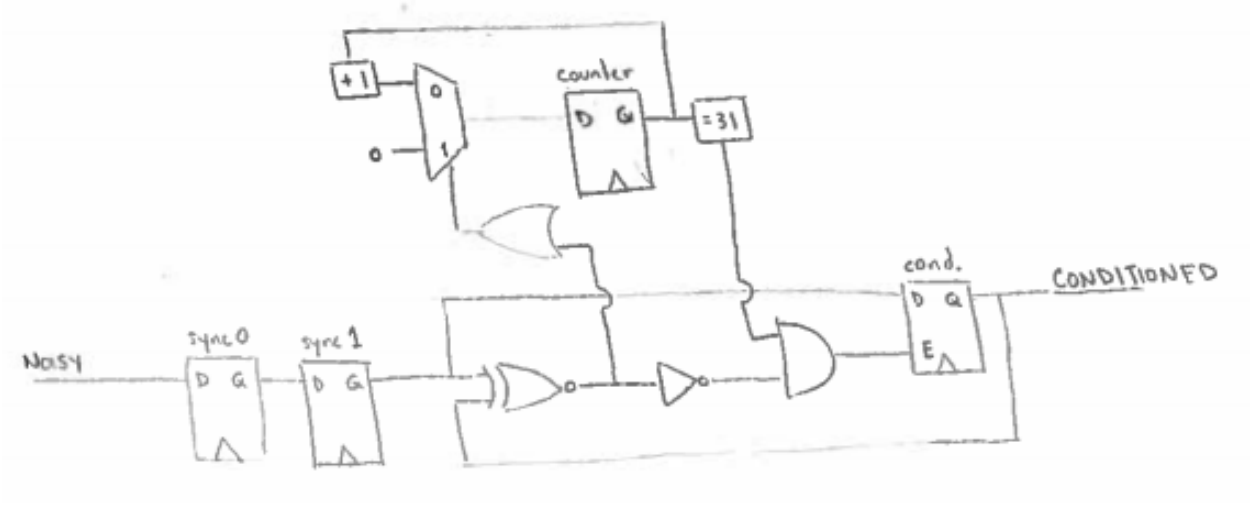
Subcomponent	Gate Inputs Per	Count	Total Gate Inputs
Input conditioner	117	1	117
4-bit ring counter	83	1	83
8- and 15- T flip flop	210	1	210
2-input AND	3	2	6
3-input OR	4	1	4
			420

3 Components

3.1 Input Conditioner

The input conditioner filters a noisy input signal by ensuring that it is consistent for some amount of time before passing it through. We assume the noisy input signal is consistent within 1 millisecond; the system clock runs at $2^{15} = 32768$Hz, so the signal is consistent after 2^5 clock cycles: $\frac{1}{2^{10}} = 0.0098$.

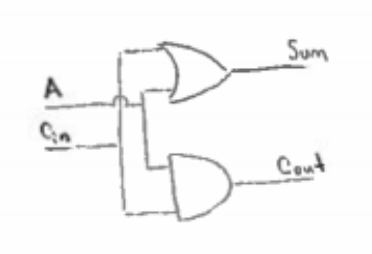
The input conditioner's inputs are a 1-bit noisy signal and the clock, and its output is a 1-bit conditioned signal.



Subcomponent	Gate Inputs Per	Count	Total Gate Inputs
Posedge-triggered D flip-flop	13	3	39
Posedge-triggered enabled DFF	20	1	20
2-to-1 multiplexer	7	1	7
2-input XNOR	8	1	8
Inverter	1	1	1
2-input AND	3	1	3
2-input OR	3	1	3
5-bit equal-to-31 checker	6	1	6
5-bit carryin adder	30	1	30
			117

3.2 1-bit carryin adder

The 1-bit carryin adder is the building block for the 5-bit carryin adder. It adds its two inputs, a 1-bit number and a carryin; it outputs the LSB of the two-bit result as the sum and the MSB of the result as the carryout.



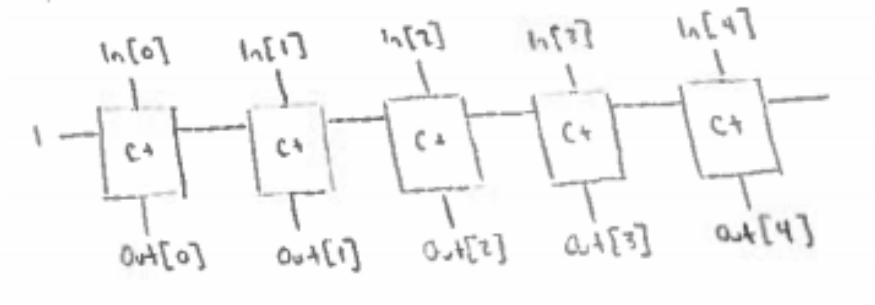
Subcomponent	Gate Inputs Per	Count	Total Gate Inputs
2-input OR	3	1	3
2-input AND	3	1	3
			6

3.3 5-bit carryin adder

The 5-bit carryin adder adds 1 to a 5-bit number via the carryin to the 1-bit adder associated with the LSB. It requires less logic to add 1 using a carryin than it does to add 00001 using a full two-operand adder.

The 5-bit carryin adder's input is a 5-bit number, and its output is also a 5-bit number: the input plus one.

This adder doesn't flag for overflow.



Subcomponent	Gate Inputs Per	Count	Total Gate Inputs
1-bit carryin adder	6	5	30
			30

3.4 5-bit equal-to-31 checker

This component checks whether its 5-bit input is equal to d31. Its output is a flag: 1 if the input is equal to 31, 0 if not.

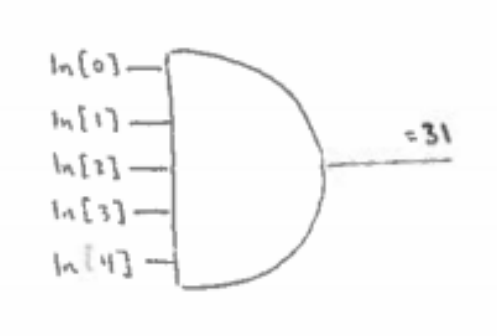


Figure 3: Caption

Subcomponent	Gate Inputs Per	Count	Total Gate Inputs
5-input AND	6	1	6
			6

3.5 T flip flop

The T flip flop's input is a clock CLK; its output is a square wave Q with half the frequency of CLK.

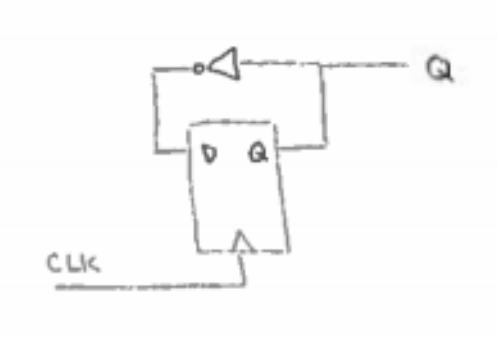


Figure 4: Caption

Subcomponent	Gate Inputs Per	Count	Total Gate Inputs
Posedge-triggered D flip flop	13	1	13
Inverter	1	1	1
			14

3.6 8- and 15- T flip flop

The 8- and 15- T flip flop produces two square waves with lower frequency than the clock. Its input is a clock; let the frequency of the clock be 2^F. It has two outputs: a square wave with a frequency of 2^{F-8} and a square wave with a frequency of 2^{F-15}.

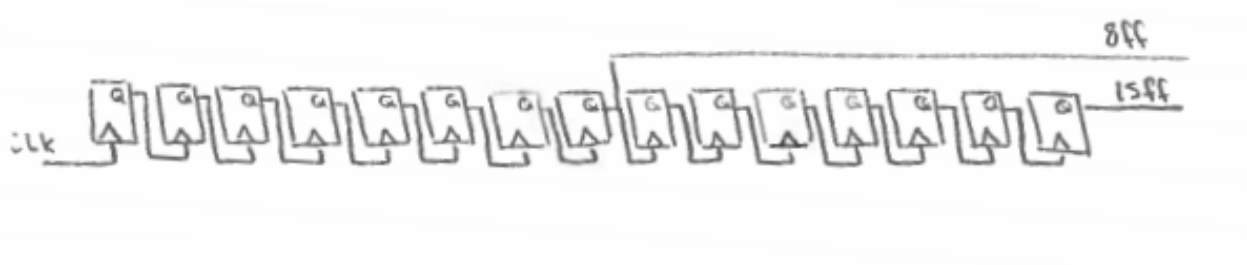


Figure 5: Caption

Subcomponent	Gate Inputs Per	Count	Total Gate Inputs
T flip flop	14	15	210
			210

3.7 2-input XNOR[2]

The 2-input XNOR outputs 1 when its two 1-bit inputs are equal and 0 when they are not.

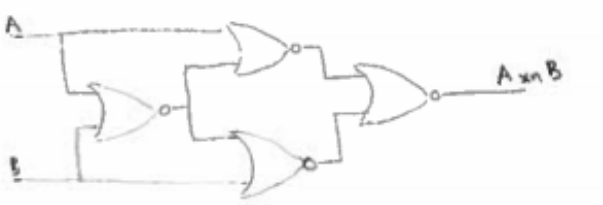


Figure 6: Caption

Subcomponent	Gate Inputs Per	Count	Total Gate Inputs
2-input NOR	2	4	8
			8

[2] https://en.wikipedia.org/wiki/XNOR_gate