3 ISA vs. Microarchitecture [45 points]

Circle whether each of the following is an aspect of the ISA or the microarchitecture.

Note: we will subtract 2 points for each ***incorrect*** *answer and award 0 points for each unanswered question.*

1. [3 points] Width of the immediate value in an ADD instruction.

   [1. ISA] 2. Microarchitecture

2. [3 points] The algorithm used by the ALU to perform multiplication.

   1. ISA [2. Microarchitecture]

3. [3 points] Number of bits required for indexing the source register of a store instruction.

   [1. ISA] 2. Microarchitecture

4. [3 points] Number of entries in the L3 cache.

   1. ISA [2. Microarchitecture]

5. [3 points] The data cache organization (e.g., direct-mapped, set-associative).

   1. ISA [2. Microarchitecture]

6. [3 points] Support for conveying prefetching hints to the hardware via the compiler.

   [1. ISA] 2. Microarchitecture

7. [3 points] Available data types (e.g., integer) for arithmetic and logic operations.

   [1. ISA] 2. Microarchitecture

8. [3 points] Cache coherence protocol in multi-core processors.

   1. ISA [2. Microarchitecture]

9. [3 points] Width of the data bus between the processor and main memory.

   1. ISA [2. Microarchitecture]

10. [3 points] The memory controller's memory request scheduling algorithm.

    1. ISA [2. Microarchitecture]

11. [3 points] Instruction encoding for control flow and branch instructions.

    [1. ISA] 2. Microarchitecture

12. [3 points] The design of the register renaming logic.

    1. ISA [2. Microarchitecture]

13. [3 points] Number of instructions decoded per cycle in a superscalar processor.

    1. ISA [2. Microarchitecture]

14. [3 points] L2 cache miss latency.

    1. ISA [2. Microarchitecture]

15. [3 points] Width of the program counter.

    [1. ISA] 2. Microarchitecture