2. For this question, use the following truth table for a 4-input logic function called Z.

Input				**Output**
A	B	C	D	Z
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

(a) (2 points) One of your friends has determined the following Boolean equation for Z:

$$Z = \overline{A} \cdot \overline{B} \cdot C + A \cdot B \cdot C + A \cdot \overline{B} \cdot C + \overline{A} \cdot B \cdot \overline{C} \cdot D$$

Does the equation match the truth table? If not, specify which terms in the equation are incorrect and what terms are missing, if any.

Solution: The equation does not match the truth table. There are the following problems:

- $\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$ is missing
- $\overline{A} \cdot \overline{B} \cdot C \cdot D$ is not in the truth table, but is included in the equation as part of the term $\overline{A} \cdot \overline{B} \cdot C$

(b) (2 points) The equation that your friend has written in 2a) also contains some redundant terms. Can you simplify it?

Solution:

$$Z = \overline{A} \cdot \overline{B} \cdot C + A \cdot C + \overline{A} \cdot B \cdot \overline{C} \cdot D$$

or

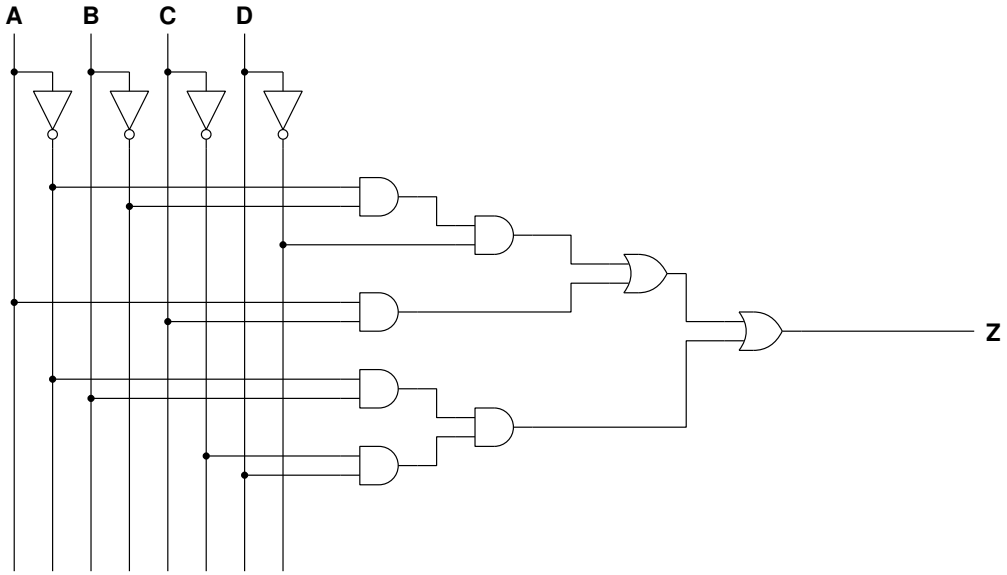
$$Z = \overline{B} \cdot C + A \cdot B \cdot C + \overline{A} \cdot B \cdot \overline{C} \cdot D$$

(c) (2 points) Derive an optimized correct Boolean equation for the same truth table. (*Hint: use a Karnaugh map*)

Solution:

$$Z = \overline{A} \cdot \overline{B} \cdot \overline{D} + A \cdot C + \overline{A} \cdot B \cdot \overline{C} \cdot D$$

(d) (4 points) Draw a gate-level schematic that realizes the function Z using **only** 2-input AND, OR gates. Assume that you have all the inputs (A, B, C, D) and their complements $(\overline{A}, \overline{B}, \overline{C}, \overline{D})$ available.



(e) (2 points) Assume that all the gates (AND, OR, NOT) in the previous diagram have a propagation delay of 100 ps and a contamination delay of 50 ps. What is the delay of the longest (*critical*) path and the *shortest* path of this circuit?

Solution: In the solution above, the *critical* path goes through one inverter, 2 AND gates, and 2 OR gates and is $(5 \times t_{pd} ==)$ 500 ps. The *short* path goes through one AND gate and two OR gates and equals to $(3timest_{cd} ==)$150 ps.
Note: Depending on how the circuit is drawn the numbers could change slightly.