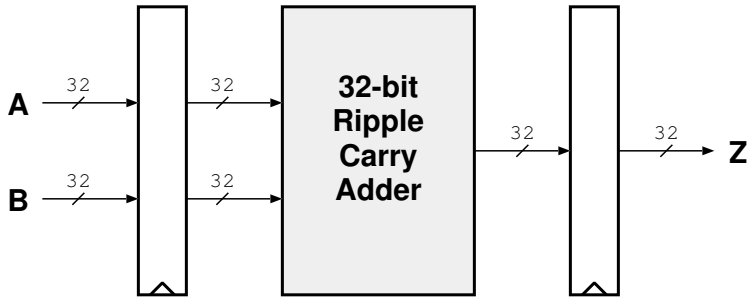
5. In this section, you will compare three structures to add 32-bit binary numbers in terms of Latency, Throughput, Area and Maximum Operating Frequency. Assume the following performance numbers for the components in the question. *Note that the registers are considered ideal for timing: no propagation delay and no setup delay*

Description	**Delay** [ns]	**Area** [µm^2]
32-bit Ripple Carry Adder	4.0	4'000
16-bit Ripple Carry Adder	2.0	2'000
32-bit Carry Lookahead Adder	2.5	6'000
64-bit register	0.0	670
49-bit register	0.0	500
32-bit register	0.0	330

(a) (4 points) Consider the following 32-bit ripple carry adder pipeline stage and answer the following questions:



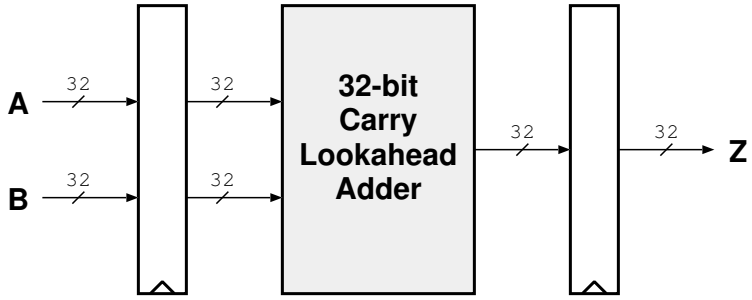
- What is the area occupied by the entire pipeline?
- How long does it take to compute one addition?
- What is the maximum operating frequency (in GHz) of this pipeline?
- How many additions can be completed in 1000 ns?

Solution:

$$
\begin{aligned}
Area &= A_{FF,64} + A_{RCA,32} + A_{FF,32} \\
&= 670 + 4000 + 330 \\
&= 5000 \\
Latency &= 4\,ns \\
MaxFrequency &= 1/4\,ns \\
&= 0.250\,GHz \\
Throughput &= 1000/4\,ns \\
&= 250\ additions\ per\ 1000\,ns
\end{aligned}
$$

Hint: $\frac{1}{1\,ns} = 1\,GHz$*, a clock with 1 GHz has a period of 1 ns.*

(b) (2 points) Consider the following 32-bit carry lookahead pipeline stage and answer the following questions:

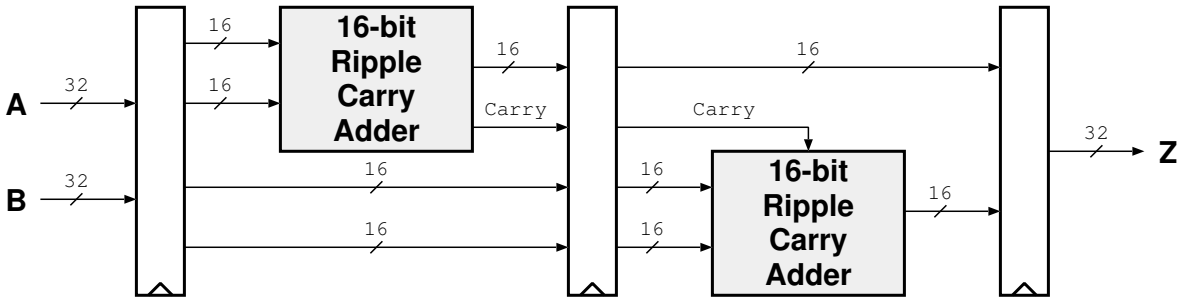


- What is the area occupied by the entire pipeline?
- How long does it take to compute one addition?
- What is the maximum operating frequency (in GHz) of this pipeline?
- How many additions can be completed in 1000 ns?

Solution:

$$
\begin{aligned}
Area &= A_{FF,64} + A_{CLA,32} + A_{FF,32} \\
&= 670 + 6000 + 330 \\
&= 7000 \\
Latency &= 2.5\,ns \\
MaxFrequency &= 1/2.5\,ns \\
&= 0.400\,GHz \\
Throughput &= 1000/2.5\,ns \\
&= 400\ additions\ per\ 1000\,ns
\end{aligned}
$$

(c) (2 points) Consider the following 32-bit adder with a 2 stage pipeline built out of two 16-bit ripple carry adders and answer the following questions:



- What is the area occupied by the entire pipeline?
- How long does it take to compute one addition?
- What is the maximum operating frequency (in GHz) of this pipeline?
- How many additions can be completed in 1000 ns?

Solution:

$$
\begin{aligned}
Area = & \quad A_{FF,64} + A_{RCA,16} + A_{FF,49} + A_{RCA,16} + A_{FF,32} \\
= & \quad 670 + 2000 + 500 + 2000 + 330 \\
= & \quad 5500 \\
Latency = & \quad 4\,ns \\
MaxFrequency = & \quad 1/2\,ns \\
= & \quad 0.500\,GHz \\
Throughput = & \quad 1000/2\,ns \\
= & \quad 500\ additions\ per\ 1000\,ns
\end{aligned}
$$

(d) (4 points) The *Latency* is the time it takes to calculate one addition, whereas the *Throughput* is the number of additions that can be calculated per unit time. It is obvious that the throughput will increase if you can reduce the latency. Is it possible to increase the throughput, even if you cannot reduce the latency? Briefly explain.

Solution: Yes. One solution is to introduce pipelining it is possible to improve the throughput as seen in the section c) of this question. Pipelining does not reduce latency, the computation of one data item still takes the same amount of time, however, the operation is broken down into smaller pieces, and as soon as the first part is completed, a new data item can be accepted, this improves the throughput. Another solution is to increase parallelism by, for example, duplicating the hardware.