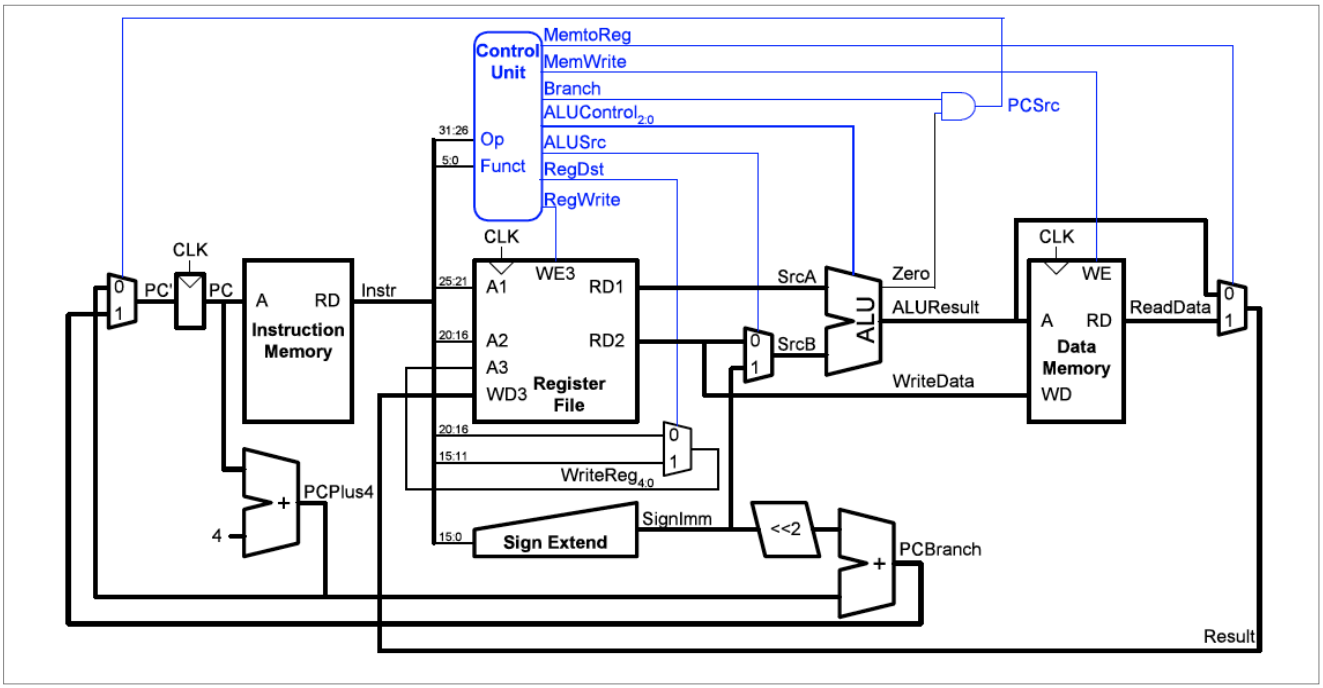
7. The following is a diagram of a single cycle MIPS architecture that is able to execute R-type and I-type instructions.



a) Determine the value of the control signals when this architecture executes a **beq** instruction, and fill in the table below. Note that the ALU can be programmed to perform the following functions: addition, subtraction, and, or. (3 points)

Control Signal	**Value**
RegDst	X
ALUSrc	0
MemWrite	0
MemtoReg	X
RegWrite	0
Branch	1
AluOperation (Add/Sub/And/Or)	Sub

b) Draw the data flow on the block diagram above (2 points)

c) Briefly explain the advantages of a multi-cycle architecture when compared to the single-cycle architecture shown above. (3 points)

In a single-cycle architecture, all instructions are given 1-cycle to execute, therefore the slowest instruction determines the speed of the processor.

In a multi-cycle processor, instructions are broken down into smaller pieces, decreasing the cycle time. Simpler instructions can be executed faster, reducing the average cycle time.

A single cycle processor, needs multiple instances of memories, and adders which may be quite large. A multi-cycle processor can share these resources, using only a single memory and ALU. This reduces the area

d) Which of the following statements about microarchitectures are **TRUE** (Mark all that apply)? (2 points)

In a pipelined architecture, a given instruction is executed faster than in a single-cycle architecture. (FALSE, a given instruction runs even slightly slower, due to the overhead, but the throughput increases)

In a pipelined architecture, control hazards can occur following the branch instruction, since the next instruction address may not be determined in time. (TRUE)

The Clocks per Instruction (CPI) of a micro-architecture is calculated as a weighted average of instructions executed in a given program/benchmark, and therefore is program dependent. (TRUE)

A multi-cycle architecture has less control overhead than a single-cycle architecture. (FALSE, first there are more resources to be shared, and there is overhead for the sequential processing)