5 Cache Coherence [40 points]

We have a system with 4 byte-addressable processors {P0, P1, P2, P3}. Each processor has a private 256-byte, direct-mapped, write-back L1 cache with a block size of 64 bytes. All caches are connected to and actively snoop a global bus, and cache coherence is maintained using the MESI protocol, as we discussed in class. Note that on a write to a cache block in the S state, the block will transition directly to the M state. Accessible memory addresses range from `0x00000` – `0xfffff`.

Each processor executes the following instructions in a *sequentially consistent* manner:

P0	
0	`st r0, 0x1ff40`
-	
-	

P1	
1	`st r0, 0x110c0`
2	`st r1, 0x11080`
3	`ld r2, 0x1ff00`

P2	
4	`ld r0, 0x1ff40`
5	`ld r1, 0x110f0`
-	

P3	
-	
-	
-	

After executing the above 6 memory instructions, the *final* tag store state of each cache is as follows:

Final Tag Store States

Cache for P0		
	Tag	*MESI state*
Set 0	`0x1ff`	`S`
Set 1	`0x1ff`	`S`
Set 2	`0x110`	`I`
Set 3	`0x110`	`I`

Cache for P1		
	Tag	*MESI state*
Set 0	`0x1ff`	`S`
Set 1	`0x1ff`	`I`
Set 2	`0x110`	`M`
Set 3	`0x110`	`M`

Cache for P2		
	Tag	*MESI state*
Set 0	`0x10f`	`I`
Set 1	`0x1ff`	`S`
Set 2	`0x10f`	`M`
Set 3	`0x110`	`I`

Cache for P3		
	Tag	*MESI state*
Set 0	`0x133`	`E`
Set 1	`0x000`	`I`
Set 2	`0x000`	`I`
Set 3	`0x10f`	`I`

(a) [30 points] Fill in the following tables with the *initial* tag store states (i.e., *Tag* and *MESI* state) before having executed the six memory instructions shown above. Answer X if a tag value is unknown, and for the *MESI* states, write in *all possible values* (i.e., `M`, `E`, `S`, and/or `I`).

Initial Tag Store States

Cache for P0		
	Tag	*MESI state*
Set 0	`0x1ff`	`M, E, S`
Set 1	`X`	`M, E, S, I`
Set 2	`0x110`	`M, E, S, I`
Set 3	`0x110`	`M, E, S, I`

Cache for P1		
	Tag	*MESI state*
Set 0	`X`	`M, E, S, I`
Set 1	`0x1ff`	`M, E, S, I`
Set 2	`X`	`M, E, S, I`
Set 3	`X`	`M, E, S, I`

Cache for P2		
	Tag	*MESI state*
Set 0	`0x10f`	`I`
Set 1	`X`	`M, E, S, I`
Set 2	`0x10f`	`M`
Set 3	`X`	`M, E, S, I`

Cache for P3		
	Tag	*MESI state*
Set 0	`0x133`	`E`
Set 1	`0x000`	`I`
Set 2	`0x000`	`I`
Set 3	`0x10f`	`I`

(b) [10 points] In what order did the memory operations enter the coherence bus?

time →					
0	4	5	1	2	3