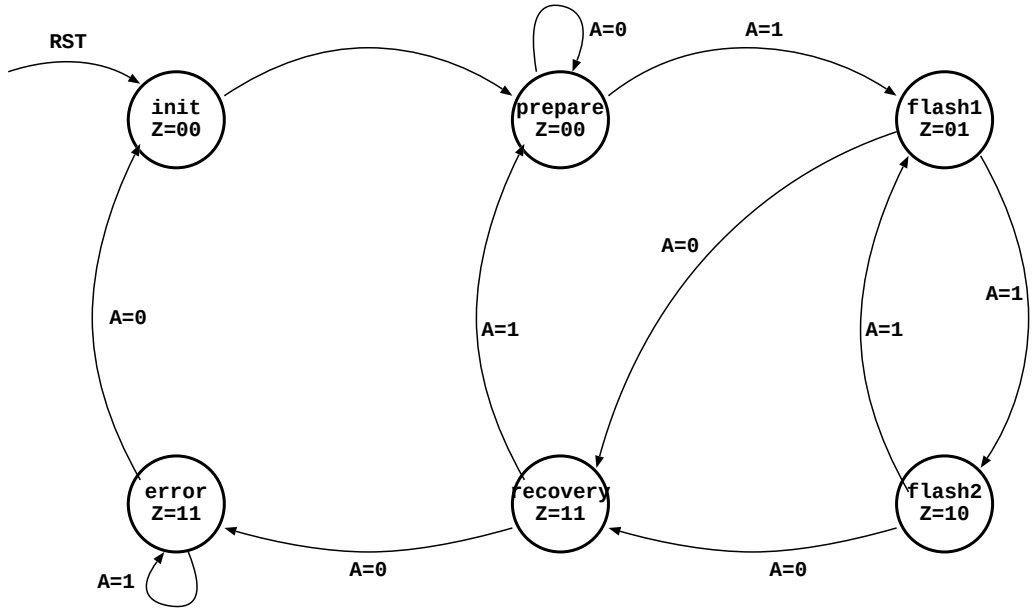
Draw a proper state transition diagram that corresponds to the FSM described in this Verilog code.

(25 points should be given only if the diagram is absolutely correct)



(c) [5 points] Is the FSM described by the previous Verilog code a Moore or a Mealy FSM? Why?

Moore, the output Z only depends on the state ($presentState$) and not on the input (A).

3 Verilog

Please answer the following four questions about Verilog.

(a) [10 points] Does the following code result in a sequential circuit or a combinational circuit? Please explain why.

```
module one (input clk, input a, input b, output reg [1:0] q);
 always @ (*)
   if (b)
      q <= 2'b01;
   else if (a)
      q <= 2'b10;
endmodule
```

Answer and concise explanation:

This code results in a sequential circuit because a latch is required to store the old value of `q` if both conditions are **not** satisfied.

(b) [10 points] What is the value of the output `z` if the input `c` is `10101111` and `d` is `01010101`?

```
module two (input [7:0] c, input [7:0] d, output reg [7:0] z);
always @ (c,d)
  begin
    z = 8'b00000001;
    z[7:5] = c[5:3];
    z[4] = d[7];
    z[3] = d[7];
  end
endmodule
```

Please answer below. Show your work.

10100001. Last assignment of a bit overrides all previous assignments.