(c) [10 points] Is the following code correct? If not, please explain the mistake and how to fix it.

```
1  module mux2 ( input [1:0] i, input sel, output z);
2    assign z= (sel) ? i[1]:i[0];
3  endmodule
4
5  module three ( input [3:0] data, input sel1, input sel2, output z);
6
7    wire m;
8
9    mux2 i0 (.i(data[1:0]), .sel(sel1), .z(m[0]) );
10   mux2 i1 (.i(data[3:2]), .sel(sel1), .z(m[1]) );
11   mux2 i2 (.i(m), .sel(sel2), .z(z) );
12
13 endmodule
```

Answer and concise explanation:

No. The wire m is declared to be only 1-bit wide but it needs to be 2-bit wide.

(d) [10 points] Does the following code correctly implement a multiplexer?

```
1  module four (input sel, input [1:0] data, output reg z);
2    always@(sel)
3    begin
4      if(sel == 1'b0)
5        z = data[0];
6      else
7        z = data[1];
8    end
9  endmodule
```

Answer and concise explanation:

No. The input `data` is not in the sensitivity list and therefore changes to the input would not be reflected in the output `z`.

4 Boolean Logic and Truth Tables

You will be asked to derive the Boolean Equations for two 4-input logic functions, X and Y. Please use the Truth Table below for the following three questions.

Inputs				**Outputs**	
A_3	A_2	A_1	A_0	X	Y
0	0	0	0	1	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	1	0
0	1	0	1	1	1
0	1	1	0	1	0
0	1	1	1	0	0
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	1	1
1	0	1	1	1	0
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	1	0	0