Q1:
What factors control the number of pipeline stages?

A. The combinational logic function
B. The operating frequency
C. The critical path propagation delay
D. B&C

Q2:
When should we pipeline an adder tree?

A. When the critical path delay is larger than the target operating frequency
B. When the adder tree is more than 5 layers
C. When we want to optimize the area
D. When we want to optimize the latency

Q3:
When should we avoid having an adder tree?

A. When the registers togeling power is less than the togeling power of the combinational path of the tree
B. When we have wide vector operation
C. When we're working with signed numbers
D. All of the above

Q4:
For better power and delay, which one of the following adder tree architectures should be used?

A. Carry-save Adder tree (Wallace reduction tree)
B. Ripple Carry Adder tree
C. Carry-look ahead adder tree
D. All of the above

Q5:
Which adder from the following is the most power efficient?

A. RCA(Ripple Carry Adder)
B. CLA(CArry Look Ahead Adder)
C. MCC (Manchester Carry Chain Adder)
D. All of the above

Q6:
For signed adder trees, which of the following would be more power efficient?

A. Signed adders (separate sign, magnitude)
B. 2's complement adders
C. They're the same
D. RCA adders

Q7: If we want to perform signed accumulation, which of the following methods would be more efficient?

A. Separate 2 unsigned accumulators and adding their signed values at the end
B. Single 2s complement accumulator
C. Single sign, magnitude accumulator
D. Any of the above