3. Cache Coherence [40 points]

We have a system with four byte-addressable processors (P0, P1, P2, and P3). Each processor has a private 256-byte, direct-mapped, write-back L1 cache with a block size of 64 bytes. Coherence is maintained using the MESI protocol we discussed in class. The protocol transitions from **Shared (S)** to **Modified (M)** on a processor write. Accessible memory addresses range from 0x10000000 to 0x1FFFFFFF.

```
Executed Memory instructions:
ld R1, 0x110000c0 \\ A memory instruction from P1
st R2, 0x11000080 \\ A memory instruction from P1
st R3, 0x1FFFFF40 \\ A memory instruction from P0
ld R4, 0x1FFFFF00 \\ A memory instruction from P1
ld R5, 0x1FFFFF40 \\ A memory instruction from P2
```

After executing the above sequence of 5 memory instructions, we find the *final tag* store state of the four caches to be as follows:

Final State

Cache 0		
	Tag	*MESI State*
Set 0	0x1FFFFF	S
Set 1	0x1FFFFF	S
Set 2	0x110000	I
Set 3	0x110000	I

Cache 1		
	Tag	*MESI State*
Set 0	0x1FFFFF	S
Set 1	0x1FFFFF	I
Set 2	0x110000	M
Set 3	0x110000	E

Cache 2		
	Tag	*MESI State*
Set 0	0x10FFFF	I
Set 1	0x1FFFFF	S
Set 2	0x10FFFF	M
Set 3	0x10FFFF	M

Cache 3		
	Tag	*MESI State*
Set 0	0x133333	E
Set 1	0x000000	I
Set 2	0x000000	I
Set 3	0x10FFFF	I

Fill in the following table with the *initial* tag store states (i.e., *Tag* and *MESI state*) before executing the five memory instructions shown above. Answer X if the tag value of the address is unknown. For the MESI states, put in all the possible values (i.e., M, E, S, and I).

Initial State

Cache 0		
	Tag	*MESI State*
Set 0	0x1FFFFF	M,E,S
Set 1	X	M,E,S,I
Set 2	0x110000	M,E,S,I
Set 3	0x110000	I

Cache 1		
	Tag	*MESI State*
Set 0	X	M,E,S,I
Set 1	0x1FFFFF	M,E,S,I
Set 2	X	M,E,S,I
Set 3	X	M,E,S,I

Cache 2		
	Tag	*MESI State*
Set 0	0x10FFFF	I
Set 1	X	M,E,S,I
Set 2	0x10FFFF	M
Set 3	0x10FFFF	M

Cache 3		
	Tag	*MESI State*
Set 0	0x133333	E
Set 1	0x000000	I
Set 2	0x000000	I
Set 3	0x10FFFF	I

Scratchpad for the cache coherence problem