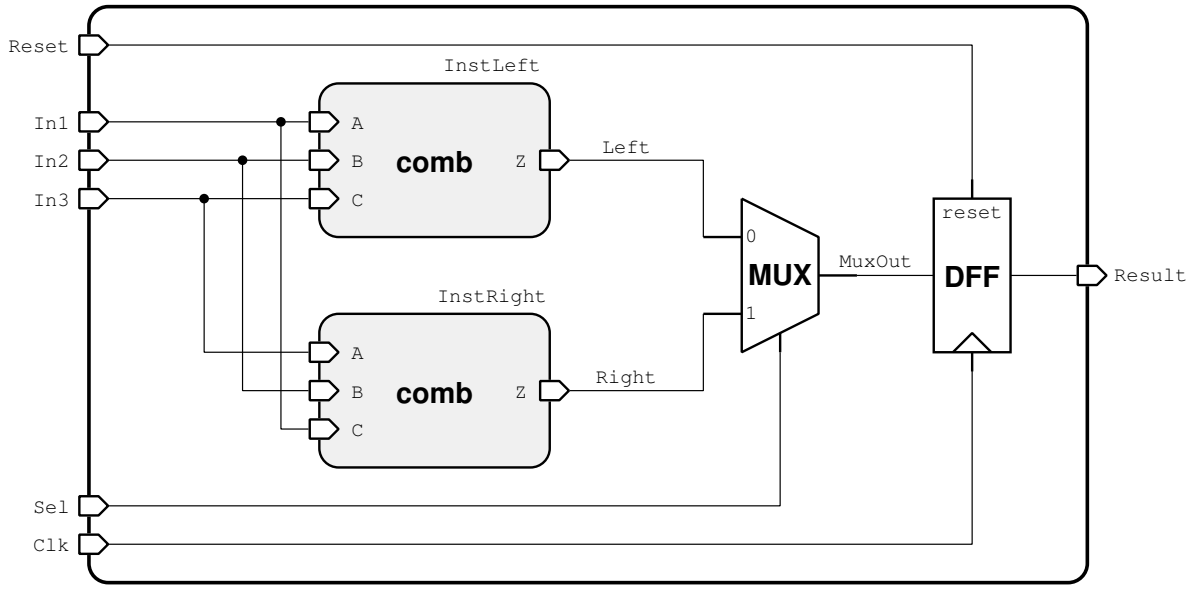
3. (15 points) In this question you are required to write the Verilog code that implements the following block diagram.



The block called *Controller* has six 1-bit inputs and a single 1-bit output (*Result*). It contains two instances of a combinational block called (*comb*). The following is the declaration part of this module:

```
1 module comb ( input A , input B , input C, output Z);
2   // definition of the combinational circuit comb
3
4 endmodule
```

Notes:

- The flip-flop and the multiplexer will not be instantiated, you will have to write the corresponding Verilog code.
- The flip-flop uses an asynchronous reset, the output is zero when reset is one.
- Note that Verilog is case sensitive.
- Write legibly.

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Solution:

```
module Controller (
  input Clk,
  input Reset,
  input In1,In2,In3,
  input Sel,
  output reg Result);

// Define internal signals
  wire Left, Right, MuxOut;

// instantiate the module comb two times
  comb InstLeft  (.A(In1), .B(In2), .C(In3), .Z(Left) );
  comb InstRight (.A(In3), .B(In2), .C(In1), .Z(Right) );

// The multiplexer
  assign MuxOut = (Sel) ? Right: Left;

// The FF
  always @ (posedge Clk, posedge Reset)
     if (Reset) Result <= 1'b0;
     else       Result <= MuxOut;

endmodule
```