2. A circuit has four inputs (A, B, C, D) and two outputs (E, T).

   - Output E should be '1' if there are **equal number** of '1's and '0's in the input.
   - Output T should be '1' if **two or more** of the inputs are '1'

   (a) (2 points) Complete the following truth table

Inputs				**Outputs**	
A	B	C	D	E	T
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	1	1
0	1	1	0	1	1
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	0	1

(b) (3 points) Write a Boolean equation for E using either SOP or POS representation. (*Hint: use a Karnaugh map*)

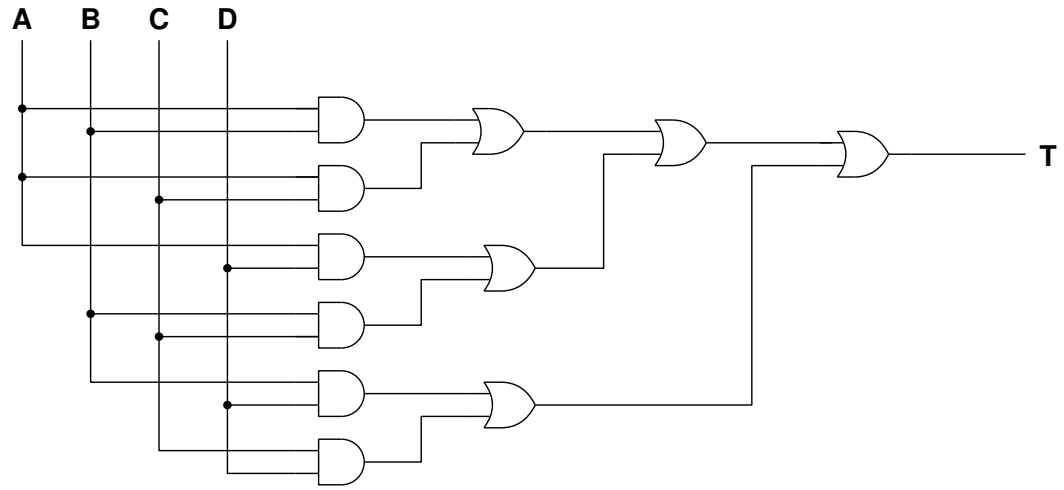
Solution: One possible solution is:
$E = (\overline{A} \cdot \overline{B} \cdot C \cdot D) + (\overline{A} \cdot B \cdot \overline{C} \cdot D) + (\overline{A} \cdot B \cdot C \cdot \overline{D}) + (A \cdot \overline{B} \cdot \overline{C} \cdot D) + (A \cdot B \cdot \overline{C} \cdot \overline{D}) + (A \cdot \overline{B} \cdot C \cdot \overline{D})$

(c) (3 points) Write a Boolean equation for T using either SOP or POS representation. (*Hint: use a Karnaugh map*)

Solution: One possible solution is:
$T = (A \cdot B) + (A \cdot C) + (A \cdot D) + (B \cdot C) + (B \cdot D) + (C\dot{D})$

(d) (3 points) Draw a gate level diagram implementing T using **only two-input** AND, OR gates and/or inverters.

Solution:



(e) (2 points) Assuming that the propagation of all 2-input gates and inverters is 100 ps and the contamination delay is 50 ps, what is the critical path (longest path), and the shortest path of the circuit you have drawn in Question 2d?

Solution:

For the solution given in Question 2d, the critical path goes through 1 AND gate and 3 OR gates = 4 propagation delays = 400ps.

The shortest path goes through one AND gate and two OR gates = 3 contamination delays = 150ps.

(f) (5 points) Note that the function T contains E (meaning T is '1' for every input that results in a '1' for E). Assume that you already have a small circuit that implements E, design a simpler Boolean function that implements T by using the output of E and draw the gate level schematic once again only using E, 2-input AND/OR gates and inverters.

Solution: One of the simpler solutions is: $T = (A \cdot D) + (B \cdot C) + E$