3 Finite State Machines [40 points]

3.1 Designing an FSM [20 points]

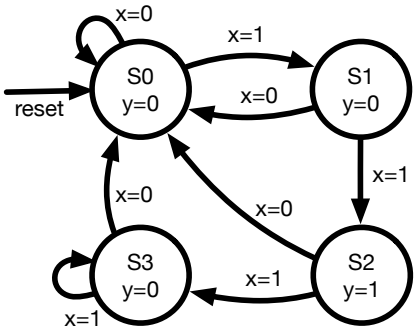
Draw a Moore finite state machine for a digital circuit that has a one-bit input x and a one-bit output y. The circuit detects the bit pattern 0-1-1 on the input x. The output bit is set (i.e., $y = 1$) during clock cycle t only if the three following values of x happen.

- $x = 0$ at clock cycle $t - 3$,
- $x = 1$ at clock cycle $t - 2$,
- $x = 1$ at clock cycle $t - 1$

Your state machine should use as few states as possible. Assume that the initial bit value of x is zero. Please clearly and comprehensively define each state and state transition. Note that you can lose points for ambiguity in your state machine.

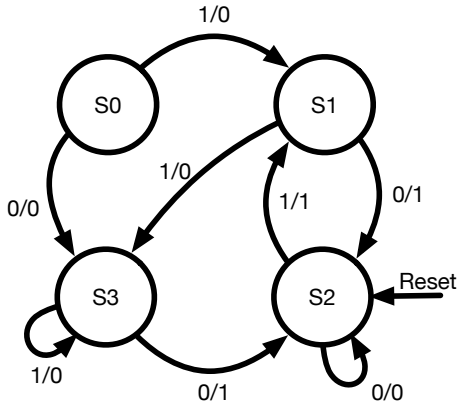
We need four states to keep track of the recent input values.

- S0: Input was zero in the last clock cycle (the initial state). The output should be zero.
- S1: Input was one in the last clock cycle, but it was zero before. The output should be zero.
- S2: Input was one in the last two clock cycles, but it was zero before. The output should be one.
- S3: Input was one in the last three clock cycles. The output should be zero.



3.2 Simplifying an FSM [20 points]

You are given the state machine of a *one-bit input / one-bit output* digital circuit design. Answer the following questions for the given state diagram.



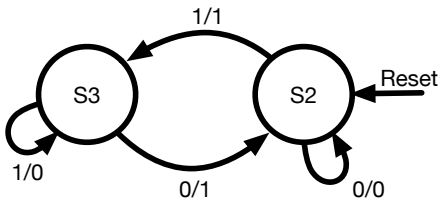
(a) [5 points] Is this a Mealy or a Moore machine? Explain why.

This is a Mealy machine because the output depends on both the state and the input.

(b) [10 points] Is it possible to simplify this state diagram to reduce the number of states? If so, simplify it to the minimum number of states. Explain each step of your simplification. Draw the simplified state diagram.

Yes, it is possible.

- There is no way the state goes to S0, so it is a non-used state. [2 points]
- S1 and S3 exhibit identical behavior, so they are redundant states. [3 points]
- We can simplify the state diagram as following.



(c) [5 points] What does this state machine do? For what purpose can it be useful? Explain.

This state machine outputs 1 when the input signal changes zero-to-one or one-to-zero. It outputs zero otherwise. (This is an edge detector. A student does not need to specify the name "edge detector" for getting full grade.)