

## 1 Potpourri [30 points]

### 1.1 Microarchitecture or ISA? [10 points]

Based on your knowledge of a basic MIPS design and the computer architecture techniques you learned throughout this course, put an “X” in the box corresponding to whether each of the following design characteristics is *better* classified as “microarchitecture” or “ISA”:

Characteristic	Microarchitecture	ISA
General purpose register \$29 is the stack pointer		X
Maximum bandwidth between the L2 and the L3 cache	X	
Maximum reservation station capacity	X	
Hardware floating point exception support		X
Instruction issue width	X	
Vector instruction support		X
Memory-mapped I/O Port Address		X
Arithmetic and Logic Unit (ALU) critical path	X	
CPU endianness		X
Virtual page size		X



### 1.3 Performance Evaluation [10 points]

The execution time of a given benchmark is 100 *ms* on a 500 *MHz* processor. An ETH alumnus, designing the next generation of the processor, notices that a new implementation enables the processor to run at 750 *MHz*. However, the modifications increase the CPI by 20% for the same benchmark.

- (a) [4 points] What is the execution time expressed in terms of the number of cycles taken for the **old** generation of the processor (i.e., before the modifications)?

Assuming that the IPC is 2, what is the number of instructions in the benchmark?

**Answer:** Execution time is **50 Million cycles**. The benchmark has **100 Million instructions**.

**Explanation:**

Clock frequency is 500 *MHz*. Then each cycle takes  $1/(500 \times 10^{-6}) = 2ns$ .

Total execution time in cycles is  $100ms/2ns = 50\text{Million}$  cycles.

2 instructions per cycle. Then, the total number of instructions:  $2 \times 50M = 100M$

- (b) [3 points] What is the execution time of the benchmark in *milliseconds* for the **new** generation of the processor?

**Answer: 80 ms.**

**Explanation:**

$Execution\ Time = [Number\ of\ Instructions] \times [CPI] \times [Frequency^{-1}]$

Let's say that the CPI of baseline is  $c$ , and number of instructions is  $i$ .

Then the execution time of baseline:

$(c \times i)/(500 \times 10^6) = 100 \times 10^{-3}\ seconds \Rightarrow (c \times i) = 5 \times 10^7$

The execution time after modifications:  $((1.2 \times c) \times i)/(750 \times 10^6)$

$T = ((1.2 \times (c \times i))/(750 \times 10^6)\ seconds.$

$T = ((1.2 \times (5 \times 10^7))/(750 \times 10^6)\ seconds.$

$T = 8 \times 10^{-2} = 80ms.$

- (c) [3 points] What is the speedup or slowdown of the new generation processor *over* the old generation?

**Answer: 25% speedup**

**Explanation:**

$Speedup = (OldExecutionTime / [NewExecutionTime]) - 1$

$Speedup = 100/80 - 1$

$Speedup = 0.25$

Then the modification introduces 25% speedup.