2. For this question, use the following truth table for a 4-input logic function called Z.

Input				**Output**
A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	X
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	X
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	X
1	1	1	1	1

(a) (1 point) What is the meaning of X in this truth table?

Solution: The output value is not important for the functionality of the circuit. It can be taken as '0' or '1' to simplify the equations

(b) (6 points) A friend of yours has determined the following Boolean equation for Z:

$$Z = (\overline{B} + D) \cdot (A + B + C) \cdot (A + B + \overline{C}) \cdot (\overline{A} + B + \overline{C}) \cdot (\overline{A} + \overline{C} + D)$$

But he is not sure if this is correct. Verify whether or not the given equation matches the truth table given above. If not, please explain how the equation can be corrected.

Solution:
The equation is not correct. You can see this if you mark the min-terms on the truth table for each equation. The following are the problems:

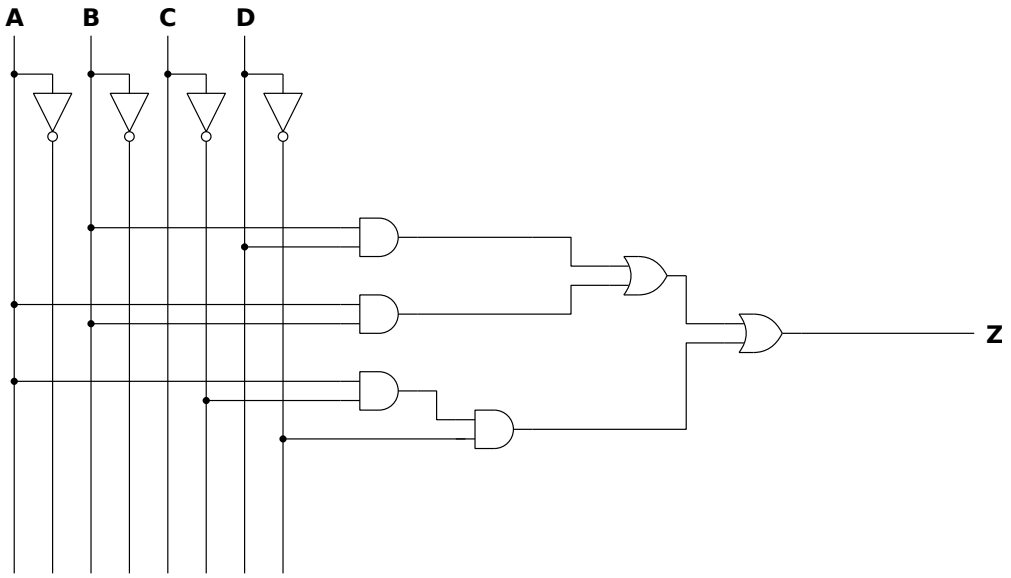
- $(\overline{B} + D)$ is wrong. Should have been $(B + \overline{D})$
- $(A + B + C)$ and $(A + B + \overline{C})$ can be merged to $(A + B)$
- min-term $(\overline{A} + B + C + \overline{D})$ is missing
- $(\overline{A} + \overline{C} + D)$ is redundant, especially if the X is taken as '1'

The X values have not been optimally used, this results in a more complex equation, if X values are chosen carefully a SOP form would probably be better, in addition there are redundant terms, the equation is not simplified

(c) (5 points) Derive your own *optimized* Boolean equation corresponding to the same truth table using *sums-of-products* form. Try to take advantage of the 'X' values to minimize the equation as much as possible. (*Hint: use a Karnaugh map*)

Solution: If you take $\overline{A}B\overline{C}\overline{D}$ as 0 and all other X's as '1', you can derive:
$Z = (B \cdot D) + (A \cdot \overline{C} \cdot \overline{D})$

(d) (4 points) Draw a gate-level schematic that realizes the function Z using **only** 2-input AND, OR gates. Assume that you have all variables (A, B, C, D) available as input. Their complements $(\overline{A}, \overline{B}, \overline{C}, \overline{D})$ are already drawn for you.



(e) (2 points) Assume that all the gates (AND, OR, NOT) in the previous diagram have a propagation delay of 100 ps and a contamination delay of 50 ps. What is the delay of the longest (*critical*) path and the *shortest* path of this circuit?

Solution: In the solution above, the *critical* path goes through 1 inverter, 2 AND gates, and 1 OR gate and is $(4 \times t_{pd} ==)$ 400 ps. The *short* path goes through one AND gate and two OR gates and equals to $(2 \times t_{cd} ==)$100 ps.

Note: Depending on how the circuit is drawn the numbers could change slightly, it is possible that the longest path is 5 gates.