12 BONUS: Prefetching [50 points]

An ETH student writes two programs (A and B) and runs them on two different toy machines (M1 and M2) to determine the type of the prefetcher used in each of these machines. She observes programs A and B to generate the following memory access patterns (note that these are *cacheblock addresses*, not byte addresses).

Program A: 27 memory accesses

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a, a + 1, a + 2, a + 3, a + 4, a + 8, a + 16, a + 32, a + 64,
a, a + 1, a + 2, a + 3, a + 4, a + 8, a + 16, a + 32, a + 64,
a, a + 1, a + 2, a + 3, a + 4, a + 8, a + 16, a + 32, a + 64
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Program B: 501 memory accesses

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b, b + 2, b + 4, ...., b + 998, b + 1000
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The student measures the coverage (i.e., the fraction of program's memory accesses correctly predicted by the prefetcher) and accuracy (i.e., the fraction of sent prefetch requests that are used by the program) of the prefetching mechanism in each of the machines. The following table shows her measurement results:

	Machine M1		**Machine M2**	
	Coverage	Accuracy	Coverage	Accuracy
Program A	6/27	6/27	1/3	9/26
Program B	499/501	499/501	499/501	499/500

The student knows the following information about the machines:

- There are three possible choices for the prefetching mechanism:
  1. Stride prefetcher
  2. 1st-next-block prefetcher with degree 1: Prefetches cacheline $A+1$ after seeing access to block A
  3. 4th-next-block prefetcher with degree 1: Prefetches cacheline $A+4$ after seeing access to block A
- Each prefetcher has large enough resources to detect and store access patterns.
- Each prefetcher starts with an empty table.
- Each prefetcher sends only one prefetch request for each program access.
- Each memory access is separated long enough in time so that all prefetch requests sent can complete before the next access occurs.
- No prefetcher employs any confidence mechanism (e.g., the stride prefetcher will send a prefetch request to address $A+4$ by only seeing two consecutive memory accesses to addresses A and $A+2$).

Determine what type of prefetching mechanism is used by M1 and M2. Show your work. Answers without explanation will not be rewarded.

Machine M1: 4th-next-line prefetcher

Machine M2: Stride prefetcher

Space for explanation:

M1: 4th-next-line prefetcher
M2: Stride prefetcher

Explanation

We calculate the accuracy and coverage for all three types of prefetchers, and then we can answer what prefetcher each machine is using. Underlined and red-marked cacheline addresses are correctly and incorrectly prefetched, respectively.

Each prefetcher works in the following way while running Application A:

Stride: Coverage: 1/3, Accuracy: 9/26
a, a + 1, $\underline{\text{a + 2}}$, $\underline{\text{a + 3}}$, $\underline{\text{a + 4}}$, a + 8, a + 16, a + 32, a + 64, (incorrect: a + 5, a + 12, a + 24, a + 48, a + 96)
a, a + 1, $\underline{\text{a + 2}}$, $\underline{\text{a + 3}}$, $\underline{\text{a + 4}}$, a + 8, a + 16, a + 32, a + 64, (incorrect: a - 64, a + 5, a + 12, a + 24, a + 48, a + 96)
a, a + 1, $\underline{\text{a + 2}}$, $\underline{\text{a + 3}}$, $\underline{\text{a + 4}}$, a + 8, a + 16, a + 32, a + 64 (incorrect: a - 64, a + 5, a + 12, a + 24, a + 48, a + 96)

1st-next-line: Coverage: 4/9, Accuracy: 4/9
a, $\underline{\text{a + 1}}$, $\underline{\text{a + 2}}$, $\underline{\text{a + 3}}$, $\underline{\text{a + 4}}$, a + 8, a + 16, a + 32, a + 64, (incorrect: a + 5, a + 9, a + 17, a + 33, a + 65)
a, $\underline{\text{a + 1}}$, $\underline{\text{a + 2}}$, $\underline{\text{a + 3}}$, $\underline{\text{a + 4}}$, a + 8, a + 16, a + 32, a + 64, (incorrect: a + 5, a + 9, a + 17, a + 33, a + 65)
a, $\underline{\text{a + 1}}$, $\underline{\text{a + 2}}$, $\underline{\text{a + 3}}$, $\underline{\text{a + 4}}$, a + 8, a + 16, a + 32, a + 64, (incorrect: a + 5, a + 9, a + 17, a + 33, a + 65)

4th-next-line: Coverage: 6/27, Accuracy: 6/27
a, a + 1, a + 2, a + 3, $\underline{\text{a + 4}}$, $\underline{\text{a + 8}}$, a + 16, a + 32, a + 64, (incorrect: a + 5, a + 6, a + 7, a + 12, a + 20, a + 36, a + 68)
a, a + 1, a + 2, a + 3, $\underline{\text{a + 4}}$, $\underline{\text{a + 8}}$, a + 16, a + 32, a + 64, (incorrect: a + 5, a + 6, a + 7, a + 12, a + 20, a + 36, a + 68)
a, a + 1, a + 2, a + 3, $\underline{\text{a + 4}}$, $\underline{\text{a + 8}}$, a + 16, a + 32, a + 64 (incorrect: a + 5, a + 6, a + 7, a + 12, a + 20, a + 36, a + 68)

The three prefetechers work in the following way while running Application B:

Stride: Coverage: 499/501, Accuracy: 499/500
b, b + 2, $\underline{\text{b + 4}}$, $\underline{\text{b + 6}}$, $\underline{\text{b + 8}}$, $\underline{\text{b + 10}}$, ..., $\underline{\text{b + 998}}$, $\underline{\text{b + 1000}}$ (incorrect: b + 1002)

1st-next-line: Coverage: 0, Accuracy: 0
b, b + 2, b + 4, b + 6, b + 8, b + 10, ... , b + 998, b + 1000 (incorrect: b + 1, b + 3, ..., b + 999, b + 1001)

4th-next-line: Coverage: 499/501, Accuracy: 499/501
b, b + 2, $\underline{\text{b + 4}}$, $\underline{\text{b + 6}}$, $\underline{\text{b + 8}}$, $\underline{\text{b + 10}}$, ..., $\underline{\text{b + 998}}$, $\underline{\text{b + 1000}}$ (incorrect: b +1002, b + 1004)