

Assume the following instruction mix: 30% ALU, 15% multiply & divide, 20% load, 10% store, 15% branch, and 10% jump.

- a) What is the total delay for each instruction class and the clock cycle for the single-cycle CPU design?

Instruction Class	Instruction Memory	Register Read	ALU	Data Memory	Register Write	Total Delay
Basic ALU	190 ps	150 ps	190 ps		150 ps	680 ps
Mul & Div	190 ps	150 ps	550 ps		150 ps	1040 ps
Load	190 ps	150 ps	190 ps	190 ps	150 ps	870 ps
Store	190 ps	150 ps	190 ps	190 ps		720 ps
Branch	190 ps	150 ps	190 ps			530 ps
Jump	190 ps	150 ps				340 ps

Clock cycle = max delay = 1040 ps.

- b) Assume we fix the clock cycle to 200 ps for a multi-cycle CPU, what is the CPI for each instruction class and the speedup over a fixed-length clock cycle?

Solution:

CPI for Basic ALU = 4 cycles

CPI for Multiply & Divide = 6 cycles

CPI for Load = 5 cycles

CPI for Store = 4 cycles

CPI for Branch = 3 cycles

CPI for Jump = 2 cycles

Average CPI = $0.3 * 4 + 0.15 * 6 + 0.2 * 5 + 0.1 * 4 + 0.15 * 3 + 0.1 * 2 = 4.15$

Speedup of multi-cycle over single-cycle = $(1040 * 1) / (200 * 4.15) = 1.253$

Q3. (10 pts) Consider the following MIPS code sequence:

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a: add $t0, $s0, $s1
b: sub $t1, $s2, $t0
c: xor $t0, $s0, $s1
d: or  $t2, $t1, $t0

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- a) (5 pts) Identify all the RAW dependencies between pairs of instructions.

Instruction b is dependent on instruction a (\$t0)

Instruction d is dependent on instruction b (\$t1)

Instruction d is dependent on instruction c (\$t0)

- b) (3 pts) Identify all the WAR dependencies between pairs of instructions
Instruction c is dependent on instruction b (\$t0)
- c) (2 pts) Identify all the WAW dependencies between pairs of instructions
Instruction c is dependent on instruction a (\$t0)