2. The following Verilog code defines a combinational circuit. We are interested in finding out the timing properties of this circuit.

```
1  module gandalf ( input [3:0] a, input e, output z);
2
3    wire b,c,d;
4    reg f;
5
6    assign d = ~(a[3] & (a[2] | b));
7
8    always @ (*)
9      f <= a[3] & b;
10
11   assign z = (~e) ? d : f;
12   assign b = a[0] & a[1];
13
14 endmodule
```

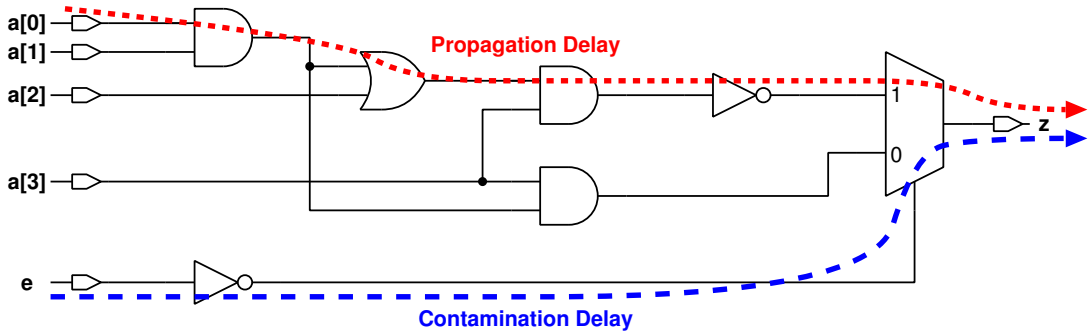
The circuit is implemented using only the following basic logic building blocks: 2-input AND, 2-input OR, 2:1 Multiplexer, Inverter. The delay from any input to the output for each basic building block is given in the table below:

Description	**Delay** [ps]
2-input AND gate	100
2-input OR gate	120
Inverter	50
2:1 Multiplexer	180

Continue to the next page.

(a) (4 points) Draw a gate-level circuit diagram of the circuit using **only** the following basic logic gates: 2-input AND, 2-input OR, 2:1 Multiplexer, Inverter. *Note: there is no need for optimizations.*

Solution:



(b) (3 points) Determine the propagation delay of the circuit. Draw it on your schematic, and calculate the propagation delay using the delay values from the table.

Solution:

$$\begin{aligned} t_{pd} &= t_{pd,AND} + t_{pd,OR} + t_{pd,AND} + t_{pd,INV} + t_{pd,MUX} \\ &= 100\,ps + 120\,ps + 100\,ps + 50\,ps + 180\,ps \\ &= 550\,ps \end{aligned}$$

(c) (3 points) Determine the contamination delay of the circuit. Draw it on your schematic, and calculate the contamination delay using the delay values from the table.

Solution:

$$\begin{aligned} t_{pd} &= t_{pd,INV} + t_{pd,MUX} \\ &= 50\,ps + 180\,ps \\ &= 230\,ps \end{aligned}$$