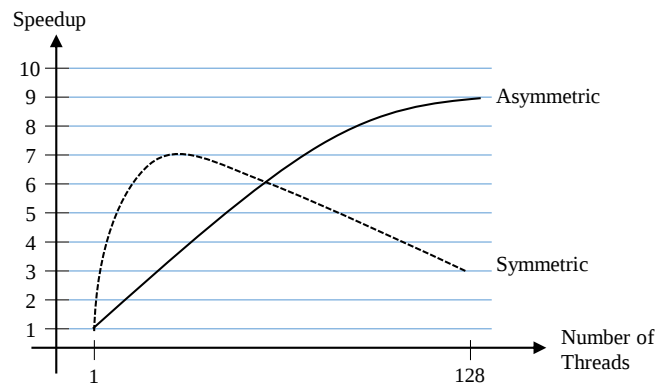# 1. Potpourri [30 points]

(a) What is the advantage of using a **virtually-indexed physically-tagged (VIPT)** L1 cache? Be precise and concise.

> To mitigate the TLB lookup latency by overlapping it with the accesses to the cache.

(b) Typically, for a realistic workload, the parallel fraction of a program is *not* perfectly parallelizable. What are the three fundamental reasons why?

1. Synchronization

2. Load imbalance

3. Resource contention

(c) The figure below shows the speedup curve for a workload on two systems: symmetric multicore and asymmetric multicore. Assume an area budget of 32 small cores.

What is the performance improvement of the asymmetric multicore over the symmetric one? Show your work.

> $9/7 = 1.29$ You need to compare the two systems at their best number of threads to make a fair comparison.

(d) In a MESI cache coherence protocol that transitions from **Shared** to **Exclusive** state on a *processor write*, what does the cache controller need to perform to correctly complete the transition? Be precise.

1. Invaldiate other cache lines. 2. Write back dirty data to memory.