4 ISA vs. Microarchitecture [20 points]

A new CPU has two comprehensive user manuals available for purchase as shown in Table 1.

Manual Title	Cost	Description
`the_isa.pdf`	CHF 1 million	describes the ISA in detail
`the_microarchitecture.pdf`	CHF 10 million	describes the microarchitecture in detail

Table 1: Manual Costs

Unfortunately, the manuals are extremely expensive, and you can only afford one of the two. If both manuals might be useful, you would prefer the cheaper one.

For each of the following questions that you would like to answer, decide which manual is more likely to help. *Note: we will subtract 1 point for each* ***incorrect*** *answer. For an unanswered question, you will get +0 points.*

1. [2 points] The latency of a branch predictor misprediction.

   1. `the_isa.pdf` [2. `the_microarchitecture.pdf`]

2. [2 points] The size of a physical memory page.

   1. `the_isa.pdf` [2. `the_microarchitecture.pdf`]

3. [2 points] The memory-mapped locations of exception vectors.

   [1. `the_isa.pdf`] 2. `the_microarchitecture.pdf`

4. [2 points] The function of each bit in a programmable branch-predictor configuration register.

   [1. `the_isa.pdf`] 2. `the_microarchitecture.pdf`

5. [2 points] The bit-width of the interface between the CPU and the L1 cache.

   1. `the_isa.pdf` [2. `the_microarchitecture.pdf`]

6. [2 points] The number of pipeline stages in the CPU.

   1. `the_isa.pdf` [2. `the_microarchitecture.pdf`]

7. [2 points] The order in which loads and stores are executed by a multi-core CPU.

   [1. `the_isa.pdf`] 2. `the_microarchitecture.pdf`

8. [2 points] The memory addressing modes available for arithmetic operations.

   [1. `the_isa.pdf`] 2. `the_microarchitecture.pdf`

9. [2 points] The program counter width.

   [1. `the_isa.pdf`] 2. `the_microarchitecture.pdf`

10. [2 points] The number of cache sets at each level of the cache hierarchy.

    1. `the_isa.pdf` [2. `the_microarchitecture.pdf`]