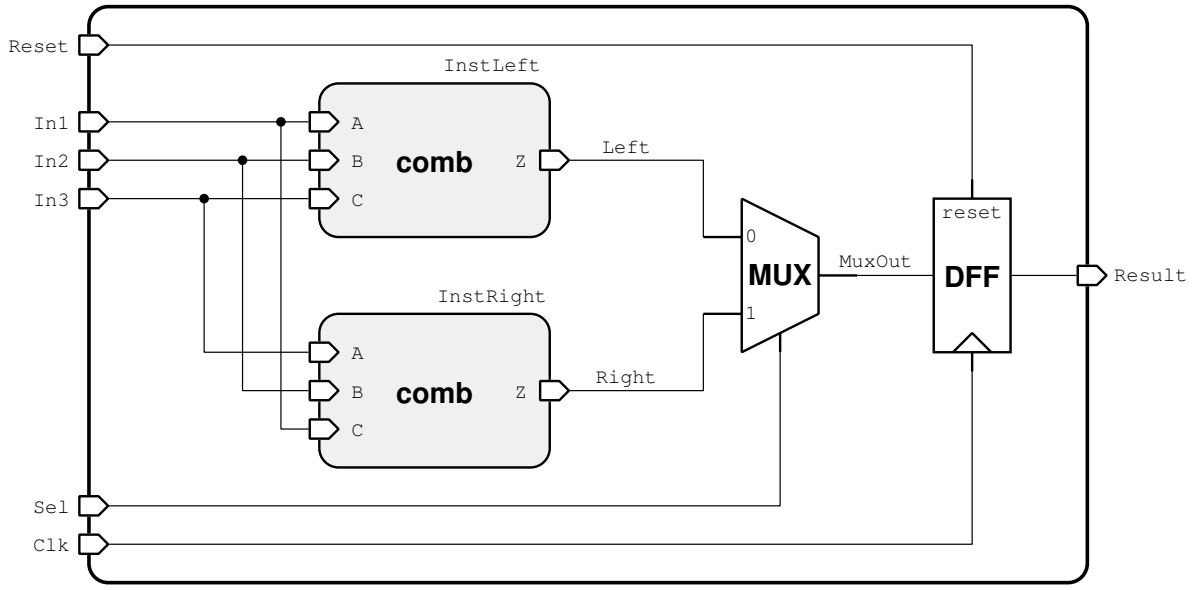
3. (15 points) In this question you are required to write the Verilog code that implements the following block diagram.



The block called *Controller* has six 1-bit inputs and a single 1-bit output (*Result*). It contains two instances of a combinational block called (*comb*). The following is the declaration part of this module:

```
1 module comb ( input A , input B , input C, output Z);
2   // definition of the combinational circuit comb
3
4 endmodule
```

Notes:

- The flip-flop and the multiplexer will not be instantiated, you will have to write the corresponding Verilog code.
- The flip-flop uses an asynchronous reset, the output is zero when reset is one.
- Note that Verilog is case sensitive.
- Write legibly.

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Solution:

```
1  module Controller (
2    input Clk,
3    input Reset,
4    input In1,In2,In3,
5    input Sel,
6    output reg Result);
7
8  // Define internal signals
9    wire Left, Right, MuxOut;
10
11 // instantiate the module comb two times
12   comb InstLeft  (.A(In1), .B(In2), .C(In3), .Z(Left) );
13   comb InstRight (.A(In3), .B(In2), .C(In1), .Z(Right) );
14
15 // The multiplexer
16   assign MuxOut = (Sel) ? Right: Left;
17
18 // The FF
19   always @ (posedge Clk, posedge Reset)
20      if (Reset) Result <= 1'b0;
21      else       Result <= MuxOut;
22
23 endmodule
```