4 Verilog [60 points]

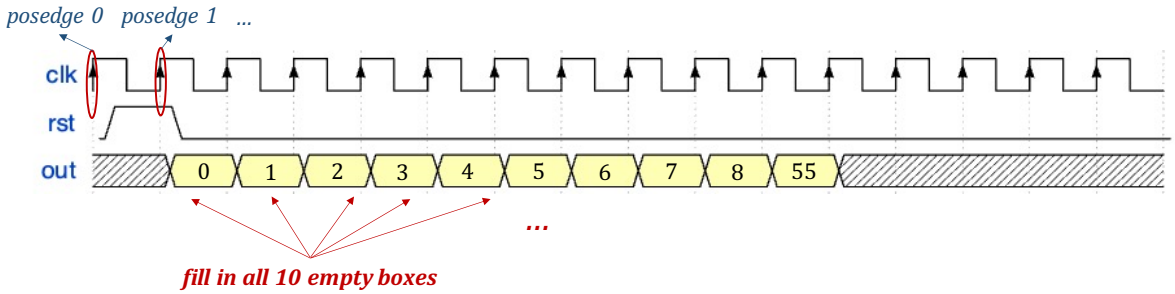
4.1 What Does This Code Do? [30 points]

Analyze the following Verilog module and answer the question.

```
1  module module_x (input wire clk, input wire rst,
2    input wire [7:0] in, output wire [7:0] out);
3
4  reg [7:0] var1, var2, var3, var4;
5
6  assign out = (var4 == in) ? var3 : var4;
7
8  always @(posedge clk) begin
9    if (rst) begin
10     var1  <= 8'b0;    var2  <= 8'b1;
11     var3  <= 8'b0;    var4  <= 8'b0;
12   end else begin
13     var1  <= var2;    var2  <= var1 + var2;
14     var3  <= var1 + var2;
15     var4  <= var4 + 8'b1;
16   end
17 end
18 endmodule
```

Assume that the input `in` *always* has the following value:
`in = 8'h09`

What **unsigned decimal** values does the `out` signal get in the following waveform diagram? Fill in the gray boxes with an `out` value for each `clk` cycle. Briefly explain your answer.



Brief explanation (to help us award you partial credit):

Explanation.
The module outputs the `in`th number in the Fibonacci sequence after `in` clock cycles. Until then, it outputs the number of clock cycles that have passed since reset.
For the given value of `in` (8'h09), the values for `out` are from leftmost yellow box to the rightmost yellow box:
`0, 1, 2, 3, 4, 5, 6, 7, 8, 55`

4.2 Is ChatGPT *not* Right? [30 points]

You gave ChatGPT the following prompt to help with your lab report: "A Verilog module that simulates a character's movement on a 2D-plane. The module takes four inputs for four directions (direction inputs) the character can move to. The module outputs x and y coordinates. The character stays in the same coordinate if none of the direction inputs are set. Initial coordinates (set on reset) are 0, 0. Stride determines how many units the character moves in one step."

```
module movement (
  input clk,    input rst,
  input up,     input down,
  input left,   input right,
  (1) stride,
  output [7:0] x_coord,
  output [7:0] y_coord
);
(2) x_internal, y_internal; // 8-bit signals
wire [2:0] move_amount = (3); // if stride is not zero, move by stride amount, else move by 1
always @(posedge clk) begin
  if (rst) begin
    x_internal <= 0; y_internal <= 0;
  end else begin
    if (up) y_internal <= y_internal + move_amount;
    else if (down) y_internal <= y_internal - move_amount;
    else if (left) x_internal <= x_internal - move_amount;
    x_internal <= x_internal + move_amount;
  end
end
(4) x_coord = x_internal; // output coordinate
(4) y_coord = y_internal; // output coordinate
endmodule
```

Provide your choice for each blank (1), (2), and (4) below. Circle only one of A, B, C, D. Provide a one-line expression for (3) (*Hint:* Use the ternary operator (`?`) to implement a MUX).

(1): A. output B. output reg C. input wire [2:0] D. input reg

(2): A. wire [7:0] B. [7:0] wire C. wire [8:0] D. reg [7:0]

(3): `stride != 3'b0 ? stride : 3'b1;`

(4): A. B. `assign` C. == D. `let`

Explanation.
(1): Signal `stride` is used as an input to the module, so it should be declared as an input. Among options that describe input signals (C and D), `input reg` is not valid Verilog syntax.
(2): The correct way to describe signals that we can assign values to in an always block is `reg [7:0]`.
(3): We describe a mux using the ternary operator as such: `stride != 3'b0 ? stride : 3'b1;`. If stride is zero, the left-hand side of the ternary operator (i.e., `stride`) is the output of the mux and otherwise the right-hand side (i.e., `3'b1`) is the output of the mux.
(4): The correct syntax for assigning a value to a signal is `assign x_coord = x_internal;`. Other options are not valid Verilog syntax.

Did ChatGPT inject any errors in this code? Write down line number(s) and a short explanation (to help us award you partial credit).

Explanation. Line 18 introduces a logical error, causing `x_internal` to always be incremented by `move_amount` regardless of the direction of movement.