

## 5 Memory Potpourri [45 points]

Read the following statements about memory organization & technology. Circle “True” if the statement is true and “False” otherwise. *Note: we will subtract 2 points for each **incorrect** answer and award 0 points for each unanswered question.*

1. [3 points] A main memory access typically has larger latency than a register file access.  
☐ 1. True      ☐ 2. False
2. [3 points] SRAM is commonly used as main memory in modern computers.  
☐ 1. True      ☐ 2. False
3. [3 points] A DRAM cell requires larger power to store data compared to an SRAM cell.  
☐ 1. True      ☐ 2. False
4. [3 points] Reads are faster than writes in DRAM.  
☐ 1. True      ☐ 2. False
5. [3 points] Reads are faster than writes in phase change memory.  
☐ 1. True      ☐ 2. False
6. [3 points] A bitline in a DRAM array connects all DRAM cells in a DRAM row to the row decoder circuitry.  
☐ 1. True      ☐ 2. False
7. [3 points] Using virtual memory reduces the memory access latency.  
☐ 1. True      ☐ 2. False
8. [3 points] Phase Change Memory (PCM) is non-volatile.  
☐ 1. True      ☐ 2. False
9. [3 points] If a hypothetical system is *not* constrained by chip area, memory cost (\$), and energy consumption, PCM would be the best memory technology to use in that system.  
☐ 1. True      ☐ 2. False
10. [3 points] A program with a streaming memory access pattern leads to very high temporal locality in the last level data cache.  
☐ 1. True      ☐ 2. False
11. [3 points] In DRAM, accesses to different rows in one bank can be serviced faster compared to accesses to different rows in different banks.  
☐ 1. True      ☐ 2. False
12. [3 points] TLB is a specialized instruction cache that caches instructions based on branch prediction results.  
☐ 1. True      ☐ 2. False
13. [3 points] Virtual memory simplifies software design.  
☐ 1. True      ☐ 2. False
14. [3 points] A page fault happens when the TLB does not contain the entry needed by an instruction.  
☐ 1. True      ☐ 2. False
15. [3 points] A fully-associative L1 TLB that only stores 4KB virtual-to-physical mappings and has 1024 entries can cover up to 4MB of memory.  
☐ 1. True      ☐ 2. False