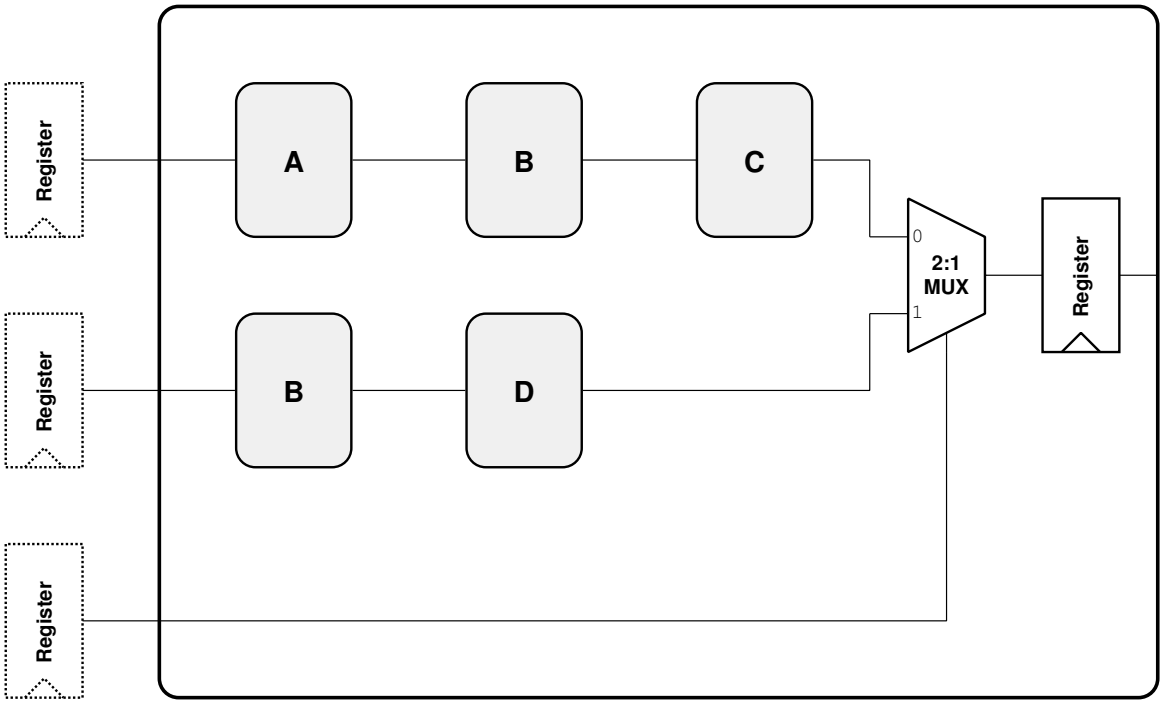
4. In this question you are required to calculate different timing paths for the circuit given below.



Note that the block B is used *twice*. All the inputs are supplied from external registers. The timing properties of all the blocks used in the circuit are given in the table below:

Block	Propagation Delay	Contamination Delay	Setup Time	Hold Time
Register	0.0 ns	0.0 ns	0.1 ns	0.0 ns
2:1 Multiplexer	0.3 ns	0.3 ns	n.a.	n.a.
A	0.6 ns	0.4 ns	n.a.	n.a.
B	1.8 ns	1.0 ns	n.a.	n.a.
C	1.2 ns	0.8 ns	n.a.	n.a.
D	1.0 ns	0.8 ns	n.a.	n.a.

Hint: $\frac{1}{1\,ns} = 1\,GHz$*, a clock with 1 GHz has a period of 1 ns. 1 GHz = 1000 MHz*

(a) (2 points) What is the *critical path* of this circuit? Calculate its path delay.

Solution:
Critical path is the longest timing path in the circuit:

$$\begin{aligned} CriticalPath = & \quad t_{pd,A} + t_{pd,B} + t_{pd,C} + t_{pd,mux} + t_{setup,FF} \\ = & \quad 0.6 + 1.8 + 1.2 + 0.3 + 0.1\,ns \\ = & \quad 4.0\,ns \end{aligned}$$

(b) (1 point) What is the maximum operating frequency of this circuit?

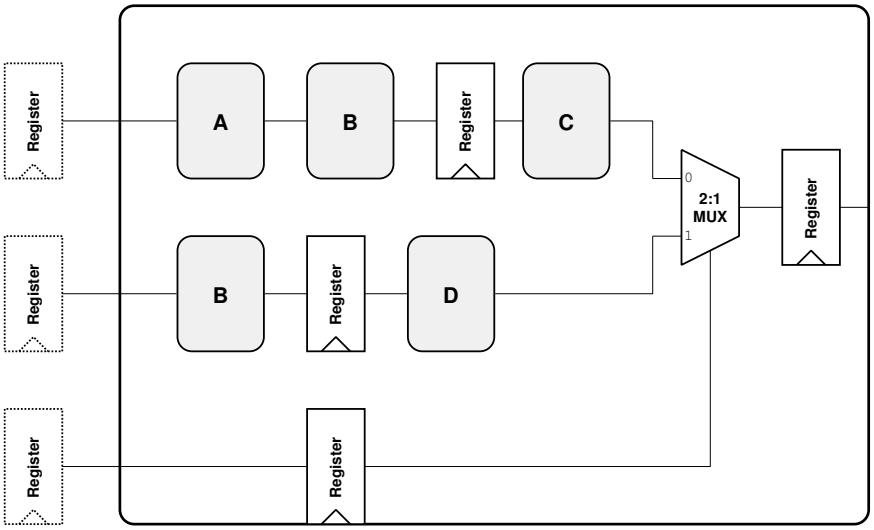
Solution: Maximum operating frequency is 1/Critical Path, $1/4\,ns = 250\,MHz$.

(c) (2 points) What is the *shortest path* of this circuit ?

Solution: The short path is the fastest route a signal can propagate through the circuit. In this case it is the signal that goes through the select input of the multiplexer and reaches the register. This signal only passes through the multiplexer, so the short path is $0.3\,ns$.

(d) (8 points) In order to make the circuit faster, it is suggested to introduce pipelining. Determine the **best** location between the blocks to place the pipeline registers assuming a **one stage** pipeline implementation and redraw the schematic. (*Hint: in a one stage pipeline, the latency increases only by 1 clock cycle*).

Solution:



Note that you will have to insert a pipeline register in all paths, including the multiplexer control register.

(e) (2 points) What is the *critical path* of this pipelined circuit and calculate its path delay.

Solution:

$$\begin{aligned} CriticalPath &= t_{pd,A} + t_{pd,B} + t_{setup,FF} \\ &= 0.6 + 1.8 + 0.1\,ns \\ &= 2.5\,ns \end{aligned}$$

(f) (1 point) What is the speed-up we have achieved by pipelining?

Solution: Old critical path / New Critical path = 4.0 / 2.5 = 1.6. The new circuit has a 60% shorter critical path, therefore it can be clocked 60% faster.

(g) (2 points) Why did we not achieve the theoretical maximum speed-up from the pipelining. State at least **two** reasons.

Solution:

1. It was not possible to place the pipeline registers at exactly half the previous critical path. Unless we move the pipeline registers into the blocks themselves we can not improve any more.
2. The pipeline register has a small overhead ($t_{setup,FF} > 0$). Even if we managed to divide the circuit in equal halves, this overhead would not allow us to reach 100% speedup. The problem gets worse the shorter the critical path is.