4. In this question we will continue with the circuit from question 3. You will first be asked to estimate the area and speed of the circuit. Then in the second part you will be asked to design a parallel implementation and report the size of the circuit.

   Use the following table to estimate the speed and area of the circuit. Consider that the FSM **is very small** and **is not part of the critical path** for this exercise.
   Note: 1 ns = 10^{-9} s and 1 μm^2 = 10^{-12} m^2

Description	**Bit-width**	**Area** [µm^2]	**Critical Path** [ns]
Adder	8-bit	300	1.0
Subtracter	8-bit	300	1.0
Adder/Subtracter	8-bit	350	1.1
Multiplier	8-bit	2,000	2.5
Multiplexer	8-bit	100	0.2
Register(with enable)	8-bit	200	0.0 (ideal)
Adder	16-bit	600	2.0
Subtracter	16-bit	600	2.0
Adder/Subtracter	16-bit	700	2.1
Multiplier	16-bit	8,000	5.0
Multiplexer	16-bit	200	0.2
Register(with enable)	16-bit	400	0.0 (ideal)

   (a) (2 points) Calculate the size of the circuit in Question 3.

   Solution:

$$\begin{aligned} A_{old} = & \quad 2 \times A_{mux\,8b} + A_{mul\,8b} + A_{mux\,16b} + A_{addsub\,16b} + 2 \times A_{reg\,16b} \\ = & \quad 2 \times 100 + 2,100 + 200 + 700 + 2 \times 400 \\ = & \quad 4'000 \end{aligned}$$

   (b) (2 points) Calculate the critical path of the circuit in Question 3.

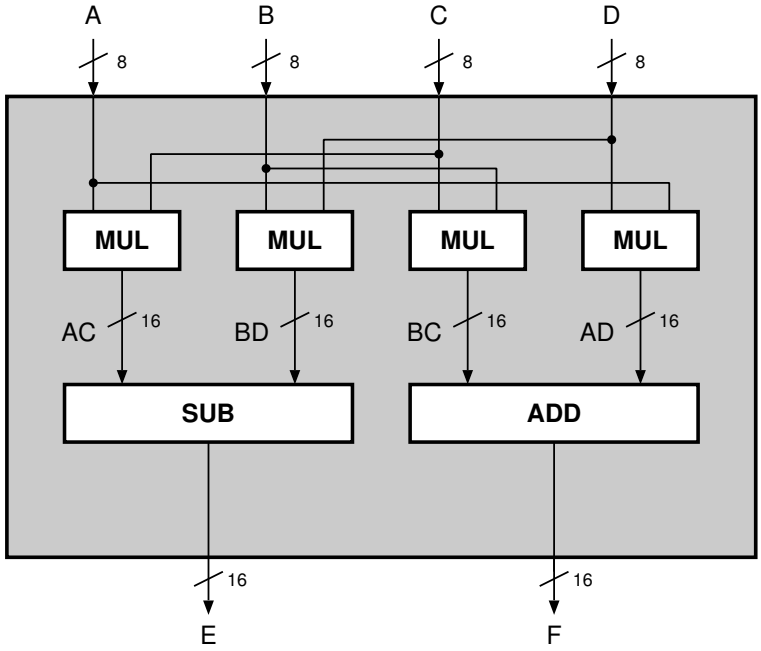
   Solution:

$$\begin{aligned} t_{crit\,old} = & \quad t_{mux\,8b} + t_{mul\,8b} + t_{addsub\,16b} + t_{mux\,16b} + t_{reg\,16b} \\ = & \quad 0.2\,ns + 2.5\,ns + 2.1\,ns + 0.2\,ns + 0\,ns(setup) \\ = & \quad 5.0\,ns \end{aligned}$$

   (c) (2 points) How long (in ns) will it take this circuit to complete one complex multiplication? *Note: it will take more than one clock cycle*

Solution: There are four cycles needed to complete the operation. Each cycle takes $t_{crit\,old} = 5\,ns$ this means that a complex multiplication can be completed every $t_{old} = 20\,ns$.

(d) (5 points) It turns out that the circuit in Question 3, is too slow for your application. Draw the block diagram for an architecture that calculates the complex multiplication combinationally (i.e. within one clock cycle).



(e) (2 points) How much larger is this new circuit when compared to the previous circuit from Question 3?

Solution:

$$\begin{aligned} A_{new} &= 4 \times A_{mult\,8bit} + A_{adder\,16bit} + A_{subtracter\,16bit} \\ &= 4 \times 2,100 + 600 + 600 \\ &= 9'600 \end{aligned}$$

The circuit is $A_{new}/A_{old} = 9,600/4,000 = 2.4$ times larger.

(f) (2 points) How much faster does this new circuit compute a complex multiplication when compared to the previous circuit from Question 3?

Solution:

$$\begin{aligned} t_{new} &= t_{mult\,8bit} + t_{adder\,16bit} \\ &= 2.5\,ns + 2.0\,ns \\ &= 4.5\,ns \end{aligned}$$

The circuit is $t_{old}/t_{new} = 20/4.5 = 4.4$ times faster.