## 5. Memory Consistency [40 points]

There are 2 threads with 4 instructions. The two threads are executed concurrently on a dual-core processor. Assume that registers in both cores are initialized with the values shown in the table below. The instructions of each thread are also shown below.

| | |
|---|---|
| R1 | 1 |
| R2 | 2 |
| R3 | 3 |
| R4 | 4 |

| Thread A | Thread B |
|---|---|
| ST R1, 0x1000 | ST R3, 0x1000 |
| LD R5, 0x1000 | LD R5, 0x1000 |
| ADD R5, R5, R2 | ADD R5, R5, R4 |
| ST R5, 0x1000 | ST R5, 0x1000 |

(a) Assume the dual-core processor implements sequential consistency. List **all** the possible values that can be stored in address 0x1000, assuming both threads run to completion.

3, 5, 7, 9

(b) How many different memory instruction interleavings of the 2 threads **will guarantee** a value of 0x9 in address 0x1000, assuming both threads run to completion? Show your work.

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(c) Assume now that the dual-core processor does **not** support sequential consistency. List **all the possible values** that can be stored in address 0x1000, assuming both threads run to completion. Explain your answer briefly.

3, 5, 7, 9
Thread B might never see the sequential updates of Thread A, but the result will be equivalent to that of a sequentially consistent model.