# 4 ISA vs. Microarchitecture [30 points]

A new CPU has two comprehensive user manuals available for purchase which describe the ISA and the microarchitecture of the CPU, respectively.

Unfortunately, the manuals are extremely expensive, and you can only afford one of the two. If both manuals might be useful, you would prefer the ISA manual since it is much cheaper than the microarchitecture manual.

For each of the following questions that you would like to answer, decide which manual is more likely to help. *Note: we will subtract 1 point for each* ***incorrect*** *answer and award 0 points for unanswered questions (the minimum number of total points you can get for this question is 0).*

1. [2 points] Number of uniquely identifiable memory locations.

   [1. ISA] 2. Microarchitecture

2. [2 points] Number of instructions fetched per clock cycle.

   1. ISA [2. Microarchitecture]

3. [2 points] Support for branch prediction hints conveyed by the compiler.

   [1. ISA] 2. Microarchitecture

4. [2 points] Number of general-purpose registers.

   [1. ISA] 2. Microarchitecture

5. [2 points] Number of non-programmable registers.

   1. ISA [2. Microarchitecture]

6. [2 points] SIMD processing support.

   [1. ISA] 2. Microarchitecture

7. [2 points] Number of integer arithmetic and logic units (ALUs).

   1. ISA [2. Microarchitecture]

8. [2 points] Number of read ports in the physical register file.

   1. ISA [2. Microarchitecture]

9. [2 points] Endianness (big endian vs. small endian).

   [1. ISA] 2. Microarchitecture

10. [2 points] Size of a virtual memory page.

    [1. ISA] 2. Microarchitecture

11. [2 points] Cache coherence protocol.

    1. ISA [2. Microarchitecture]

12. [2 points] Number of cache blocks in the L3 cache.

    1. ISA [2. Microarchitecture]

13. [2 points] Ability to flush (i.e., invalidate) a cache line using the operating system code.

    [1. ISA] 2. Microarchitecture

14. [2 points] Number of pipeline stages.

    1. ISA [2. Microarchitecture]

15. [2 points] How many prefetches the hardware prefetcher generates in a clock cycle.

    1. ISA [2. Microarchitecture]