Fast PVT-Tolerant Physical Design of RF IC Components

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Background and Motivation

Application Space

- RF communication circuits and components
  - Mobile phones, RF transceivers, etc.
  - Phase-Locked Loops (PLLs) and components (VCO).
  - Low-Noise Amplifiers (LNAs).

How this research fills a key need

- PVT variability makes it hard to achieve “safe” designs in nanoscale CMOS technologies; also reduces yield.
- Some attempts have been made to address PVT variation issues in digital circuits.
- No major attempts have been made to address these for RF integrated circuits (RFICs) due to increased complexity, non-linearity and bottlenecks of analog simulation.

Comparison with existing research

Reference	Technology	Performance	Power
Tiebout et. al.	250nm	1.8GHz	20mW
Dehghani et.al.	250nm	2.5GHz	2.6mW
Long et. al.	180nm	2.4GHz	1.8mW
Kwok et. al.	180nm	1.4GHz	1.46mW
Our Aim	**180nm scaled to 90nm**	**2.0-5.0 GHz**	**< 1mw**

Task Overview

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- **Thrust Area**: High-performance, low-cost RF and analog/mixed-signal solutions.
- **Task Leader**: Saraju P. Mohanty
- **Co-PI**: Elias Kougianos
- **Student**: Garima Thakral (PhD student in CE)
- **Industrial Liaisons**: Priyadarsan Patra, Intel and other interested parties
- **Anticipated Results**: Novel design and optimization methodologies that can produce PVT-tolerant RFICs in one design iteration only and with minimal (two or less) manual layout steps to improve circuit yield and reduce chip cost.

Overall Approach and Key Technical Challenges

Key circuit performance objectives

- **Power** (including all leakage mechanisms) dissipation: in the order of 1mW.
- **Oscillating frequency**: in the order of 4GHz.
- **Variability**: Statistical distribution functions representing power, oscillating-frequency, phase noise and relevant metrics have 30% less variability.

Technical Challenges to Address

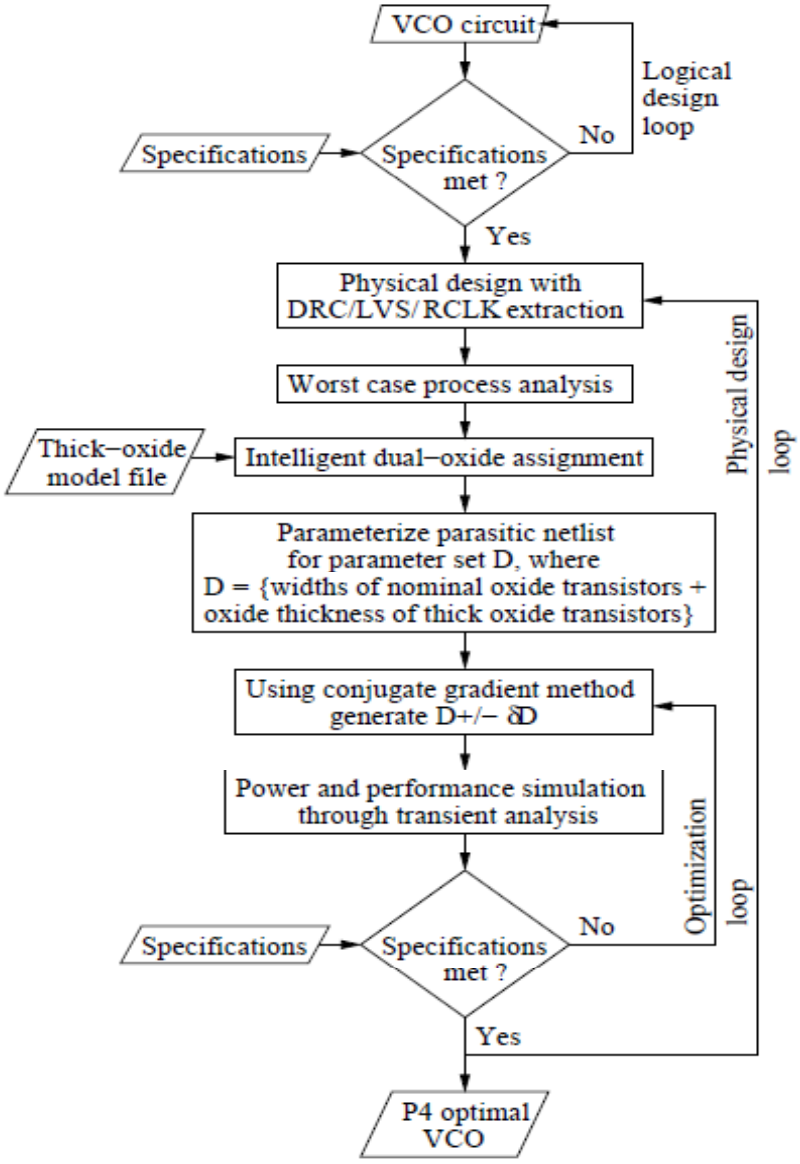
- **ITRS Grand Challenge:**
  - Logic device scaling (Process Integration, Devices, and Structures, Front End Processes, Modeling and Simulation, and Metrology)
  - High-Performance, Low-Cost RF and Analog/Mixed-Signal Solutions (Radio Frequency and Analog/Mixed Signal Technologies for Wireless Communications)

Technical Challenges to Address

- **Reducing design cycle time**: currently multiple manual design/layout iterations are needed.
- **Accounting for PVT in the design flow**: to make design PVT-tolerant to enhance circuit yield.

Our Approach

- The logical design is done to meet the required specifications.
- Initial physical design is subjected to DRC/LVS/RCLK extraction.
- Worst case process variation analysis of the physical design is done with respect to performance (e.g, center frequency).
- Intelligent dual-oxide assignment (*Toxp, Toxn*) to the power-hungry transistors of the VCO.
- Parasitic netlist is parameterized for parameter set D (widths of transistors and *Toxpth, Toxnth*). The parameterized parasitic netlist is subjected to an optimization loop to meet the specifications (performance, power) in a *worst case process* environment.
- Parameter values for which the specifications are met are obtained, and a final physical design of the VCO is created using these parameter values.



Our Approach

- **Input:** Parasitic parameterized netlist, baseline model file, thick oxide model file, objective set $F = [\, f_c,\ P_{VCO}\,]$, stopping criteria S, design variable set $D = [\ Wn,\ Wp,\ Wncs,\ Wpcs,\ Toxpth,\ Toxnth\ ]$, lower constraint C_{low}, upper constraint C_{up}.
- **Output:** Optimized objective set F_{opt}, optimal design variable set D_{opt} for $S = \pm\ \beta$, {where $1\% \leq \beta \leq 5\%$}.
- Run initial simulation in order to obtain feasible values of design variables for the given specifications.
- **while** $(C_{low} < D < C_{up})$ **do**
- Using conjugate gradient, generate new set of design variables $D' = D \pm \delta D$.
- Compute objective set $F = [\, f_c,\ P_{VCO}\,]$.
- **if** $(S == \pm\ \beta)$ **then**

  return $D_{opt} = D'$.
- **end if**
- **end while**
- Using D_{opt}, construct final physical design and simulate.
- Record F'_{opt} $(\ \| F'_{opt} - F_{opt} \| \leq S\ )$

Technical Goals and Objectives

Initial Objectives for Year 1

- Determination of impact of process variations on RF IC design flows.
- Determination of impact of voltage variations on RF IC design flows.
- Process and voltage optimal RF IC design flow.

Demonstration Plans

- 180/90nm physical design of LC-VCO.
- Simulation study on full-blown parasitic extracted netlist of physical design.

Planned Task Deliverables

- A single-iteration design-flow.
- Algorithm for fast statistical optimization.
- A physical design.

Questions/Discussion

- What technology will be used?
- How variability will be accounted for (i.e., fab data)?
- Specific designs/components.


Thank you !