CSCE 3730 – Reconfigurable Logic
Lab 4 – 11/11/2008 (Tuesday)

Design a 1 bit And-gate, OR-gate, NOR-gate, Adder, 2 to 1 Multiplexer and 4 to 1 Multiplexer in VHDL. Each of these modules should be coded in separate VHDL files. This lab helps you to build the individual components of your ALU project. All these modules are single bit components. Check for syntax errors after coding and then simulate your design by writing suitable Test-benches for each module. Show the results to T.A. and ask the T.A. for any help regarding the design.