Design of a Reconfigurable Embedded Data Cache

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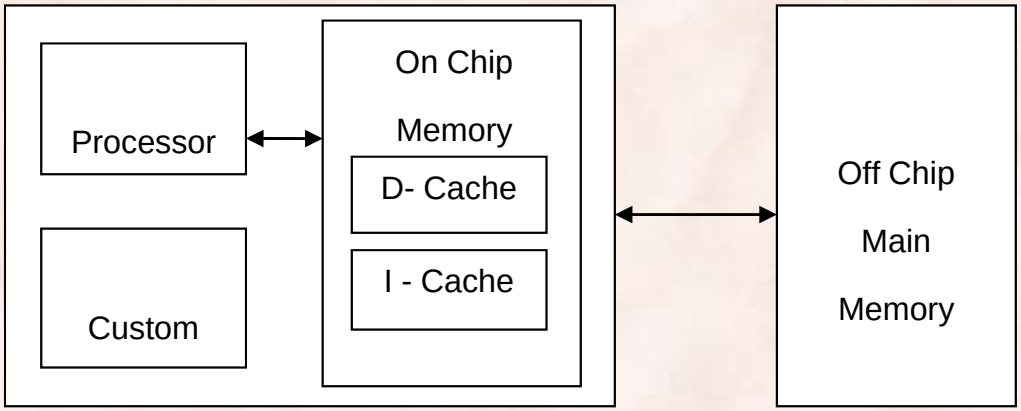
Agenda

- Cache Memory : Introduction and Motivation
- Related Prior Research
- Proposed Architecture
- Prototype Development
- Experiments and Simulation Results
- Conclusion and Future Research

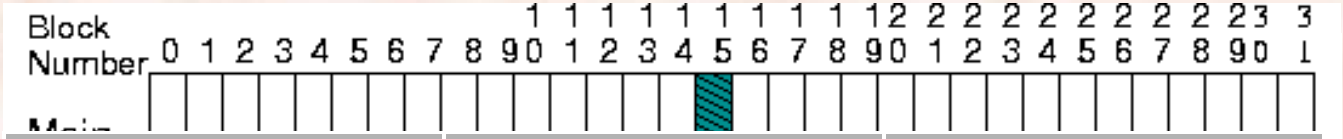
Cache Memory : Introduction

- Cache is a small on chip memory situated between high speed processor and low speed main memory
- Cache occupies about fifty percent of the total area and also accounts for about fifty percent of a processor's total power.
- A particular embedded microprocessor uses a specific cache architecture as per its requirement.
- It is implemented using SRAM which makes it fast



Cache Architecture

- Direct-Mapped Cache
- Fully Associative Cache
- Set Associative Cache



Cache Type	Access Time	Hit Ratio
Direct Mapped	Less	Poor Comparatively
N-way Set Associative	Moderate, (worsen as N increases)	Very Good, (improves further as N increases)
Fully Associative	Highest	Best

Direct Mapped

Block 15 can be placed only in block 7 (15 Mod 8)

Set Associative

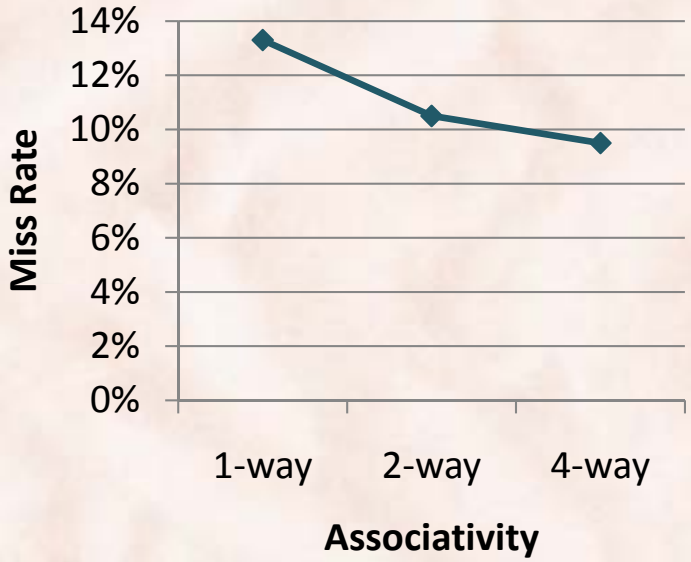
Block 15 can be placed anywhere in set 3 (15 Mod 4)

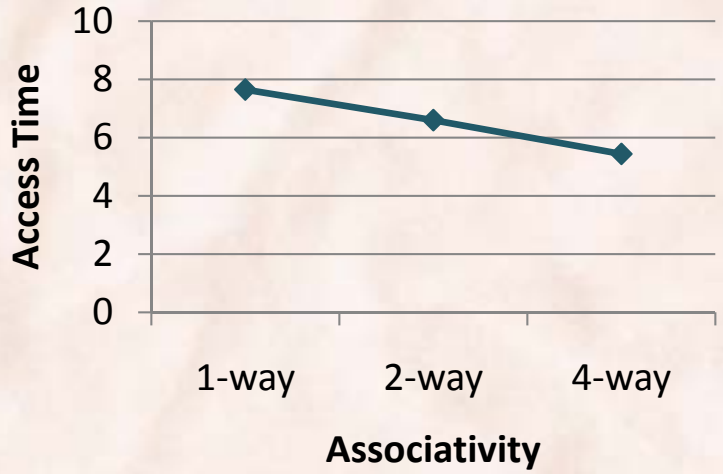
Fully Associative

Block 15 can be placed anywhere

Impact of Cache Associativity

Associativity	Miss Rate	Access Time(Clk cycle)
1-way	13.3%	7.65
2-way	10.5%	6.60
4-way	9.5%	5.44

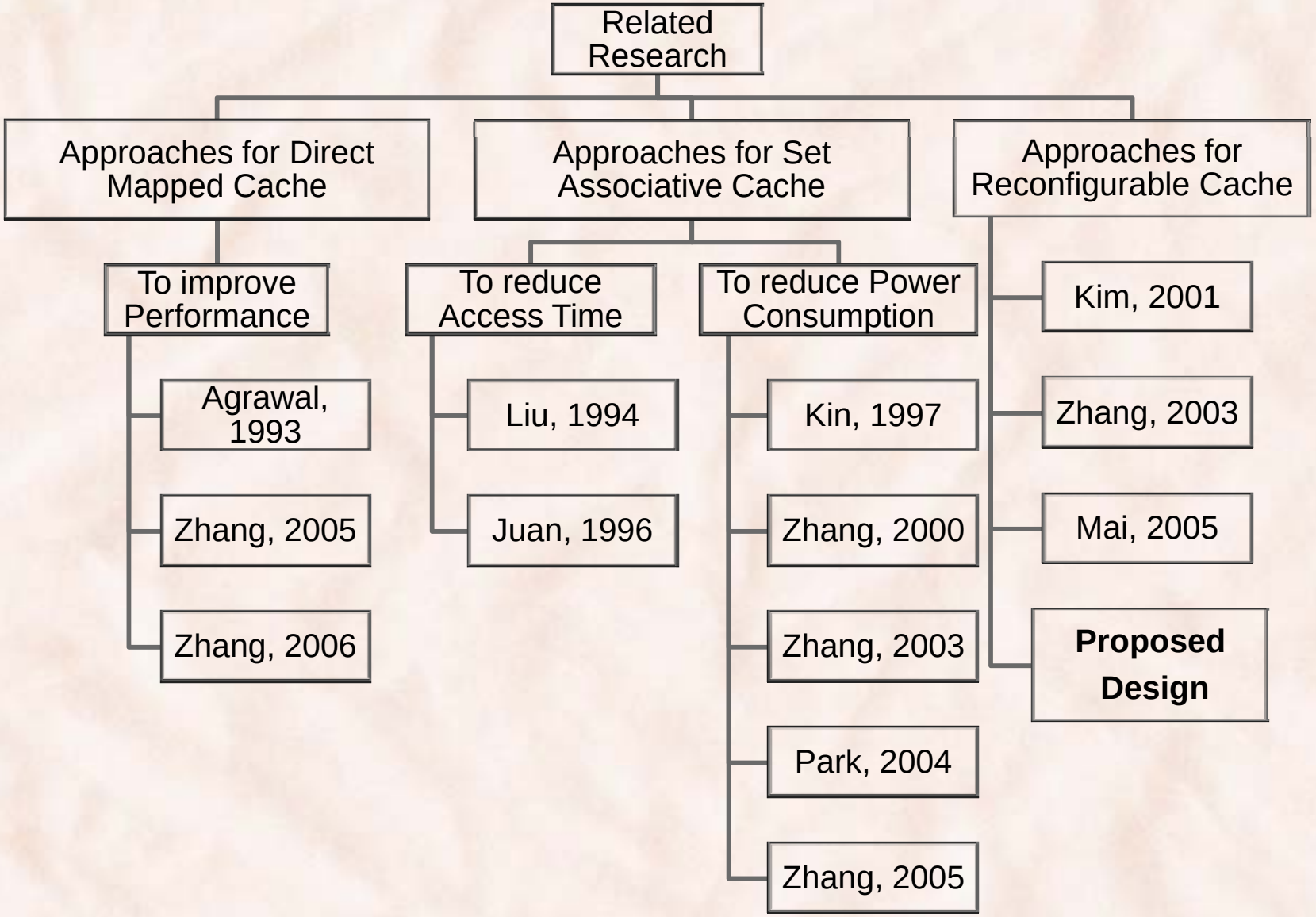




Motivation

- Most commonly used embedded microprocessors use either 1-way, 2-way or 4-way associative data cache.
- Proposed design can be configured as direct-mapped, two-way or four-way set associative according to the system's requirement.
- We have obtained this re-configurability through mode selector unit.

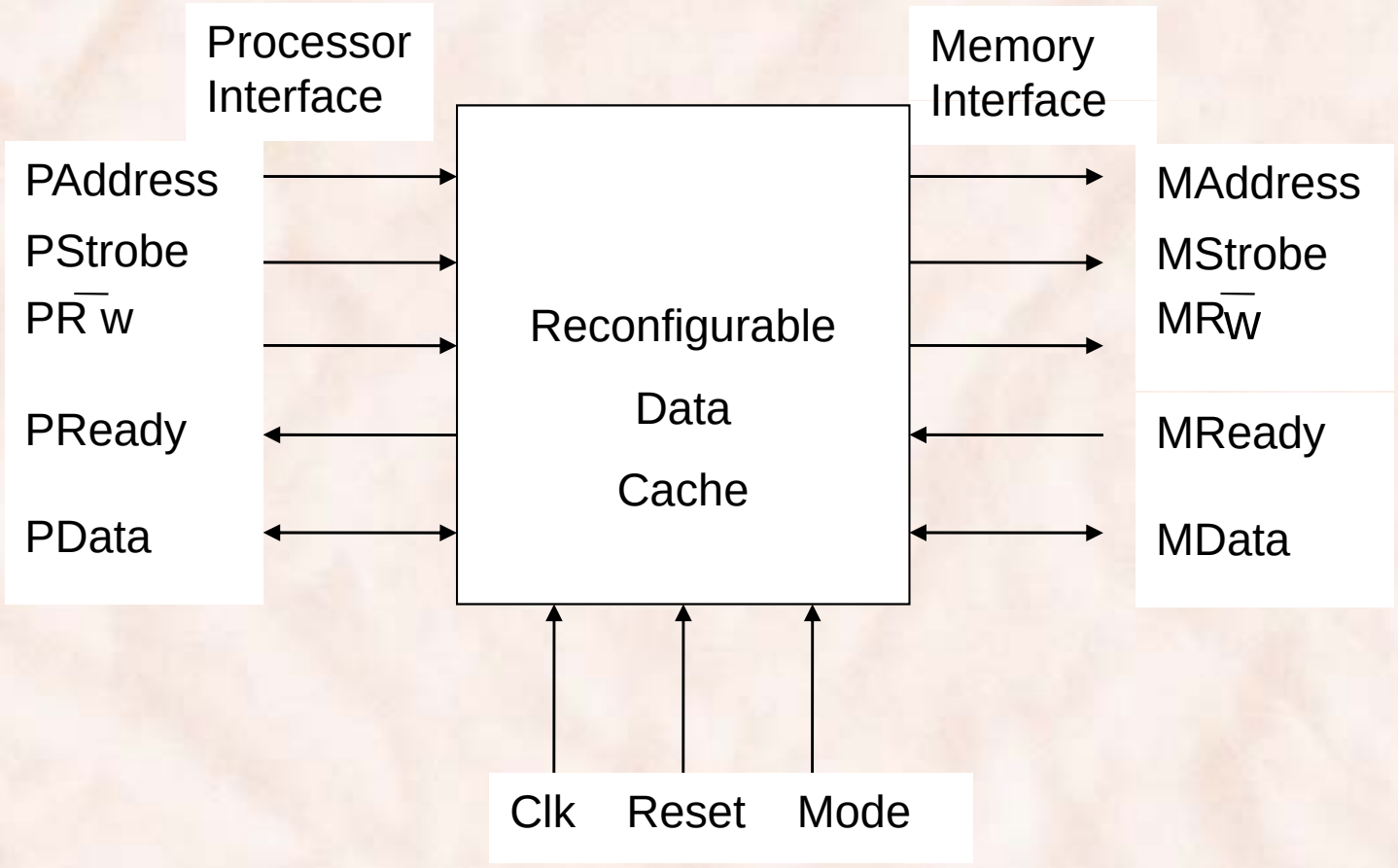
Prior Related Research



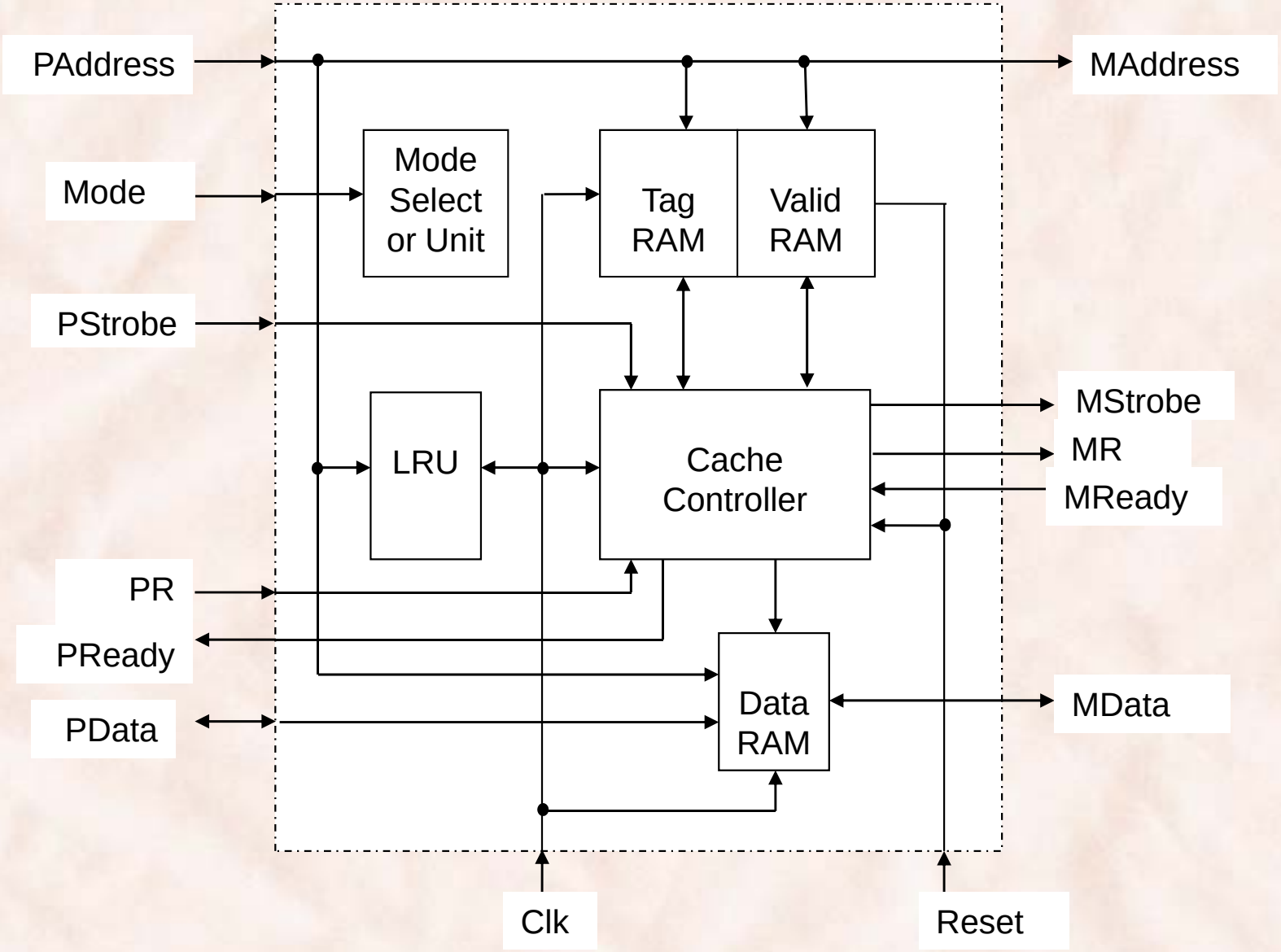
Elements of Cache Design

Elements	Existing	Proposed Architecture
Cache Size	Few bytes to several Kbytes	256 bytes
Mapping Function	Direct Fully Associative N-way Set Associative	Direct Mapped Two-way Set-associative Four-way Set-associative
Replacement Policy	Least Recently Used (LRU) First-in-first-out (FIFO) Least Frequently Used (LFU) Random	Least Recently Used (LRU)
Write Policy	Write through Write Buffer Write Back	Write through
Block Size	Multiple Words	1 Word

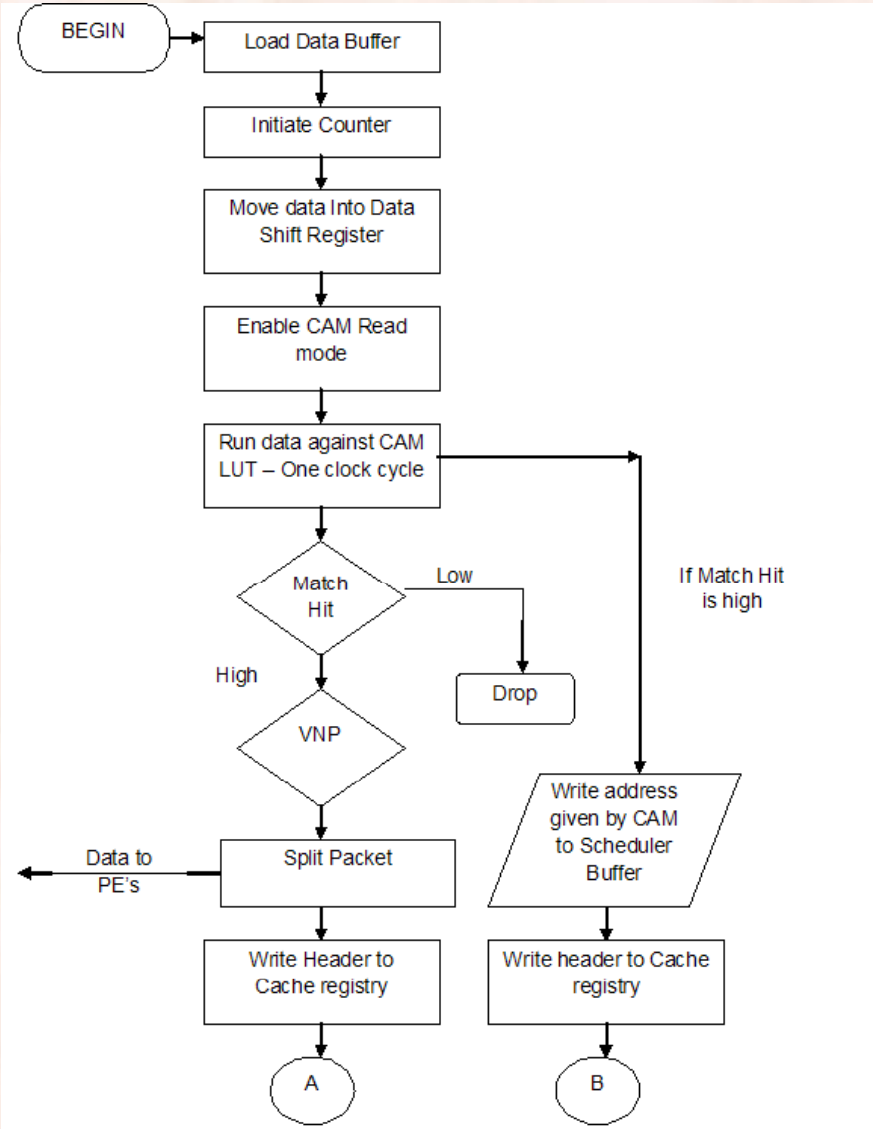
High level view of proposed Architecture of Reconfigurable Data Cache

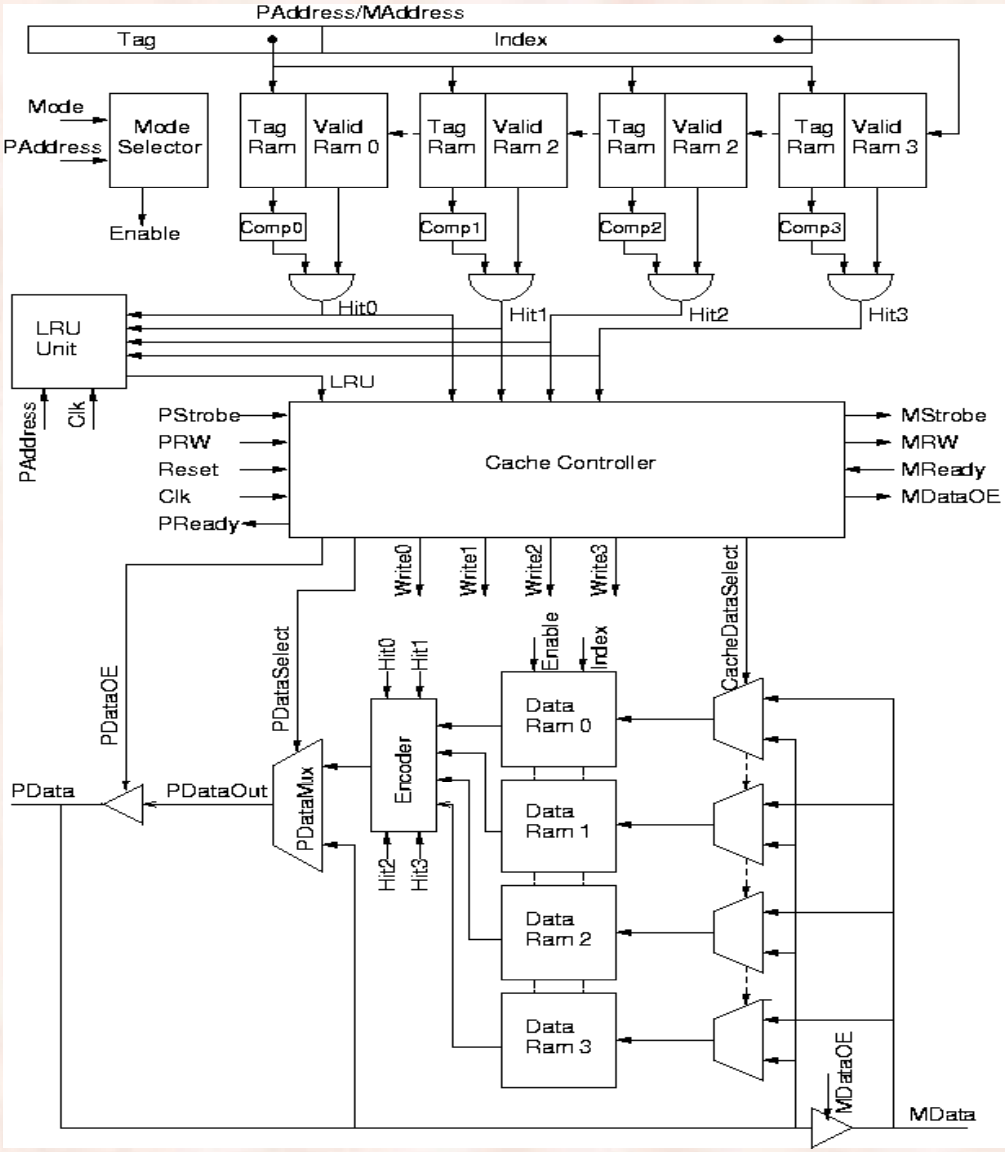


Proposed Architecture



Proposed Detailed Architecture





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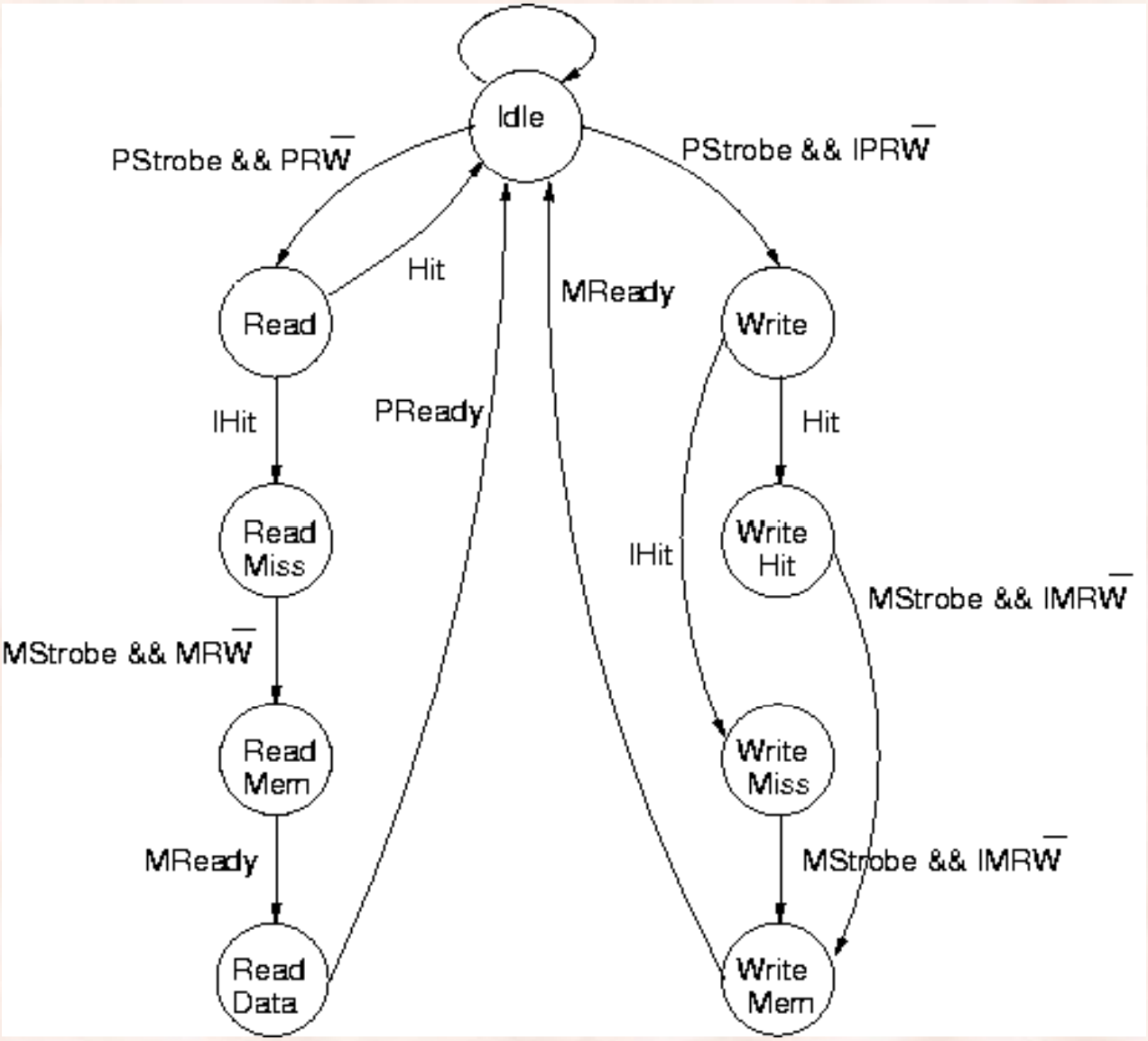
Cache Controller



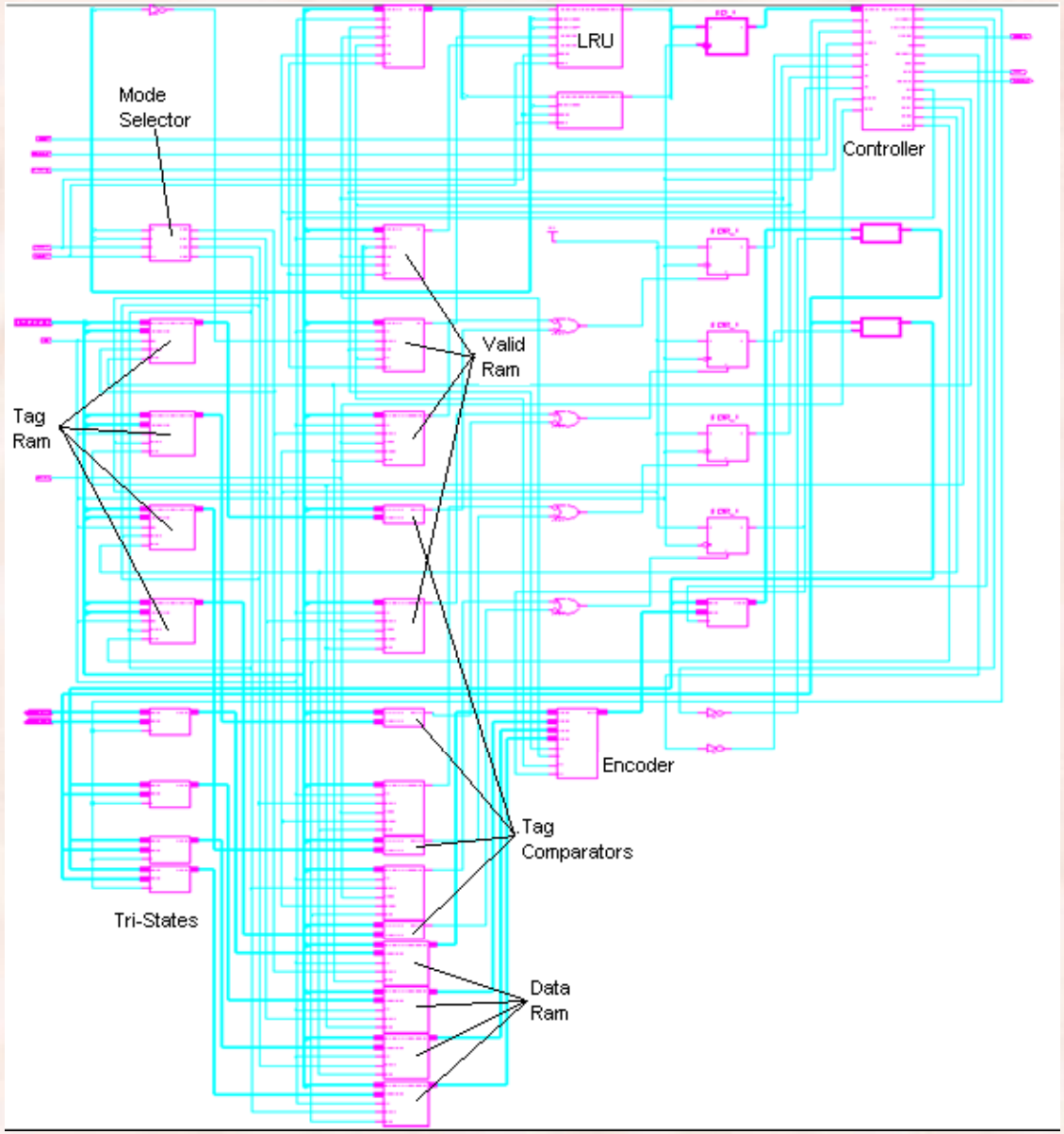
Cache Controller : Control Signals

State	Active Control Signals
Idle	**None**
Read	**PStrobe,** $PR\overline{W}$**, PDataOE, PReadyEnable, Hit (in case of read hit)**
ReadMiss	$PR\overline{W}$**, PDataOE, Miss, Mstrobe,** $MR\overline{W}$
ReadMemory	$PR\overline{W}$**, PDataOE,** $MR\overline{W}$
ReadData	$MR\overline{W}$**, PDataOE, PDataSelect, CacheDataSelect,** $MR\overline{W}$**, Ready**
Write	**PStrobe**
WriteHit	**Hit, MStrobe, MDataOE**
WriteMiss	**Miss, MStrobe, MDataOE**
WriteMemory	**MStrobe, Ready**

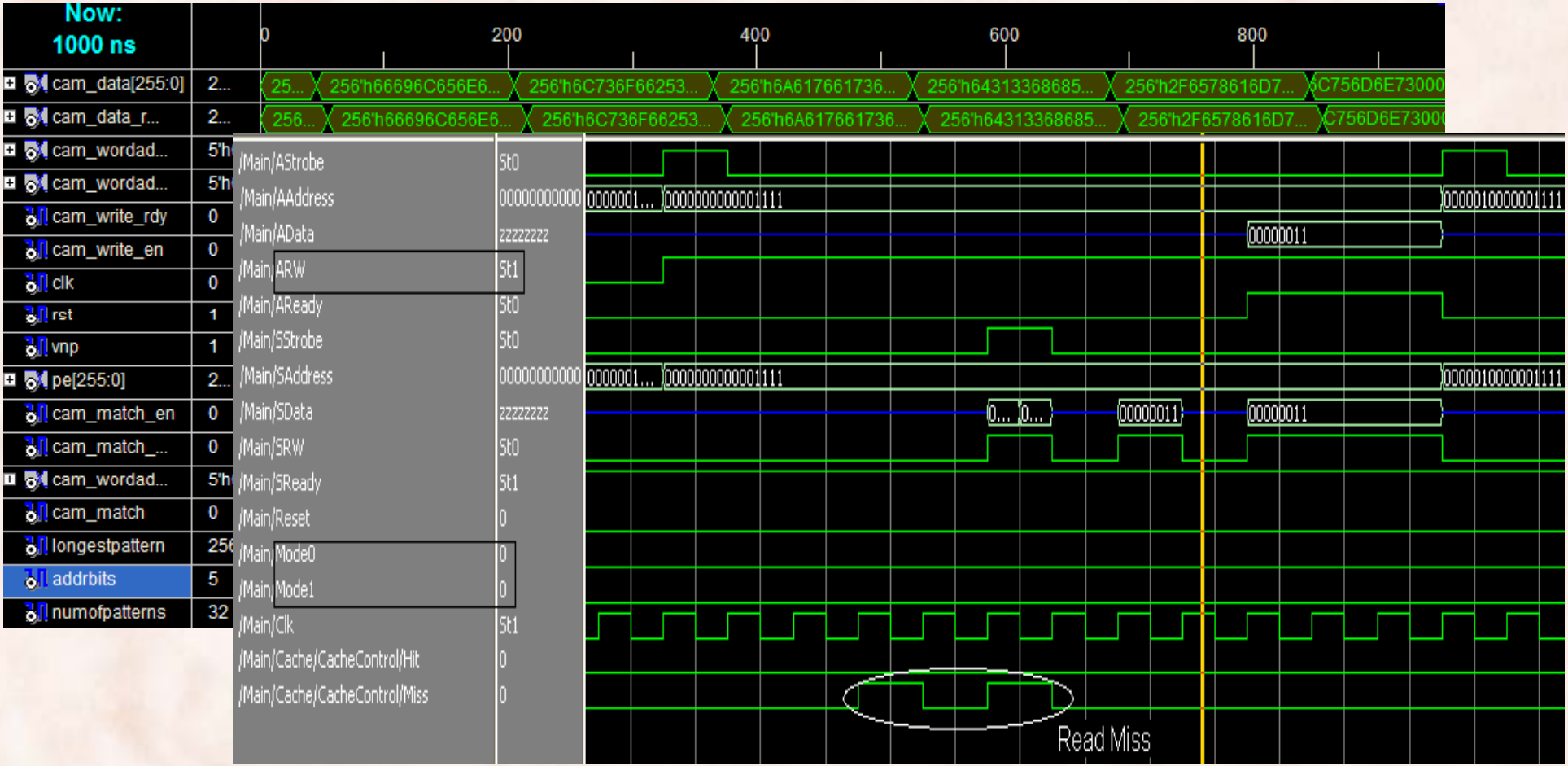
Prototype Development

- The proposed architecture of Reconfigurable Data Cache has been developed in Verilog in Xilinx ISE 9.1i. The implementations are targeted for Xilinx's Virtex-5 family of FPGAs.
- Functional simulation of the design has been carried out in ModelSim SE 6.3e using a trace file containing 20 different cases.
- Experimental Set up
  - 16-bit address bus,
  - 256 bytes of cache,
  - Data bus of 8 bit.

RTL Schematic



Simulation Waveform in Mode ‘00’ (Direct Mapped) showing Read Miss



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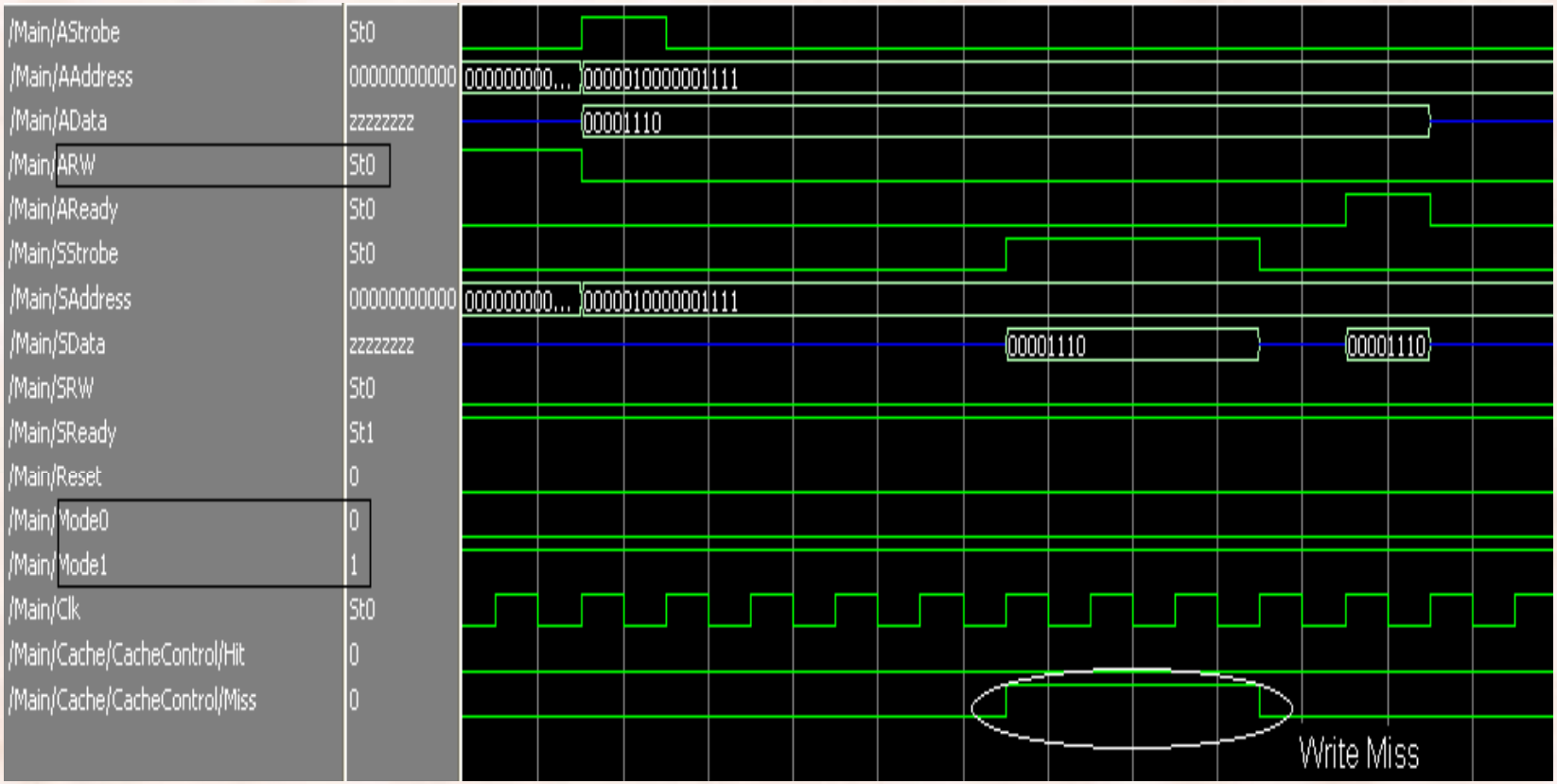
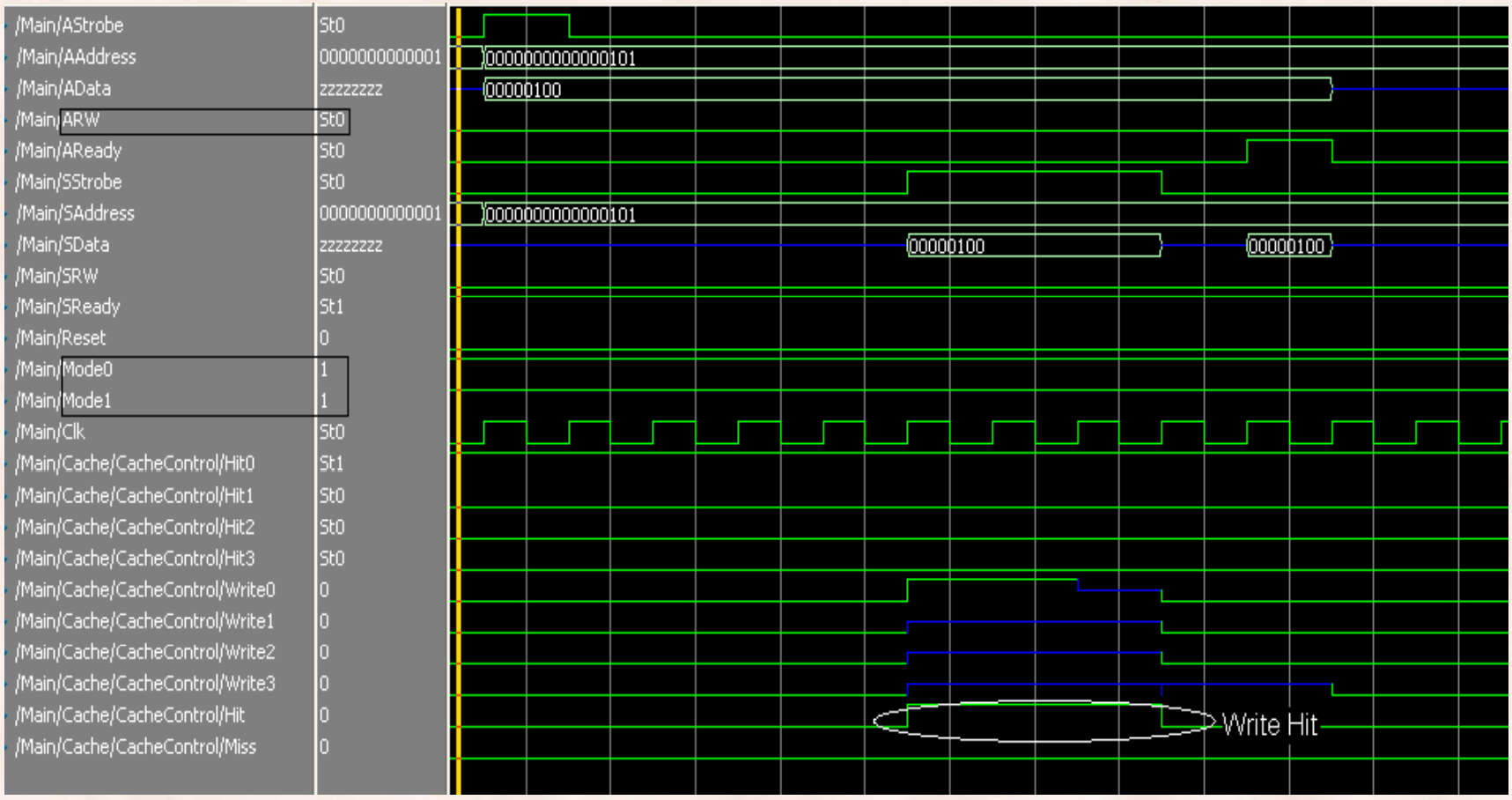
Simulation Waveform in Mode '01' (Two-way Set-associative) showing Write Miss



Simulation Waveform in Mode ‘11’ (Four-way Set-associative) showing Write Hit



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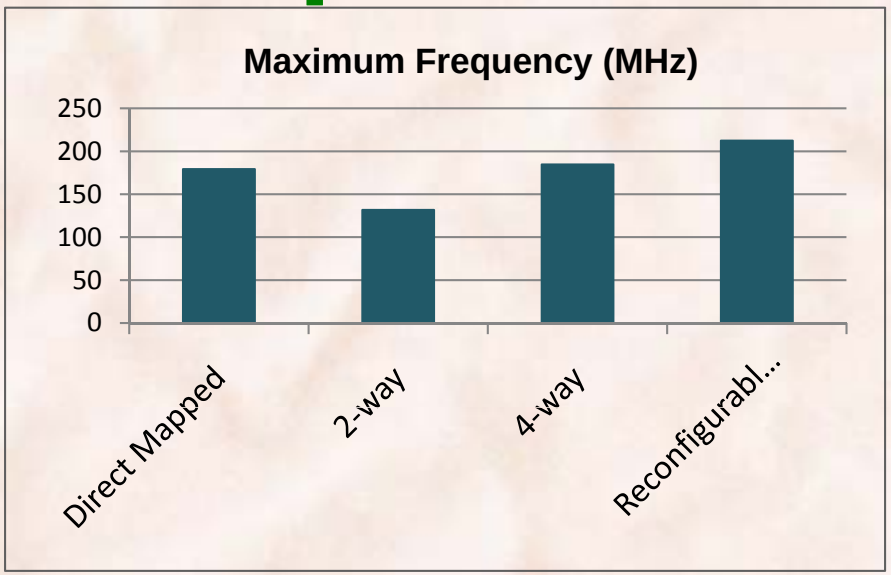
Summary of Reconfigurable Cache Operation

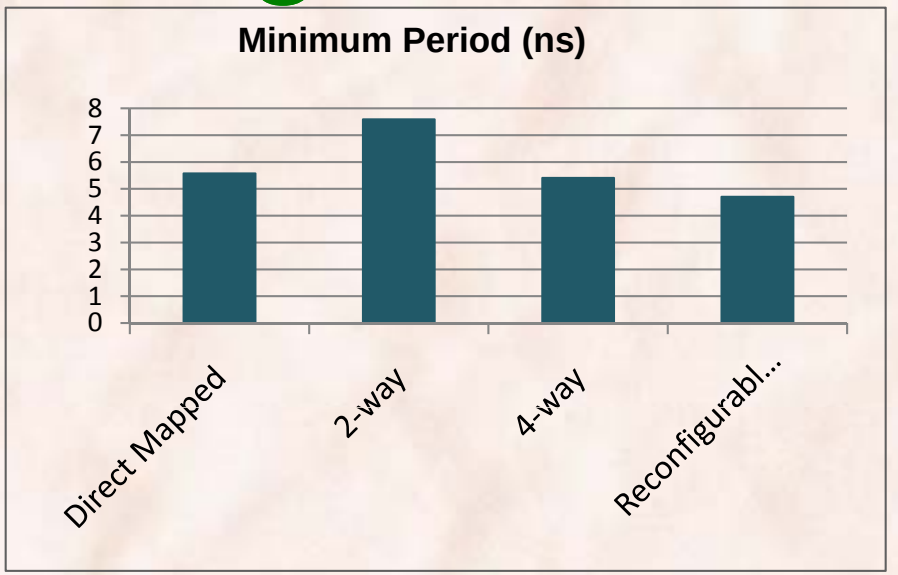
Design Metrics	Direct Mapped	2-Way	4-Way
Mode	00	01/10	11
No. of Access	20	20	20
Read Access	11	11	11
Write Access	9	9	9
Read Hits	2	7	7
Read Miss	9	4	4
Write Hits	2	4	4
Write Miss	7	5	5
Total Hits	4	11	11
Total Miss	16	9	9
Memory Read Time	1,030	730	730
Memory Write Time	945	945	945

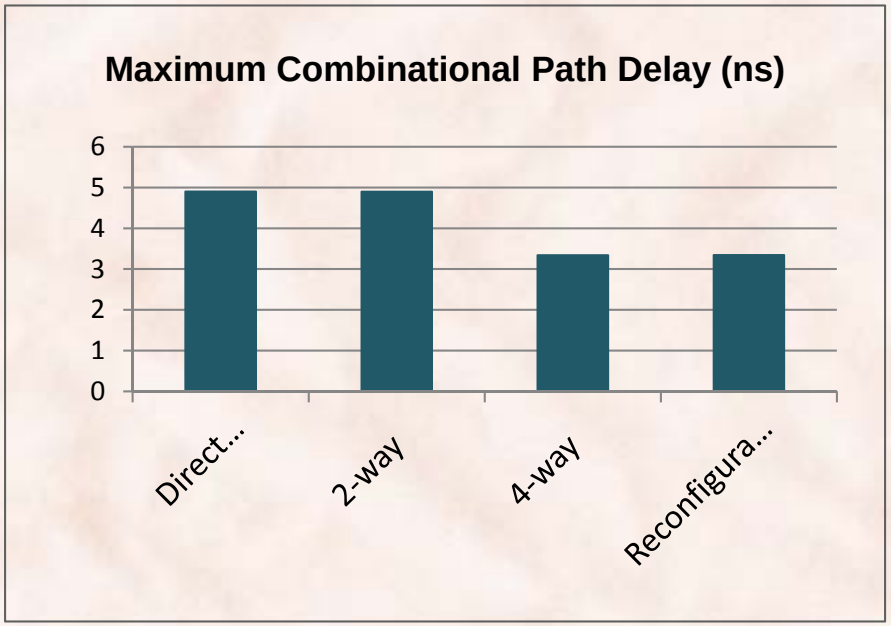
Design Metrics

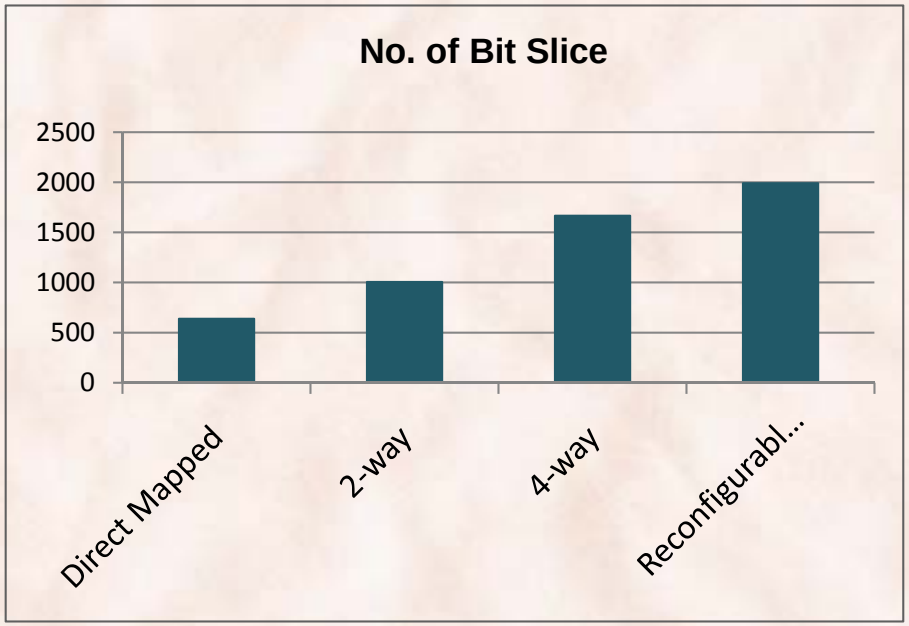
Design Metrics	Direct Mapped	2 Way	4 Way	Reconfigurable Cache
Maximum Frequency (MHz)	154.036	131.683	184.706	212.513
Minimum Period (ns)	6.492	7.594	5.41	4.706
Maximum Combinational Path Delay (ns)	4.901	4.897	3.338	3.342
Cell Usage (BELS)	399	782	1,468	1,888
FlipFlops/Slice Reg	267	530	946	1,228
Slice LUTs	395	776	1,446	1,881
IO Utilization	56	56	56	58
No of Bit Slices	638	1,006	1,666	1,991
Power (mW)	-	-	1,033	1,362
Gate Count	135,952	271,795	280,781	288,986

Comparison of Design Metrics









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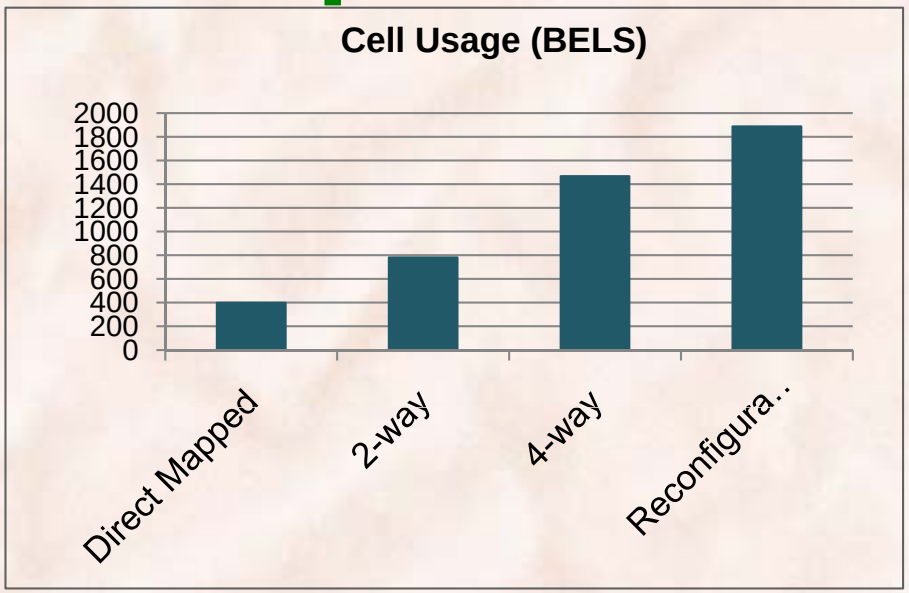

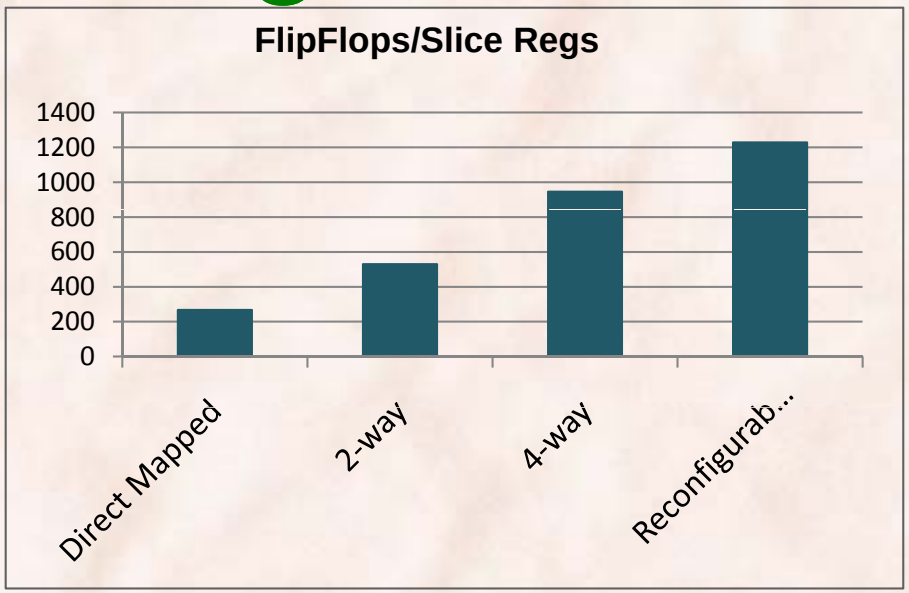

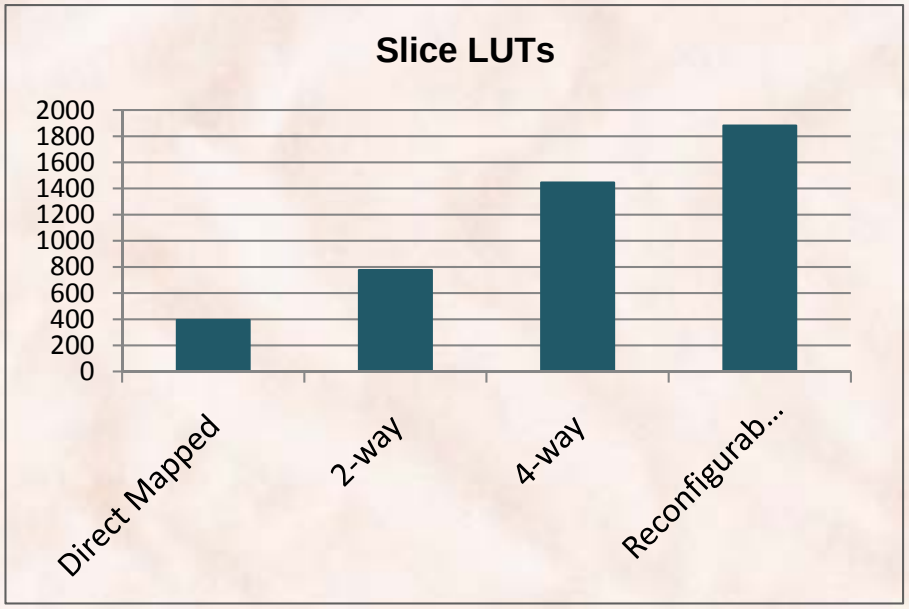

Comparison with existing Research

Name	Multi-function Computing Cache [11]	Way Concatenation Cache [2]	Reconfigurable Memory [16]	Proposed Design
Year	2001	2003	2005	2009
Performance Improvement	Up to factor of 50-60 for computational applications	In terms of Dynamic power reduction		In terms of maximum frequency and combinational delay
Hardware & area overhead	~10-20% of base cache memory	Due to way concatenation and way shutdown circuitry	~15%	Due to mode selector unit
Access Time	Increased by 1.6%	As 4-way	Increased by ~10%	
Associativity/ Configuration		1,2,4-way	Cache, FIFO, Scratchpad	1,2,4-way
Power		Dynamic Power savings up to 40% compared to conventional 4-way	Power Overhead ~10%	Static Power Overhead ~ 20%
Simulation approach		Simple Scalar		ModelSim

Conclusion & Future Research

- The proposed data cache can be configured as direct-mapped, two-way and four-way set-associative cache to fulfill the systems' requirements.
- We propose to improve the performance of Reconfigurable Data Cache by using approximate LRU instead of fair LRU.
- We propose to evaluate the performance of designed module in terms of Hit ratio and access time using real application.


Thank you !!!