Optimization of a $45nm$ CMOS Voltage Controlled Oscillator using Design of Experiments

Gayathri Sarivisetti, Elias Kougianos, Saraju P. Mohanty, Atmaram Palakodety and Anil Kumar Ale
{gs0097, eliask, smohanty, ap0179, aa0222}@unt.edu

VLSI Design and CAD Laboratory (http://www.vdcl.cse.unt.edu)
P.O. Box 311366, University of North Texas, Denton, TX 76203

Abstract

We present a design of experiments (DOE) approach to nanometer design of an analog voltage controlled oscillator (VCO) using CMOS technology. The functional specifications of the VCO optimized in this design are the center frequency and minimization of overall power consumption as well as minimization of power due to gate tunneling current leakage, a component that was not important in previous generations of CMOS technologies but is dominant at $45nm$. Due to the large number of available design parameter (gate oxide thickness and transistor sizes), the concurrent achievement of all optimization goals is difficult. A DOE approach is shown to be very effective and a viable alternative to standard design exploration in the nanometer regime.

1 Introduction and Contributions

Accurate frequency or time reference signals are required practically in every analog, digital or mixed-signal design. Traditionally, Phase-Locked Loops (PLLs) have been used to provide such stable references [1]. One of the basic and important components of a PLL is the Voltage Controlled Oscillator (VCO) [2].

VCO design involves the simultaneous satisfaction of a number of design criteria as well as power optimization, particularly for portable applications. With the introduction of nanometer CMOS processes, geared towards low-power portable designs, an additional leakage mechanism is introduced: gate oxide tunneling current [10].

This mechanism must be carefully accounted for during the design process as it has detrimental effects for both performance and power consumption. As a consequence, the possible factors determining the performance of analog blocks, such as VCOs, increases and makes the exploration of the design space more difficult. We will demonstrate how a Design of Experiments (DOE) approach [7] is a powerful and viable alternative to traditional design methods.

This paper is organized as follows: A VCO design is presented and SPICE simulation results confirm its functionality in Sec. 2. In Sec. 3 we identify the dominant factors for the performance criteria and analyze our DOE approach. Prediction equations are then derived and simultaneously optimized. Finally we conclude in Sec. 4.

We now present related works currently available in the literature. A collection of PLL and VCO designs are presented in [8] while high performance CMOS designs are given by Xu *et al.* in [14] and by Larsson in [5]. Simulation aspects of ring oscillators are examined in [3]. A modern and comprehensive study of design issues for low-power VCOs is given by Zhan *et al.* in [4]. Ring oscillator VCOs are described in [12] and [6].

The contributions of this paper are as follows: 1) we designed a Voltage Control Oscillator using a $45nm$ CMOS process, 2) we identified the primary factors affecting the performance of this design, and, 3) we applied a novel Design of Experiments approach in order to satisfy the design criteria for low-power portable applications.

2 Design of the VCO

The design type of VCO selected for this work is of the "Current Starved" type [9]. This is essentially a ring oscillator, comprised of an odd number of inverters each biased by a complimentary pair of transistors operating as current sources as shown in Fig. 1. The function of the current sources is to limit the amount of current supplied to the inverter (starve the inverter.) An additional pair of transistors acts as an input stage with very large input impedance.

To determine the operating frequency of the VCO, we note that the total capacitance (C_{tot}) on the drains of the inverter transistors is given by the sum of the input (C_{in})

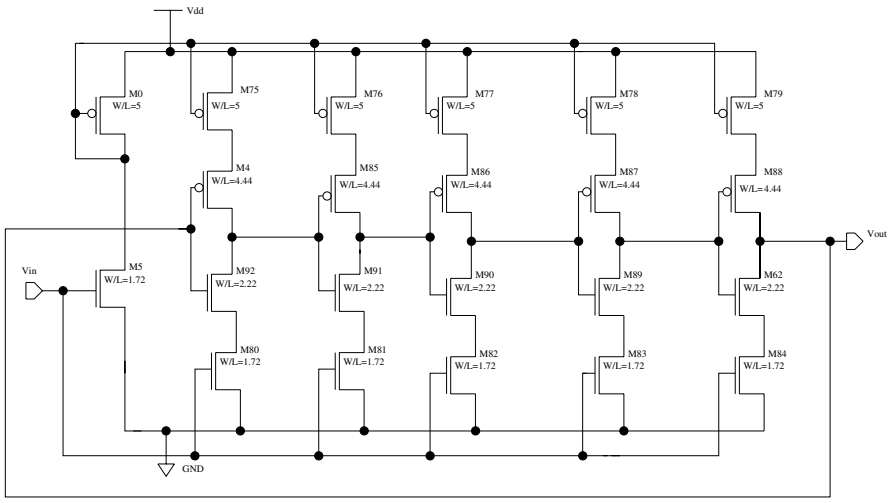


Figure 1: Schematic diagram of the VCO. It consists of: 1) input stage (transistors M0 and M5,) 2) 5 stages of inverters (center transistors) and 3) current starve circuitry (top and bottom transistors.)

and output capacitances (C_{out}) of the inverter:

$$\begin{aligned} C_{tot} &= C_{out} + C_{in} \\ &= C^*_{ox}(W_pL_p + W_nL_n) \\ &\quad + \tfrac{3}{2}C^*_{ox}(W_pL_p + W_nL_n) \\ &= \tfrac{5}{2}C^*_{ox}(W_pL_p + W_nL_n), \end{aligned} \tag{1}$$

where W_n and W_p are the widths of the transistors and L_n and L_p are their lengths. C^*_{ox} is the gate oxide capacitance per unit area.

The total time required to charge and discharge the capacitance of an inverter stage is then given by:

$$T = C_{tot}\frac{V_{dd}}{I_d}, \tag{2}$$

where V_{dd} is the power supply and I_d is the current flowing through the inverter.

If there are N inverters in the oscillator (where N is an odd number,) the frequency of oscillation is given by:

$$f_{osc} = \frac{1}{NT} = \frac{1}{NC_{tot}}\frac{I_d}{V_{dd}}. \tag{3}$$

It is clear from this expression that the frequency of oscillation is dependent not only on the size and number of inverters but is also proportional to I_d which can be controlled via the input voltage V_{in}.

We used the Predictive Technology Model (PTM) [13] $45nm$ BSIM4 models for our design. Simulation results are shown in Fig. 2.

We also present in Table 1 the individual contributions of each transistor in terms of gate leakage and average power consumption. From the table we can see that the total leakage power of the VCO due to gate tunneling is a significant portion (almost 10%) of the total power consumed.

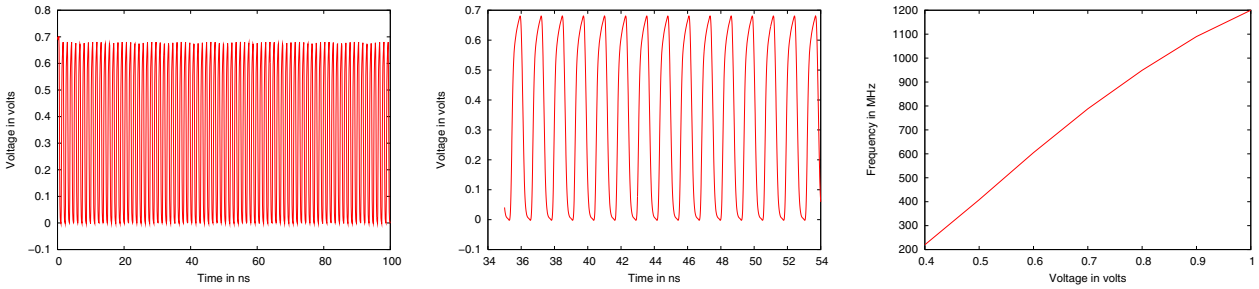
3 Optimization via Design of Experiments

Once a baseline design has been accomplished, we proceeded to optimize its performance. Three basic performance criteria were identified: 1) The frequency response with respect to input voltage (measured by center frequency, achieved when the input voltage is equal to the supply), 2) The total power consumed by the VCO, and 3) The power consumption due to gate tunneling current.

The fundamental parameters under design control are the sizing of the various transistors (W/L ratio) and the oxide thickness (T_{ox}) used in the process. Clearly higher values of T_{ox} will reduce the leakage power but will also reduce the frequency of operation. The optimization problem then becomes quite involved due to the number of variables involved:

- The gate oxide thickness T_{ox}.
- $\beta_1 = W/L$ ratio for the PMOS inverter transistors.
- $\beta_2 = W/L$ ratio for the NMOS inverter transistors.
- $\beta_3 = W/L$ ratio for the PMOS current starve transistors.
- $\beta_4 = W/L$ ratio for the NMOS current starve transistors.

Thus we have 5 input factors and 3 desired responses. In a circuit of small size, an exhaustive exploration of the design space is feasible in a reasonable amount of time. We chose, however, to use a Design of Experiments (DOE) [7] approach in order to demonstrate the power of this method as well as its feasibility, particularly for large circuits.



(a) Output waveform at $V_{dd} = 0.7V$ (b) Magnification of (a) (c) Voltage vs. Frequency response

Figure 2: Functional Verification of the VCO. SPICE simulations were performed for $100ns$ (Figs. a and b.) The input voltage was varied from $0.4V$ to $1.0V$ to obtain the VCO response (Fig. c) while V_{dd} was held at $0.7V$.

Table 1: Gate leakage and dynamic current for individual transistors in the VCO. The input voltage was set at 0.7V.

Transistor type	Transistors	Average Power	Leakage Power	Percentage
Input	PMOS (M0)	12.26uW	33.09pW	0.00027
	NMOS (M5)	4.69uW	4.82nW	0.103
Current Starved	PMOS (M75, M76, M77, M78, M79)	0.215uW	345.5pW	0.159
	NMOS (M80, M81, M82, M83, M84)	0.255uW	30.41nW	0.0193
Inverter	PMOS (M4, M85, M86, M87, M88)	0.912uW	207.07nW	0.715
	NMOS (M92, M91, M90, M89, M62)	0.832uW	95.87nW	0.539
Total		28.02	338.54	9.36

We selected a Taguchi L_8 design matrix [11] and the following upper and lower design limits:

- $1.4nm$ and $1.7nm$ for T_{ox}
- 5 and 10 for β_1 and β_3.
- 1.72 and 3.44 for β_2 and β_4.

The results are shown in Table 2. From the tabular data, Pareto diagrams were generated for the three responses, as shown in Fig. 3. Pareto diagrams are very useful in identifying the dominant factors for a response. Based on the tabular and Pareto results, we obtain the following response equations for our design:

$$f_{osc} = 786.43 - 93.36T_{ox} + 60.3\beta_2, \quad (4)$$

$$P_{av} = 35.05 + 5.7\beta_4 + 3.3\beta_3, \quad (5)$$

$$P_{leak} = 376.35 - 28.58T_{ox} + 29.32\beta_1 + 36.17\beta_2, \quad (6)$$

where the design variables take *coded* values from -1 (corresponding to the lower experimental value) to +1 (corresponding to the upper experimental value.)

From Eq. 4 we see that in order to maximize the frequency of oscillation, T_{ox} must be -1 while β_2 must be +1. Similarly, from Eqs. 5 and 6 we see that average power minimization requires both β_3 and β_4 to be -1. On the other hand, leakage power minimization requires that T_{ox} must be +1 while β_1 and β_2 should be -1. All of these constraints can be satisfied simultaneously with the exception of T_{ox} and β_2. Maximum frequency of oscillation requires thinner oxide but gate leakage requires thicker oxide. Since f_{osc} is the primary design metric we select the value that maximizes it, i.e. $T_{ox} = -1$ and $\beta_2 = +1$.

In terms of actual values we see that $T_{ox} = 1.4nm$, $\beta_2 = 3.44$, $\beta_4 = 1.72$ and $\beta_1 = \beta_3 = 5$ will provide maximum frequency of oscillation, minimum total power consumption and low leakage power due to gate tunneling.

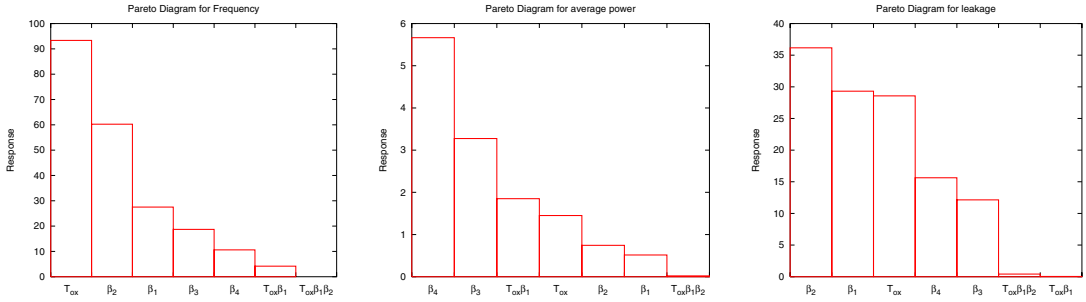
4 Conclusions

We presented a Design of Experiments (DOE) approach for the solution of an optimization problem arising during the design of nanometer CMOS analog components. The effect of the additional gate tunneling leakage component complicates the design by introducing an additional power consumption factor that must be minimized, or, if total minimization is not possible, must be kept low. Instead of pursuing an exhaustive design space exploration, which is typically not feasible in medium and large designs, DOE allows the designer to reduce dramatically the number of required simulations while providing for near-optimal design.

In our test VCO we demonstrated how DOE indicates that the simultaneous maximization of f_{osc} and minimization of

Table 2: Experimental Results. CS refers to the Current Starve transistors.

Run	T_{ox}	$\beta_1 = W/L$ for PMOS CS	$\beta_2 = W/L$ for NMOS CS	$\beta_3 = W/L$ for PMOS Input	$\beta_4 = W/L$ for NMOS Input	Frequency f_{osc} (MHz)	Correlation Coefficient R (%)	Average Power P_{av} (uW)	Leakage Power P_{leak} (pW)
1	1.4	5	1.72	10	3.44	787.91	99.21	46	342.66
2	1.4	5	3.44	5	1.72	925.04	99.28	29.64	408.83
3	1.4	10	1.72	10	1.72	813.78	99.06	32.05	370.58
4	1.4	10	3.44	5	3.44	992.46	98.91	38.29	497.63
5	1.7	5	1.72	5	3.44	630.65	99.85	32.90	310.35
6	1.7	5	3.44	10	1.72	692.12	99.82	29.57	326.29
7	1.7	10	1.72	5	1.72	672.32	99.77	26.25	337.14
8	1.7	10	3.44	10	3.44	777.18	99.81	45.66	417.31



(a) Center Frequency (b) Average Dynamic Power (c) Average Gate Leakage Power

Figure 3: Pareto diagrams showing the effects of various design factors on the center frequency of the VCO (Fig. a,) the total average power consumed (Fig. b,) and leakage power due to gate oxide tunneling (Fig. c.)

P_{leak} are incompatible but provides a solution by minimizing P_{av} instead.

References

[1] R. E. Best. *Phase-Locked Loops, Theory, Design and Applications*. McGraw-Hill, 2nd edition, 1993.

[2] F.Azais, A.Ivanov, M.Renovell, and Y.Bertrand. A Methododlogy and Design for Effective Testing of Voltage-Controlled Oscillators(VCOs). In *Proceedings of the Seventh Asian Test Symposium (ATS'98)*, pages 383–387, 1998.

[3] A. Hajimiri, S. Limotyrakis, and T. H. Lee. Jitter and Phase Noise in Ring Oscillators. *IEEE Journal of Solid-State Circuits*, 34(6):790–804, June 1999.

[4] J.H.C.Zhan, J.S.Duster, and K.T.Kornegay. A Comparative Study of MOS VCOs for Low Voltage High Performance Operation. In *Proceedings of the International Symposium on Low Power Electronics and Design*, pages 244–247, 2004.

[5] P. Larsson. A 2-1600-MHz CMOS Clock Recovery PLL with Low-Vdd Capability. *IEEE Journal of Solid-State Circuits*, 34(12):1951–1960, December 1999.

[6] J. McNeill. Jitter in Ring Oscillators. *IEEE Journal of Solid-State Circuits*, 32(6):201–204, June 1997.

[7] D. C. Montgomery. *Design and Analysis of Experiments*. John Wiley & Sons, Inc., 6th edition, 2005.

[8] B. Razavi. *Monolithic Phase-Locked-Loops and Clock Recovery Circuits*. IEEE Press, 1996.

[9] D. E. R.Jacob Baker, Harry W.Li. *CMOS Circuit Design, Layout, and Simulation*. IEEE Press, 1998.

[10] K. Roy, S. Mukhopadhyay, and H. M. Meimand. Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits. *Proceedings of the IEEE*, 91(2):305–327, Feb. 2003.

[11] R. K. Roy. *A Primer on the Taguchi Method*. John Wiley & Sons, Inc., 1990.

[12] S.Joeres, A.Kruth, O.Meike, G.Ordu, S.Sappok, R.Wunderlich, and S.Heinen. Design of a Ring-Oscillator with a Wide Tuning Range in 0.13um CMOS for the use in Global Navigation Satellite Systems. *Proceedings ProRISC*, pages 529–535, 2004.

[13] P. T. M. P. website. http://www.eas.asu.edu/ ptm/.

[14] C. Xu, W. Sargeant, K. R. Laker, and J. van der Spiegel. An Extended Frequency Range CMOS Voltage Controlled Oscillator. In *Proceedings of the IEEE International Conference on Electronics, Circuits and Systems*, pages 425–428, 2002.