Compact Behavioral Modeling and Time Dependent Performance Degradation Analysis of Junction and Doping Free Transistors

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***Abstract*—The junctionless as well as dopingless field effect transistor (JLFET) can be a potential candidate for future CMOS technology due its innate properties, such as simplified fabrication process, low thermal budget and better immunity towards process variations. In this paper, time dependent performance degradation (or temporal variations due to silicon aging) of Common Source (CS) amplifier designed with conventional and dopingless JLFETs has been investigated for channel hot carrier (CHC) stress under different time spans. The time dependent performance degradation of both devices was compared at device as well as circuit level. The compact behavioral Verilog-A models of both devices have been developed that capture the DC as well as transient behavior accurately for circuit level analysis. From our proposed device-circuit co-simulations approach, we observed that the voltage gain of a CS amplifier based on conventional JLFET is degraded by 20.2% and 32.6% due to CHC stress of 2000 seconds and 6000 seconds, respectively. However, the dopingless JLFET experiences 8.5% to 13.2% degradation for the same time span. Similarly the phase shift, output resistance and transconductance of the CS amplifier are also degraded due to CHC stress for JLFET more severely than dopingless JLFET.**

***Keywords*—Dopingless FET, Junctionless FET, Channel Hot Carrier (CHC), Verilog-A Models, CS amplifier.**

I. Introduction

The ever increasing need for energy-efficient and high-performance systems has driven the device scaling trends for last few decades [1]–[3]. As a result, nanoscale devices with shrinking dimensions as well as different architectures have been explored for design of energy-efficient and fast integrated circuits and systems. The junctionless field effect transistor (JLFET) has emerged as a strong candidate to replace the conventional metal oxide semiconductor field-effect transistor (MOSFET) due to its simplified fabrication process, adequate current-driving capability to meet modern requirements, and better immunity to short-channel effects (SCEs) [4]. However, innate properties of the JLFET such as high gate work function metal requirement to deplete the heavily doped channel, and impact ionization phenomenon due to high electric field in the channel near the drain region causes time dependent performance degradation. This high electric field generates energetic electrons and holes that get injected into the gate dielectric near to drain region, hence it causes interface states. As a result, the electrical characteristics of these devices are degraded [5]. In order to minimize the electric field in the channel near the drain region, the concept of junction as well as doping free transistors was introduced [6]–[8] that employs reduced gate work function metal electrode. This results in improved performance even in presence of channel hot-carrier (CHC) stress.

The time dependent performance degradation due to CHC stress in n-type JLFET has also been investigated and experimentally found less sensitive than conventional inversion mode MOSFETs [9], [10]. JLFETs have been studied mostly via device numerical simulation employing technology computer-aided design (TCAD) or experimentally [11], and a multitude of efforts have been made using TCAD to capture the aging behavior of specific degradation mechanisms, such as hot carrier injection [12]. Analytical models have also been developed to investigate the hot carrier effect (HCE) in terms of threshold voltage variations for the junctionless transistor [13], [14]. But there is no study that provides a comparative perspective of dopingless JLFET [6] with conventional JLFET [15]. Moreover, it is a challenging task to accurately characterize the time dependent performance degradation at device level and predict its impact at circuit level. In another work by the authors of this paper [16], the performance of digital circuits (ring oscillator and SRAM) based on junction- and doping-less FETs under CHC stress was presented. Also the concept of compact behavioral models of these devices and incorporation of CHC stress was introduced. In contrast, in this paper we have investigated the performance of both devices under CHC stress specifically for 'analog circuits', as these circuits are more vulnerable. For circuit level analysis, we have also developed behavioural Verilog-A compact models for both devices that allow computationally efficient circuit simulations with good convergence and accuracy. These models are elaborated along with device-circuit co-simulation approach, and how CHC stress can be incorporated with them.

The dopingless (DL) JLFET has recently attracted the attention of the research community as a potential candidate that relaxes the requirements of high work function of gate metal electrode and heavy doping throughout the source, channel and drain regions, while all the innate benefits of conventional JLFETs are preserved. The DL-JLFET employs intrinsic silicon nanowire, whereas the source and drain regions were

formed through charge-plasma [17], thereby it provides better immunity towards process variation induced random dopant fluctuations (RDFs) [6]–[8]. For time dependent performance degradation due to CHC stress at device and circuit level, we have adopted the device-circuit co-simulation approach for both conventional JLFET (junction free device with heavy doping) and DL-JLFET (free from external doping as well as junctions). We have considered the most damaging CHC condition for short-channel devices when V_G = V_D at room temperature, however long-channel devices experience the same phenomena severely when V_G = $V_D/2$ [18].

The remainder of the paper is organized as follows. Section II, describes the schematics of both previously reported devices under CHC and their TCAD simulation parameters, and dimensions. The device-circuit co-simulation approach and development of behavioral Verilog-A model for both devices are described in Section III. Section IV discuss how time dependent performance degradation (i.e. CHC stress) was modeled and incorporated at device and circuit level simulations. Section V describes the mathematical small signal model of CS amplifier considered for analysis under CHC stress and its performance parameters. Finally, Section VI concludes the finding of this study and future guidelines.

II. Device Structures and Simulation Parameters

Cross-sectional schematics of both conventional and dopingless JLFETs under CHC stress are shown in Fig. 1(a-b). The TCAD simulation parameters and dimensions of both devices are kept same as that of conventional JLFET excluding doping concentrations and gate work functions. The device dimensions and other simulation parameters are as follows [16]: gate length (L_g) = 15nm, silicon film thickness (T_{si}) = 10nm, effective oxide thickness (EOT) = 1nm, and S/D extension (L_{ext}) = 15nm. The gate electrode metal work function for conventional JLFET with uniform doping ($10^{19}cm^{-3}$) throughout source–channel–drain regions is 5.5eV [6]. For DL-JLFET, the gate electrode metal work function with intrinsic silicon body ($10^{15}cm^{-3}$) is assumed as $4.73eV$ in this current paper. In DL-JLFETs, the doped source/drain regions are formed with different metal electrodes with work functions which is in the range of ϕ_m < χ_{Si}+(E_G/2q). In this expression, χ_{Si} is the electron affinity of bulk silicon has a value of 4.17, E_G is the bulk silicon bandgap, and q is the elementary charge. The device thickness is chosen in such a manner that the thickness of the silicon body should be less than the Debye length L_D=$\sqrt{(\epsilon_{Si}\upsilon_T/qN)}$, where, ϵ_{Si} is the dielectric constant of the intrinsic silicon, N is the carrier concentration in the bulk intrinsic silicon and υ_T is the thermal voltage. Therefore, a Hafnium metal contact with a work function of $3.9eV$ is used to create the source and drain region with silicon layer thickness of $10nm$. We have introduced new schematic symbols for both p-type and n-type dopingless and junctionless transistors, as shown in Fig. 2.

The conventional and dopingless JLFETs are simulated using the Silvaco ATLAS device simulator with default parameters of silicon [19]. Shockley-Read-Hall (SRH) and Auger recombination models have been incorporated to account for minority carrier recombination. The Lombardi mobility model (CVT) has been considered because it gives accurate results with large temperature ranges. The Energy Balance Transport model (EBT) is included for non local transport effects. The hot electron injection model is used to analyze the impact of HCE on the device performance. We have also considered the FLDMOB model for high field velocity saturation depending on parallel electric field in the direction of current flow. For analyzing the impact of higher doping concentration, the bandgap-narrowing (BGN) model has also included. Similarly for analyzing the device degradation (shift in threshold voltage, degradation of transconductance and other parameters) the device degradation model (DEVDEG) is enabled.

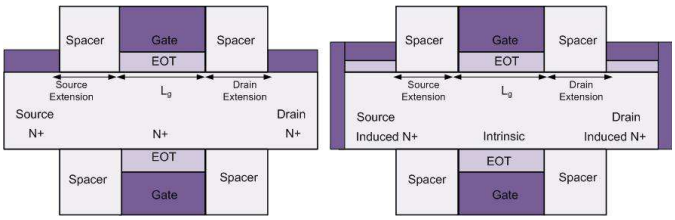

Fig. 1. Cross-sectional views of devices under test for CHC stress (a) conventional JLFET [15], and (b) dopingless JLFET [6].

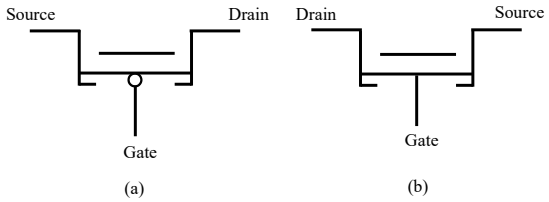

Fig. 2. Schematic symbols for dopingless and junctionless transistor (a) p-type, and (b) n-type.

III. Simulation Framework and Model Description

Fig. 3(a) shows the compact behavioral model developed in Verilog-A. Here a JLFET is formed as a three-terminal device (source, gate, and drain) and current is supposed to flow only between source and drain. Gate leakage is insignificant with high-κ gate dielectrics. Since the drain current is a function of gate-to-source and drain-to-source voltages, the drain current is modeled as a voltage dependent current source. Furthermore, the voltage-dependent gate-to-drain capacitance (C_{GD}) and gate-to-source capacitance (C_{GS}) are also included in the model to observe the capacitive effect during transient simulations. These capacitances resemble fringing capacitances which are located inside the device and overlap capacitances between gate-to-drain and gate-to-source, respectively. The charge of source (Q_S) and drain (Q_D) terminals is also calculated with respect to terminal voltages and capacitances, respectively. The developed approach preserves the charge conservation during transient analysis. Therefore, both transient and DC characteristics of JLFETs can easily be captured from this model.

Fig. 3(b) shows the framework of device-circuit co-simulation approach, where electrical characteristics ($I-V$ and $C-V$) of both devices were extracted using two dimensional TCAD tool for bias conditions varying finely over a wide operating range. The extracted electrical characteristics from the TCAD simulator were used to produce two-dimensional

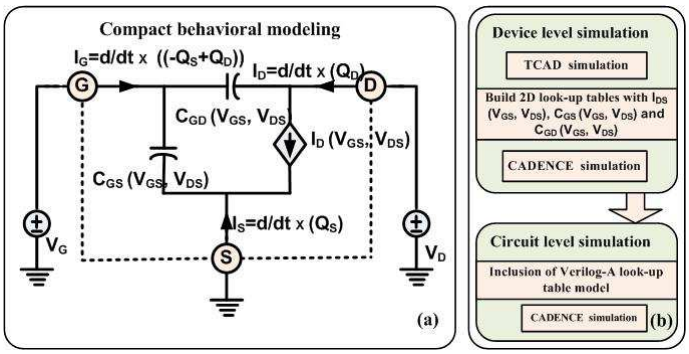

Fig. 3. Device-circuit co-simulation approach (a) compact behavioral model for conventional and dopingless JLFETs, and (b) TCAD (ATLAS) device and Cadence (circuit) co-simulation framework.

look-up tables. These tables include $I-V$ and $C-V$ data extracted from transfer characteristics of drain current I_{DS}, gate to source capacitance C_{GS} and gate to drain capacitance C_{GD} as functions of (V_{GS}, V_{DS}) across a wide range of operating voltages through DC and small-signal simulations. Hence, the developed Verilog-A models for both devices are capable of capturing both DC and transient characteristics accurately. We have calibrated our Verilog-A models with TCAD simulations and reproduced the previously reported transfer characteristics of both conventional JLFET and DL-JLFET, as shown in Fig. 4(a-b). It can be observed that the developed Verilog-A models for both n- and p-type, JLFET and DL-JLFET show very good agreement with TCAD simulations.

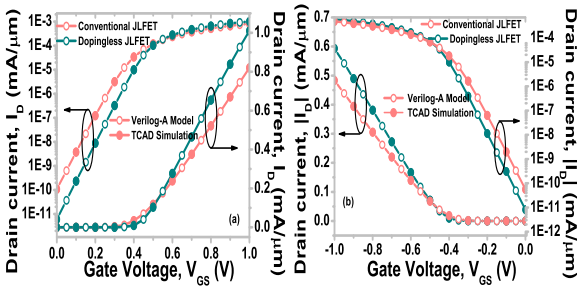

Fig. 4. Calibration of Verilog-A models (open symbols) with TCAD simulations (solid symbols) for transfer characteristics of both conventional (JLFET) and dopingless (DL-JLFET) devices (pre-CHC) at V_{DS}= $\pm 1V$ (a) n-type device, and (b) p-type device.

The assessment of capacitive behavior of JLFET is also important for the development of a precise device model. Hence, the capacitive components (C_{GS}, C_{GD}) of both devices are presented as a function of gate bias voltage, as shown in Fig. 5. These capacitive components are extracted at V_{DS} = 1V with small signal ac frequency of 1MHz. Generally, the capacitive component of devices depends on the operating region. In the linear region, the capacitive components of JLFETs are equally distributed between drain and source. In the saturation region, a large amount of capacitance appears between gate to source and a small amount of overlap capacitance exist between gate to drain. This C_{GD} is lower in JLFETs because electron depletion is much higher near the drain side of the channel when V_{DS} increases. Also, in some cases, C_{GD} can be zero or even negative in a JLFET due to low drain induced barrier lowering (DIBL) effect, hence, it exhibits very low Miller capacitance. Further, we observed that the gate-to-drain capacitance (i.e., Miller capacitance) in the conventional JLFET is larger in comparison with the DL-JLFET. This happens because the gate to drain capacitance of a conventional JLFET is highly influenced by the variation in drain to source potential and thereby produces undesirable artifacts in the switching behavior of the conventional JLFET which are not present in the DL-JLFET. Also, The enhanced Miller capacitance in conventional JLFET induces voltage spikes during circuit switching, which may increase power consumption.

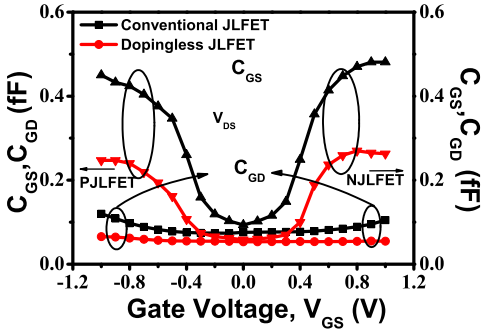

Fig. 5. Gate to source (C_{GS}) and gate to drain capacitance (C_{GD}) as a function of gate voltage for n and p-type dopingless and conventional JLFETs at V_{DS}= 1.

IV. Time Dependent Performance Degradation

Fig. 6(a) shows the block diagram of time dependent CHC stress simulation set-up and how the CHC stress mechanism is incorporated at circuit level simulations. For evaluation of CHC stress, we have applied the stress voltage higher than the nominal stress voltage, therefore the most damaging CHC stress condition at room temperature for short channel transistors has been considered: V_G=V_D=1.9V for 2000 sec. and 6000 sec. Fresh and degraded device characteristics were estimated by the cumulative measure-stress-measure approach [20]. The output characteristics of both fresh (pre-CHC stress) and stressed (post-CHC stress) devices were simulated by including fresh and degraded device models in Verilog-A. The drain current variation was monitored by sweeping the drain voltage with various values of gate bias voltage. Here, the CHC stress is measured by applying voltage to the gate and drain terminals with the source terminal grounded, as shown in Fig. 6(b) by the simulation setup of the stressed device. It also shows that the most damaging CHC stress is located close to the drain side.

The output characteristics of conventional and dopingless JLFETs under hot carrier stress (V_G = V_D = 1.9 V for 2000 sec. and 6000 sec.) were obtained from TCAD simulations (solid symbols), as shown in Fig. 7(a-d). For Verilog-A models (open symbols), we have followed the same look-up table based approach in which the resulting stressed device electrical characteristics ($I-V$ and $C-V$) were incorporated, as shown in Fig. 7(a-d). It can be observed that the Verilog-A models follow the TCAD simulations very closely for both fresh and stressed devices. For CHC stress of 2000 sec., the conventional JLFET experiences drain current degradation of

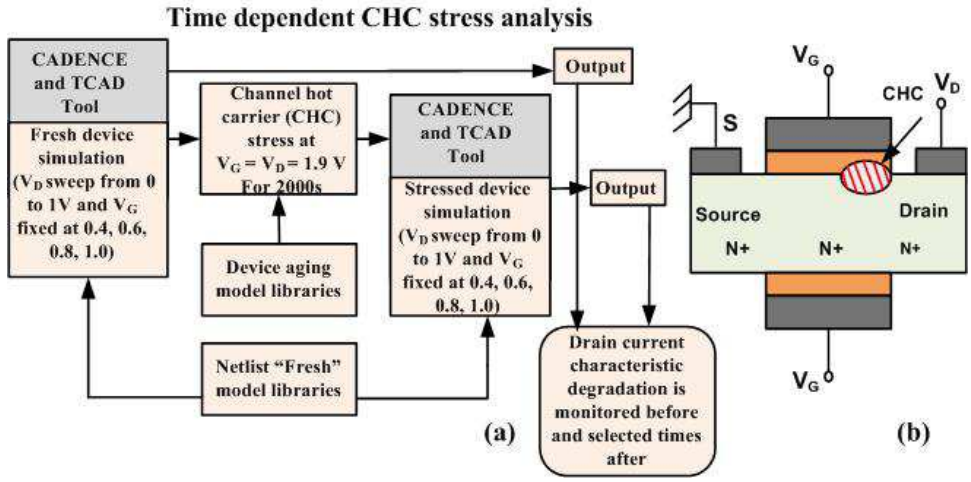

Fig. 6. Time dependent CHC stress (a) analysis, and (b) simulation set-up, showing CHC effect near drain side.

20.5 % in contrast to dopingless JLFET of 10.4% for V_G = V_D = 1.9 V, as shown in Fig.7 (a-b). Degradation in drain current for both devices mainly occurs due to shift in threshold voltage under CHC stress. However, for lower gate biases both devices experienced less degradation in drain current which is consistent as well as in line of applied electric field.

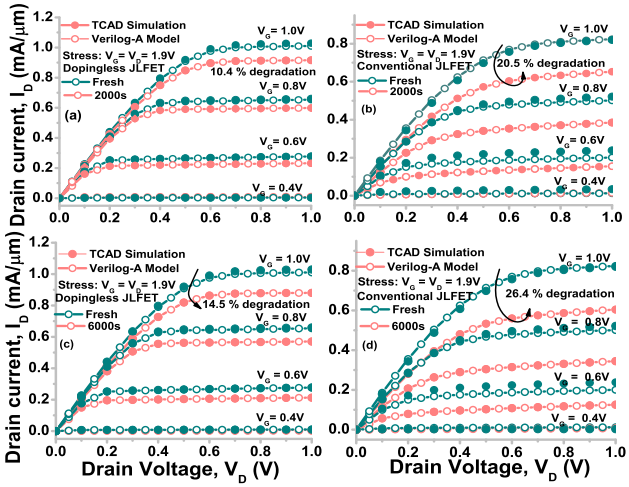

Fig. 7. Output characteristics of conventional and dopingless n-type JLFETs fresh and stressed (V_G = V_D = 1.9V) for 2000 seconds (a-b), and 6000 seconds (c-d).

The time dependent degradation in drain current due to CHC stress was also observed for 6000 sec., where drain current degradation was slightly higher for both devices, as shown in Fig. 7(c-d). From these transfer characteristics, it can be inferred that the conventional JLFET experiences higher degradation due to CHC stress as compared to its counterpart dopingless JLFET. Higher degradation of drain current in conventional JLFET is due to highly doped channel and high gate work function metal electrode that causes injection of abundant carriers in the drain side oxide region. As a result, a significant shift in threshold voltage occurs. However, degradation in the drain current of DL-JLFET is comparatively low due to intrinsic channel and lower gate work function of the metal electrode which leads to reduction in electric field and thereby ensures high reliability against impact ionization and hot carrier effects. Further, it can be seen from Fig. 8(a-b) that the threshold voltage increases with increasing drain voltage and stress time. This may be due to increased density of interface states which increase the threshold voltage of a device, with drain current degraded. Reduction in mobility of the electrons in the channel in DL-JLFET is lower than the conventional JLFET due to lower electric field, hence, fewer amount of interface charges are generated at interface and there is less mobility degradation in channel.

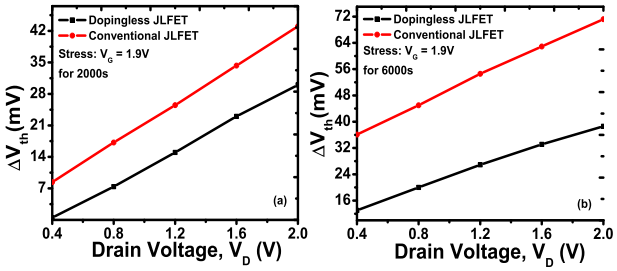

Fig. 8. The threshold voltage degradation of the conventional and dopingless JLFETs under V_G = 1.9 V and various V_D for 2000s (a), and 6000s (b).

V. CS Amplifier Performance

From the previous simulations and observations, it can be inferred that the time dependent CHC stress degrades the conventional JLFET drain current more severely than the dopingless JLFET. Projection of this device level degradation to circuit level may be difficult, so we have developed compact behavioral model of these devices that accurately capture the device behavior and characteristics. This approach is computationally efficient having good convergence and accuracy, and allows simulation of complex circuits. We have considered an analog benchmark circuit for evaluating both devices' performance under CHC stress of different time spans. The standard common-source amplifier circuit realized with conventional and dopingless JLFETs is shown in Fig. 9(a) along with other circuit components. For analytical study,

the small signal equivalent model of the same common-source amplifier is shown Fig. 9(b). Generally, the frequency response or performance of FET based circuits depends on the transconductance g_m and the output resistance r_o derived from the transfer characteristics of a FET. Therefore, small-signal parameters of a JLFET are calculated for different bias voltages and drain currents which can be expressed by:

$$g_m = \Delta I_D / \Delta V_{gs}; r_o = \Delta V_{ds} / \Delta I_{ds} \tag{1}$$

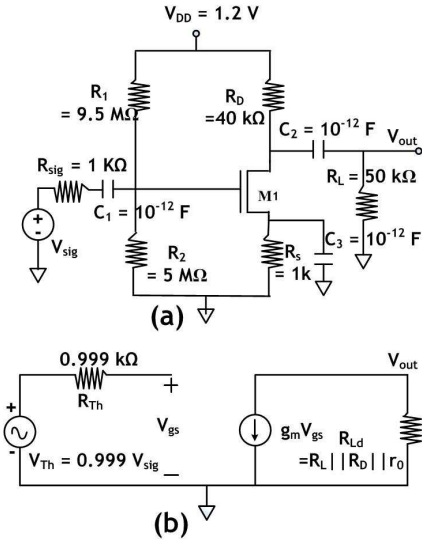

Fig. 9. (a) Common source amplifier circuit using bypass capacitor, and (b) small signal model for dopingless and conventional JLFETs

Fig. 9(b) shows the small-signal model of the CS amplifier where the drain current is represented as a function of the gate-source voltage (voltage-dependent current source) which is equal to $g_m\ V_{gs}$. As drain current also varies with drain to source voltage, this effect can be modeled by a voltage dependent current source which should have linear dependency on voltage across it, hence can be denoted as a linear resistor (r_o). The terminal characteristics of a CS amplifier can be obtained by its input resistance, voltage gain and output resistance. At the outset we observe that this amplifier is unilateral. Therefore, R_{in} does not depend on R_L. So, the input and Thevenin equivalent resistances of the small signal circuit are expressed by:

$$R_G = R_{in} = R_1 \parallel R_2; R_{th} = R_{sig} \parallel R_G \tag{2}$$

From the output side of the small signal circuit

$$V_{out} = -g_m V_{gs}(r_o \parallel R_D \parallel R_L), \tag{3}$$

while at the input,

$$v_{th} = V_{gs}. \tag{4}$$

Substituting (4) into (3), we find the partial voltage gain:

$$A_v = \frac{V_{out}}{V_{th}} = -g_m(r_o \parallel R_D \parallel R_L) \tag{5}$$

From equation (5), the overall small signal voltage gain can also be written as:

$$G_v = \frac{V_{out}}{V_{sig}} = \frac{V_{th}}{V_{sig}} \frac{V_{out}}{V_{th}} = \frac{V_{th}}{V_{sig}} A_v \tag{6}$$

Applying voltage division at the input of the small signal equivalent circuit,

$$v_{th} = \frac{R_{in}}{R_{in} + R_{sig}} v_{sig} = \frac{R_G}{R_G + R_{sig}} v_{sig} \tag{7}$$

Substituting (7) into (6) and using (5), we find the overall small signal voltage gain:

$$G_v = -\frac{R_G}{R_G + R_{sig}} g_m(r_o \parallel R_D \parallel R_L) \tag{8}$$

From the above expressions, we find the small-signal parameters such as small-signal gain, transconductance and output resistance of both devices under pre- and post-CHC stress for 2000s. It is observed that the time dependent CHC stress degrades the small-signal parameters of conventional JLFET based CS amplifier more severally than the CS amplifier based on dopingless JLFET. From Fig. 10(a-b), the dopingless JLFET based CS amplifier experiences 8.5-13.2% degradation in voltage gain, whereas, the voltage gain of CS amplifier based on conventional JLFET is degraded by 20.2-32.6% for CHC stress of 2000s and 6000s. Similarly, the phase shift, transconductance and output resistance of the CS amplifier are also degraded by CHC stress condition. The degradation in voltage gain is mainly caused by change in transconductance and output resistance of CS amplifier.

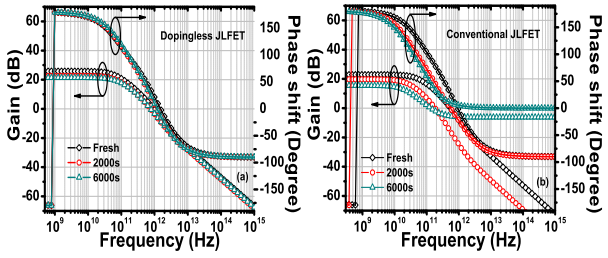

Fig. 10. Gain and phase shift response of (a) Dopingless, and (b) conventional JLFET based common source amplifier under CHC stress of V_G = V_D = 1.9 V for 2000 and 6000s.

TABLE I. PERFORMANCE PARAMETERS OF CS AMPLIFIER UNDER CHC STRESS REALIZED WITH CONVENTIONAL AND DOPINGLESS JLFETS.

Stress conditions	Devices (JLFETs)	Parameters			
		A_V (dB) Simulated	G_V (dB) Analytical	r_o ($K\Omega$)	g_m (mS)
Without stress	Conventional JLFET	22.8	21.4	44.7	0.78
	Dopingless JLFET	25.8	25.6	45.9	1.28
With 2000s	Conventional JLFET	18.2	16.7	39.5	0.48
	Dopingless JLFET	23.6	23.3	44.5	0.99
With 6000s	Conventional JLFET	15.4	11.8	36.7	0.25
	Dopingless JLFET	22.40	21.8	43.7	0.86

Other performance parameters of CS amplifiers realized with conventional and dopingless JLFET are summarized in Table I. Analytically, we also estimated the overall gain from Eqn (8) under pre- and post-CHC stress of 2000s and 6000s which shows good consistency with simulation results. It can be inferred that there is no significant change in transconductance and output resistance of dopingless JLFET based CS amplifier as compared to conventional JLFET based CS amplifier. Further, from transient simulations shown in Fig. 11(a-b), it can be observed that the dopingless JLFET based CS amplifier provides better amplification due to lower degradation caused from CHC stress as compared with conventional JLFET based CS amplifier.

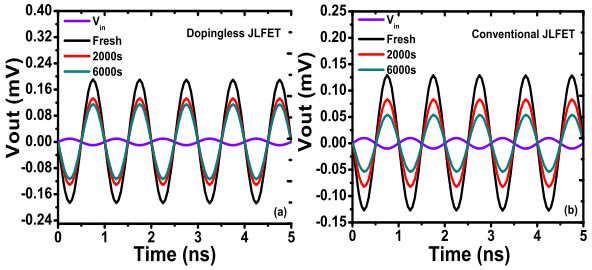

Fig. 11. Timing response of (a) dopingless, and (b) conventional JLFET based common source amplifier under CHC stress for 2000s and 6000s.

VI. Conclusions and Future Research

It is evident from this research that time dependent CHC stress causes significant drain current degradation in conventional JLFET as compared to its counterpart dopingless JLFET. Hence, temporal variation due to silicon aging may also causes reliability concerns for circuits and systems based on emerging (doping- and junction-less) devices. To incorporate the temporal variations due to stres or aging, developed compact behavioral models are presented that offer a computationally efficient and accurate way to translate the device level performance degradation to circuit level. It is clearly observed from the TCAD as well as Verilog-A simulations that the initial phase (e.g. 2000 seconds) of CHC stress is more crucial than the longer one (e.g. 6000 seconds) for both devices and circuits. The proposed model can be used to estimate the drain current degradation due to CHC effects and its effect at circuit level performance. Further, the outcome of our work at device and circuit level may provide incentives and guidelines for further exploration of dopingless JLFETs.

For future research work, temporal process variations of these devices may also be exploited for designing the physical unclonable function (PUFs) as security primitives. These circuits have the potential of generating unique signatures that can be used for authentication or secure communication of interconnected platforms such as the internet of things (IoT).

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