Curriculum Vitae
Saraju P. Mohanty

CONTACT INFORMATION

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RESEARCH INTERESTS

My research is on Smart Electronic Systems, the backbone of which is a combination of AI/ML, Data Analytics, Security at the Edge of IoT (not just at the Cloud of IoT) in the Cyber-Physical Systems (CPS) that make the smart cities. The key aspects of the smart electronics are Energy-Smart, Security-Smart, and Response-Smart. Energy-Smart ensures that energy consumption of electronic-systems is minimal for longer battery life and reduced energy costs. Security-Smart deals with the security/protection of electronics systems as well as that of the information/media that these systems capture, process, or store. Response-Smart refers to accurate sensing, intelligent processing (Data Curation and Analytics), and fast decision/actuation/response (based on the AI/ML Models). My *Smart Electronic Systems research can be grouped into the following inter-related thrusts*:

- Security and Energy Aware Cyber-Physical Systems (CPS)
- IoT-based Approaches for Smart Healthcare and Smart Agriculture
- IoT-enabled Consumer Electronics for Smart Cities and Smart Villages

PROFESSIONAL PREPARATION

Institutes	Major	Degree	Year
University of South Florida Tampa, USA	Computer Science and Engineering *Dissertation*: Energy and Transient Power Minimization During Behavioral Synthesis. *Advisor*: Prof. N. Ranganathan.	Ph.D.	2003
Indian Institute of Science Bengaluru, India	Systems Science and Automation (currently rebranded as Artificial Intelligence program) *Thesis*: Watermarking of Digital Images. *Advisor*: Prof. K. R. Ramakrishnan.	M.E.	1999
Orissa University of Agriculture and Technology Bhubaneswar, India	Electrical Engineering *Project*: Study of the Effects of High-Voltage on Communications & Biological Systems. *Advisor*: Prof. B. Sahu.	B.Tech. (Honors)	1995

APPOINTMENTS

Year	Position	Institutes
June 2015 - Present	Professor (Tenured)	Computer Science and Engineering, University of North Texas
April 2015 - Aug 2017	Technical Consultant	Chen Malin LLP, Dallas, TX 75201.
June 2010 - May 2015	Associate Professor (Tenured)	Computer Science and Engineering, University of North Texas
Sep 2004 - May 2010	Assistant Professor	Computer Science and Engineering, University of North Texas
Jan 2000 - Dec 2003	Instructor / TA	Computer Science and Engineering, University of South Florida
Aug 1996 - Apr 1997	Trainee Manager	Orissa Mining Corporation, India
Aug 1995 - July 1996	Adjunct Lecturer	Orissa University of Agriculture and Technology, Bhubaneswar

HONORARY POSITIONS

1. Distinguished Adjunct Professor, International Institute of Information Technology, Naya Raipur (IIIT-NR), India, 2023–Present.
2. Adjunct Faculty, Malaviya National Institute of Technology Jaipur (MNIT), India, 2023–Present.
3. Honorary Visiting Professor, Oriental University, Indore (OUI), India, 2017–Present.

AWARDS and HONORS

1. Best Paper Award at the 7th International Conference on Data Analytics and Cyber Security (DACS), 2024.
2. Best Paper Award at the 21st OITS International Conference on Information Technology (OCIT), 2023.
3. Best Research Demo Session Paper Award at the 9th IEEE International Symposium on Smart Electronic Systems (IEEE-iSES), 2023.
4. Best Research Demo Session Paper Award at the 6th IFIP International Internet of Things Conference (IFIP-IoT), 2023.
5. Best Paper Award at the 20th OITS International Conference on Information Technology (OCIT), 2022.
6. Fulbright Specialist Award by the Bureau of Educational and Cultural Affairs of U.S. Department of State in 2021.
7. Editor-in-Chief (EiC), IEEE Consumer Electronics Magazine (MCE), 2016–2021.
8. Member of Board of Governors (BoG), IEEE Consumer Electronics Society (CESoc), 2019–2021.
9. IEEE Computer Society Best Paper Award Runner-Up, IEEE Transactions on Sustainable Computing for 2021.
10. Best Paper Award at the 19th OITS International Conference on Information Technology (OCIT), 2021.
11. IEEE Consumer Technology Society Best Paper Award (Second Place), IEEE Consumer Electronics Magazine (MCE) for 2020.
12. IEEE Consumer Electronics Society Outstanding Service Award in 2020 for leadership contributions to the IEEE Consumer Electronics society.
13. IEEE Consumer Electronics Society Chester Sall Award in 2020 for the Second place best paper in the IEEE Transactions on Consumer Electronics.
14. Best Paper Award at the 21st International Symposium on Quality Electronic Design (ISQED), 2020.

15. Top 2% Scientist List, PLOS Biology, https://doi.org/10.1371/journal.pbio.3000384, August 2019.
16. Best Paper Award (Third Place) at the 5th IEEE International Symposium on Smart Electronic Systems (iSES), 2019.
17. Best Paper Award at the 37th IEEE International Conference on Consumer Electronics (ICCE), 2019.
18. Founding Editor-in-Chief (EiC), IEEE-CS-TCVLSI VLSI Circuits and Systems Letter (VCAL), 2015–2018.
19. IEEE Consumer Electronics Society Best Paper Award (First Place), IEEE Consumer Electronics Magazine (CEM) for 2018.
20. IEEE Consumer Electronics Society Best Paper Award (Second Place), IEEE Consumer Electronics Magazine (CEM) for 2018.
21. IEEE Distinguished Lecturer by the Consumer Electronics Society (CESoc) in 2017.
22. Ex-Officio Member of Board of Governors, IEEE Consumer Electronics Society, 2017–2018.
23. IEEE-CS-TCVLSI Distinguished Leadership Award for services to the IEEE, and to the VLSI research community in 2018.
24. IEEE-CS Certificate of Recognition for dedicated services to VLSI community in 2018.
25. Chair, IEEE-CS Technical Committee on Very Large Scale Integration (TCVLSI), 2014–2018.
26. Glorious India Award - Rich and Famous NRIs of America for exemplary contributions to the discipline in 2017.
27. Society for Technical Communication (STC) Award of Merit for outstanding contributions to the IEEE Consumer Electronics Magazine (CEM) in 2017.
28. The PROSE Award for best Textbook in Physical Sciences & Mathematics category from the Association of American Publishers (AAP) in 2016.
29. The UNT Toulouse Scholars Award for outstanding scholarship and teaching achievements in 2016-2017.
30. Distinguished Alumnus Award from the Government College of Engineering and Technology, Bhubaneswar, India in 2016.
31. Best Poster Award (First Place with a cash prize of $1000) at the 31st IEEE MetroCon Conf., 2018.
32. Best Poster Award (Second Place with a cash prize of $500) at the 31st IEEE MetroCon Conf., 2018.
33. IEEE Consumer Electronics Society Best Paper Award (First Place), IEEE Consumer Electronics Magazine (CEM) for 2016.
34. Best Poster Award (First Place with a cash prize of $1000) at the 30th IEEE MetroCon Conf., 2017.
35. Best Poster Award (Second Place with a cash prize of $500) at the 30th IEEE MetroCon Conf., 2017.
36. Best Ph.D. Forum Paper Award at the 14th IEEE Computer Society Annual Sympo. on VLSI, 2015.
37. Elected to the grade of Senior Member of ACM in 2010.
38. Elected to the grade of Senior Member of IEEE in 2008.
39. UNT Provost's Thank a Teacher Recognition in 2016, 2015, 2014.
40. UNT Honors Day Recognition as Inspirational Faculty in 2016, 2014, 2012, 2011, 2009, 2008.
41. President's Scout Award by the Honorable President of India for Community Services in 1988.
42. Governor's Scout Award by the Honorable Governor of Orissa for Community Services in 1988.
43. Listed in:
    (a) Marquis Who's Who in American Education: 7th Edition 2005.
    (b) Marquis Who's Who of Emerging Leaders: 1st Edition 2006.
    (c) Marquis Who's Who in Science and Engineering: 9th Edition 2006 and 10th Edition 2007.
    (d) Marquis Who's Who in America: 60th Edition 2005, 61st Edition 2006, and 64th Edition 2009.
44. Computing Research Association (CRA) funding Award for Academic Career Workshop 2004.
45. USF Provost's Certificate of Recognition for outstanding performance as a Teaching Assistant in 2003 and 2002.
46. ACM SIGDA Design Automation Summer School (DASS) Fellowship Award for 2001.
47. 139th Ranking in all India level Graduate Aptitude Test in Engineering (GATE) in Electrical

Engineering, 1997.
48. 44th Ranking in all India level Graduate Aptitude Test in Engineering (GATE) in Electrical Engineering, 1996.
49. 3rd Ranking in the University during Bachelors degree in Electrical Engineering, Orissa University of Agriculture and Technology, Bhubaneswar, India, 1995.
50. Council of Scientific and Industrial Research (CSIR), India Junior Research Fellowship Award in 1995.
51. Orissa University of Agriculture and Technology, India University Merit Scholarship Award during 1992-1995.
52. 98th Ranking in Orissa Joint Engineering Entrance Examination (OJEE), India in 1991.

KEYNOTES, PANELS, DISTINGUISHED LECTURES, and INVITED TALKS

Keynotes:

1. Cyberfortifying CPS through Security-by-Design, IEEE Conference on Secure and Trustworthy CyberInfrastructure for IoT and Microelectronics (SaTC 2025), Dayton, Ohio, 25 Feb 2025.
2. Towards Sustainable Smart Healthcare, 3rd International Conference on Communication, Control and Intelligent Systems (CCIS 2024), 2024, Mathura, India, 07 Dec 2024.
3. Sustainable Healthcare Cyber-Physical Systems (H-CPS), 5th International Conference on Data Science and Applications (ICDSA), 2024, Jaipur, India, 18 July 2024.
4. Towards Cyber-Fortifying the Smart Healthcare System, 8th Students' Conference on Engineering and Systems (SCES), 2024, Prayagraj, India, 21 June 2024.
5. Security-by-Design for Fortifying Cybersecurity of IoT/CPS, 2nd International Workshop on Energy Efficient Trustworthy Sustainable Edge-Cloud Computing (ET-Edge), 24th IEEE/ACM International Symposium on Cluster, Cloud and Internet Computing (CCGRID), 2024, Philadelphia, USA, 06 May 2024.
6. Everything You Wanted to Know About Smart Agriculture, 18th Annual Wilmington Information Technology eXchange (WITX), 2024, Wilmington, USA, 18 Apr 2024.
7. Agriculture Cyber-Physical Systems (A-CPS) - Demystified, International Conference on Artificial Intelligence and Applications (ICAIA), 2024, New Delhi, India, 19 Mar 2024.
8. Towards Sustainable Healthcare Cyber-Physical Systems (H-CPS), International Conference on Cognitive, Green and Ubiquitous Computing (IC-CGU), 2024, Bhubaneswar, India, 01 Mar 2024.
9. Smart Healthcare - Cybersecurity Perspectives, IEEE International Symposium on Smart Electronic Systems (IEEE-iSES), 2023, Ahmedabad, India, 19th December 2023.
10. Everything You Wanted to Know About Smart Agriculture, OITS International Conference on Information Technology (OCIT), 2023, Raipur, India, 14th December 2023.
11. Smart Agriculture – The Need of the Hour, International Conference on Data Science and Applications (ICDSA), 2023, Jaipur, India, 14 July 2023.
12. Internet-of-Agro-Things (IoAT) – Demystified, International Conference on Communication and Computational Techniques (ICCCT), 2023, Bhubaneswar, India, 07 July 2023.
13. Smart Healthcare - Cybersecurity Perspectives, Cybersecurity and Cloud Computing Workshop 2023, Grambling State University, 21 Mar 2023.
14. Healthcare Cyber-Physical Systems (H-CPS) - Cybersecurity Perspectives, OITS International Conference on Information Technology (OCIT), 2022, Bhubaneswar, India, 16th December 2022.
15. Machine Learning in Smart Healthcare, International Conference on Recent Advancements in Artificial Intelligence and Soft Computing (ICAISC), 2022, Hyderabad, India, 03rd December 2022.
16. Healthcare Cyber-Physical Systems (H-CPS) - Demystified, International Conference on Innovative Computing and Applications (ICICA), 2022, Nagpur, India, 26th November 2022.
17. Smart Healthcare – Reality or Hype?, International Conference on Artificial Intelligence and Signal

Processing (AISP), 2022, Vijayawada, India, 12th February 2022.

18. Everything You wanted to Know about Smart Healthcare, OITS International Conference on Information Technology (OCIT), 2021, Bhubaneswar, India, 16th December 2021.
19. Security by Design for IoT-Enabled Systems, International Conference on Security, Privacy and Data Analytics (ISPDA), 2021, Surat, India, 13th December 2021.
20. Secure Cyber-Physical Systems by Design, International Conference on Control, Automation, Power and Signal Processing (CAPS), 2021, Jabalpur, India, 10th December 2021.
21. Secure IoT by Design, 4th IFIP International Internet of Things Conference (IFIP-IoT), 2021, Amsterdam, Netherlands, 5th November 2021.
22. Healthcare Cyber-Physical System - Pandemic Era Perspectives, International E-Conference on Advances in Information Technology and Research (ICAITR), 2021, Mumbai, India, 31st May 2021.
23. Healthcare Cyber-Physical System (H-CPS) is More Important than Before, 7th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON), 2020, Prayagraj, India, 27th November 2020.
24. Security and Energy Trade-Offs in Smart City Cyber-Physical Systems, Keynote, 5th IEEE Smart Cities Conference (ISC2), 2019, Casablanca, Morocco, 16th Oct 2019.
25. Consumer Technologies for Smart Cities, Keynote, 23rd IEEE International Symposium on Consumer Technologies (ISCT), 2019, Ancona, Italy, 19th June 2019.
26. Smart City - Are We There Yet?, Keynote, 37th IEEE International Conference on Consumer Electronics (ICCE), 2019, Las Vegas, USA, 12th January 2019.
27. Smart Electronic Systems - Myths and Realities, Keynote, 4th IEEE International Symposium on Smart Electronic Systems (IEEE-iSES), 2018, Hyderabad, India, 17th December 2018.
28. Security and Energy Tradeoffs in Consumer Electronics, Keynote, 3rd Zooming Innovation in Consumer Electronics International Conference (ZINC), 2018, Novi Sad, Serbia, 31st May 2018.
29. Smart Cities - Demystified, Keynote, 2nd International Conference on Man and Machine Interfacing (MAMI), 2017, Bhubaneswar, India, 23rd December 2017.
30. Internet of Things (IoT) - Demystified, Keynote, 16th International Conference on Information Technology (ICIT), 2017, Bhubaneswar, India, 22nd December 2017.
31. iVAMS: A Paradigm Shift System Simulation Framework for the IoT Era, Keynote Presentation, 17th IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), Montpellier, France, 19th Apr 2016.
32. DfX for Nanoelectronic Embedded Systems, Keynote, International Conference on Control, Automation, Robotics and Embedded System (CARE), Indian Institute of Information Technology, Design and Manufacturing Jabalpur, India, 18th December 2013.

Conference Panels:

33. Career Opportunities in Engineering, 8th Students' Conference on Engineering and Systems (SCES), 2024, Prayagraj, India, 22 June 2024.
34. AI in IoT: Security-by-Design Incorporating AI and Cybersecurity is Critical for IoT-Enabled Systems, IFIP International Internet of Things Conference (IFIP-IoT), 2022, Amsterdam, Netherlands, 27 Oct 2022.
35. IoT Empowered Solutions for Smart Villages, 7th IEEE International Symposium on Smart Electronic Systems (IEEE-iSES), 2021, Jaipur, India, 21 Dec 2021.
36. IoT and AI Will Develop Revolutionary Solutions to Critical Global Problems: A Real Promise or Just a Hype?, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2021, Tampa, USA, 08 July 2021.
37. Overcoming healthcare challenges by means of technology - can we prevent future pandemics?, Zooming Innovation in Consumer Technologies International Conference (ZINC), 2021, Novi Sad, Serbia, 27 May 2021.

38. Smart Cities and Smart Villages - Design Optimization Perspectives, 6th IEEE International Symposium on Smart Electronic Systems (IEEE-iSES), 2020, 14th December 2020.
39. Security by Design for Sustainable Cyber-Physical Systems, 10th IEEE International Conference on Consumer Electronics (ICCE) Berlin, 2020, 10th November 2020.
40. Security by Design for Sustainable CPS, Session: Data Sciences - Data Privacy and Security, VAIBHAV Summit 2020, 18 Oct 2020.
41. TinyML - Key for Smart Cities and Smart Villages, Session: Data Sciences - Applications, VAIBHAV Summit 2020, 16 Oct 2020.
42. Smart Healthcare, 37th IEEE International Conference on Consumer Electronics (ICCE), 2020, Las Vegas, 5th January 2020.
43. Cybersecurity of Smart Electronics from IoT to Vehicles - Cybersecurity in Smart Electronics: A Multi-Objective Trade-off, 36th IEEE International Conference on Consumer Electronics (ICCE), 2019, Las Vegas, 11th January 2019.
44. Key Technologies for CE Product Designs - Cybersecurity and Home Health Care, Consumer Electronics Show (CES), 2019, Las Vegas, 10th January 2019.
45. What Makes Smart Cities Smart?, 3rd Zooming Innovation in Consumer Electronics International Conference (ZINC), 2018, Novi Sad, Serbia, 31st May 2018.
46. Energy and Security Tradeoffs in CE Systems, 36th IEEE International Conference on Consumer Electronics (ICCE), 2018, Las Vegas, 13th January 2018.
47. Best of ICCE Sessions - Smart Electronics for Healthcare, Consumer Electronics Show (CES), 2018, Las Vegas, 12th January 2018.

Distinguished Lectures and Tutorials:

48. Security-by-Design to Fortify Cyber-Physical Systems, Silicon University, Bhubaneswar, India, 10 Dec 2024.
49. Sustainable Healthcare Cyber-Physical Systems, Nirma University, Ahmadabad, India, 25 Nov 2024.
50. Keys to Research Productivity, National Institute of Technology (NIT) Jaipur, India, 24 July 2024.
51. Everything You Wanted to Know about Smart Healthcare, Nalla Malla Reddy Engineering College (NMREC) and IEEE NMREC Students Branch, Hyderabad, 07 Jan 2023.
52. Everything You Wanted to Know about Smart Agriculture, Silicon Institute of Technology, Bhubaneswar, India, 03 Jan 2023.
53. Keys to Research Productivity, Nalla Malla Reddy Engineering College (NMREC) and IEEE Education Society, Hyderabad, 07 Jan 2023.
54. Physical Unclonable Function (PUF) as the Security-by-Design (SbD) Primitive for CPS, National Institute of Technology (NIT) Rourkela, India, 06 December 2022.
55. Cybersecurity Perspectives of Smart Healthcare, Malaviya National Institute of Technology Jaipur, India, 29 July 2022.
56. Machine Learning in Smart Healthcare, Malaviya National Institute of Technology Jaipur, India, 28 July 2022.
57. Physical Unclonable Function (PUF) as the Hardware-Assisted Security (HAS) Primitive, VIT-AP University, India, 23 June 2022.
58. Smart Healthcare - Pandemic Era Perspectives, Smart Cities and Communities (SMACCs) Summer School, University of Mons, Belgium, 08 July 2021.
59. Cybersecurity, Energy, and Intelligence Tradeoffs in IoT, Odisha University of Technology and Research (OUTR), Bhubaneswar, India, 06 July 2021.
60. Everything You Wanted to Know about Smart Healthcare, IEEE Smart Cities Webinar, 25 May 2021.
61. Consumer Technologies for Smart Cities to Smart Villages, 39th IEEE International Symposium on Smart Electronic Systems (ICCE), 2021, 10 Jan 2021.
62. Cybersecurity, Energy, and Intelligence Tradeoffs in IoT, Indian Institute of Technology, Banaras

Hindu University (IIT-BHU) Varanasi, 25th December 2020.

63. Security by Design for Cyber-Physical Systems, Malaviya National Institute of Technology, Jaipur, 27th July 2020.
64. Healthcare Cyber-Physical System (H-CPS), Malaviya National Institute of Technology, Jaipur, 26th July 2020.
65. Secure Cyber-Physical Systems by Design, Government College of Engineering and Technology, Bhubaneswar - 20th Sep 2020.
66. Smart Healthcare - An Overview, Government College of Engineering and Technology, Bhubaneswar - 19th Sep 2020.
67. Blockchain - Demystified, Oriental University, Indore, 06th Nov 2020.
68. Healthcare Cyber-Physical System (H-CPS), Oriental University, Indore, 21st May 2020.
69. Prof. M. Ramamoorty Distinguished Lecture - Energy and Security Trade-Offs in Smart City Components, Indian Institute of Technology, Kanpur, 5th Aug 2019.
70. Security and Energy Tradeoffs in Electronic Systems, Malaviya National Institute of Technology, Jaipur, 31st July 2018.
71. Internet of Things (IoT) - The State-of-Art, Malaviya National Institute of Technology, Jaipur, 30th July 2018.
72. Everything you Wanted to Know about Internet of Things (IoT), IEEE Consumer Electronics Society Webinar, 16th November 2017.
73. Everything you Wanted to Know about Smart Cities, IEEE Consumer Electronics Society Webinar, 5th October 2017.

Invited Talks:

74. Security-by-Design (SbD) for Integrated Robust Cybersecurity of CPS, VIT University AP, Guntur, India, 22 July 2023.
75. Smart Agriculture - Demystified, SRM University AP, Guntur, India, 21 July 2023.
76. Everything You wanted to Know about Internet-of-Medical-Things (IoMT), Gandhi Institute for Technology (GIFT), Bhubaneswar, India, 23 November 2021.
77. Healthcare Cyber-Physical System - Pandemic Era Perspectives, Build and Broaden: Conference on Social Connections to Promote Individual and Community Resilience in Post-COVID-19 Society, University of Texas at Arlington, 7th Oct 2021.
78. Healthcare Cyber-Physical System (H-CPS), Oriental University, Indore, India, 28 September 2021.
79. Smart Healthcare - Demystified, Texas Tech University, 16th March 2021.
80. Smart Healthcare - Demystified, Saint Louis University, 9th March 2021.
81. Healthcare Cyber-Physical System (H-CPS) - Demystified, IEEE Consumer Technology Society Odisha Chapter - Bhubaneswar Subsection, 12th Sep 2020.
82. Cyber-Physical Systems (CPS), IEEE-Bombay-Section-OPJU, 18th July 2020.
83. Security by Design for Cyber-Physical Systems, National Workshop on IoT and Sensor Embedded Applications, Silicon Institute of Technology, Bhubaneswar, 20th Dec 2019.
84. Secure Cyber-Physical Systems by Design, University of Texas at Arlington, 15th Nov 2019.
85. Smart Healthcare - Demystified, IEEE MetroCon, 2019, Hurst Conference Center, TX, USA, 6th Nov 2019.
86. Consumer Technologies for the Smart Cities, Malaviya National Institute of Technology, Jaipur, 13th Aug 2019.
87. Everything You Wanted to Know about the Internet-of-Things (IoT), Oriental University, Indore, 30th July 2019.
88. Smart Electronic Systems - Facts Vs Fictions, International Institute of Information Technology, Naya Raipur, 24th July 2019.
89. Smart Cities - Myths and Realities, Indian Institute of Technology Bhubaneswar, India, 25th July

2018.

90. DFX for Nanoelectronic Systems, Government College of Engineering and Technology, Bhubaneswar, India, 18th December 2014.
91. DfX for Nanoelectronic Circuits and Systems, Oriental Group of Institutes, Bhopal, India, 23rd December 2013.
92. Energy Efficient Nanoelectronic System Design, Energy Efficient Buildings and Communities Workshop, Tartu, Estonia, 21st May 2013.
93. Ultra-Fast Design Exploration of Nanoscale Circuits through Metamodeling, Semiconductor Research Corporation (SRC), Texas Analog Center for Excellence (TxACE), 27th April 2012.
94. Towards The Design of Robust Secure Digital Cameras (SDC), Department of Electrical and Computer Engineering, University of Calgary, Canada, 25th May 2010.
95. Unified Challenges in Nano-CMOS High-Level Synthesis, 22nd International Conference on VLSI Design (VLSID), New Delhi, India, 7th January 2009.
96. Research in VLSI Design and CAD Laboratory (VDCL), Industry Council meeting, Department of Computer Science and Engineering University of North Texas (UNT), Denton, TX, on 2nd May 2008.
97. Low-Power Image Watermarking Chip Design, CV Raman College of Engineering (CVRCE), Bhubaneswar, India, 3rd January 2008.
98. Power Dissipation in Nano-CMOS Circuits, Department of Electrical Engineering, University of North Texas, Denton, TX, 24th March 2008.
99. Circuits and Systems for Real-Time DRM of Multimedia, Department of Electrical and Computer Engineering, Utah State University (USU), Utah, 15th May 2007.
100. Circuits and Systems for Real-Time DRM of Multimedia, Department of Computer Science and Electrical Computer Engineering, University of Missouri-Kansas City (UMKC), MO, 5th May 2007.
101. A Secure Digital Camera for Real-Time Security and Copyright Protection of Multimedia, Department of Electrical and Computer Engineering, University of Texas, San Antonio (UTSA), TX, 20th March 2007.
102. A Secure Digital Camera for Real-Time Security and Copyright Protection of Multimedia, Department of Computer Science and Electrical Engineering, University of Maryland, Baltimore County (UMBC), Baltimore, MD, 9th March 2007.
103. Secure Digital Camera, Department of Electrical Engineering, Indian Institute of Science (IISc), Bangalore, India, 8th January 2007.
104. Secure Digital Camera, Indian Institute of Technology (IIT), Kharagpur, India, 27th December 2006.
105. Design of a Image Watermarking Low-Power Chip, Institute of Technical Education and Research (ITER), Bhubaneswar, India, 23rd December 2006.
106. Secure Digital Camera, College of Engineering and Technology (CET), Biju Patnaik University of Technology (BPUT), Bhubaneswar, India, 18th December 2006.
107. VLSI Design and CAD Research at University of North Texas, Current Research in CSCE course (CSCE-5020), Department of Computer Science and Engineering, University of North Texas (UNT), Denton, TX, 15th February 2006.
108. Gate Leakage Analysis and Reduction in Nanoscale CMOS circuits, Department of Computer Science and Engineering, Southern Methodist University (SMU), Dallas, TX, 16th November 2005.
109. DKDT: A Performance Aware Dual Dielectric Assignment for Tunneling Current Reduction, Department of Electrical Engineering, University of Texas, Dallas (UTD), TX, 28th March 2005.
110. DKDT: A Performance Aware Dual Dielectric Assignment for Tunneling Current Reduction, Department of Electrical and Computer Engineering, Oklahoma State University (OSU), Stillwater, OK, 10th March 2005.
111. DKDT: A Performance Aware Dual Dielectric Assignment for Tunneling Current Reduction, Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, UT, 4th February 2005.

112. Research at VLSI Design and CAD Laboratory (VDCL), Industry Council meeting, Department of Computer Science and Engineering University of North Texas (UNT), Denton, TX, on 3rd December 2004.
113. A Dual Voltage Dual Frequency Low Power VLSI Chip for Image Watermarking, Current Research in CSCE course (CSCI-5170), Department of Computer Science and Engineering, University of North Texas (UNT), Denton, TX, November 2004.
114. Low Power Design and Synthesis using Voltage and Frequency Reduction, Department of Computer Science and Engineering University of North Texas (UNT), Denton, TX, 16th January 2004.
115. Low Power Design and Synthesis using Multiple Supply Voltage, Variable Frequency and Multicycling, Department of Computer Engineering, Rochester Institute of Technology (RIT), Rochester, NY, 11th December 2003.
116. Energy and Transient Power Minimization using Multiple Supply Voltages and Dynamic Frequency Clocking, Department of Electrical and Computer Engineering, New Jersey Institute of Technology (NJIT), Newark, NJ, 29th October 2003.

PROFESSIONAL LEADERSHIP

Proposal-Review Panelist:

1. Panelist, National Science Foundation (NSF), Accelerating Computing-Enabled Scientific Discovery (ACED) Program.
2. Panelist, National Science Foundation (NSF), SBIR/STTR Program.
3. Panelist, National Science Foundation (NSF), Smart and Connected Health (SCH).
4. Panelist, National Science Foundation (NSF), Advanced Cyberinfrastructure (OAC).
5. Panelist, National Science Foundation (NSF), Smart and Connected Community (S&CC).
6. Panelist, National Science Foundation (NSF), Division of Electrical, Communications and Cyber Systems (ECCS).
7. Panelist, National Science Foundation (NSF), Division of Computer and Network Systems (CNS), Secure and Trustworthy Cyberspace (SaTC).
8. Panelist, National Science Foundation (NSF), Division of Computer and Network Systems (CNS), Cyber-Physical Systems (CPS).
9. Reviewer, National Science Foundation (NSF), Office of Cyberinfrastructure, Strategic Technologies for Cyberinfrastructure (STCI).
10. Invited Researcher, Workshop on NSF Nanoelectronics: Circuits, Systems, and CAD Tools, October 2007 to review the impacts of the Emerging Models and Technologies for Computation (EMT) Program of National Science Foundation (NSF) on various fronts.
11. Reviewer, Swiss National Science Foundation, Switzerland.
12. Reviewer, National Center of Science and Technology Evaluation, Kazakhstan.
13. Reviewer, Division of Physics and applied Mathematics, Israeli Ministry of Science, Technology and Space.
14. Reviewer, The Austrian Science Fund (FWF), Natural and Technical Sciences.
15. Reviewer, U.S. Civilian Research & Development Foundation (CRDF, `http://www.crdf.org/`).

Journal Editorship:

16. **Editor-in-Chief (EiC)**, IEEE Consumer Electronics Magazine (MCE), 2016–2021.
17. **Founding Editor-in-Chief (EiC)**, IEEE-CS-TCVLSI VLSI Circuits and Systems Letter (VCaSL), 2015–2018.
18. **Section Editor**, Emerging Trends in Sensors, IoT and Smart Systems Section, Springer Nature Computer Science (SNCS), 2020–present.
19. **Section Editor**, Quantum Computing and Emerging Technologies Section, Springer Nature Computer

Science (SNCS), 2020–present.
20. Associate Editor, IEEE Potentials Magazine, 2025–present.
21. Associate Editor, IEEE Transactions on Big Data (TBD), 2018–present.
22. Associate Editor, ACM Journal on Emerging Technologies in Computing Systems (JETC), 2016–present.
23. Associate Editor, IEEE Transactions on Nanotechnology (TNANO), 2017–present.
24. Associate Editor, IET Circuits, Devices and Systems (CDS), 2014–present.
25. Associate Editor, Elsevier The VLSI Integration Journal (VLSIJ), 2014–present.
26. Associate Editor, ASP Journal of Low Power Electronics (JOLPE), 2011–present.
27. Editorial Board Member, OAE Journal of Surveillance, Security and Safety (JSSS), 2020–present.
28. Review Editor, Frontiers in High Performance Computing Journal (FHPC), 2022–present.
29. Review Editor, Frontiers in Electronics Journal (FEJ), 2022–present.
30. Associate Editor, IEEE Transactions on Consumer Electronics (TCE), 2018–2022.
31. Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2016–2022.
32. Secretary, Steering Committee, IEEE Transactions on Big Data (TBD), 2018–2019.
33. Senior Editor, IEEE Consumer Electronics Magazine (MCE), 2015–2016.
34. Associate Editor, Elsevier International Journal on Computers and Electrical Engineering (JCEE), 2010–2014.
35. Guest Editor, "Special Issue on Camera as a Smart-Sensor (CaaSS)", MDPI Sensors, 2020–2023.
36. Guest Editor, "Special Issue on Novel Paradigm for Consumer Electronics Security", IEEE Transactions on Consumer Electronics (TCE), Vol. 68, No. 1, February 2022.
37. Guest Editor, "Special Issue on Hardware-Assisted Security for Emerging Internet of Things", ACM Journal on Emerging Technologies in Computing Systems (JETC), Vol. 18, No. 1, January 2022.
38. Guest Editor, "Special Section on Machine Learning for Smart Electronic Systems", IEEE Transactions on Consumer Electronics (TCE), Vol. 67, No. 4, November 2021.
39. Guest Editor, "Special Section on New Frontiers in Computing for Next-Generation Healthcare Systems", IEEE Transactions on Emerging Topics in Computing (TETC), Vol. 9, No. 3, July-September 2021.
40. Guest Editor, "Special Section on Consumer Technologies for Smart Healthcare", IEEE Transactions on Consumer Electronics (TCE), Vol. 67, No. 1, February 2021.
41. Guest Editor, "Special Issue on Cybersecurity for the Smart Grid", IEEE Computer, Vol. 53, No. 5, May 2020.
42. Guest Editor, "Special Section on Recent Advances on Trust, Security and Privacy in Computing and Communications", Wiley Concurrency and Computation: Practice and Experience Journal, Volume 31, Issue 23, December 2019.
43. Guest Editor, "Special Issue on Smart Consumer Electronics Systems", IEEE Potentials Magazine, Volume 38, Issue 1, January 2019.
44. Guest Editor, "Special Issue on Hardware-Assisted Techniques for Security and Protection of Consumer Electronics", IET Computers & Digital Techniques (CDT), Volume 12, Issue 6, November 2018.
45. Guest Editor, "Special Issue on Circuit and System Design Automation for Internet of Things", IEEE Transactions on Computer Aided Design (TCAD), Volume 37, Issue 1, January 2018.
46. Guest Editor, "Special Section on Nanoelectronic Devices and Circuits for Next Generation Sensing and Information Processing", IEEE Transaction on Nanotechnology (TNANO), Volume 16, Issue 3, May 2017.
47. Guest Editor, "Special Issue on Hardware Assisted Techniques for IoT and Bigdata Applications", Elsevier The VLSI Integration Journal (VLSIJ), Volume 58, June 2017.
48. Guest Editor, "Special Section on Nanoelectronic Circuit and System Design Methods for Mobile

Computing Era", ACM Journal on Emerging Technologies in Computing Systems (JETC), Volume 13, Issue 2, March 2017.

49. Guest Editor, "Special Issue on Security and Reliability Aware System Design for Mobile Computing Systems", IEEE Access Journal (Access), Volume 4, 2016.
50. Guest Editor, "Special Section on Circuit and System Design Methodologies for Emerging Technologies", IEEE Transactions on Emerging Topics in Computing (TETC), Vol. 3, No. 4, October-December 2015.
51. Guest Editor, "Special Issue on Advanced Techniques for Efficient Electronic System Design", Springer Circuits, Systems, and Signal Processing Journal (CSSP), Volume 32, Issue 6, December 2013.
52. Guest Editor, "Special Issue on Design Methodologies for Nanoelectronic Digital and Analog Circuits", IET Circuits, Devices, & Systems Journal (CDS), Volume 7, Issue 5, September 2013.
53. Guest Editor, "Special Section on New Circuit and Architecture Level Solutions for Multidiscipline Systems", ACM Journal on Emerging Technologies in Computing Systems (JETC), Volume 8, Issue 3, August 2012.
54. Guest Editor, "Special Issue on Power, Parasitics, and Process-Variation (P3) Awareness in Mixed-Signal Design", ASP Journal of Low Power Electronics (JOLPE), Volume 8, Issue 3, June 2012.
55. Guest Editor, "Special Issue on Circuits and Systems for Real-Time Security and Copyright Protection of Multimedia", Elsevier International Journal on Computers and Electrical Engineering (JCEE), Volume 35, Issue 2, March 2009.

Conference Leadership Chairs:

56. **Founding Steering Committee Chair**, IEEE International Symposium on Smart Electronic Systems (iSES), 2015–Present.
57. **Steering Committee Vice-Chair**, IEEE-CS Annual Symposium on VLSI (ISVLSI), 2016–Present.
58. **Steering Committee Chair**, OITS International Conference on Information Technology (OCIT), 2014–Present.
59. Chair, Workshop on Quantum Solutions for Technology Resilience and Infrastructure Development Enhancement (QSTRIDE), 26th IEEE International Symposium on a World of Wireless, Mobile and Multimedia Networks (WoWMoM), May 27-30, 2025, Fort Worth, TX, USA.
60. Special Session Chair, 32nd IFIP/IEEE International Conference on Very Large-Scale Integration (VLSI-SoC), October 6-9, 2024, Tangier, Morocco.
61. Special Session Chair, 22nd IEEE Computer Society Annual Symposium on VLSI (ISVLSI), July 1-3, 2024, Knoxville, USA.
62. **General Chair**, 6th IFIP International Internet of Things Conference (IFIP-IoT), November 2–3, 2023, DFW Metroplex, USA.
63. Special Session Chair, 21st IEEE Computer Society Annual Symposium on VLSI (ISVLSI), June 20-23, 2023, Foz do Iguaçu, Brazil.
64. **General Chair**, 20th OITS International Conference on Information Technology (OCIT), December 14–16, 2022, Bhubaneswar, India.
65. **General Chair**, 7th IEEE International Symposium on Smart Electronic Systems (iSES), December 20-22, 2021, Jaipur, India.
66. **General Chair**, 18th IEEE-CS Annual Symposium on VLSI (ISVLSI), July 15-17, 2019, Miami, FL, USA.
67. **General Chair**, 36th IEEE International Conference on Consumer Electronics (ICCE), January 12-14, 2018, Las Vegas, NV, USA.
68. Media Outreach Chair, 3rd IEEE Canada International Humanitarian Technology Conference (IHTC), July 20–22, 2017, Toronto, Canada.
69. Special Session Chair, 16th IEEE-CS Annual Symposium on VLSI (ISVLSI), July 3-5, 2017,

Bochum, Germany.

70. **General Chair**, 2nd IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), December 19-21, 2016, Gwalior, India.
71. **General Chair**, 15th International Conference on Information Technology (ICIT), December 22-24, 2016, Bhubaneswar, India.
72. **Program Chair**, 15th IEEE-CS Annual Symposium on VLSI (ISVLSI), July 11-13, 2016, Pittsburgh, PA, USA.
73. **Founding General Chair**, 1st IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), December 21-23, 2015, Indore, India.
74. Publication Chair, 14th International Conference on Information Technology (ICIT), December 21-23, 2015, Bhubaneswar, India.
75. **Program Chair**, 14th IEEE-CS Annual Symposium on VLSI (ISVLSI), July 8-10, 2015, Montpellier, France.
76. **General Chair**, 13th International Conference on Information Technology (ICIT), December 22-24, 2014, Bhubaneswar, India.
77. **General Chair**, 13th IEEE-CS Annual Symposium on VLSI (ISVLSI), July 9-11, 2014, Tampa, FL, USA.
78. **General Chair**, 11th IEEE-CS Annual Symposium on VLSI (ISVLSI), May 19-21, 2012, Amherst, MA, USA.
79. Publication Chair, 2nd International Symposium on Electronic System Design (ISED), December 19-21, 2011, Kochi, India.
80. **Founding Steering Committee Chair**, International Symposium on Electronic System Design (ISED), 2010–2011.
81. **Founding Program Chair**, 1st International Symposium on Electronic System Design (ISED), December 20-22, 2010, Bhubaneswar, India.
82. Journal Special Issues Chair, 5th IEEE International Smart Cities Conference (ISC2), October 14-17, 2019, Casablanca, Morocco.
83. Publication Chair, 12th International Conference on Information Technology (ICIT), December 21-24, 2009, Bhubaneswar, India.
84. Publication Chair, 8th IEEE-CS Annual Symposium on VLSI (ISVLSI), May 13-15, 2009, Tampa, FL, USA.
85. Publicity Chair, 10th International Conference on Information Technology (ICIT), December 18-20, 2007, Bhubaneswar, India.
86. Publicity Chair, 2nd International Conference on Web Engineering and Application (ICWA), December 14-16, 2007, Bhubaneswar, India.
87. Publicity Chair, International Conference on IP Multimedia Subsystems Architecture and Applications (IMSAA-2007), December 6-8, 2007, Bangalore, India.
88. **Program Chair**, 9th International Conference on Information Technology (ICIT), December 18-26, 2006, Bhubaneswar, India.

Conference Track/Session Chairs:

89. Track Chair, "Special Session: Security By Design (SbD)", IEEE Computer Society Annual Symposium on VLSI, Kalamata, Greece, July 6-9, 2025.
90. Track Chair, "Special Session: Advanced Electronics for Smart Agriculture", IEEE Computer Society Annual Symposium on VLSI, Kalamata, Greece, July 6-9, 2025.
91. Track Chair, "IoT and Smart Systems", 34th ACM Great Lakes Symposium on VLSI (GLSVLSI), June 12-14, 2024, Tampa, FL, USA.
92. Track Chair, "Special Session: Secure and Dependable Cyber-Physical Systems", 21st IEEE Computer Society Annual Symposium on VLSI (ISVLSI), June 20-23, 2023, Foz do Iguaçu, Brazil.

93. Track Chair, “Special Session: Smart Healthcare Technologies”, 33rd ACM Great Lakes Symposium on VLSI (GLSVLSI), June 5-7, 2023, Knoxville, TN, USA.
94. Track Chair, “IoT and Smart Systems”, 33rd ACM Great Lakes Symposium on VLSI (GLSVLSI), June 5-7, 2023, Knoxville, TN, USA.
95. Track Chair, “VLSI Design”, 32nd ACM Great Lakes Symposium on VLSI (GLSVLSI), June 6-8, 2022, Irvine, CA, USA.
96. Track Chair, “Smart Cities, Internet of Everything, Industry 4.0”, ACM/IEEE Design, Automation, and Test in Europe Conference (DATE), March 14-15, 2022, Antwerp, Belgium.
97. Track Chair, “Smart Health and Wellbeing”, 7th IEEE International Smart Cities Conference (ISC2), September 7-10, 2021, Online due to COVID-19 pandemic.
98. Track Chair, “Smart Cities, Internet of Everything, and Smart Consumer Electronics”, ACM/IEEE Design, Automation, and Test in Europe Conference (DATE), February 1-5, 2021, Grenoble, France.
99. Track Chair, “Artificial Intelligence, IoT, Blockchain & Augmented City”, 6th IEEE International Smart Cities Conference (ISC2), September 28 - October 1, 2020, Virtual Conference due to COVID-19 pandemic.
100. Session Chair, “IoT based Consumer Technologies for Smart Cities”, 6th IEEE World Forum on Internet of Things (WF-IoT), September 2-16, 2020, New Orleans, USA (Online due to COVID-19 pandemic).
101. Session Chair, “Law, Privacy, and Security”, 4th IEEE International Smart Cities Conference (ISC2), September 16-19, 2018, Kansas City, USA.
102. Session Co-Chair, “Galvanizing Software Safety and Security”, 3rd Zooming Innovation in Consumer Electronics International Conference (ZINC), May 30-31, 2018, Novi Sad, Serbia.
103. Track Chair, “Consumer Healthcare & Systems”, 35th IEEE International Conference on Consumer Electronics (ICCE), January 8-11, 2017, Las Vegas, USA.
104. Session Chair, “Electromagnetic Compatibility”, 6th IEEE International Conference on Consumer Electronics - Berlin (ICCE-Berlin), September 5-7, 2016, Berlin, Germany.
105. Track Chair, “VLSI Design”, 25th ACM Great Lakes Symposium on VLSI (GLSVLSI), May 20-22, 2015, Pittsburgh, PA.
106. Session Chair, “Analog Design”, 24th ACM Great Lakes Symposium on VLSI (GLSVLSI), May 21-23, 2014, Houston, TX.
107. Track Chair, “VLSI Design”, 24th ACM Great Lakes Symposium on VLSI (GLSVLSI), May 21-23, 2014, Houston, TX.
108. Track Co-Chair, “Design for Manufacturability/Yield & Quality (DFQ)”, 13th International Symposium on Quality Electronic Design (ISQED), March 19-21, 2012, Santa Clara, CA.
109. Track Chair, “CAD for Analog and Mixed Signal Circuits”, 25th International Conference on VLSI Design (VLSID), January 7-11, 2012, Hyderabad, India.
110. Session Chair, “Design Methodologies for CMOS and Beyond”, 12th International Symposium on Quality Electronic Design (ISQED), March 14-16, 2011, Santa Clara, CA.
111. Track Co-Chair, “Design for Manufacturability/Yield & Quality (DFQ)”, 12th International Symposium on Quality Electronic Design (ISQED), March 14-16, 2011, Santa Clara, CA.
112. Session Chair, “Poster Session II”, 20th ACM Great Lakes Symposium on VLSI (GLSVLSI), 2010, 18th May, 2010, Providence, RI.
113. Session Chair, “SRAM Manufacturability”, 11th International Symposium on Quality Electronic Design (ISQED), March 22-24, 2010, San Jose, CA.
114. Session Chair, “Low-Power Architecture”, 23rd International Conference on VLSI Design (VLSID), 6th January 2010, Bangalore, India.
115. Session Chair, 12th International Conference on Information Technology (ICIT), 24th December 2009, Bhubaneswar, India.
116. Session Chair, International Symposium on Biologically Inspired Computing And Applications

(BICA), 22nd December 2009, Bhubaneswar, India.

117. Session Chair, "Process Variation", 10th International Symposium on Quality Electronic Design (ISQED), March 16-18, 2009, San Jose, CA.
118. Session Co-Chair, "Low Voltage Design", 10th International Symposium on Quality Electronic Design (ISQED), March 16-18, 2009, San Jose, CA.
119. Session Chair, "SoC Verification", 22nd International Conference on VLSI Design (VLSID), January 5-9, 2009, New Delhi, India.
120. Session Chair, "Networks - 1" and "Database and Web Technology", 11th International Conference on Information Technology (ICIT), December 17-20, 2008, Bhubaneswar, India.
121. Session Chair, "System-Level Testing, Verification and Design" and "Poster Session 2", 18th ACM Great Lake Symposium on VLSI (GLSVLSI), May 4-6, 2008, Orlando, FL.
122. Session Chair, "Low Power - I", 21st International Conference on VLSI Design (VLSID), January 4-8, 2008, Hyderabad, India.
123. Session Chair, "Security and Digital Rights Management", IEEE International Symposium on Consumer Electronics (ISCE), 20-23 June 2007, Dallas, TX.
124. Session Chair, "Internet, Network Protocol and Architecture", 8th International Conference on Information Technology (CIT), December 20-23, 2005, Bhubaneswar, India.

Conference Committees:

125. Steering Committee Member, International Conference on Data Analytics and Cyber Security (DACS) – 2025–Present.
126. Steering Committee Member, IFIP International Internet of Things Conference (IFIP-IoT) – 2024–Present.
127. Steering Committee Member, IEEE-CS Annual Symposium on VLSI (ISVLSI) – 2015–Present.
128. Steering Committee Member, IEEE International Symposium on Smart Electronic Systems (IEEE-iSES) – 2015–Present.
129. Steering Committee Member, OITS International Conference on Information Technology (OCIT) – 2015–Present.
130. Program Committee Member, IFIP/IEEE International Conference on Very Large-Scale Integration (VLSI-SoC) – 2024.
131. Program Committee Member, IEEE Conference on Digital Health (ICDH) – 2023, 2024, 2025.
132. Program Committee Member, International Congress on Blockchain and Applications (BLOCKCHAIN) – 2022, 2023, 2024, 2025.
133. Program Committee Member, IEEE World Forum on Internet of Things (WF-IoT) – 2019, 2020, 2021, 2023, 2024, 2025.
134. Program Committee Member, IEEE International Conference on Computer Design (ICCD) – 2012, 2013, 2014, 2015, 2016, 2018, 2019, 2020, 2021, 2022, 2023, 2024.
135. Program Committee Member, Advanced Doctoral Conference on Computing, Electrical and Industrial Systems (DoCEIS) – 2023, 2024, 2025.
136. Program Committee Member, International Conference on VLSI Design (VLSID) – 2008, 2009, 2010, 2011, 2013, 2015, 2022, 2023.
137. Program Committee Member, ACM Great Lake Symposium on VLSI (GLSVLSI) – 2008, 2009, 2010, 2011, 2012, 2013, 2016, 2018, 2019, 2020, 2021, 2022.
138. Program Committee Member, IEEE Future Networks World Forum (FNWF) – 2024.
139. Program Committee Member, International Conference on Innovations in Computing Research (ICR) – 2023, 2024, 2025.
140. Program Committee Member, IEEE International Smart Cities Conference (ISC2) – 2018, 2019, 2020.
141. Executive Committee Member, IEEE International Conference on Consumer Electronics (ICCE) – 2017–2020.

142. Program Committee Member, International Conference on the Internet of Things (IoT) – 2020, 2021, 2022.
143. Program Committee Member, IEEE International Conference on Autonomous Systems (ICAS) – 2021.
144. Program Committee Member, International Conference on Urban Data Science (UDS) – 2020.
145. Program Committee Member, International Symposium on Quality Electronic Design (ISQED) – 2009, 2010, 2013, 2014, 2015.
146. Program Committee Member, Asia Symposium on Quality Electronic Design (ASQED) – 2009, 2010, 2011, 2012, 2013, 2014, 2015.
147. Program Committee Member, IEEE-CS Annual Symposium on VLSI (ISVLSI) – 2009, 2010, 2011, 2014, 2015.
148. Student Design Contest Judge, Design Automation Conference – 2005, 2006, 2007, 2008, 2009, 2010.
149. Program Committee Member, IEEE/IFIP International Conference on VLSI and System-on-Chip (VLSI-SoC) – 2010.
150. Program Committee Member, International Conference on Intelligent Information Hiding and Multimedia Signal Processing (IIH-MSP) – 2007, 2008, 2009, 2010, 2011, 2012, 2013.
151. Program Committee Member, IEEE Dallas Circuits and Systems Workshop (DCAS) – 2007, 2008.
152. Program Committee Member, VLSI Design and Test Symposium (VDAT) - 2012, 2014.
153. The first Annual National Aspire Science Competition Judge, The Texas Academy of Mathematics and Science, 2011, http://www.aspiresciencecompetition.com/.
154. Program Committee Member, The 6th International Workshop on Unique Chips and Systems (UCAS-6), December 4, 2010, Atlanta, GA, USA.
155. Program Committee Member, International Conference on Computer Technology (ICCT-2010), December 3-5, 2010, Bhubaneswar, India.
156. Program Committee Member, International Conference on VLSI Design and Communication Systems (ICVLSICOM-10), January 8-10, 2010, Chennai, India.
157. Program Committee Member, International Conference on IP Multimedia Subsystems Architecture and Applications (IMSAA) – 2007, 2008, 2009.
158. Program Committee Member, 10th International Conference on Information Technology (ICIT), December 18-26, 2007, Bhubaneswar, India.
159. Technical Review Committee, Global Signal Processing Expo & Conference (GSPx) 2005.

STUDENT/SCHOLAR MENTORING

Postdoctoral Scholars Mentored:

1. C. Sahu, Visiting Scholar, Malaviya National Institute of Technology Jaipur, India, Fall 2022 – Spring 2023.
2. J. Singh, Visiting Scholar, PDPM-Indian Institute of Information Technology Design and Manufacturing (IIITDM), Jabalpur, India, Fall 2016.
3. P. Ghosal, UGC Raman Post Doctoral Fellow, Indian Institute of Engineering Science and Technology (IIEST), Shibpur, India, Summer 2013 – Summer 2014.

Ph.D. Dissertations Supervised or co-Supervised:

4. S. Aarella, Ph.D.(Computer Science and Engineering), Dissertation: "Fortified-Edge: PUF-based Security-by-Design for Integrated Cybersecurity in Collaborative Edge Computing", Department of Computer Science and Engineering, University of North Texas, Spring 2025. (First Employment: Austin College)
5. A. K. Bapatla, Ph.D.(Computer Science and Engineering), Dissertation: "PharmaChain: Distributed Ledger based Robust Solutions for Counterfeit-Free Pharmaceutical Supply Chain", Department of Computer Science and Engineering, University of North Texas, Summer 2024. (**Received Best Paper**

Award at the 20th OITS International Conference on Information Technology (OCIT) 2022.) (**Received Second Prize at the IEEE Brain Data Bank Challenge 2020**.) (First Employment: University of Central Missouri)

6. L. S. T. Vangipuram, Ph.D.(Computer Science and Engineering), Dissertation: "AgroString: Exploring Distributed Ledger for Effective Data Management in Smart Agriculture", Department of Computer Science and Engineering, University of North Texas, Summer 2024. (**Received Best Paper Award at the 21st OITS International Conference on Information Technology (OCIT) 2023**.) (**Received Best Research Demo Session Paper Award at the 9th IEEE International Symposium on Smart Electronic Systems (IEEE-iSES) 2023**.) (**Received IEEE ICC 2022 NSF Student Conference Grant Award**.) (First Employment: Texas A&M University – Texarkana)
7. A. Alkhodair, Ph.D.(Computer Science and Engineering), Dissertation: "Scalable Next Generation Blockchains For Large Scale Complex Cyber Physical Systems in Smart Cities", Department of Computer Science and Engineering, University of North Texas, Summer 2023. (First Employment: University of Tabuk, Saudi Arabia)
8. A. Mitra, Ph.D.(Computer Science and Engineering), Dissertation: "Machine Learning Methods for Data Quality Aspects in Edge Computing Platforms", Department of Computer Science and Engineering, University of North Texas, Fall 2022. (**Received Outstanding Ph.D. Student in Computer Science and Engineering Award for the Year 2022**.) (**Received IEEE INFOCOM 2022 Student Conference Grant Award**.) (**Received IEEE ICC 2022 NSF Student Conference Grant Award**.) (**Received Best Paper Award at the 19th OITS International Conference on Information Technology (OCIT) 2021**.) (First Employment: University of Nebraska-Lincoln)
9. L. Rachakonda, Ph.D.(Computer Science and Engineering), Dissertation: "IoMT-based Accurate Stress Monitoring for Smart Healthcare", Department of Computer Science and Engineering, University of North Texas, Spring 2021. (**Received the Best Paper Award at the IEEE-iSES 2019**.) (**Received Best Poster Award, with a cash prize of $500, at the 30th IEEE MetroCon Conference, 2017**.) (**Received Second Prize at the IEEE Brain Data Bank Challenge 2020**.) (First Employment: University of North Carolina at Wilmington)
10. I. "Tunde" Olokodana, Ph.D.(Computer Science and Engineering), Dissertation: "Kriging Methods to Exploit Spatial Correlations of EEG Signals for Fast and Accurate Seizure Detection in the IoMT", Department of Computer Science and Engineering, University of North Texas, Summer 2020. (**Received Second Prize at the IEEE Brain Data Bank Challenges and Competitions 2018**.) (**Received Best Poster Award, with a cash prize of $500, at the 31st IEEE MetroCon Conference, 2018**.) (First Employment: IBM Corporation)
11. M. A. Sayeed, Ph.D.(Computer Science and Engineering), Dissertation: "Epileptic Seizure Detection and Control in The Internet of Medical Things (IoMT) Framework", Department of Computer Science and Engineering, University of North Texas, Spring 2020. (**Received Best Poster Award, with a cash prize of $1000, at the 30th IEEE MetroCon Conference, 2018**.) (First Employment: Eastern New Mexico University)
12. V. P. Yanambaka, Ph.D.(Computer Science and Engineering), Dissertation: "Exploring Physical Unclonable Functions for Hardware-Assisted Efficient Security in the IoT", Department of Computer Science and Engineering, University of North Texas, Spring 2019. (**Received Best Poster Award, with a cash prize of $1000, at the 30th IEEE MetroCon Conference, 2017**.) (First Employment: Central Michigan University)
13. P. Sundaravadivel, Ph.D.(Computer Science and Engineering), Dissertation: "Application-Specific Things Architectures for IoT-based Smart Healthcare", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2018. (**Received Best Poster Award, with a cash prize of $500, at the 30th IEEE MetroCon Conference, 2017**.) (First Employment: University of Texas at Tyler)
14. U. Albalawi, Ph.D.(Computer Science and Engineering), Dissertation: "New Frameworks for Secure

Image Communication in the Internet of Things (IoT)", Department of Computer Science and Engineering, University of North Texas (UNT), Summer 2016. (First Employment: University of Tabuk, Saudi Arabia)

15. S. Joshi, Ph.D.(Computer Science and Engineering), Dissertation: "Analysis and Optimization of Graphene FET Based Integrated Circuits", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2016. (First Employment: Oklahoma State University)
16. O. Okobiah, Ph.D.(Computer Science and Engineering), Dissertation: "Geostatistical Inspired Metamodeling and Optimization of Nanoscale Analog Circuits", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2014. (**Received Outstanding Ph.D. student in Computer Science and Engineering Award for the year 2013-2014**.) (**Received scholarship for ACM A. M. Turing Centenary Celebration 2012**.) (**Received scholarship for ACM SIGDA Design Automation Summer School 2011**.) (First Employment: Samsung Semiconductor)
17. S. Nimgaonkar, Ph.D.(Computer Science and Engineering), Dissertation: "Secure and Energy Efficient Execution Frameworks Using Virtualization and Light-Weight Cryptographic Components", Department of Computer Science and Engineering, University of North Texas (UNT), Summer 2014. (First Employment: Cisco Systems, Inc.)
18. G. Zheng, Ph.D.(Computer Science and Engineering), Dissertation: "Layout-Accurate Ultra-Fast System Level Design Exploration Through Verilog-AMS", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2013. (**Received Outstanding Ph.D. student in Computer Science and Engineering Award for the year 2012-2013**.) (**Received scholarship for ACM A.M. Turing Centenary Celebration 2012**.) (**Received scholarship for ACM SIGDA Design Automation Summer School 2011**.) (First Employment: Analog Devices, Inc.)
19. O. Garitselov, Ph.D.(Computer Science and Engineering), Dissertation: "Metamodeling-Based Fast Optimization of Nanoscale AMS-SoCs", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2012. (**Received Outstanding Ph.D. student in Computer Science and Engineering Award for the year 2011-2012**.) (**Received scholarship for ACM SIGDA Design Automation Summer School 2011**.) (First Employment: Spectracom Corporation)
20. G. Thakral, Ph.D.(Computer Science and Engineering), Dissertation: "Process-Voltage-Temperature Aware Nanoscale Circuit Optimization", Department of Computer Science and Engineering, University of North Texas (UNT), Fall 2010. (**First UNT woman Computer Science and Engineering Ph.D. with VLSI specialization**.) (Current Position: Professor and Dean (Academics), Oriental University, Indore, India.)
21. D. V. Ghai, Ph.D.(Computer Science and Engineering), Dissertation: "Variability Aware Low-Power Techniques for Nanoscale Mixed-Signal Circuits", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2009. (**First UNT Computer Science and Engineering Ph.D. with VLSI specialization**.) (**Received 2019 UNT CSE Recent Alumni Award**.) (Current Position: Pro-Vice Chancellor and Professor of Electronics and Communication, Oriental University, Indore, India.)

Masters Theses Supervised or co-Supervised:

22. F. Alamri, M.S.(Computer Engineering), Thesis: "InoculLedger: Distributed Ledger based Secure and Scalable Solution for Efficient Vaccine Supply Chain Management", Department of Computer Science and Engineering, University of North Texas (UNT), Fall 2024. (First Employment: Joined Ph.D. Program.)
23. C. Dockendorf, M.S.(Computer Engineering), Thesis: "Lite-Agro: Integrating Federated Learning and TinyML on IoAT-Edge for Plant Disease Classification", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2024. (First Employment: Lockheed Martin.)
24. A. Alkinani, M.S.(Computer Engineering), Thesis: "FruitPAL: An IoT-Enabled Framework for

Automatic Monitoring of Fruit Consumption in Smart Healthcare", Department of Computer Science and Engineering, University of North Texas (UNT), Fall 2023. (First Employment: Joined Ph.D. Program.)

25. V. Dhayal, M.S.(Computer Science), Thesis: "Exploring Simscape™ Modeling for Piezoelectric Sensor Based Energy Harvester", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2017. (First Employment: North Carolina State University.)
26. N. Mukka, M.S.(Computer Engineering), Thesis: "Simulink® Based Modeling of A Multi Global Navigation Satellite System", Department of Computer Science and Engineering, University of North Texas (UNT), Summer 2016. (**Received Outstanding Master's student in Computer Engineering Award for the year 2015-2016**.) (First Employment: Sirius XM Radio Inc.)
27. G. Aluru, M.S.(Computer Engineering), Thesis: "Exploring Analog and Digital Design using the Open-source Electric VLSI Design System", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2016.
28. M. K. Mukka, M.S.(Computer Engineering), Thesis: "Simulink based Design and Implementation of a Solar Power based Mobile Charger", Department of Computer Science and Engineering, University of North Texas (UNT), Fall 2015. (First Employment: Zoro, Inc.)
29. M. L. Rajaram, M.S.(Electrical Engineering Technology), Thesis: "Comparative Analysis and Implementation of High Data Rate Wireless Sensor Network Simulation Frameworks", Department of Engineering Technology, University of North Texas (UNT), Fall 2015.
30. A. Hanson, M.S.(Computer Science), Thesis: "General Purpose Computing in GPU - A Watermarking Case Study", Department of Computer Science and Engineering, University of North Texas (UNT), Summer 2014. (First Employment: AGS Consultants, LLC.)
31. M. Gautam, M.S.(Computer Engineering), Thesis: "Exploring Memristor Based Analog Design in Simscape", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2013.
32. J. Franco, M.S.(Computer Engineering), Thesis: "Rapid Prototyping and Design of a Fast Random Number Generator", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2012. (First Employment: Raytheon Company.)
33. G. Coelho, M.S.(Engineering Systems), Thesis: "OTA-Quadrotor: An Object-Tracking Quadrotor for Real-Time Detection and Recognition", Department of Engineering Technology, University of North Texas (UNT), Spring 2012. (First Employment: Peterbilt Motors Company.)
34. O. Okobiah, M.S.(Computer Engineering), Thesis: "Exploring Process-Variation Tolerant Design of Nanoscale Sense Amplifier Circuits", Department of Computer Science and Engineering, University of North Texas (UNT), Fall 2010. (**Received Outstanding Master's student in Computer Engineering Award for the year 2010-2011**.) (First Employment: Joined Ph.D. Program.)
35. I. Zarate, M.S.(Engineering Systems), Thesis: "Software and Hardware in the Loop Modeling of an Audio Watermarking Algorithm", Department of Engineering Technology, University of North Texas (UNT), Fall 2010. (First Employment: Weatherford Inc.)
36. R. Rastogi Bani, M.S.(Computer Engineering), Thesis: "A New N-Way Reconfigurable Data Cache Architecture for Embedded Systems", Department of Computer Science and Engineering, University of North Texas (UNT), Fall 2009. (**Received Outstanding Master's student in Computer Engineering Award for year 2009-2010**.) (**Received International Education Committee Scholarship Award for the year 2009-2010**.) (First Employment: Center for Development of Advanced Computing (CDAC), Pune, India.)
37. S. Rangoonwala, M.S.(Engineering Systems), Thesis: "A Verilog 8051 Softcore for FPGA Applications", Department of Engineering Technology, University of North Texas (UNT), Spring 2009.
38. S. Naraharisetti, M.S.(Computer Engineering), Thesis: "Region Aware DCT Domain Invisible Robust Blind Watermarking for Color Images", Department of Computer Science and Engineering, University of North Texas (UNT), Fall 2008. (**Received Outstanding Master's student in**

Computer Engineering Award for the year 2008-2009.)

39. A. Mendoza, M.S.(Engineering Systems), Thesis: "Hardware Software Co-Design of a JPEG2000 Watermarking Encoder", Department of Engineering Technology, University of North Texas (UNT), Fall 2008. (First Employment: Olympus Controls.)
40. S. Tarigopula, M.S.(Computer Engineering), Thesis: "A CAM based High-Performance Classifier-Scheduler for a Video Network Processor", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2008. (**Received Outstanding Master's student in Computer Engineering Award for the year 2007-2008**.) (First Employment: GE.)
41. N. Pati, M.S.(Computer Engineering), Thesis: "Occlusion Tolerant Object Recognition Methods for Video Surveillance and Tracking of Moving Civilian Vehicles", Department of Computer Science and Engineering, University of North Texas (UNT), Fall 2007. (First Employment: FedEx.)
42. S. T. Vadlamudi, M.S.(Computer Engineering), Thesis: "A Nano-CMOS Based Universal Voltage Level Converter for Multi-V_{DD} SoCs", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2007.
43. A. Palakodety, M.S.(Computer Engineering), Thesis: "CMOS Active Pixel Sensors for Digital Cameras: Current State-of-the-Art", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2007. (First Employment: Vertex Pharmaceuticals.)
44. W. Cai, M.S.(Electronics Engineering Technology), Thesis: "FPGA Prototyping of a Watermarking Algorithm for MPEG-4", Department of Engineering Technology, University of North Texas (UNT), Spring 2007. (First Employment: Microsoft Corporation.)
45. G. Sarivisetti, M.S.(Computer Engineering), Thesis: "Design and Optimization of Components in a 45nm CMOS Phase Locked Loop", Department of Computer Science and Engineering, University of North Texas (UNT), Fall 2006. (**First UNT woman Computer Engineering graduate with VLSI specialization**.) (Current Employment: Walt Disney World.)
46. A. K. Ale, M.S.(Computer Engineering), Thesis: "Comparison and Evaluation of Existing Analog Circuit Simulators Through a Sigma-Delta Modulator", Department of Computer Science and Engineering, University of North Texas (UNT), Fall 2006. (First Employment: Texas Medical Center.)
47. O. B. Adamo, M.S.(Computer Engineering), Thesis: "VLSI Architecture and FPGA Prototyping of a Secure Digital Camera for Biometric Application", Department of Computer Science and Engineering, University of North Texas (UNT), Summer 2006. (**Third UNT Computer Engineering graduate with VLSI specialization**.) (First Employment: Joined Ph.D. Program.)
48. R. Velagapudi, M.S.(Computer Engineering), Thesis: "Modeling and Reduction of Gate Leakage during Behavioral Synthesis of NanoCMOS Datapath Circuits", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2006. (**Second UNT Computer Engineering graduate with VLSI specialization**.)
49. V. Mukherjee, M.S.(Computer Engineering), Thesis: "A Dual Dielectric Approach for Performance Aware Reduction of Gate Leakage in Combinational Circuits", Department of Computer Science and Engineering, University of North Texas (UNT), Spring 2006. (**First UNT Computer Engineering graduate with VLSI specialization**.) (**Received 2019 UNT CSE Recent Alumni Award**.) (First Employment: Amdocs Inc.)
50. C. Renuka Kumara, Masters of Science in VLSI CAD, Thesis: "VLSI Implementation of Invisible Robust/Fragile Digital Watermarking Algorithms", Manipal Centre for Information Science, Manipal Academy of Higher Education, India, Spring 2004. (I remotely guided the master's thesis.) (First Employment: Synopsys India.)

Undergraduate Students Mentored:

51. A. Mazumder, Texas Academy of Math and Science (TAMS), Spring 2024 – Fall 2025. (**Received Undergraduate Research Fellowship (URF) for the Year 2024-2025**.) (**Received Best Under-**

graduate Poster Award at the IEEE MetroCon Conference 2024.) (**Top 300 Finalists for the Regeneron Science Talent Search in 2025 to Receive a Cash Prize of $2,000**.)

52. A. Kumar, Texas Academy of Math and Science (TAMS), Fall 2023 – Fall 2025. (**Received Undergraduate Research Fellowship (URF) for the Year 2024-2025**.)
53. V. Gollapalli, Texas Academy of Math and Science (TAMS), Fall 2024 – Spring 2025.
54. A. Kanakamedala, Texas Academy of Math and Science (TAMS), Fall 2024 – Spring 2025.
55. N. Subhash, Texas Academy of Math and Science (TAMS), Fall 2024 – Spring 2025.
56. S. Jasti, Texas Academy of Math and Science (TAMS), Fall 2024 – Spring 2025.
57. S. Narra, Texas Academy of Math and Science (TAMS), Fall 2024 – Spring 2025.
58. P. Jampana, Marcus High School, Spring 2024 – Spring 2025.
59. M. Narra, Issaquah High School, Spring 2024 – Spring 2025.
60. G. Praveen, B.E. (Computer Science), M. S. Ramaiah Institute of Technology (MSRIT), India, Fall 2024.
61. S. Agarwal, Texas Academy of Math and Science (TAMS), Summer 2024 – Fall 2024.
62. A. Mungale, Texas Academy of Math and Science (TAMS), Spring 2024 – Fall 2024.
63. S. Sattiraju, Texas Academy of Math and Science (TAMS), Summer 2024 – Fall 2024.
64. A. Thebe, B.S. (Cybersecurity), University of North Texas, Summer 2024 – Fall 2024.
65. D. Raajeev, Round Rock High School, Spring 2024 – Fall 2024.
66. A. Lella, Texas Academy of Math and Science (TAMS), Spring 2024 – Fall 2024.
67. S. Shah, B. Tech. (Electronics and Instrumentation), Nirma University, Summer 2024.
68. S. Rout, B. Tech. (Computer Science), Indian Institute of Technology Madras (IITM), Fall 2023 – Spring 2024. (**Selected to JP Morgan Chase & Co. Quantitative Mentorship Program**.) (**Received Texas Instrument Embedded Software WiSH Scholarship**.) (**Received Bain & Company True North Scholarship**.)
69. S. S. Panigrahi, B. Tech. (Information Technology), Rajiv Gandhi Institute of Petroleum Technology (RGIPT), Fall 2023 – Spring 2024.
70. P. Mittal, B. Tech. (Computer Science), Kalinga Institute of Industrial Technology (KIIT), Spring 2023 – Spring 2024.
71. A. Gupta, Texas Academy of Math and Science (TAMS), Spring 2023 – Spring 2024.
72. R. Rajan, Texas Academy of Math and Science (TAMS), Fall 2022 – Spring 2024.
73. S. Goel, Texas Academy of Math and Science (TAMS), Fall 2022 – Spring 2023. (**Received Barry M. Goldwater Scholarship in 2024**.) (**Top 40 Finalists for the Regeneron Science Talent Search in 2024 to Receive a Cash Prize of $25,000**.)
74. M. Huang, Texas Academy of Math and Science (TAMS), Spring 2022 – Summer 2022.
75. J. Toney, B.S. (Computer Engineering), Spring 2022.
76. A. Singhal, Texas Academy of Math and Science (TAMS), Fall 2021.
77. N. Madireddi, Texas Academy of Math and Science (TAMS), Summer 2020.
78. P. Rajkumar, Texas Academy of Math and Science (TAMS), Fall 2019.
79. B. Hart, B.S. (Computer Engineering), Fall 2019.
80. J. Choi, Texas Academy of Math and Science (TAMS), Fall 2019.
81. A. Sharma, Texas Academy of Math and Science (TAMS), Spring 2019 – Fall 2019.
82. A. Kothari, Texas Academy of Math and Science (TAMS), Fall 2017 – Spring 2019.
83. E. Zhou, Texas Academy of Math and Science (TAMS), Spring 2018 – Summer 2018.
84. I. Lee, Texas Academy of Math and Science (TAMS), Spring 2017.
85. M. Behnia, Texas Academy of Math and Science (TAMS), Spring 2014 – Summer 2014.
86. J. E. Barcenas, B.S.(Computer Engineering), University of North Texas, Fall 2013 – Spring 2014.
87. R. A. Cerrato, B.S.(Computer Engineering), University of North Texas, Spring 2014.
88. T. Ali, B.S.(Computer Engineering), University of North Texas, Spring 2013.
89. T. T. Jost, B.S.(Pre Engineering), University of North Texas, Fall 2012 – Spring 2013.

90. R. Patel, B.S.(Computer Engineering), University of North Texas, Spring 2011.
91. J. Judge, Texas Academy of Math and Science (TAMS), Fall 2010.

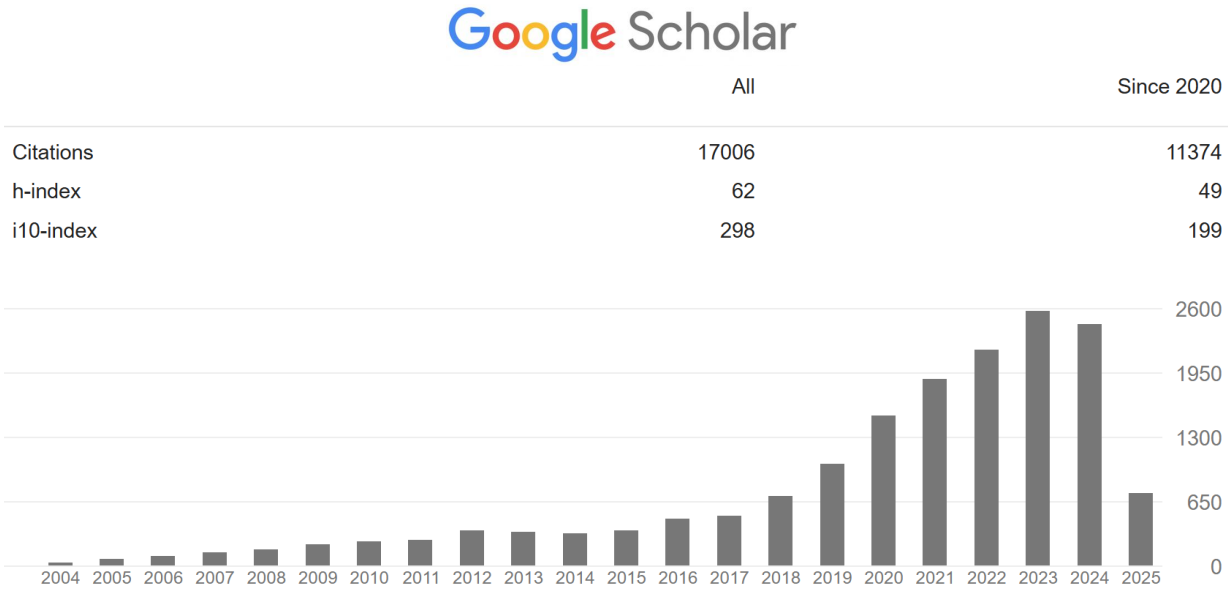
GRANTS and PROJECTS

No.	Project Title	Agency	Total Amount	Duration	Role
34	Discovering Capabilities for Community Living and Participation for Older Adults with Autism Spectrum Disorder	NIDILRR	$599,992	2024-2027	Co-PI
33	iMed-Sec: Exploring Hardware-Assisted Solutions for Energy-Efficient Low-Overhead Security and Privacy for the Internet-of-Medical-Things	NSF	$499,500 (UNT - $200,000)	2021-2026	Co-PI
32	NSF Student Travel Grant for 2024 IEEE Computer Society International Symposium on VLSI (IEEE ISVLSI)	NSF	$20,000	2024-2026	PI
31	Easy-Med: Interdisciplinary Training in Security, Privacy-Assured Internet of Medical Things	NSF	$495,970 (UNT - $247,373)	2019-2023	PI
30	Design and development of System on Chip based next generation IoT System for Industry 4.0 with Functional Safety and Security Features	Ministry of Electronics and IT (MeitY), India	$580,000 (Estimated)	2023-2028	SP
29	Methods for Cybersecurity in AI-Enabled Smart Systems	Saudi Arabian Cultural Mission (SACM)	$130,000 (Estimated)	2021-2025	SP
28	Distributed Ledgers for Smart City Applications	Saudi Arabian Cultural Mission (SACM)	$130,000 (Estimated)	2021-2025	SP
27	Security, Communication and Interoperability in LPWAN for IoT	Bureau of Educational and Cultural Affairs at US Department of State (Fulbright)	$12,000 (Estimated)	2023	PI

No.	Project Title	Agency	Total Amount	Duration	Role
26	Scalable Next Generation Blockchains for Large Scale Complex Cyber-Physical Systems	Saudi Arabian Cultural Mission (SACM)	$130,000 (Estimated)	2019-2023	SP
25	NSF Student Travel Grant for 2019 IEEE Computer Society International Symposium on VLSI (IEEE ISVLSI)	NSF	$10,000	2019-2022	PI
24	Development of Smart Adulteration Detection System for Vegetables/Fruits in Food Supply Chain Management System	SERB, India	$18,000 (Estimated)	2022	SP
23	Mix-Energy-Source Electric Vehicle Charging System Design and its Impact on Indian Smart-Distribution-Grid	Mission Innovation, India	$518,000 (Estimated)	2018-2021	SP
22	Technical Committee on VLSI (TCVLSI)	IEEE-CS	$13,840	2018	PI
21	Technical Committee on VLSI (TCVLSI)	IEEE-CS	$11,977	2017	PI
20	Memory Design Optimization for Low-Latency Embedded Vision Processor (LLEVS)	Air Force STTR (NanoWatt Design Inc.)	$150,000 (UNT - $45,000)	2015-2016	PI
19	Exploring Emerging Technology based Energy Efficient IoT Sensors for Smart Cities	IUSSTF	$25,000	2016	SP
18	Technical Committee on VLSI (TCVLSI)	IEEE-CS	$15,312	2016	PI
17	New Frameworks for Secure Image Communication in the Internet of Things (IoT)	Saudi Arabian Cultural Mission (SACM)	$80,000 (Estimated)	2014-2016	SP
16	International Outreach for Nanoelectronic and Information Systems	IEEE-CASS	$2,000	2015	PI
15	Technical Committee on VLSI (TCVLSI)	IEEE-CS	$6,400	2015	PI
14	Power and Thermal Aware Design of 3D ICs and Network-on-Chips	UGC, India	$50,000 (Estimated)	2013-2014	SP
13	Introduction of Nanoelectronics Courses in Undergraduate Computer Science and Computer Engineering Curricula	NSF	$180,000 (UNT - $90,000)	2010-2013	PI
12	Infrastructure Acquisition for Statistical Power, Leakage, and Timing Modeling Towards Realization of Robust Complex Nanoelectronics Circuits	NSF	$269,265 ($20,000 match)	2009-2012	PI
11	Fast PVT-Tolerant Physical Design of RF IC Components	SRC	$134,140	2009-2012	PI
10	Process Variation Aware Synthesis of Nano-CMOS Circuits	EPSRC, UK	$400,000 (Estimated)	2009-2012	SP

No.	Project Title	Agency	Total Amount	Duration	Role
09	International Symposium on Electronic System Design (ISED)	NSF	$14,000 ($4,000 match)	2010-2011	PI
08	A Comprehensive Methodology for Early Power-Performance Estimation of Nano-CMOS Digital Systems	NSF	$200,000 (UNT - $112,764)	2007-2010	PI
07	Asian Faculty Mentoring Network UNT Team Mentoring Grants	UNT	$2,000	2015-2016	Co-PI
06	Nanoelectronics Unified Fault Modeling and Experimentation - From Devices to Systems	UNT	$24,000	2008-2009	PI
05	Watermarking Algorithms for Real-Time Copyright Protection and Subtitling during Digital Video Broadcasting in Internet Protocol TV (IP-TV)	UNT	$5,000	2008-2009	PI
04	Secure Digital Camera (SDC) for Biometric Authentication	UNT	$5,000	2007	PI
03	VLSI Architecture and Implementation of a Digital Video Broadcasting Network Processor (VNP) with Digital Rights Management (DRM) Facility	UNT	$5,000	2006	PI
02	Leakage Current Reduction in Nanometer VLSI Circuits using Dual Gate Dielectrics	UNT	$4,000	2005-2006	PI
01	A Low Power Smart VLSI Controller for Nano-Characterization in Atomic Force Microscope (AFM)	UNT	$5,000	2005	PI

PI: Principal Investigator, Co-PI: Co-Principal Investigator, SP: Senior Personnel



Citations received by my articles as calculated by the Google Scholar.

PATENTS

1. **S. P. Mohanty**, E. Kougianos, and A. Mitra, System to Assist Farmers, USA Patent Application Number: 18/755,561, Filed on: 28 June 2024.
2. **S. P. Mohanty**, E. Kougianos, and A. Mitra, Method for Synthetic Video/Image Detection, USA Patent Application Number: 18/485,285, Filed on: 11 Oct 2023.
3. **S. P. Mohanty**, E. Kougianos, and L. Rachakonda, System and Method For Monitoring A State of A Driver, USA Patent Application Number: 18/185,717, Filed on: 17 March 2023.
4. **S. P. Mohanty**, E. Kougianos, and L. Rachakonda, Intelligent Diet, Sleep and Stress Management, USA Patent Application Number: 17/540,076, Filed on: 01 Dec 2021.
5. A. K. Tripathy, P. K. Tripathy, N. K. Ray, and **S. P. Mohanty**, IoT Based Personal Security System, India Patent Application Number: 202111004091, Filed on: 29 January 2021.
6. A. M. Joshi, P. Jain, and **S. P. Mohanty**, A Device For Non-Invasive Blood and Serum Glucose-Level Monitoring and Control, India Patent Number: 518131, Issued on: 05 March 2024.
7. **S. P. Mohanty** and E. Kougianos, Methodology for Nanoscale Technology based Mixed-Signal System Design, USA Patent Number: 9053276, Issued on: 09 June 2015.
8. **S. P. Mohanty**, E. Kougianos, and G. Zheng, Intelligent Metamodel Integrated Verilog-AMS for Fast and Accurate Analog Block Design Exploration, USA Patent Number: 9026964, Issued on: 05 May 2015.
9. **S. P. Mohanty**, Apparatus and Method for Transmitting Secure and/or Copyrighted Digital Video Broadcasting Data Over Internet Protocol Network, USA Patent Number: 8423778, Issued on: 16 Apr 2013.
10. **S. P. Mohanty**, Methods and Devices for Enrollment and Verification of Biometric Information in Identification Documents, USA Patent Number: 8058972, Issued on: 15 Nov 2011.

BOOKS

1. D. Puthal, **S. P. Mohanty**, and B. -Y. Choi (Editors), Internet of Things - Advances in Information and Communication Technology, Proceedings of 6th IFIP International Cross-Domain Conference - IFIP-IoT 2023 - Part I, Springer Cham, 2024, ISBN: 978-3-031-45880-4.
2. D. Puthal, **S. P. Mohanty**, and B. -Y. Choi (Editors), Internet of Things - Advances in Information and Communication Technology, Proceedings of 6th IFIP International Cross-Domain Conference - IFIP-IoT 2023 - Part II, Springer Cham, 2024, ISBN: 978-3-031-45884-2.
3. N. Panigrahi and **S. P. Mohanty**, Brain Computer Interface: EEG Signal Processing, CRC Press, 2022, ISBN: 978-1032148410.
4. A. Sengupta and **S. P. Mohanty**, IP Core Protection and Hardware-Assisted Security for Consumer Electronics, The Institute of Engineering and Technology (IET), 2019, ISBN: 978-1785617997.
5. **S. P. Mohanty**, Nanoelectronic Mixed-Signal System Design, McGraw-Hill, 2015, ISBN-10: 0071825711, ISBN-13: 978-0071825719.
6. J. Singh, **S. P. Mohanty**, and D. K. Pradhan, Robust SRAM Designs and Analysis, Springer, 2012, ISBN-10: 1461408172, ISBN-13: 978-1461408178.
7. **S. P. Mohanty**, N. Ranganathan, E. Kougianos, and P. Patra, Low-Power High-Level Synthesis for Nanoscale CMOS Circuits, Springer, 2008, ISBN-10: 0387764739, ISBN-13: 978-0387764733.
8. A. Srivastava and **S. P. Mohanty** (Editors), Advanced Technologies for Next Generation Integrated Circuits, The Institute of Engineering and Technology (IET), 2020, ISBN-10: 1785616641, ISBN-13: 978-1785616648.
9. **S. P. Mohanty** and A. Srivastava (Editors), Nano-CMOS and Post-CMOS Electronics: Devices and Modelling, The Institute of Engineering and Technology (IET), 2016, ISBN-10: 1849199973, ISBN-13: 978-1849199971.
10. **S. P. Mohanty** and A. Srivastava (Editors), Nano-CMOS and Post-CMOS Electronics: Circuits and Design, The Institute of Engineering and Technology (IET), 2016, ISBN-10: 184919999X, ISBN-13:

978-1849199995.

11. **S. P. Mohanty**, A. Singh, and B. Panda (Editors), Proceedings of 12th International Conference on Information Technology (ICIT), McGraw-Hill, 2009, ISBN: 978-0-07-068014-2.

BOOK CHAPTERS

1. V. P. Yanambaka, **S. P. Mohanty**, E. Kougianos, and D. Ghai, "Memristor Devices and Memristor-based Circuits", in Advanced Technologies for Next Generation Integrated Circuits, Edited by A. Srivastava and S. P. Mohanty, The Institute of Engineering and Technology (IET), 2020, ISBN-10: 1785616641, ISBN-13: 978-1785616648.
2. A. Sengupta and **S. P. Mohanty**, "High-Level Synthesis of Digital Integrated Circuits in the Nanoscale Mobile Electronics Era", in Nano-CMOS and Post-CMOS Electronics: Circuits and Design, Edited by S. P. Mohanty and A. Srivastava, The Institute of Engineering and Technology (IET), 2016, ISBN-10: 184919999X, ISBN-13: 978-1849199995.
3. E. Kougianos and **S. P. Mohanty**, "SPICEless RTL Design Optimization of Nanoelectronic Digital Integrated Circuits", in Nano-CMOS and Post-CMOS Electronics: Circuits and Design, Edited by S. P. Mohanty and A. Srivastava, The Institute of Engineering and Technology (IET), 2016, ISBN-10: 184919999X, ISBN-13: 978-1849199995.
4. V. P. Yanambaka, **S. P. Mohanty**, E. Kougianos, and D. Ghai, "Nanoscale High-κ/Metal-Gate CMOS and FinFET based Logic Libraries", in Nano-CMOS and Post-CMOS Electronics: Devices and Modelling, Edited by S. P. Mohanty and A. Srivastava, The Institute of Engineering and Technology (IET), 2016, ISBN-10: 1849199973, ISBN-13: 978-1849199971.
5. **S. P. Mohanty** and E. Kougianos, "Polynomial Metamodel-Based Fast Optimization of Nanoscale PLL Components", in Models, Methods, and Tools for Complex Chip Design: Selected Contributions from FDL 2012, Edited by J. Haase, Springer, 2014, ISBN: 978-3-319-01417-3.
6. B. Joshi, D. K. Pradhan, and **S. P. Mohanty**, "Fault Tolerant Nano-Computing", in Robust Computing with Nano-scale Devices: Progresses and Challenges, Edited by C. Huang, Springer, 2010, ISBN: 978-90-481-8539-9.

JOURNAL ARTICLES

Year 2025:

1. S. K. Ram, S. R. Sahoo, B. B. Das, K. K. Mahapatra, and **S. P. Mohanty**, "sThing: A Novel Configurable Ring Oscillator based PUF for Hardware-Assisted Security and Recycled IC Detection", *IEEE Access Journal (Access)*, Vol. 13, Jan 2025, pp. 2994–3013.
2. B. Hildebrand, A. Ghimire, F. Amsaad, A. Razaque, and **S. P. Mohanty**, "Quantum Communication Networks: Design, Reliability, and Security", *IEEE Potentials Magazine (MPOT)*, Vol. 44, No. 1, Jan-Feb 2025, pp. 4–10.
3. V. K. V. V. Bathalapalli , **S. P. Mohanty**, C. Pan, and E. Kougianos, "QPUF: Quantum Physical Unclonable Functions for Security-by-Design of Industrial Internet-of-Things", *MDPI Cryptography*, Vol. XXX, No. YYY:ZZZ, Accepted on 22 May 2025, 19-pages.
4. D. Puthal, A. K. Mishra, **S. P. Mohanty**, A. Longo, and C. Y. Yeun, "Shadow AI: Cyber Security Implications, Opportunities and Challenges in the Unseen Frontier", *Springer Nature Computer Science (SN-CS)*, Vol. 6, No. 5, June 2025, Article: 405.
5. M. N. Alruwaill, **S. P. Mohanty**, and E. Kougianos, "hChain 2.0: Leveraging Blockchain and Distributed File System for EHR Management in Smart Healthcare", *Springer Nature Computer Science (SN-CS)*, Vol. 6, No. 1, Jan 2025, Article: 116.
6. P. Mohanty, U. C. Pati, K. K. Mahapatra, and **S. P. Mohanty**, "bSlight 2.0: Battery-free Sustainable Smart Street Light Management System", *IEEE Transactions on Sustainable Computing (TSUSC)*, Vol. 10, No. 1, Jan-Feb 2025, pp. 146–160.
7. M. N. Alruwaill, **S. P. Mohanty**, and E. Kougianos, "hChain: Blockchain Based Large Scale EHR

Data Sharing with Enhanced Security and Privacy", *arXiv Computer Science*, arXiv:2505.12610, May 2025, 23-pages.

8. M. N. Alruwaill, **S. P. Mohanty**, and E. Kougianos, "hChain 4.0: A Secure and Scalable Permissioned Blockchain for EHR Management in Smart Healthcare", *arXiv Computer Science*, arXiv:2505.13861, May 2025, 21-pages.
9. D. Puthal, A. K. Mishra, **S. P. Mohanty**, A. Longo, and C. Y. Yeun, "Shadow AI: Cyber Security Implications, Opportunities and Challenges in the Unseen Frontier", *ResearchGate*, DOI: 10.13140/RG.2.2.19510.61760, Mar 2025, 13-pages.
10. A. Alkinani, A. Mitra, **S. P. Mohanty**, and E. Kougianos, "FruitPAL: An IoT-Enabled Framework for Automatic Monitoring of Fruit Consumption in Smart Healthcare", *arXiv Computer Science*, arXiv:2502.01643, Jan 2025, 22-pages.

Year 2024:

11. V. K. V. V. Bathalapalli, **S. P. Mohanty**, E. Kougianos, V. Iyer, and B. Rout, "PUFchain 3.0: Hardware-Assisted Distributed Ledger for Robust Authentication in the Healthcare Cyber-Physical Systems", *MDPI Sensors*, Vol. 24, No. 3, Jan 2024, pp. 938:1–938:29.
12. A. K. Bapatla, **S. P. Mohanty**, and E. Kougianos, "PharmaChain 3.0: Efficient Tracking and Tracing of Drugs in Pharmaceutical Supply Chain using Blockchain Integrated Product Serialization Mechanism", *Springer Nature Computer Science (SN-CS)*, Vol. 5, No. 1, Jan 2024, Article: 149, 22-pages.
13. V. S. Rathor, M. Singh, K. S. Sahoo, and **S. P. Mohanty**, "GateLock: Input Dependent Key-based Locked Gates for SAT Resistant Logic Locking", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 32, No. 2, Feb 2024, pp. 361–371.
14. G. Sharma, A. M. Joshi, and **S. P. Mohanty**, "sTrade 2.0: Efficient Mutual Authentication Scheme for Energy Trading in V2G using Physically Unclonable Function", *IEEE Journal of Emerging and Selected Topics in Industrial Electronics (JESTIE)*, Vol. 5, No. 4, Oct 2024, pp. 1549–1559.
15. B. B. Das, S. K. Ram, K. S. Babu, R. K. Mohapatra, and **S. P. Mohanty**, "Person Identification using Autoencoder-CNN Approach with Multitask-based EEG Biometric", *Springer Multimedia Tools and Applications (MTAP)*, Vol. 83, No. 35, October 2024, pp. 83205–83225.
16. S. C. Sethuraman, G. R. Tadkapally, A. Kiran, **S. P. Mohanty**, and A. Subramanian, "SimplyMime: A Dynamic Gesture Recognition and Authentication System for Smart Remote Control", *IEEE Sensors Journal*, Vol. 24, No. 24, 15 Dec 2024, pp. 42472–42483.
17. M. A. Sayeed, F. Nasrin, **S. P. Mohanty**, and E. Kougianos, "eSeiz 2.0: An Optimized Pulse Exclusion Mechanism for Accurate and Energy Efficient Seizure Detection in the IoMT", *Springer Nature Computer Science (SN-CS)*, Vol. 5, No. 1, Jan 2024, Article: 165, 11-pages.
18. K. Patel, A. K. Tripathy, L. N. Padhy, S. K. Kar, S. K. Padhy, and **S. P. Mohanty**, "Accu-Help: A Machine Learning based Smart Healthcare Framework for Accurate Detection of Obsessive Compulsive Disorder", *Springer Nature Computer Science (SN-CS)*, Vol. 5, No. 1, Jan 2024, Article: 36, 19-pages.
19. P. Mohanty, U. C. Pati, K. K. Mahapatra, and **S. P. Mohanty**, "bSlight: Battery-less Energy Autonomous Street Light Management System for Smart City", *IEEE Transactions on Sustainable Computing (TSUSC)*, Vol. 9, No. 1, Jan-Feb 2024, pp. 100–114.
20. P. Maurya, V. M. R. Tummala, A. Hazra, and **S. P. Mohanty**, "Advancing Industry 5.0 With UAV-Driven Transformations: Future Prospectives", *IEEE Consumer Electronics Magazine (CEM)*, Vol. 13, No. 5, Sep 2024, pp. 30–35.
21. A. Mitra, S. L. T. Vangipuram, A. K. Bapatla, V. K. V. V. Bathalapalli, **S. P. Mohanty**, E. Kougianos, and C. Ray, "Smart Agriculture: A Comprehensive Overview", *Springer Nature Computer Science (SN-CS)*, Vol. 5, No. 8, Oct 2024, Article: 969.
22. P. Jain, A. M. Joshi, and **S. P. Mohanty**, "iGLU 4.0: Intelligent Non-Invasive Glucose Measurement

and Its Control with Physiological Parameters", *Springer Nature Computer Science (SN-CS)*, Vol. 5, No. 1, Mar 2024, Article: 368, 13-pages.

23. P. Jain, A. M. Joshi, **S. P. Mohanty**, and L. R. Cenkeramaddi, "Non-invasive Glucose Measurement Technologies: Recent Advancements and Future Challenges", *IEEE Access Journal*, Vol. 12, Apr 2024, pp. 61907–61936.
24. N. Sinha, A. M. Joshi, and **S. P. Mohanty**, "iCardo 3.0: ECG-based Prediction of Conduction Disturbances using Demographic Features", *Springer Nature Computer Science (SN-CS)*, Vol. 5, No. 1, Mar 2024, Article: 382, 13-pages.
25. A. Sharma, A. Jain, S. Sharma, A. Gupta, P. Jain, and **S. P. Mohanty**, "iPAL: A Machine Learning based Smart Healthcare Framework for Automatic Diagnosis of Attention Deficit/Hyperactivity Disorder", *Springer Nature Computer Science (SN-CS)*, Vol. 5, No. 1, Apr 2024, Article: 433, 19-pages.
26. V. K. V. V. Bathalapalli, **S. P. Mohanty**, C. Pan, and E. Kougianos, "QPUF 2.0: Exploring Quantum Physical Unclonable Functions for Security-by-Design of Energy Cyber-Physical Systems", *arXiv Quantum Physics*, arXiv:2410.12702, Oct 2024, 26-pages.
27. A. Mitra, **S. P. Mohanty**, and E. Kougianos, "The World of Generative AI: Deepfakes and Large Language Models", *arXiv Computer Science*, arXiv:2402.04373, Feb 2024, 9-pages.
28. V. S. Rathor, M. Singh, K. S. Sahoo, and **S. P. Mohanty**, "SubLock: Sub-Circuit Replacement based Input Dependent Key-based Logic Locking for Robust IP Protection", *arXiv Computer Science*, arXiv:2406.19091, June 2024, 22-pages.
29. K. K. Kethineni, **S. P. Mohanty**, E. Kougianos, S. Bhowmick, and L. Rachakonda, "SprayCraft: Graph-Based Route Optimization for Variable Rate Precision Spraying", *arXiv Computer Science*, arXiv:2412.12176, Dec 2024, 28-page.
30. M. Veeramreddy, A. K. Pradhan, S. Ghanta, L. Rachakonda, and **S. P. Mohanty**, "NutriVision: A System for Automatic Diet Management in Smart Healthcare", *arXiv Computer Science*, arXiv:2409.20508, Oct 2024, 25-page.
31. P. Maji, A. K. Mondal, H. K. Mondal, and **S. P. Mohanty**, "EasyDiagnos: A Framework for Accurate Feature Selection for Automatic Diagnosis in Smart Healthcare", *arXiv Computer Science*, arXiv:2410.00366, Oct 2024, 21-pages.
32. P. Mohanty, U. C. Pati, K. K. Mahapatra, and **S. P. Mohanty**, "Everything You Wanted to Know About Consumer Light Management in Smart Energy", *arXiv Computer Science*, arXiv:2411.08353, Nov 2024, 39-pages.
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to Monitor Blood Alcohol Concentration using Physiological Signals", in *Proceedings of the 38th IEEE International Conference on Consumer Electronics (ICCE)*, 2020.

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123. I. L. Olokodana, **S. P. Mohanty**, E. Kougianos, and M. Manzo, "Photonic Sensor Based Real-Time and Low-Noise IoT-Enabled Brain-Computer Interface (BCI)", Poster, in *45th National Society of Black Engineers (NSBE) Annual Convention*, Detroit MI, March 27-31, 2019. (**Selected among top 10 finalists out of over 60 participants.**)

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125. I. L. Olokodana, **S. P. Mohanty**, E. Kougianos, and M. Manzo, "Towards Photonic Sensor based Brain-Computer Interface (BCI)", in *Proceedings of the 4th IEEE International Smart Cities Conference (ISC2)*, 2018.
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135. L. Rachakonda, P. Sundaravadivel, **S. P. Mohanty**, E. Kougianos, and M. Ganapathiraju, "A Smart Sensor in the IoMT for Stress Level Detection", in *Proceedings of the 4th IEEE International Symposium on Smart Electronic Systems (iSES)*, 2018, pp. 141–145.
136. M. A. Sayeed, **S. P. Mohanty**, E. Kougianos, and H. P. Zaveri, "iDDS: An IoT based System for Refractory Epilepsy in Smart Healthcare", Poster, *IEEE MetroCon 2018 Conference*, November 07, 2018. (**Awarded Best Student Poster of the Conference with a cash prize of $1000.**)
137. I. L. Olokodana, **S. P. Mohanty**, E. Kougianos, and M. Manzo, "Real Time Monitoring of Electric Field Via Photonic Sensing For Effective Brain-computer Interface (BCI)", Poster, *IEEE MetroCon 2018 Conference*, November 07, 2018. (**Awarded Second Best Student Poster of the Conference with a cash prize of $500.**)
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139. V. P. Yanambaka, **S. P. Mohanty**, and E. Kougianos, "Hybrid Oscillator Arbiter PUF Using Manufacturing Variations for Robust Security in the Internet of Things", Poster, *International Workshop on Design Automation for Analog and Mixed-Signal Circuits, ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, November 08, 2018.
140. V. P. Yanambaka, **S. P. Mohanty**, and E. Kougianos, "Reconfigurable HOA-PUF Using Manufacturing Variations for Efficient Security in the Internet of Things", Poster, *International Workshop on Design Automation for Analog and Mixed-Signal Circuits, ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, November 08, 2018.
141. M. A. Sayeed, **S. P. Mohanty**, E. Kougianos, and H. Zaveri, "An Edge-Device for Accurate Seizure Detection in the IoT", Poster, *2nd Annual Texas Symposium on Computing with Emerging Technologies (ComET)*, 23rd April, 2018.
142. V. P. Yanambaka, **S. P. Mohanty**, and E. Kougiano, "PUFs Using Manufacturing Variations for Robust Security in the IoT", Poster, *2nd Annual Texas Symposium on Computing with Emerging Technologies (ComET)*, 23rd April, 2018.

Year 2017:

143. V. P. Yanambaka, **S. P. Mohanty**, E. Kougianos, P. Sundaravadivel, and J. Singh, "Reconfigurable Robust Hybrid Oscillator Arbiter PUF for IoT Security based on DL-FET", in *Proceedings of the 16th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2017, pp. 665–670.

144. V. P. Yanambaka, **S. P. Mohanty**, E. Kougianos, P. Sundaravadivel, and J. Singh, "Dopingless Transistor Based Hybrid Oscillator Arbiter Physical Unclonable Function", in *Proceedings of the 16th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2017, pp. 609–614.
145. Z. Zhao, X. Chen, A. Srivastava, L. Peng, and **S. P. Mohanty**, "Compact Modeling of Graphene Barristor for Digital Integrated Circuit Design", in *Proceedings of the 16th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2017, pp. 562–567.
146. V. P. Yanambaka, **S. P. Mohanty**, and E. Kougianos, "Energy-Efficient Physical Unclonable Functions for Secure IoT Environment", Poster, *IEEE MetroCon 2017 Conference*, October 26, 2017. (**Awarded Best Student Poster of the Conference with a cash prize of $1000.**)
147. L. Rachakonda, P. Sundaravadivel, **S. P. Mohanty**, and E. Kougianos, "I-Stress: A Stress Monitoring System through the IoT", Poster, *IEEE MetroCon 2017 Conference*, October 26, 2017. (**Awarded Second Best Student Poster of the Conference with a cash prize of $500.**)

Year 2016:

148. U. Albalawi, **S. P. Mohanty**, and E. Kougianos, "Energy-Efficient Design of the Secure Better Portable Graphics Compression Architecture for Trusted Image Communication in the IoT", in *Proceedings of the 15th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2016, pp. 302–307.
149. P. Sundaravadivel, **S. P. Mohanty**, E. Kougianos, V. P. Yanambaka, H. Thapliyal, "Exploring Human Body Communications for IoT Enabled Ambulatory Health Monitoring Systems", in *Proceedings of the 2nd IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, 2016, pp. 17–22.
150. U. Albalawi, **S. P. Mohanty**, and E. Kougianos, "SBPG: A Secure Better Portable Graphics Compression Architecture for High Speed Trusted Image Communication in IoT", in *Proceedings of the 17th IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, 2016, pp. 1–5.
151. A. Sengupta, S. Bhadauria, and **S. P. Mohanty**, "Embedding Low Cost Optimal Watermark During High Level Synthesis for Reusable IP Core Protection", in *Proceedings of the 48th IEEE International Symposium on Circuits and Systems (ISCAS)*, 2016, pp. 974–977.
152. V. P. Yanambaka, **S. P. Mohanty**, and E. Kougianos, "Novel FinFET based Physical Unclonable Functions for Efficient Security Integration in the IoT", in *Proceedings of the 2nd IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, 2016, pp. 172–177.
153. P. Sundaravadivel, **S. P. Mohanty**, E. Kougianos, and U. Albalawi, "An Energy Efficient Sensor for Thyroid Monitoring through IoT", in *Proceedings of the 17th IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, 2016, pp. 1–4.
154. V. P. Yanambaka, **S. P. Mohanty**, E. Kougianos, and J. Singh, "Secure Multi-Key Generation Using Ring Oscillator based Physical Unclonable Function", in *Proceedings of the 2nd IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, 2016, pp. 200–205.
155. M. L. Rajaram, E. Kougianos, **S. P. Mohanty**, and P. Sundaravadivel, "A Wireless Sensor Network Simulation Framework for Structural Health Monitoring in Smart Cities", in *Proceedings of the 6th IEEE International Conference on Consumer Electronics - Berlin (ICCE-Berlin)*, 2016, pp. 78–82.
156. A. Bose, P. Ghosal, and **S. P. Mohanty**, "STA: A Highly Scalable Low Latency Butterfly Fat Tree Based 3D NoC Design", in *Proceedings of the 15th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2016, pp. 496–501. (**blind review**)
157. M. Panchore, J. Singh, **S. P. Mohanty**, and E. Kougianos, "Compact Behavioral Modeling and Time Dependent Performance Degradation Analysis of Junction and Doping Free Transistors", in *Proceedings of the 2nd IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, 2016, pp. 194–199.

158. Z. Zhao, A. Srivastava, L. Peng, and **S. P. Mohanty**, "A Low-Cost Mixed Clock Generator for High Speed Adiabatic Logic", in *Proceedings of the 15th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2016, pp. 587–590. (**blind review**)
159. S. Joshi, **S. P. Mohanty**, E. Kougianos, and V. P. Yanambaka, "Graphene Nanoribbon Field Effect Transistor based Ultra-Low Energy SRAM Design", in *Proceedings of the 2nd IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, 2016, pp. 76–79.
160. V. P. Yanambaka, **S. P. Mohanty**, E. Kougianos, and J. Singh, "FinFET based Novel Physical Unclonable Functions for Efficient Security in the IoT", Poster, *International Workshop on Design Automation for Analog and Mixed-Signal Circuits, ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, November 10, 2016.
161. O. Okpokwasili, **S. P. Mohanty**, E. Kougianos, and P. Sundaravadivel, "Simulink Modeling of an Intelligent Battery System towards Sustainable Electronics", Poster, *International Workshop on Design Automation for Analog and Mixed-Signal Circuits, ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, November 10, 2016.
162. M. Panchore, J. Singh, **S. P. Mohanty**, and E. Kougianos, "Compact Behavioral Modeling and Time Dependent Performance Degradation Analysis of Doping and Junction Less Transistors for Analog Designs", Poster, *International Workshop on Design Automation for Analog and Mixed-Signal Circuits, ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, 10 Nov, 2016.

Year 2015:

163. **S. P. Mohanty**, E. Kougianos, and V. P. Yanambaka, "Ultra-Fast Process-Aware Design Optimization of PLL using Bootstrapped Kriging and PSO", in *Proceedings of the 16th International Symposium on Quality Electronic Design (ISQED)*, pp. 239–242, 2015. (**blind review**)
164. S. Joshi, E. Kougianos, and **S. P. Mohanty**, "Simscape based Ultra-Fast Design Exploration of Graphene-Nanoelectronic Systems", in *Proceedings of the 14th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2015, pp. 292–296.
165. E. Kougianos, S. Joshi, and **S. P. Mohanty**, "Multi-Swarm Optimization of a Graphene FET Based Voltage Controlled Oscillator Circuit", in *Proceedings of the 14th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2015, pp. 567–572.
166. U. Albalawi, **S. P. Mohanty**, and E. Kougianos, "A Hardware Architecture for Better Portable Graphics (BPG) Compression Encoder", in *Proceedings of the 1st IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, 2015, pp. 291–296. (**blind review**)
167. P. Ghosal and **S. P. Mohanty**, "Power Minimization of a Memristor-Based Wien Bridge Oscillator through a Simscape Framework", in *Proceedings of the 1st IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, 2015, pp. 83–88. (**blind review**)
168. Z. Zhao, A. Srivastava, S. Chen, and **S. P. Mohanty**, "An Algorithm Used in a Power Monitor to Mitigate Dark Silicon on VLSI Chip", in *Proceedings of the 14th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2015, pp. 191–194. (Ph.D. Forum) (**Awarded Best Ph.D. Forum Paper.**)
169. G. Coelho, E. Kougianos, **S. P. Mohanty**, P. Sundaravadivel, and U. Albalawi, "An IoT-Enabled Modular Quadrotor Architecture for Real-Time Aerial Object Tracking", in *Proceedings of the 1st IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, 2015, pp. 197–202. (**blind review**)
170. Z. Zhao, A. Srivastava, L. Peng, S. Chen and **S. P. Mohanty**, "Circuit Implementation of Switchable Pins in Chip Multiprocessor", in *Proceedings of the 1st IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, 2015, pp. 89–94. (**blind review**)
171. S. Joshi, **S. P. Mohanty**, and E. Kougianos, "Unconventional EDA for Mixed-Signal Circuits: A Graphene FET based LC-VCO Case Study", Poster, *International Workshop on Design Automation for Analog and Mixed-Signal Circuits, ACM/IEEE International Conference on Computer-Aided*

Design (ICCAD), November 5-6, 2015.

172. P. V. Yanambaka, **S. P. Mohanty**, and E. Kougianos, "Memristor-based AMS Circuits: A Relaxation Oscillator For Vehicle Turn Signaling Case Study", Poster, *International Workshop on Design Automation for Analog and Mixed-Signal Circuits, ACM/IEEE International Conference on Computer-Aided Design (ICCAD)*, November 5-6, 2015.

Year 2014:

173. A. Khan, **S. P. Mohanty**, and E. Kougianos, "Statistical Process Variation Analysis of a Graphene FET based LC-VCO for WLAN Applications", in *Proceedings of the 15th International Symposium on Quality Electronic Design (ISQED)*, 2014, pp. 569–574. (**blind review**)
174. D. Ghai, **S. P. Mohanty**, G. Thakral, and O. Okobiah, "Variability-Aware DG FinFET-based Current Mirrors", in *Proceedings of the 23rd ACM Great Lakes Symposium on VLSI (GLSVLSI)*, 2014, pp. 347–352. (**blind review**, 29 regular papers and 20 short papers accepted out of 179 submissions, acceptance rate - 27.4%).
175. O. Okobiah, **S. P. Mohanty**, and E. Kougianos, "Kriging Bootstrapped Neural Network Training for Fast and Accurate Process Variation Analysis", in *Proceedings of the 15th International Symposium on Quality Electronic Design (ISQED)*, 2014, pp. 365–372. (**blind review**)
176. D. Roy, P. Ghosal, and **S. P. Mohanty**, "FuzzRoute: A Method For Thermally Efficient Congestion Free Global Routing in 3D ICs", in *Proceedings of the 13th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2014, pp. 71–76. (**blind review**, 56 regular papers accepted out of 164 submissions, acceptance rate - 34.1%)
177. E. Agu, **S. P. Mohanty**, E. Kougianos and M. Gautam, "Simscape Based Design Flow for Memristor Based Programmable Oscillators", in *Proceedings of the 23rd ACM Great Lakes Symposium on VLSI (GLSVLSI)*, 2014, pp. 223–224. (**blind review**, 29 regular papers, 20 short papers, and 27 poster papers accepted out of 179 submissions, acceptance rate - 42.4%)
178. T. S. Das, P. Ghosal, **S. P. Mohanty**, and E. Kougianos, "A Performance Enhancing Hybrid Locally Mesh Globally Star NoC Topology", in *Proceedings of the 23rd ACM Great Lakes Symposium on VLSI (GLSVLSI)*, 2014, pp. 69–70. (**blind review**, 29 regular papers, 20 short papers, and 27 poster papers accepted out of 179 submissions, acceptance rate - 42.4%)
179. A. Bose, P. Ghosal, and **S. P. Mohanty**, "A Low Latency Scalable 3D NoC Using BFT Topology with Table Based Uniform Routing", in *Proceedings of the 13th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2014, pp. 136–141. (**blind review**, 56 regular papers and 25 poster papers accepted out of 164 submissions, acceptance rate - 49.4%)
180. S. Ghosh, P. Ghosal, N. Das, **S. P. Mohanty**, and O. Okobiah, "Data Correlation Aware Serial Encoding for Low Switching Power On-Chip Communication", in *Proceedings of the 13th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2014, pp. 124–129. (**blind review**, 56 regular papers and 25 poster papers accepted out of 164 submissions, acceptance rate - 49.4%)
181. O. Okobiah, **S. P. Mohanty**, and E. Kougianos, "Exploring Kriging for Fast and Accurate Design Optimization of Nanoscale Analog Circuits", in *Proceedings of the 13th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2014, pp. 244–247. (Ph.D. Forum)
182. D. Ghosh, P. Ghosal, and **S. P. Mohanty**, "A Highly Parameterizable Simulator for Performance Analysis of NoC Architectures", in *Proceedings of the 13th International Conference on Information Technology (ICIT)*, pp. 311–315, 2014. (**blind review**, 68 papers accepted out of 186 submissions, acceptance rate - 36.5%)
183. O. Okobiah, **S. P. Mohanty**, and E. Kougianos, "Exploring Kriging for Fast and Accurate Design Optimization of Nanoscale Analog Circuits", Poster, *IEEE Texas Workshop on Integrated System Exploration (TexasWISE)*, University of Texas at Austin, Texas, March 21, 2014.
184. P. Ghosal and **S. P. Mohanty**, "Architectural and Layout Level Optimization of Performance Centric 3D Nanosystem Design", Poster, *IEEE Texas Workshop on Integrated System Exploration*

(TexasWISE), University of Texas at Austin, Texas, March 21, 2014.

Year 2013:

185. O. Okobiah, **S. P. Mohanty**, and E. Kougianos, "Geostatistics Inspired Fast Layout Optimization of Nanoscale CMOS Phase Locked Loop", in *Proceedings of the 14th International Symposium on Quality Electronic Design (ISQED)*, pp. 546–551, 2013. (**blind review**)
186. D. Ghai, **S. P. Mohanty**, and G. Thakral, "Fast Analog Design Optimization using Regression based Modeling and Genetic Algorithm: A Nano-CMOS VCO Case Study", in *Proceedings of the 14th International Symposium on Quality Electronic Design (ISQED)*, pp. 422–427, 2013. (**blind review**)
187. G. Zheng, **S. P. Mohanty**, E. Kougianos, and O. Okobiah, "Polynomial Metamodel Integrated Verilog-AMS for Memristor-Based Mixed-Signal System Design", in *Proceedings of the 56th IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, 2013, pp. 916–919.
188. O. Okobiah, **S. P. Mohanty**, and E. Kougianos, "Fast Statistical Process Variation Analysis using Universal Kriging Metamodeling: A PLL Example", in *Proceedings of the 56th IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, 2013, pp. 277–280.
189. G. Zheng, **S. P. Mohanty**, E. Kougianos, and O. Okobiah, "iVAMS: Intelligent Metamodel-Integrated Verilog-AMS for Circuit-Accurate System-Level Mixed-Signal Design Exploration", in *Proceedings of the 24th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, 2013, pp. 75–78. (24 full, 15 short, and 22 poster papers accepted out of 125 submissions, acceptance rate – 48.8%)
190. D. Ghai, **S. P. Mohanty**, and G. Thakral, "Comparative Analysis of Double Gate FinFET Configurations for Analog Circuit Design", in *Proceedings of the 56th IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, 2013, pp. 809–812.
191. D. Ghai, **S. P. Mohanty**, and G. Thakral, "Double Gate FinFET based Mixed-Signal Design: A VCO Case Study", in *Proceedings of the 56th IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, 2013, pp. 177–180.
192. M. Sarkar, P. Ghosal, and **S. P. Mohanty**, "Reversible Circuit Synthesis Using ACO and SA based Quinne-McCluskey Method", in *Proceedings of the 56th IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, 2013, pp. 416–419.
193. G. Zheng, **S. P. Mohanty**, E. Kougianos, "Verilog-AMS-POM: Verilog-AMS Integrated POlynomial Metamodelling of a Memristor-based Oscillator", *Work-in-Progress Session Poster, Design Automation Conference (DAC)*, 2013.
194. G. Zheng, **S. P. Mohanty**, E. Kougianos, "iVAMS: Intelligent Metamodel-Integrated Verilog-AMS for Fast Analog Block Optimization", *Work-in-Progress Session Poster, Design Automation Conference (DAC)*, 2013.

Year 2012:

195. O. Okobiah, **S. P. Mohanty**, E. Kougianos, and O. Garitselov, "Kriging-Assisted Ultra-Fast Simulated-Annealing Optimization of a Clamped Bitline Sense Amplifier", in *Proceedings of the 25th International Conference on VLSI Design (VLSID)*, pp. 310–315, 2012 (**blind review**, 71 papers accepted out of 223 submissions, acceptance rate – 31.8%).
196. O. Garitselov, **S. P. Mohanty**, and E. Kougianos, "Fast-Accurate Non-Polynomial Metamodeling for nano-CMOS PLL Design Optimization", in *Proceedings of the 25th International Conference on VLSI Design (VLSID)*, pp. 316–321, 2012 (**blind review**, 71 papers accepted out of 223 submissions, acceptance rate – 31.8%).
197. O. Okobiah, **S. P. Mohanty**, and E. Kougianos, "Ordinary Kriging Metamodel-Assisted Ant Colony Algorithm for Fast Analog Design Optimization", in *Proceedings of the 13th International Symposium on Quality Electronic Design (ISQED)*, pp. 458–463, 2012 (**blind review**).
198. O. Garitselov, **S. P. Mohanty**, E. Kougianos, and O. Okobiah, "Metamodel-Assisted Ultra-Fast Memetic Optimization of a PLL for WiMax and MMDS Applications", in *Proceedings of the 13th*

International Symposium on Quality Electronic Design (ISQED), pp. 580–585, 2012 (**blind review**).

199. G. Zheng, **S. P. Mohanty**, E. Kougianos, and O. Garitselov, "Verilog-AMS-PAM: Verilog-AMS integrated with Parasitic-Aware Metamodels for Ultra-Fast and Layout-Accurate Mixed-Signal Design Exploration", in *Proceedings of the 21st ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 351–356, 2012 (**blind review**, 23 full and 18 short papers accepted out of 144 submissions, acceptance rate – 28.5%).
200. G. Zheng, **S. P. Mohanty**, and E. Kougianos, "Metamodel-Assisted Fast and Accurate Optimization of an OP-AMP for Biomedical Applications", in *Proceedings of the 11th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 273–278, 2012 (**blind review**).
201. O. Okobiah, **S. P. Mohanty**, and E. Kougianos, "Geostatistical-Inspired Metamodeling and Optimization of Nano-CMOS Circuits", in *Proceedings of the 11th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 326–331, 2012 (**blind review**).
202. O. Garitselov, **S. P. Mohanty**, E. Kougianos, and G. Zheng, "Particle Swarm Optimization over Non-Polynomial Metamodels for Fast Process Variation Resilient Design of Nano-CMOS PLL", in *Proceedings of the 21st ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 255–258, 2012 (**blind review**, 23 full, 18 short, and 30 poster papers accepted out of 144 submissions, acceptance rate – 49.3%).
203. O. Okobiah, **S. P. Mohanty**, E. Kougianos, O. Garitselov, and G. Zheng, "Stochastic Gradient Descent Optimization for Low Power Nanoscale CMOS Thermal Sensor Design", in *Proceedings of the 11th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 285–290, 2012 (**blind review**).
204. **S. P. Mohanty**, E. Kougianos, O. Garitselov, and J. M. Molina, "Polynomial-Metamodel Assisted Fast Power Optimization of Nano-CMOS PLL Components", in *Proceedings of the Forum on specification and Design Languages (FDL)*, pp. 233–238, 2012.
205. M. Poolakkaparambil, J. Mathew, A. M. Jabir, and **S. P. Mohanty**, "Low Complexity Cross Parity Codes for Multiple and Random Bit Error Correction", in *Proceedings of the 13th International Symposium on Quality Electronic Design (ISQED)*, pp. 57–62, 2012 (**blind review**).
206. M. Poolakkaparambil, J. Mathew, A. M. Jabir, and **S. P. Mohanty**, "An Investigation of Concurrent Error Detection over Binary Galois Fields in CNTFET and QCA Technologies", in *Proceedings of the 11th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 141–146, 2012 (**blind review**).
207. G. K. Reddy, K. Jainwal, J. Singh, and **S. P. Mohanty**, "Process Variation Tolerant 9T SRAM Bitcell Design", in *Proceedings of the 13th International Symposium on Quality Electronic Design (ISQED)*, pp. 492–496, 2012 (**blind review**).
208. P. Yeolekar, R. A. Shafik, J. Mathew, D. K. Pradhan, and **S. P. Mohanty**, "STEP: A Unified Design Methodology for Secure Test and IP Core Protection", in *Proceedings of the 21st ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 333–338, 2012 (**blind review**, 23 full and 18 short papers accepted out of 144 submissions, acceptance rate – 28.5%).
209. R. A. Shafik, B. M. Al-Hashimi, J. Mathew, D. K. Pradhan, and **S. P. Mohanty**, "RAEF: A Power Normalized System-Level Reliability Analysis and Estimation Framework", in *Proceedings of 11th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pp. 189–194, 2012 (**blind review**).
210. G. Zheng, **S. P. Mohanty**, and E. Kougianos, "Design and Modeling of a Continuous-Time Delta-Sigma Modulator for Biopotential Signal Acquisition: Simulink Vs Verilog-AMS Perspective", in *Proceedings of the 3rd International Conference on Computing, Communication and Networking Technologies (ICCCNT)*, pp. 1–6, 2012.

Year 2011:

211. S. Banerjee, J. Mathew, D. K. Pradhan, **S. P. Mohanty**, and M. Ciesielski, "Variation-Aware TED-Based Approach for Nano-CMOS RTL Leakage Optimization", in *Proceedings of the 24th International Conference on VLSI Design (VLSID)*, pp. 304–309, 2011 (**blind review**, 66 papers

accepted out of 330 submissions, acceptance rate – 20.0%).

212. O. Okobiah, **S. P. Mohanty**, and E. Kougianos, M. Poolakkaparambil, "Towards Robust Nano-CMOS Sense Amplifier Design: A Dual-Threshold versus Dual-Oxide Perspective", in *Proceedings of the 21st ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 145–150, 2011 (**blind review**, 57 papers accepted out of 207 submissions, acceptance rate - 27.5%).
213. **S. P. Mohanty** and E. Kougianos, "PVT-Tolerant 7-Transistor SRAM Optimization via Polynomial Regression", in *Proceedings of the 2nd International Symposium on Electronic System Design (ISED)*, pp. 39–44, 2011 (**blind review**, 62 papers accepted out of 146 submissions, acceptance rate – 42.4%).
214. O. Garitselov, **S. P. Mohanty**, E. Kougianos, and P. Patra, "Bee Colony Inspired Metamodeling Based Fast Optimization of a Nano-CMOS PLL", in *Proceedings of the 2nd International Symposium on Electronic System Design (ISED)*, pp. 6–11, 2011 (**blind review**, 62 papers accepted out of 146 submissions, acceptance rate – 42.4%).
215. M. Poolakkaparambil, J. Mathew, A. Jabir, D. K. Pradhan, and **S. P. Mohanty**, "BCH Code Based Multiple Bit Error Correction in Finite Field Multiplier Circuits", in *Proceedings of the 12th International Symposium on Quality Electronic Design (ISQED)*, pp. 615–620, 2011 (**blind review**, 92 regular papers accepted out of 290 submissions, acceptance rate - 31.7%).
216. O. Garitselov, **S. P. Mohanty**, and E. Kougianos, "Fast Optimization of Nano-CMOS Mixed-Signal Circuits Through Accurate Metamodeling", in *Proceedings of the 12th International Symposium on Quality Electronic Design (ISQED)*, pp. 405–410, 2011 (**blind review**, 92 regular papers and 34 poster papers accepted out of 290 submissions, acceptance rate - 43.4%).
217. L. Sun, J. Mathew, D. K. Pradhan, and **S. P. Mohanty**, "Statistical Blockade Method for Fast Robustness Estimation and Compensation of Nano-CMOS Arithmetic Circuits", in *Proceedings of the 2nd International Symposium on Electronic System Design (ISED)*, pp. 194–199, 2011 (**blind review**, 62 papers accepted out of 146 submissions, acceptance rate – 42.4%).
218. M. Hosseinabady, P. Lotfi-Kamran, J. Mathew, **S. P. Mohanty**, and D. K. Pradhan, "Single-Event Transient Analysis in High Speed Circuits", in *Proceedings of the 2nd International Symposium on Electronic System Design (ISED)*, pp. 112–117, 2011 (**blind review**, 62 papers accepted out of 146 submissions, acceptance rate – 42.4%).

Year 2010:

219. **S. P. Mohanty**, D. Ghai, and E. Kougianos, "A P4VT (Power-Performance-Process-Parasitic-Voltage-Temperature) Aware Dual-V_{Th} Nano-CMOS VCO", in *Proceedings of the 23rd International Conference on VLSI Design (VLSID)*, pp. 99-104, 2010 (**blind review**, 70 papers accepted out of 320 submissions, acceptance rate - 21.8%).
220. G. Thakral, **S. P. Mohanty**, D. Ghai, and D. K. Pradhan, "A Combined DOE-ILP Based Power and Read Stability Optimization in Nano-CMOS SRAM", in *Proceedings of the 23rd International Conference on VLSI Design (VLSID)*, pp. 45-50, 2010 (**blind review**, 70 papers accepted out of 320 submissions, acceptance rate - 21.8%).
221. G. Thakral, **S. P. Mohanty**, D. Ghai, and D. K. Pradhan, "A DOE-ILP Assisted Conjugate-Gradient Approach for Power and Stability Optimization in High-κ/Metal-Gate SRAM", in *Proceedings of the 20th ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 323-328, 2010 (**blind review**, 30 full papers accepted out of 165 submissions, acceptance rate - 18.1%).
222. S. K. Mandal, R. Denton, **S. P. Mohanty**, and R. N. Mahapatra, "Low Power Nanoscale Buffer Management for Network on Chip Routers", in *Proceedings of the 20th ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 245-250, 2010 (**blind review**, 30 full papers accepted out of 165 submissions, acceptance rate - 18.1%).
223. J. Singh, D. S. Aswar, **S. P. Mohanty**, and D. K. Pradhan, "A 2-Port 6T SRAM Bitcell Design with Multi-Port Capabilities at Reduced Area Overhead", in *Proceedings of the 11th International Symposium on Quality Electronic Design (ISQED)*, pp. 131-138, 2010 (**blind review**, 84 regular

papers accepted out of 270 submissions, acceptance rate - 31.1%).

224. S. Banerjee, J. Mathew, D. K. Pradhan, and **S. P. Mohanty**, "Layout-Aware Illinois Scan Design for High Fault Coverage", in *Proceedings of the 11th International Symposium on Quality Electronic Design (ISQED)*, pp. 683-688, 2010 (**blind review**, 84 regular papers accepted out of 270 submissions, acceptance rate - 31.1%).
225. J. Mathew, S. Banerjee, H. Rahaman, D. K. Pradhan, **S. P. Mohanty**, and A. M. Jabir, "On the Synthesis of Attack Tolerant Cryptographic Hardware", in *Proceedings of the 18th IEEE/IFIP International Conference on VLSI and System-on-Chip (VLSI-SoC)*, pp. 286-291, 2010 (41 full papers accepted out of 199 submissions, acceptance rate - 20.6%).
226. O. Garitselov, **S. P. Mohanty**, E. Kougianos, and P. Patra, "Nano-CMOS Mixed-Signal Circuit Meta-modeling Techniques: A Comparative Study", in *Proceedings of the 1st International Symposium on Electronic System Design (ISED)*, pp. 191–196, 2010 (**blind review**, 41 papers accepted out of 120 submissions, acceptance rate - 34.1%).
227. S. Banerjee, J. Mathew, D. K. Pradhan, **S. P. Mohanty**, and M. Ciesielski, "A Taylor Expansion Diagram Approach for Nano-CMOS RTL Leakage Optimization", in *Proceedings of the 1st International Symposium on Electronic System Design (ISED)*, pp. 71–76, 2010 (**blind review**, 41 papers accepted out of 120 submissions, acceptance rate - 34.1%).
228. L. Sun, J. Mathew, D. K. Pradhan, and **S. P. Mohanty**, "Algorithms for Rare Event Analysis in Nano-CMOS Circuits Using Statistical Blockade", in *Special Session on New Horizons in SoC and ASIC Design, Proceedings of the International SoC Design Conference (ISOCC)*, pp. 162–165, 2010.
229. G. Thakral, **S. P. Mohanty**, D. Ghai, and D. K. Pradhan, "P3 (Power-Performance-Process) Optimization of Nano-CMOS SRAM using Statistical DOE-ILP", in *Proceedings of the 11th International Symposium on Quality Electronic Design (ISQED)*, pp. 176-183, 2010 (**blind review**, 84 regular papers and 40 poster papers accepted out of 270 submissions, acceptance rate - 45.9%).
230. J. Mathew, H. Rahaman, A. Jabir, **S. P. Mohanty**, and D. K. Pradhan, "On the Design of Different Concurrent EDC Schemes for S-box and GF(P)", in *Proceedings of the 11th International Symposium on Quality Electronic Design (ISQED)*, pp. 211-218, 2010 (**blind review**, 84 regular papers and 40 poster papers accepted out of 270 submissions, acceptance rate - 45.9%).
231. R. R. Bani, **S. P. Mohanty**, E. Kougianos, and G. Thakral, "Design of a Reconfigurable Embedded Data Cache", in *Proceedings of the 1st International Symposium on Electronic System Design (ISED)*, pp. 163–168, 2010 (**blind review**, 41 papers accepted out of 120 submissions, acceptance rate - 34.1%).
232. J. Mathew, S. Banerjee, M. Poolakkaparambil, **S. P. Mohanty**, A. Jabir, and D. K. Pradhan, "Multiple-Bit Error Detection and Correction in GF Arithmetic Circuits", in *Proceedings of the 1st International Symposium on Electronic System Design (ISED)*, pp. 101–106, 2010 (**blind review**, 41 papers accepted out of 120 submissions, acceptance rate - 34.1%).
233. E. Kougianos and **S. P. Mohanty**, and P. Patra, "Digital Nano-CMOS VLSI Design Courses in Electrical and Computer Engineering Through Open-Source/Free Tools", in *Proceedings of the 1st International Symposium on Electronic System Design (ISED)*, pp. 265–270, 2010.

Year 2009:

234. J. Singh, D. K. Pradhan, S. Hollis, **S. P. Mohanty**, and J. Mathew, "Single Ended 6T SRAM with Isolated Read-Port for Low-Power Embedded Systems", in *Proceedings of the 12th IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 917-922, 2009 (**blind review**, 226 papers accepted out of 965 submissions, acceptance rate - 23.4%).
235. J. Singh, J. Mathew, **S. P. Mohanty**, and D. K. Pradhan, "Single Ended Static Random Access Memory for Low-V_{dd}, High-Speed Embedded Systems", in *Proceedings of the 22nd International Conference on VLSI Design (VLSID)*, pp. 307-312, 2009 (**blind review**, 57 regular papers and 22 short papers accepted out of 320 submissions, acceptance rate - 24.6%).

236. **S. P. Mohanty**, D. Ghai, E. Kougianos, and B. Joshi, "A Universal Level Converter Towards the Realization of Energy Efficient Implantable Drug Delivery Nano-Electro-Mechanical-Systems", in *Proceedings of the 10th International Symposium on Quality Electronic Design (ISQED)*, pp. 673-679, 2009 (**blind review**, 87 regular papers accepted out of 300 submissions, acceptance rate - 29%).
237. D. Ghai, **S. P. Mohanty**, E. Kougianos, and P. Patra, "A PVT Aware Accurate Statistical Logic Library for High- Metal-Gate Nano-CMOS", in *Proceedings of the 10th International Symposium on Quality Electronic Design (ISQED)*, pp. 47-54, 2009 (**blind review**, 87 regular papers accepted out of 300 submissions, acceptance rate - 29%).
238. D. Ghai, **S. P. Mohanty**, and E. Kougianos, "Unified P4 (Power-Performance-Process-Parasitic) Fast Optimization of a Nano-CMOS VCO", in *Proceedings of the 19th ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 303-308 , 2009 (**blind review**, 62 regular papers accepted out of 215 submissions, acceptance rate - 29%).
239. D. Ghai, **S. P. Mohanty**, and E. Kougianos, "Variability-Aware Optimization of Nano-CMOS Active Pixel Sensors using Design and Analysis of Monte Carlo Experiments", in *Proceedings of the 10th International Symposium on Quality Electronic Design (ISQED)*, pp. 172-178, 2009 (**blind review**, 87 regular papers and 50 poster papers accepted out of 300 submissions, acceptance rate - 45.7%).
240. **S. P. Mohanty**, E. Kougianos, Wei Cai, and M. Ratnani, "VLSI Architectures of Perceptual Based Video Watermarking for Real-Time Copyright Protection", in *Proceedings of the 10th International Symposium on Quality Electronic Design (ISQED)*, pp. 527-534, 2009 (**blind review**, 87 regular papers and 50 poster papers accepted out of 300 submissions, acceptance rate - 45.7%).
241. **S. P. Mohanty**, "GPU-CPU Multi-Core For Real-Time Signal Processing", in *Proceedings of the 27th IEEE International Conference on Consumer Electronics (ICCE)*, pp. 55-56, 2009.
242. **S. P. Mohanty**, D. Ghai, E. Kougianos, and P. Patra, "A Combined Packet Classifier and Scheduler Towards Net-Centric Multimedia Processor Design", in *Proceedings of the 27th IEEE International Conference on Consumer Electronics (ICCE)*, pp. 11-12, 2009.
243. **S. P. Mohanty** and D. K. Pradhan, "Tabu Search Based Gate Leakage Optimization using DKCMOS Library in Architecture Synthesis", in *Proceedings of the 12th International Conference on Information Technology (ICIT)*, pp. 3-9, 2009 (**blind review**, 54 papers accepted out of 148 submissions, acceptance rate - 36.4%).
244. **S. P. Mohanty** and B. K. Panigrahi, "ILP Based Leakage Optimization During Nano-CMOS RTL Synthesis: A DOXCMOS Versus DTCMOS Perspective", in *Proceedings of the International Symposium on Biologically Inspired Computing And Applications (BICA)*, pp. 1367-1372, 2009 (70 papers accepted out of 130 submissions, acceptance rate - 53.8%).
245. E. Kougianos, **S. P. Mohanty**, and D. K. Pradhan, "Simulink Based Architecture Prototyping of Compressed Domain MPEG-4 Watermarking", in *Proceedings of the 12th International Conference on Information Technology (ICIT)*, pp. 10-16, 2009 (**blind review**, 54 papers accepted out of 148 submissions, acceptance rate - 36.4%).

Year 2008:

246. S. K. Mandal, P. Bhojwani, **S. P. Mohanty**, and R. N. Mahapatra, "IntellBatt: Towards Smarter Battery Design", in *Proceedings of the 45th ACM/IEEE Design Automation Conference (DAC)*, pp. 872-877, 2008 (**blind review**, 147 papers accepted out of 639 submissions, acceptance rate - 23%).
247. **S. P. Mohanty**, "ILP based Gate Leakage Optimization using DKCMOS Library during RTL Synthesis", in *Proceedings of the 9th International Symposium on Quality Electronic Design (ISQED)*, pp. 174-177, 2008 (**blind review**, 90 regular papers accepted out of 300 submissions, acceptance rate - 30%).
248. D. Ghai, **S. P. Mohanty**, and E. Kougianos, "A Process and Supply Variation Tolerant Nano-CMOS Low Voltage, High Speed, A/D Converter for System-on-Chip", in *Proceedings of the 18th ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 47-52, 2008 (**blind review**, 40 regular papers

accepted out of 220 submissions, acceptance rate - 18.2%).

249. D. Ghai, **S. P. Mohanty**, and E. Kougianos, "A Dual Oxide CMOS Universal Voltage Converter for Power Management in Multi-VDD SoCs", in *Proceedings of the 9th International Symposium on Quality Electronic Design (ISQED)*, pp. 257-260, 2008 (**blind review**, 90 regular papers and 65 poster papers accepted out of 300 submissions, acceptance rate - 51.6%).
250. D. Ghai, **S. P. Mohanty**, and E. Kougianos, "Parasitic Aware Process Variation Tolerant Voltage Controlled Oscillator (VCO) Design", in *Proceedings of the 9th International Symposium on Quality Electronic Design (ISQED)*, pp. 330-333, 2008 (**blind review**, 90 regular papers and 65 poster papers accepted out of 300 submissions, acceptance rate - 51.6%).
251. J. Singh, J. Mathew, D. K. Pradhan, and **S. P. Mohanty**, "A Subthreshold Single Ended I/O SRAM Cell Design for Nanometer CMOS Technologies", in *Proceedings of the IEEE International SOC Conference (SOCC)*, pp. 243-246, 2008 (**blind review**).
252. J. Singh, J. Mathew, D. K. Pradhan, and **S. P. Mohanty**, "Failure Analysis for Ultra Low Power Nano-CMOS SRAM Under Process Variations", in *Proceedings of the IEEE International SOC Conference (SOCC)*, pp. 251-254, 2008 (**blind review**).
253. J. Singh, J. Mathew, **S. P. Mohanty**, and D. K. Pradhan, "A Nano-CMOS Process Variation Induced Read Failure Tolerant SRAM Cell", in *Proceedings of the 40th IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 3334-3337, 2008 (911 papers accepted out of 1858 submissions, acceptance rate - 49%).
254. Y. -T. Pai, L. -T. Lee, S. -J. Ruan, Y. -H. Chen, **S. P. Mohanty**, and E. Kougianos, "Honeycomb Model Based Skin Color Detector for Face Detection", in *Proceedings of the 15th International Conference on Mechatronics and Machine Vision in Practice (M2VIP)*, pp. 11-16, 2008.

Year 2007:

255. **S. P. Mohanty** and E. Kougianos, "Simultaneous Power Fluctuation and Average Power Minimization during Nano-CMOS Behavioral Synthesis", in *Proceedings of the 20th International Conference on VLSI Design (VLSID)*, pp. 577-582, 2007 (**blind review**, 141 papers accepted out of 444 submissions, acceptance rate - 31.7%).
256. E. Kougianos and **S. P. Mohanty**, "Metrics to Quantify Steady and Transient Gate Leakage in Nanoscale Transistors: NMOS Vs PMOS Perspective", in *Proceedings of the 20th International Conference on VLSI Design (VLSID)*, pp. 195-200, 2007 (**blind review**, 141 papers accepted out of 444 submissions, acceptance rate - 31.7%).
257. **S. P. Mohanty**, N. Pati, and E. Kougianos, "A Watermarking Co-Processor for New Generation Graphics Processing Units", in *Proceedings of the 25th IEEE International Conference on Consumer Electronics (ICCE)*, pp. 303-304, 2007.
258. **S. P. Mohanty**, O. B. Adamo, and E. Kougianos, "VLSI Architecture of an Invisible Watermarking Unit for a Biometric-Based Security System in a Digital Camera", in *Proceedings of the 25th IEEE International Conference on Consumer Electronics (ICCE)*, pp. 485-486, 2007.
259. **S. P. Mohanty**, E. Kougianos, and R. N. Mahapatra, "A Comparative Analysis of Gate Leakage and Performance of High-K Nanoscale CMOS Logic Gates", in *Proceedings of the 16th ACM/IEEE International Workshop on Logic and Synthesis (IWLS)*, pp. 31-38, 2007.
260. **S. P. Mohanty**, E. Kougianos, D. Ghai, and P. Patra, "Interdependency Study of Process and Design Parameter Scaling for Power Optimization of Nano-CMOS Circuits under Process Variation", in *Proceedings of the 16th ACM/IEEE International Workshop on Logic and Synthesis (IWLS)*, pp. 207-213, 2007.
261. J. Singh, J. Mathew, **S. P. Mohanty**, and D. K. Pradhan, "Statistical Analysis of Steady State Leakage Currents in Nano-CMOS Devices", in *Proceedings of the 25th IEEE Norchip Conference (NORCHIP)*, pp. 1-4, 2007.
262. **S. P. Mohanty**, S. T. Vadlamudi, and E. Kougianos, "A Universal Voltage Level Converter for Multi-

V_{DD} Based Low-Power Nano-CMOS Systems-on-Chips (SoCs)", in *Proceedings of the 13th NASA Symposium on VLSI Design*, 2007, CD-ROM Electronic Proceedings paper # 2.2 (7 pages).

263. D. Ghai, **S. P. Mohanty**, and E. Kougianos, "A $45nm$ Flash Analog to Digital Converter for Low Voltage High Speed System on Chips", in *Proceedings of the 13th NASA Symposium on VLSI Design*, 2007, CD-ROM Electronic Proceedings paper # 2.4 (6 pages).
264. **S. P. Mohanty** and E. Kougianos, "Impact of Gate Leakage on Mixed Signal Design and Simulation of Nano-CMOS Circuits", in *Proceedings of the 13th NASA Symposium on VLSI Design*, 2007, CD-ROM Electronic Proceedings paper # 3.1 (10 pages).
265. **S. P. Mohanty**, R. Sheth, A. Pinto, and M. Chandy, "CryptMark: A Novel Secure Invisible Watermarking Technique for Double Layer Protection of Color Images", in *Proceedings of the 11th IEEE International Symposium on Consumer Electronics (ISCE)*, 2007, pp. 1-6.

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266. **S. P. Mohanty**, R. Velagapudi, and E. Kougianos, "Physical-Aware Simulated Annealing Optimization of Gate Leakage in Nanoscale Datapath Circuits", in *Proceedings of the 9th IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 1191-1196, 2006 (**blind review**, 233 papers accepted out of 834 submissions, acceptance rate - 27.9%).
267. **S. P. Mohanty** and E. Kougianos, "Steady and Transient State Analysis of Gate Leakage Current in Nanoscale CMOS Logic Gates", in *Proceedings of the 24th IEEE International Conference on Computer Design (ICCD)*, pp. 210-215, 2006 (**blind review**, 72 papers accepted out of 231 submissions, acceptance rate - 31%).
268. **S. P. Mohanty** and E. Kougianos, "Modeling and Reduction of Gate Leakage during Behavioral Synthesis of NanoCMOS Circuits", in *Proceedings of the 19th International Conference on VLSI Design (VLSID)*, pp. 83-88, 2006 (**blind review**, 88 regular papers accepted out of 328 submissions, acceptance rate - 26.8%).
269. **S. P. Mohanty**, R. Velagapudi, and E. Kougianos, "Dual-K Versus Dual-T Technique for Gate Leakage Reduction: A Comparative Perspective", in *Proceedings of the 7th International Symposium on Quality Electronic Design (ISQED)*, pp. 564-569, 2006 (**blind review**, 93 regular papers accepted out of 256 submissions, acceptance rate - 36.3%).
270. O. B. Adamo, **S. P. Mohanty**, E. Kougianos, and M. Varanasi, "VLSI Architecture for Encryption and Watermarking Units Towards the Making of a Secure Digital Camera", in *Proceedings of the IEEE International SOC Conference (SOCC)*, pp. in press, 2006 (**blind review**, 53 regular papers accepted out of 169 submissions, acceptance rate - 31.3%).
271. N. M. Kosaraju, M. Varanasi, and **S. P. Mohanty**, "A High-Performance VLSI Architecture for Advanced Encryption Standard (AES) Algorithm", in *Proceedings of the 19th International Conference on VLSI Design (VLSID)*, pp. 481-484, 2006 (**blind review**, 88 regular papers and 48 short papers accepted out of 328 submissions, acceptance rate - 41.5%).
272. **S. P. Mohanty**, P. Guturu, E. Kougianos, and N. Pati, "A Novel Invisible Color Image Watermarking Scheme using Image Adaptive Watermark Creation and Robust Insertion-Extraction", in *Proceedings of the IEEE International Symposium on Multimedia (ISM)*, pp. 153-160, 2006 (acceptance rate - 35%).
273. **S. P. Mohanty**, E. Kougianos, R. Velagapudi, and V. Mukherjee, "Scheduling and Binding for Low Gate Leakage NanoCMOS Datapath Circuit Synthesis", in *Proceedings of the 38th IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 5291-5294, 2006 (1439 papers accepted out of 2429 submissions, acceptance rate - 59%).
274. E. Kougianos and **S. P. Mohanty**, "Effective Tunneling Capacitance: A New Metric to Quantify Transient Gate Leakage Current", in *Proceedings of the 38th IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2937-2940, 2006 (1439 papers accepted out of 2429 submissions, acceptance rate - 59%).

275. Y. Zhuo, H. Li, and **S. P. Mohanty**, "A Congestion Driven Placement Algorithm for FPGA Synthesis", in *Proceedings of the 16th IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 683-686, 2006 (85 full papers and 80 poster papers accepted out of 307 submissions, acceptance rate - 53.7%).
276. W. Li, **S. P. Mohanty**, and K. Kavi, "A Hardware Assisted High Performance PHK Memory Manager", in *Proceedings of the ISCA 19th International Conference on Parallel and Distributed Computing Systems (PDCS)*, pp. 229-234, 2006.
277. V. Mukherjee, **S. P. Mohanty**, E. Kougianos, R. Allawadhi, and R. Velagapudi, "Gate Leakage Current Analysis in READ/WRITE/IDLE States of a SRAM Cell", in *Proceedings of IEEE Region 5 Technology and Science Conference*, pp. 196-200, 2006.
278. O. B. Adamo, **S. P. Mohanty**, E. Kougianos, M. Varanasi, and W. Cai, "VLSI Architecture and FPGA Prototyping of a Digital Camera for Image Security and Authentication", in *Proceedings of IEEE Region 5 Technology and Science Conference*, pp. 154-158, 2006.
279. C. A. Kincaid, **S. P. Mohanty**, A. R. Mikler, E. Kougianos, and B. Parker, "A High Performance ASIC for Cellular Automata (CA) Applications", in *Proceedings of the 9th International Conference on Information Technology (ICIT)*, pp. 289-290, 2006 (**blind review**, 83 papers accepted out of 231 submissions, acceptance rate - 35.9%).
280. G. Sarivisetti, E. Kougianos, **S. P. Mohanty**, A. Palakodety, and A. K. Ale, "Optimization of a $45nm$ CMOS Voltage Controlled Oscillator using Design of Experiments", in *Proceedings of IEEE Region 5 Technology and Science Conference*, pp. 87-90, 2006.

Year 2005:

281. V. Mukherjee, **S. P. Mohanty**, and E. Kougianos, "A Dual Dielectric Approach for Performance Aware Gate Tunneling Reduction in Combinational Circuits", in *Proceedings of the 23rd IEEE International Conference on Computer Design (ICCD)*, pp. 431-436, 2005 (**blind review**, 101 papers accepted out of 313 submissions, acceptance rate - 32%).
282. **S. P. Mohanty**, N. Ranganathan, and K. Balakrishnan, "Design of a Low Power Image Watermarking Encoder using Dual Voltage and Frequency", in *Proceedings of the 18th International Conference on VLSI Design (VLSID)*, pp. 153-158, 2005 (**blind review**, 97 regular papers accepted out of 352 submissions, acceptance rate - 28%).
283. **S. P. Mohanty**, V. Mukherjee, and R. Velagapudi, "Analytical Modeling and Reduction of Direct Tunneling Current during Behavioral Synthesis of Nanometer CMOS Circuits", in *Proceedings of the 14th ACM/IEEE International Workshop on Logic and Synthesis (IWLS)*, 2005, pp. 249-256.
284. **S. P. Mohanty**, R. Velagapudi, V. Mukherjee, and H. Li , "Reduction of Direct Tunneling Power Dissipation during Behavioral Synthesis of Nanometer CMOS Circuits", in *Proceedings of the IEEE CS Annual Symposium on VLSI (ISLVSI)*, 2005 (37 regular papers and 31 poster papers accepted out of 126 submissions, acceptance rate - 53.9%).

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285. **S. P. Mohanty**, N. Ranganathan, and R. K. Namballa, "VLSI Implementation of Visible Watermarking for a Secure Digital Still Camera Design", in *Proceedings of the 17th International Conference on VLSI Design (VLSID)*, pp. 1063-1068, 2004 (**blind review**, 92 full papers accepted out of 330 submissions, acceptance rate - 27.8%).
286. **S. P. Mohanty**, N. Ranganathan, and S. K. Chappidi, "ILP Models for Energy and Transient Power Minimization During Behavioral Synthesis", in *Proceedings of the 17th International Conference on VLSI Design (VLSID)*, pp. 745-748, 2004 (**blind review**, 92 full papers and 46 short papers accepted out of 330 submissions, acceptance rate - 41.8%).
287. **S. P. Mohanty**, R. Kumara C., and S. Nayak, "FPGA Based Implementation of an Invisible-Robust Image Watermarking Encoder", *Lecture Notes in Computer Science (LNCS), Internal Conference on Information Technology 2004*, Springer-Verlag, Vol. 3356, pp. 344-353, 2004 (**blind review**, 44 full

papers accepted out of 200 submissions, acceptance rate - 22%).

Year 2003:

288. **S. P. Mohanty**, N. Ranganathan, and S. K. Chappidi, "Power Fluctuation Minimization During Behavioral Synthesis using ILP-Based Datapath Scheduling", in *Proceedings of the 21st IEEE International Conference on Computer Design (ICCD)*, pp. 441-443, 2003 (**blind review**, 61 full papers and 17 short papers accepted out of 233 submissions, acceptance rate - 33.4%).
289. **S. P. Mohanty** and N. Ranganathan, "A Framework for Energy and Transient Power Reduction during Behavioral Synthesis", in *Proceedings of the 16th International Conference on VLSI Design 2003 (VLSID)*, pp. 539-545, 2003 (**blind review**, 84 accepted out of 210 submissions, acceptance rate - 40%) (**Nominated for best paper award; ranked within top 5 out of 210 submissions.**).
290. **S. P. Mohanty** and N. Ranganathan, "Energy Efficient Scheduling for Datapath Synthesis", in *Proceedings of the 16th International Conference on VLSI Design 2003 (VLSID)*, pp. 446-451, 2003 (**blind review**, 84 accepted out of 210 submissions, acceptance rate - 40%).
291. **S. P. Mohanty**, N. Ranganathan, and S. K. Chappidi, "Simultaneous Peak and Average Power Minimization during Datapath Scheduling for DSP Processors", in *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 215-220, 2003 (**blind review**, 17 full papers accepted out of 136 submissions, acceptance rate - 12.5%).
292. **S. P. Mohanty**, N. Ranganathan, and S. K. Chappidi, "An ILP-Based Scheduling Scheme for Energy Efficient High Performance Datapath Synthesis", in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, Vol. 5, pp. 313-316, 2003.
293. **S. P. Mohanty**, N. Ranganathan, and S. K. Chappidi, "Transient Power Minimization Through Datapath Scheduling in Multiple Supply Voltage Environment", in *Proceedings of the 10th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Vol. 1, pp. 300-303, 2003.
294. **S. P. Mohanty**, N. Ranganathan, and S. K. Chappidi, "Peak Power Minimization Through Datapath Scheduling", in *Proceedings of the IEEE-CS Annual Symposium on VLSI (ISVLSI)*, pp. 121-126, 2003 (26 full papers accepted out of 115 submissions, acceptance rate - 22.6%).
295. **S. P. Mohanty**, N. Ranganathan, and R. K. Namballa, "VLSI Implementation of Invisible Digital Watermarking Algorithms Towards the Development of a Secure JPEG Encoder", in *Proceedings of the IEEE Workshop on Signal Processing Systems (SIPS)*, pp. 183-188, 2003 (67 papers accepted out of 118 submissions, acceptance rate - 56.7%).

Year 2002 and Before:

296. **S. P. Mohanty**, N. Ranganathan, and V. Krishna, "Datapath Scheduling using Dynamic Frequency Clocking", in *Proceedings of the IEEE-CS Annual Symposium on VLSI (ISVLSI)*, pp. 65-70, 2002.
297. **S. P. Mohanty**, K. R. Ramakrishnan, and M. S. Kanakanhalli, "A DCT Domain Visible Watermarking Technique for Images", in *Proceedings of the IEEE International Conference on Multimedia and Expo (ICME)*, Vol. 2, pp. 1029-1032, 2000 (400 accepted out of 650 submissions, acceptance rate - 61.5%).
298. **S. P. Mohanty**, K. R. Ramakrishnan, and M. S. Kanakanhalli, "An Adaptive DCT Domain Visible Watermarking Technique for Protection of Publicly Available Images", in *Proceedings of the International Conference on Multimedia Processing and Systems (ICMPS)*, pp. 195-198, 2000.
299. **S. P. Mohanty**, K. R. Ramakrishnan, and M. S. Kanakanhalli, "A Dual Watermarking Technique for Images", in *Proceedings of the 7th ACM International Multimedia Conference (ACMMM)*, Vol. 2, pp. 49-51, 1999.

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