Energy-Efficient Design of the Secure Better Portable Graphics Compression Architecture for Trusted Image Communication in the IoT

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***Abstract*—Energy consumption has become a major concern in portable applications. This paper proposes an energy-efficient design of the Secure Better Portable Graphics Compression (SBPG) Architecture. The architecture proposed in this paper is suitable for imaging in the Internet of Things (IoT) as the main concentration is on the energy efficiency. The novel contributions of this paper are divided into two parts. One is the energy efficient SBPG architecture, which offers encryption and watermarking, a double layer protection to address most of the issues related to privacy, security and digital rights management. The other novel contribution is the Secure Digital Camera integrated with the SBPG architecture. The combination of these two gives the best quality imaging in an energy efficient way without compromising security. To estimate the power in the proposed architecture a pattern-independent method has been adopted where many simulations run in the design with different inputs and the average of the power dissipated is considered. The current and voltage values are considered from the output of the design, in order to calculate power. This is achieved with the help of sensor and power blocks available in Simulink®. From the results obtained, it was observed that with the same peak signal to noise ratio, the power consumption is substantially reduced, up to 19%.**

***Index Terms*—Internet of Things (IoT), Image Communications, VLSI Architecture, Secure Better Portable Graphics Compression (SBPG), Energy-Efficient Design**

I. Introduction

One of the most important aspects of any portable application is power consumption. Low power consumption means extended battery life, which increases portability. Moreover, it decreases packaging costs, and is beneficial for cooling in both portable and non-portable applications [1]. It is very important for consumers to adapt their behaviors to the requirements of the devices, yet few people are aware of how they use and spend energy. The lack of awareness regarding this topic makes it difficult for people to change and adapt their behavior in order to increase efficiency. Any battery-powered system is dependent on its energy consumption level, thus understanding how a device uses energy is crucial in optimizing energy consumption. Energy consumption can be studied in terms of both software and hardware optimization. Innovators of the hardware industry investigate the levels of energy consumption for every new device and technique in order to optimize it. On the other hand, researchers from the software field investigate how the software itself and its different uses can influence energy consumption. An efficient software is capable of adapting to the requirements of everyday usage while saving as much energy as possible. Software engineers contribute to improving energy consumption by designing frameworks and tools used in the process of energy metering and profiling [2].

As a specific type of data, images can have a long life if stored properly. However, images require a large storage space. The process of storing an image starts with its compression. Through compression, the data volume is reduced, which facilitates both storage and transmission. A compression algorithm that can easily manage this task, BPG [3] is a novel step in the field of image compression that is highly effective because it is based on the High Efficiency Video Coding (HEVC) [4] standard, released in the beginning of 2013. HEVC/H.265 uses innovative tools and efficient methods for coding. While it can do impressive work when compared to its predecessor, H.264/ Advanced Video Coding, HEVC demands more resources because of its complexity. Specific requirements are needed to encode and decode high-resolution videos which only multi-core platforms can meet. These types of applications perform a reduction of bandwidth for transmission and storage by using video coding and real-time imaging.

Multimedia data such as images, video, or audio consume many resources and require complex computational operations that might be difficult to handle by the system. A limited memory for storage or limited energy supply might become challenges which decrease the possibility of maximizing the capabilities of the platform. VLSI technology is highly concerned with low power design, in an attempt to optimize battery-powered portable systems. These multimedia devices process large amounts of data [5]. When it comes to digital cameras, the operations done by the device are highly complex and include capturing real-time images, compressing and storing them.

This paper is structured in the follow manner: Section II highlights the novel contributions. In section III related research in the area of energy efficient design of secure digital camera as well as image communication in the IoT

are discussed. Section IV illustrates the SBPG for trusted image communication in the IoT from a broad application perspective. Section V provides an architectural overview of the SBPG integrated SDC. Section VI proposes the energy efficient design of the SBPG, followed by experimental results in Section VII and conclusions in Section VIII.

II. Novel Contributions of this Paper

Optimizing a hardware architecture of compression encoder for SBPG that is integrated with Secure Digital Camera is the main objective of this paper. High quality, energy efficiency and smaller size are the technological requirements that can be met as a result of BPG. To the best of the authors knowledge this is the first attempt to propose an energy efficient hardware architecture of Secure Digital Camera integrated with Secure Better Portable Graphics Compression encoder. The novel contributions of this work include: (1) The first-ever architecture for an energy efficient hardware of SBPG compression integrated with SDC, (2) The concept of SBPG that is integrated with SDC, which is suitable for low power intelligent traffic surveillance (ITS), (3) A Simulink® -based prototype of the algorithm implementation, and (4) An experimental analysis and evaluation of the proposed architecture.

III. Related Prior Research

The High Efficiency Video Coding (HEVC) standard is a newly designed video compressor. To evaluate its performance, the Joint Collaborative Team [6] has conducted verification tests, comparing HEVC with its most recent predecessor, the Advanced Video Coding (AVC). The results of the tests have shown that the HEVC standard distinguishes itself significantly from the AVC, being able to work at only half of the bit rate, while providing the same subjective quality.

The development of a low-power HEVC standard requires a detailed analysis of characteristics such as power consumption, temperature, or computational complexity. The study in [7] demonstrated a next-generation HEVC that maintains the right balance between power efficiency and quality of output but presents many challenges in terms of architectural techniques. In [8] motion compensation was partially studied. The complexity of this function makes motion compensation difficult to implement in hardware. However, the presented motion compensation architecture is able to overcome several hardware implementation challenges by integrating key elements like a 2D reference pixel data caching scheme, a pixel interpolation engine, and a DMA engine.

The study in [9] discovered that image encoding and decoding algorithms consume different levels of energy. It concluded that JPEG compression is the most energy efficient algorithm. Portable devices that use JPEG instead of PNG for image rendering and compression may increase battery life time by more than 50%. A new low-power and high-speed Discrete Cosine Transform (DCT) for image compression is proposed in [10]. The DCT has been designed for implementation on Field Programmable Gate Arrays (FPGAs). The DCT optimization requires less computations and less material complexity, which makes it highly power-efficient.

Rizzo et al. [11] presented lossless coding of AVIRIS data, which can be performed by two new methods. The two algorithms for hyperspectral image compression are low-complexity, yet outperform any other existent technique. The first algorithm is a based on a linear predictor, while the second one is based on a least-squares optimized linear predictor.The performance of a video compression algorithm is dependent upon its implementation on power-efficient systems. The implementation of an H. 264/AVC encoder on an Analog Devices Blackfin processor is presented in [12].

IV. SBPG for Trusted Image Communication in the IoT: A Broad Application Perspective

The IoT is an evolutionary step in technology. Home and mobile devices, or embedded applications connect to the Internet and extract information by using analytics. At any moment, the number of devices connected to the Internet is in the range of billions. Moreover, as time goes by, more and more devices will connect, until hundreds of billions of devices will be online. Devices from the same class also connect with each other, forming an intelligent network of systems. Making these systems of systems to communicate with each other, and share or analyze data through the cloud, can transform our relationship with technology forever. The new technology can add improvements in many important fields and can contribute significantly to our lives. It can develop medical applications, optimize energy consumption, or offer advanced products with low development. Thus, the IoT is an elastic technology that raises high expectations regarding its potential network capabilities, but which raises, at the same time, security concerns that threaten its future application. Some of these security concerns are connected to the common attacks conducted upon networked environments, such as Replay or Man in the middle attack [13]. Without a good protection system that could address these security issues and reduces the risks to a minimum, the technology is compromised. It is mandatory to ensure that the IoT data processing and high-source heterogeneous data are efficiently protected by keeping them private through hiding methods.

The Secure Digital Camera (SDC) is a device that combines the common features of a digital camera with a build-in system that facilitates functioning on low-power, low-cost and in real-time [1]. The device can easily incorporate a build-in BPG compression, encryption facility, and a watermarking function. Compared to JPEG compression, BPG compression proves to be more efficient. Not only it offers higher quality on lower size, but BPG is also better fit for real-time capability and bandwidth requirements. Usually integrated with SBPG, the SDC has multiple high standard functions, including encryption, or double-layered protection system. These functions have a key role in tasks that cover DRM-related issues, such as tracking usage, ownership rights, content authentication or tampering extent. Considering all its features, the SDC device represents, undoubtedly, one of the best methods available

for real-time rights management. Thus, the device is highly recommendable for real-time applications, including the IoT as a highway surveillance system.

In this paper, we propose an intelligent traffic surveillance system that uses the SDC device integrated with SBPG through the IoT. Essentially, the role of this smart traffic camera would be to monitor roads and keep track of all possible issues such as accidents, congestion, or severe weather conditions. The system communicates the status of the road to a main gateway which analyzes data from all cameras. This way, a large chain of communication forms and this wide chain leads to the creation of an intelligent traffic system which can cover an entire city. Moreover, more cities can connect their traffic systems and make them communicate to form an even wider and more intelligent system of systems. The possibilities of using such a system are endless. Analyzing data from one end of the system to understand its impact on the other end of the system could be done effortlessly. For example, an accident on a highway can be detected by the smart camera which will send the information to the city wide transportation system, where the information will be analyzed and the impact of the accident will be calculated, to understand how it will influence traffic on other segments of the road. If the accident takes place, for example, near an airport or near a school, then the systems could communicate with each other to adjust flights or change school schedule. The systems could also notify drivers through the city digital sign system about alternative routes and give them instructions on how to avoid the accident. While this is just a simple example, the introduction of the IoT in ITS could bring countless advantages and benefits. Fig. 1 shows the components of Intelligent Traffic Surveillance in IoT.

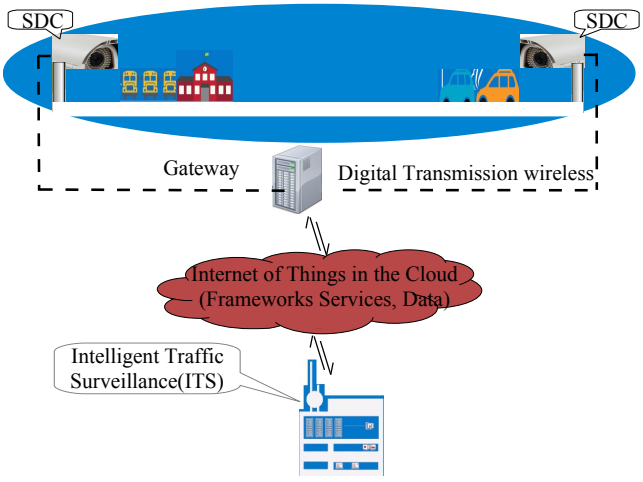

Fig. 1: Components of Intelligent Traffic Surveillance in the IoT.

V. Architectural Overview of SBPG Integrated SDC

Fig. 2 shows the system-level block diagram of the proposed Secure Better Portable Graphics integrated with Secure Digital Camera. The image sensor captures the image and converts it to a digital signal. The scratch memory then stores this digital signal temporarily and transmits it to the SBPG. This entire sequence of events is controlled by the controller unit. The schematic overview of the proposed SBPG module showing the order of operations is illustrated in Fig. 3, and is documented in more detail in [14]. The new Better Portable Graphics format has many significant advantages over the JPEG format [3]. The simplified BPG compression algorithm is illustrated in Algorithm 1, and details of its design are given in [15].

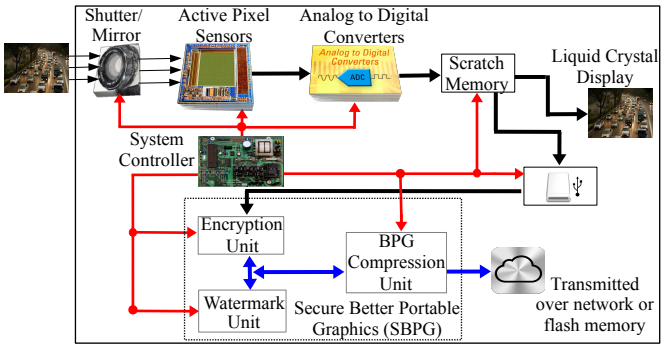

Fig. 2: System-level block diagram of SBPG integrated with SDC.

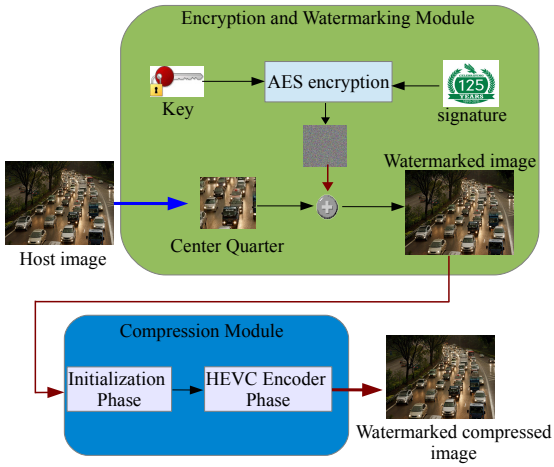

Fig. 3: Schematic overview of the proposed SBPG module.

VI. The Proposed Low Power of Secure Better Portable Graphics: Optimization Perspective

The optimized architecture of HEVC encoding is show in Fig. 4. First, advanced motion vector prediction is used for the prediction of the current motion vector, which uses a specific scheme belonging to a candidate group that includes both temporal motion vectors. To ensure that the best candidate is selected from the group, the encoder uses a rate distortion optimization process. The decoder is thus able to indicate and extract the best motion vector predictor by knowing the index. The proposed architecture includes in the competitive group

Algorithm 1 BPG Encoder Algorithm.

input $imageX$
get $Parameters \leftarrow \{PixelDpth, ColorSpace, Alpha\}$
calculate $Resolution \leftarrow \{pixels/inch\}$
calculate $ColorType \leftarrow \{TrueColor, GrayScale\}$
if $Length > 2$ **then**
    $Bitdepth \leftarrow \{MateData/ImageSize\}$
    if $Bitdepth \neq 8$ **then**
        $AlphaChannel \leftarrow \emptyset$
        print "ERROR: while opening bitdepth encoder"
else
if $Bitdepth \neq 8$ **then**
    $AlphaChannel \leftarrow \emptyset$
    print "ERROR: while opening bitdepth encoder"
if $ColorType < 12$ **then**
    print "ERROR: Color space is not supported"
end
print "Bit Depth and color space is supported"
print "Image accepted for BPG compression"
if $AlphaChannel \neq Null$ **then**
    use appropriate BPG CS RGB converter
else
if $AlphaChannel < 51$ **then**
    modify alpha to BPG configurable
end
use alpha image RGBA compatible HEVC
save output file BPG image
end

of candidates two neighboring candidates and one candidate from a co-located temporal area. After the derivation of the candidates, they go through a scanning process that checks for redundancy and eliminates duplicates from the existing list of candidates. If the number of the candidates in the list is lower than two, the list will receive an additional zero motion vector, which is useful for increasing the efficiency of partitioning representation. To make the prediction possible, the motion information of the reference pictures requires proper storage and must be made easily accessible. To keep the storage requirements to a minimum, the resolution of the motion information is kept at 16×16 for each block. The second key factor in the proposed architecture is DCT optimization and quantization, which is used to drive the interpolation filter to achieve the low-power design.

A. Motion Compensated Prediction

The HEVC encoding standard uses inter-prediction for the prediction block (PB) level [6]. Inter-prediction is best described as a motion compensated prediction, understood as the interchange and manipulation of areas from the reference picture in the construction of the current PB. Because of the distortion rate, the motion vectors are capable of representing a solid approximation of the motion, even though they cannot represent the true motion of the area involved. Analysis shows

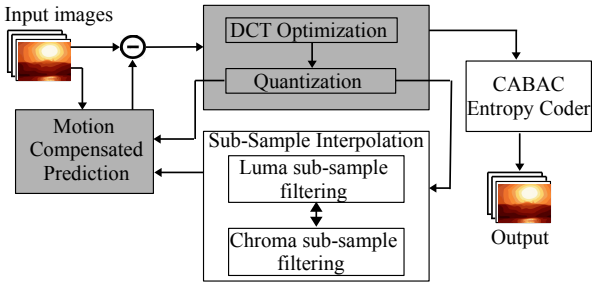

Fig. 4: Overview of the optimized HEVC encoding System.

that bi-prediction is the best choice because it provides a balance between compression performance and implementation complexity [16]. The only concern is with regard to the high amount of required memory, which can only be alleviated by hardware optimization. To limit the number of maximum possible motion compensation operations, inter-prediction is done only with smallest block sizes, 4×8 or 8×4.

The possibility of merging motion information is useful in efficiently encoding motion in cases of randomly shaped areas in a picture. Merge mode extracts the applicable motion information from a configurable group of candidates. The PB syntax can indicate which candidate motion information should be utilized by adding a merge index to the list of candidates.

B. DCT Optimization

The aim of DCT optimization is to minimize the number of arithmetic operations. Once the DCT is performed on the image block, there is a clear distinction of higher and lower frequency coefficients of the image. Lower frequency coefficients contain most of the visual information. The first row and first column in the block represent the DC component while the remaining blocks represent AC component. Since, it is possible to reconstruct the image just with the DC component along with few AC component of lower frequencies, this method results in a very computationally efficient circuit without compromising the quality of the image. By discarding the high frequency coefficients, high image compression can be achieved as well.

For DCT-based interpolation, initially a forward DCT is performed over N neighboring samples. Then the DCT coefficients are reconstructed from the shifted center location with a shift δ [16]. The above two steps are merged to derive the filter coefficients.

C. Sub-Sample Interpolation

In dealing with the luma and chroma components, HEVC uses the same motion vectors. To reduce these effects and raise the level of precision, HEVC also uses an increased dynamic range. In motion compensated prediction, a series of steps including filtering, dynamic range change, and horizontal or vertical shifting are performed in order to generate the prediction signal. Sub-sample locations are extracted using corresponding fixed interpolation filters from the sub-sample

luma values in the case of luma sub-sample interpolation. The sub-sample location on the corresponding motion vector is determined using a modulo operation. A similar process is executed for the chroma sub-sample interpolation as for the luma sub-sample interpolation.

D. Mechanism of Power Measurement

Speed and power are a trade off when the devices are used in real-time. Power estimation can be broadly categorized into pattern-dependent and pattern-independent approaches. In the pattern-dependent method, the simulation results are considered for estimating the power dissipation. In this design the pattern-independent method has been adopted, i.e. many simulations were run in the design with different inputs and the average of the power dissipated was considered. The design is considered as a black box and the current and voltage values are considered from the design, in order to calculate power. This was achieved with the help of sensors and power blocks available in Simulink®. The design is simulated using the `ode45` solver configuration, as shown in fig. 5.

VII. Experimental Results

The low-power architecture of SBPG was implemented in MATLAB®/Simulink® Version 8.3 (R2014a), with the computer vision System Toolbox Version 9.7 [17]. The reason behind using MATLAB® is due to the fact that it provides a better understanding of the low-level implementation while Simulink® provides top-level functional blocks such as sensors and power blocks as well as dataflow visualization [1]. With different spatial and frequency characteristics, five standard images were selected randomly from a set of Joint Picture Expert Graphics (JPG) images. For a sample image, the cover image and corresponding BPG image are shown in Fig. 6. Table I illustrates the related metrics for the baseline design [14] and the proposed optimal design. The experimental results prove that the proposed-SBPG architecture is an energy-efficient design with no significant effect on the quality, compared with the baseline design. It is observed that for almost the same PSNR, the power consumption of the optimal SBPG design is substantially reduced. Figures 7, 8, and 9 analyze and illustrate the related metrics for the "Wallpaper", "Resort", "Squirrel", "F16", and "Lena" images.

TABLE I: Quality Metrics for the proposed architecture and Comparative Perspective with Baseline Design.

Test Image	SBPG Baseline [14]		SBPG Optimal Design		Power Reduction
	PSNR	Power	PSNR	Power	
Wallpaper 128×128	50.2	8.09	49.31	6.63	18%
Resort 256×156	47.14	8.2	46.82	6.89	16%
Squirrel 256×256	50.37	8.22	50.19	6.85	17%
F16 512×512	48.09	8.3	47.5	6.90	17%
Lena 512×512	51.9	8.55	50.03	6.94	19%

VIII. Conclusions And Future Directions for Research

In this paper, an energy-efficient architecture to perform secure BPG compression encoding is proposed as a built-in function in a secure digital camera (SDC), which is suitable for image communications in the Internet of Things (IoT). The proposed architecture is prototyped in Simulink®. The experimental results prove that the proposed architecture is a low-power design with no significant change in the quality compared with the baseline design. To the best of the authors knowledge, this is the first ever proposed energy-efficient architecture for SBPG compression integrated with SDC. The experimental results demonstrate that the optimal SBPG design yields a power consumption up to 19% lower than the unoptimized design. Further work could introduce the SBPG in medical image communication in the IoT.

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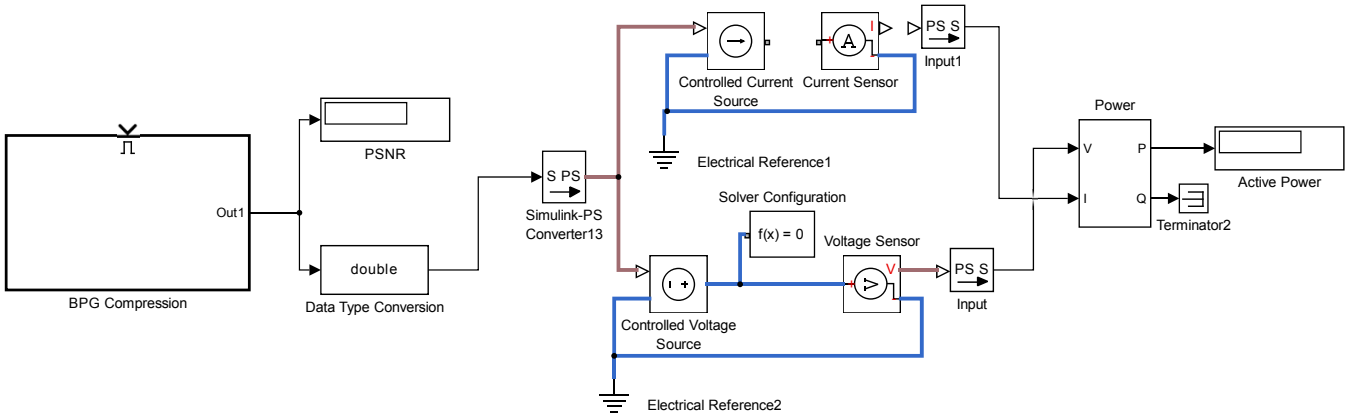

Fig. 5: Simulink® power measurement setup.

(a) Cover Image. (b) Watermarked Image (c) Watermarked Compressed Image

Fig. 6: Secure BPG Compression of "Resort" Image (256×256).

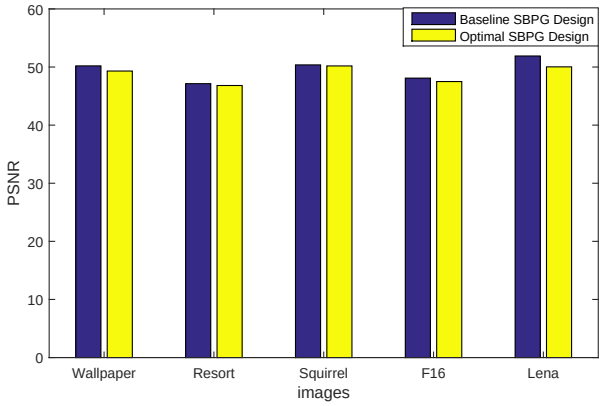

Fig. 7: Comparison of Baseline SBPG with Final Optimal Design in Terms of PSNR.

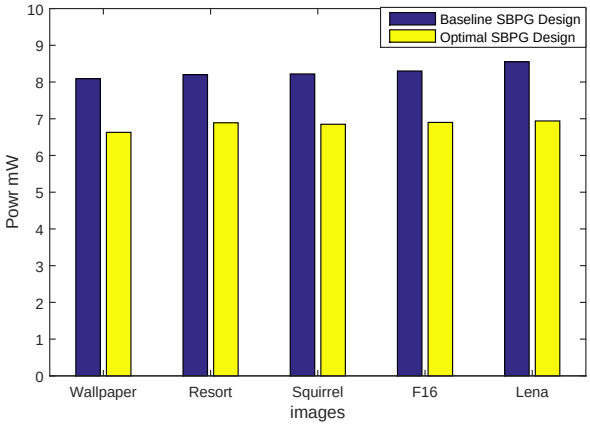

Fig. 8: Comparison of Baseline SBPG with Final Optimal Design in Terms of Power Consumption.

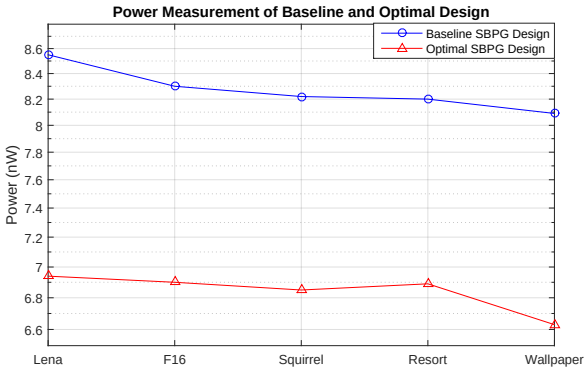

Fig. 9: Comparison of Baseline SBPG with Final Optimal Design in Terms of Power Consumption.

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