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~~SPECIAL SECTION ON IEEE/ACM SLIP WORKSHOP 2016~~

SPECIAL SECTION ON HARDWARE ASSISTED TECHNIQUES FOR IOT AND BIGDATA APPLICATIONS

~~SPECIAL SECTION ON PRIME 2016 AND SMACD 2016~~

Special section on Hardware Assisted Techniques for IoT and Bigdata Applications

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Guest Editorial - Special Issue on Hardware Assisted Techniques for IoT and Bigdata Applications

The emerging concept of "Smart Cities" or "Intelligent Cities" gains increasing popularities. There is a push for it due to the fact that resources are limited, while population growth (particularly the urban population growth) are uncontrolled. The smart cities can be conceptualized as the regular cities with information and communication technology and smart technology (e.g. sensors, actuators, WiFi connectivity). A typical smart city can have one or more smart components such as smart grid, smart healthcare, and smart transportations. For the realization as well as efficient operation of the smart cities the two related emerging technology frameworks viz. Internet of Things and Big Data are crucial. The core technology for communication infrastructure in smart city implementation is the Internet of Things (IoT). IoT infrastructure consists of various components including electronics, software, sensors, and networks. Big Data refers to a collection of complex data sets difficult to process using conventional processors, database tools, and data processing applications. The urban data with spatial and temporal characteristics generated in the smart cities may be Big Data. For example, The Big Data in the smart cities may be generated from a large collection of sensors, databases, emails, websites, and social media.

The research on IoT studies the network of interconnected physical objects referred to as "things', such as computers, mobile phones, sensors, actuators, wearable devices, vehicles, homes, buildings, and even energy systems etc. It enables the communications of many diverse types of applications for providing increasingly smart, reliable and secure services. The vision of IoT is to connect each and every object and thereby utilize the enormous capability of internetworked knowledge base during their operations. It is not about how to add a particular service to a specific product, but to turn the signal and information generated by several sensors, devices, things, and services to some meaningful knowledge about the environment and thereby to initiate some meaningful action. All the devices can be monitored and can be controlled remotely in real-time manner, if required. RFID tagging, sensor technology, networking, and nanoscale computing are playing major roles to enable IoT in reality. In a complex as well as real time IoT infrastructure, data exchanged during communication among manufacture, operators, and connected devices are typically of large volume called as the Big Data.

IoT, together with the processing of the involved Big Data, requires high performance computational techniques for real-time physical object control and data processing. When the data are big, the challenges become proportionately big. In an IoT system huge amount of data needs to be managed in each second. It is estimated that 220 Exabytes of data will be stored in the current year. The big-data concept must be implemented in IoT to manage this enormous amount of data. The development of IoT techniques needs the consideration of many factors such as computational performance, energy efficiency, security, privacy, reliability and flexibility that necessitate salient big data modeling and analytical techniques. More importantly, they impose significant hardware design challenges on the associated embedded systems and VLSI circuits. Examples include optimization of IoT system performance considering stringent energy limit in the embedded system and ensuring high security in information exchange. The salient IoT infrastructure development needs to address these challenges at all scales, ranging from sensors, integrated circuits to embedded systems. The full-customer design methodology can no longer handle the increasing IoT design complexity. Thus, there is a pressing need for developing high performance design automation techniques for the next generation IoT systems.

Based on the above background and motivation, this special issue initiated to serve as a framework to present state-of-the-art hardware assisted techniques and solutions for IoT system designs and big data applications. The call for papers for this Special Issue was widely distributed in various social media, mailing lists, and well known conferences. The submission was open to any researcher to submit their research findings having scientific contributions matching the scope of the special issue. The guest editors also selectively invited some potential authors to submit extended versions of their conference papers which come under the scope of this special issue. All the papers open or invited from conferences went through rigorous review process through the online system

(http://ees.elsevier.com/vlsi/) to meet the quality control guidelines of Elsevier Integration journal. This special issue consists of several interesting contributions. In the rest of the editorial, these papers will be briefly discussed.

The IoT design and operation framework considering energy consumption, area, performance, and security is important. Hamadeh, et al. in "Area, Energy, and Time Assessment for a Distributed trusted platform module (TPM) for Distributed Trust in IoT Clusters" present a mechanism for the assessment and optimization of them in IoT clusters. Typically, IoT clusters are heterogeneous in characteristics and can have application in various smart city components such as airport and highways in which trust is an important feature. This research demonstrates significant reductions in both the energy consumption and the execution time per IoT node while supporting TPM protocols.

Wired and wireless network form the backbone of IoT technology. It is of paramount importance that the network is robust, fault tolerant, secure, and recovers to healthy state if anything goes wrong for any reasons. Roy, et al. in "A Framework for Post-Disaster Communications using Wireless Ad Hoc Networks" present an ad hoc wireless network framework for post-disaster communications. The proposed solution provides higher longevity, lower end-to-end delay, and higher throughput.

Signal sensing for analysis and action based on the sensed information is key functions of the IoT in smart cities applications. He, et al, in "A High Precise E-nose for Daily Indoor Air Quality Monitoring in Living Environment" present an E-nose that uses neural network learning for low-cost accurate indoor air quality monitoring.

In the IoT enabled smart cities, smart healthcare can be a major component. Singh, et al. in "Energy Efficient Electroencephalogram (EEG) Acquisition and Reconstruction for a Wireless Body Area Network" present design of optimal system components which can be potentially used for smart healthcare. It presents an Analog to Information Converter (AIC) which makes sensing energy efficient and can be deployed easily in Wireless Body Area Networks (WBAN).

The application of IoT and bigdata frameworks for real-life applications is crucial to ensure that these are useful in the user domains. DiBiano, et al. in "Automated Diagnostics for Manufacturing Machinery Based on Well-Regularized Deep Neural Networks", present such a research. In this research deep neural network that relies on hierarchical learning is used in a bigdata framework for full-automation of diagnostics of manufacturing machinery. Various forms of signals such as emitted sound, emitted vibrations, and magnetic field data are used for fault detection and day-to-day operation metering in the noninvasive machine diagnostics.

It is a fact that there are often differences in the algorithm view and hardware view of the data. This leads to various issues such as energy and delay bottleneck of memory, particularly large datasets. Venkatesan, et al. in "Shaping Data for Application Performance and Energy Optimization in Dynamic Data View Framework" present a solution for this issue. The technique relies on arranging the non-contiguous large data set to a contiguous data set. The dynamic data view (DDV) framework results in a lower cache access energy and program execution time reduction.

Power dissipation and performance trade-offs points of view the heterogeneous computing systems consisting of application specific accelerators, graphics processing unit (GPU) along with the General Purpose Processors can be helpful. Nalesh, et al. "Energy Aware Synthesis of Application Kernels through Composition of Datapaths on a Coarse Grained Composable Reconfigurable Array (CGCRA)", present synthesizing application kernels expressed as functions to generate the optimal accelerators automatically. This can be very effective for dark silicon problem mitigation in which a portion of circuitry is underutilized as need to operate below nominal voltage and maximum frequency due to thermal design power (TDP) constraints. It may be noted that one reason

for dark silicon is that supply voltage doesn't scale at the same rate as the operating frequency and integration density.

Dark silicon problem has been addressed by Zhao et al. in "A Novel Switchable Pin Method for Regulating Power in Chip-Multiprocessor". The method relies on the placement of several groups of parallel switchable pins between the memory and core such that the proposed bi-directional I/O pads can dynamically switch between power supply and data transmission modes.

Digital signal processors are omnipresent in all modern electronic systems that deals with some form of media. One example of digital signal processing is Discrete Fourier Transform (DFT). Fenga, et al. in "AutoNFT: Architecture Synthesis for Hardware DFT of Length-of-Coprime-Number Products" present a novel synthesis tool called AutoNFT. AutoNFT can synthesize parallel DFT architectures.

For high speed communication in IoT, better communication hardware is absolutely necessary. Majumder, et al. "Threshold Adjustment of Receiver Chip to Achieve a Data Rate > 66Gbit/sec in point to point interconnect" present an efficient design for very high speed communication. Specifically, implementation of two methods of receiver chip threshold voltage specification is presented for high-speed square wave transmission.

The design of energy efficient transreceiver chips can be useful for sustainable communication networks. Mondal, et al., "A Mathematical Formulation to Design and Implementation of a Low Voltage Swing Transceiver Circuit" designs for accurate sending of low voltage swings. The proposed design approach reduces the short circuit power due to low voltage swing to a negligible value.

In the long distance and high speed data transmission data can have errors which lead to bad and even unreliable communications. Mitra, et al., in "Reconfigurable Very High Throughput Low latency VLSI (FPGA) Design Architecture of Cyclic Redundancy Checksum (CRC) 32" present hardware for CRC implementation so that it can be used for efficiently in a transreceiver chip.

Security and Intellectual Property (IP) protection are of paramount importance in IoT besides the energy consumption and performance. Kumar, et al. in "Design Exploration of a Symmetric Pass Gate Adiabatic Logic for Energy-Efficient and Secure Hardware" present the use of adiabatic logic for energy efficiency and security enhancement of the hardware. Specifically, a novel Symmetric Pass Gate Adiabatic Logic (SPGAL) for uniform power dissipation profile as well as low power operations so that the hardware is tolerant to Differential Power Analysis (DPA).

The use of third party IP cores in emerging hardware and system design for increasing design productivity in the reduced time to market is getting popular. In such case, IP protection of hardware in the context of global design and manufacturing flow is crucial to protect the ownership of the hardware. Sengupta, et al. in "Low Cost Optimized Trojan Secured Schedule at Behavioral Level for Single & Nested Loop Control Data Flow Graphs" secured a low cost HLS approach for hardware IP core designs that can detect Trojan as well.

The physical unclonable functions (PUFs) are being considered as security primitives which rely on features of the semiconductor manufacturing process technology to create randomness. Kumar, et al. in "Secure Split Test Techniques to Prevent IC Piracy for IoT Devices" introduce a PUF based secure split test with functional testing capability (SSTF) to mitigate the counterfeits coming out from untrusted foundries. The proposed PUF-SSTF are fully prototypes and validated in bother FPGA and ASIC forms.

Efficient design of PUFs can be useful for better security implementation. Sahoo, et al. in "A Novel Current Controlled Configurable Ring Oscillator (RO) PUF with Improved Security Metrics" propose ring oscillator based PUF with that objective. Specifically, a novel Current-Controlled RO PUF in which inverters of RO uses different logic for both power and area efficient realizations.

The guest editors would like to thank editor-in-chief (EiC) of Elsevier Integration Dr. Sheldon Tan for the opportunity for this special issue. The guest editors are grateful to the active reviewers around the globe for their timely reviews. The guest editors thank the authors for their patience and dedication at all stages of the review process without which this successful special issue would not have been possible. The guest editors are also thankful to the Elsevier staffs for their help during this special issue. The guest editors sincerely think that this special issue on the hot topic will be a great reading for the contemporary researchers worldwide.

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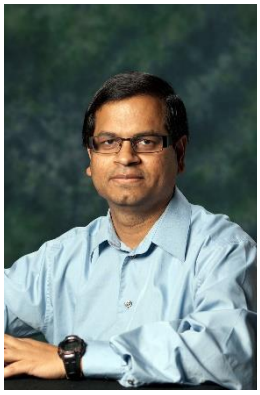

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