

CSCE 3730: Reconfigurable Logic -- Course Project

Deadline: 2nd Dec 2008 (Tuesday)

Design and simulate a 4-bit ALU using hierarchical VHDL. You should first design a 1-bit ALU and then use component and port map statements to instantiate it in your top level architecture. The operation codes of the 4-bit ALU is shown in Table 1. Your ALU should generate the same outputs (“Result” and “Overflow”) for the given inputs shown in Table 2.

Table 1: ALU Operation Code Table.

ALU control lines				Function
Binvert	S1		S0	
0	0		0	and
0	0		1	or
0	1		0	add
1	1		0	subtract
1	1		1	set on less than

Things you need to know:

1. “Input A”, “Input B”, and “Result” are represented in two’s complement format.
2. The output “Overflow” should be ‘1’ to indicate an overflow, otherwise, it should be ‘0’.)
3. “Opcode” is a vector of control lines “Binvert” (MSB), “S1”, and “S0” (LSB).

Table 2: Sample inputs and outputs of the 4-bit ALU.

Opcode	Input A	Input B	Result	Overflow
000	1001	1101	1001	0
001	1001	1101	1101	0
010	0110	0001	0111	0
010	1010	0010	1100	0
010	0110	0010	1000	1
110	0110	0011	0011	0
110	1000	0100	0100	1
111	0100	0011	0000	0
111	1000	0110	0001	0

Requirements:

1. This project is a group project with each group consisting of exactly two students.
2. Each group submits only one project report.
3. The report should cover aspects required in previous labs. Include all VHDL source codes and your test bench file. In addition, clearly describe each member’s role in this project.
4. There will be project demo on 2nd Dec 08 (Tuesday) and 4th Dec 08 (Thursday).