

NOC

- Introduction:

Interconnection networks are used to interconnect either single or sets of components within a computer system, or multiple computer systems; the interconnection aspect of computer architecture has gained significant importance in recent years, with regard to the impact of different solutions on the overall performance and cost of the whole system.

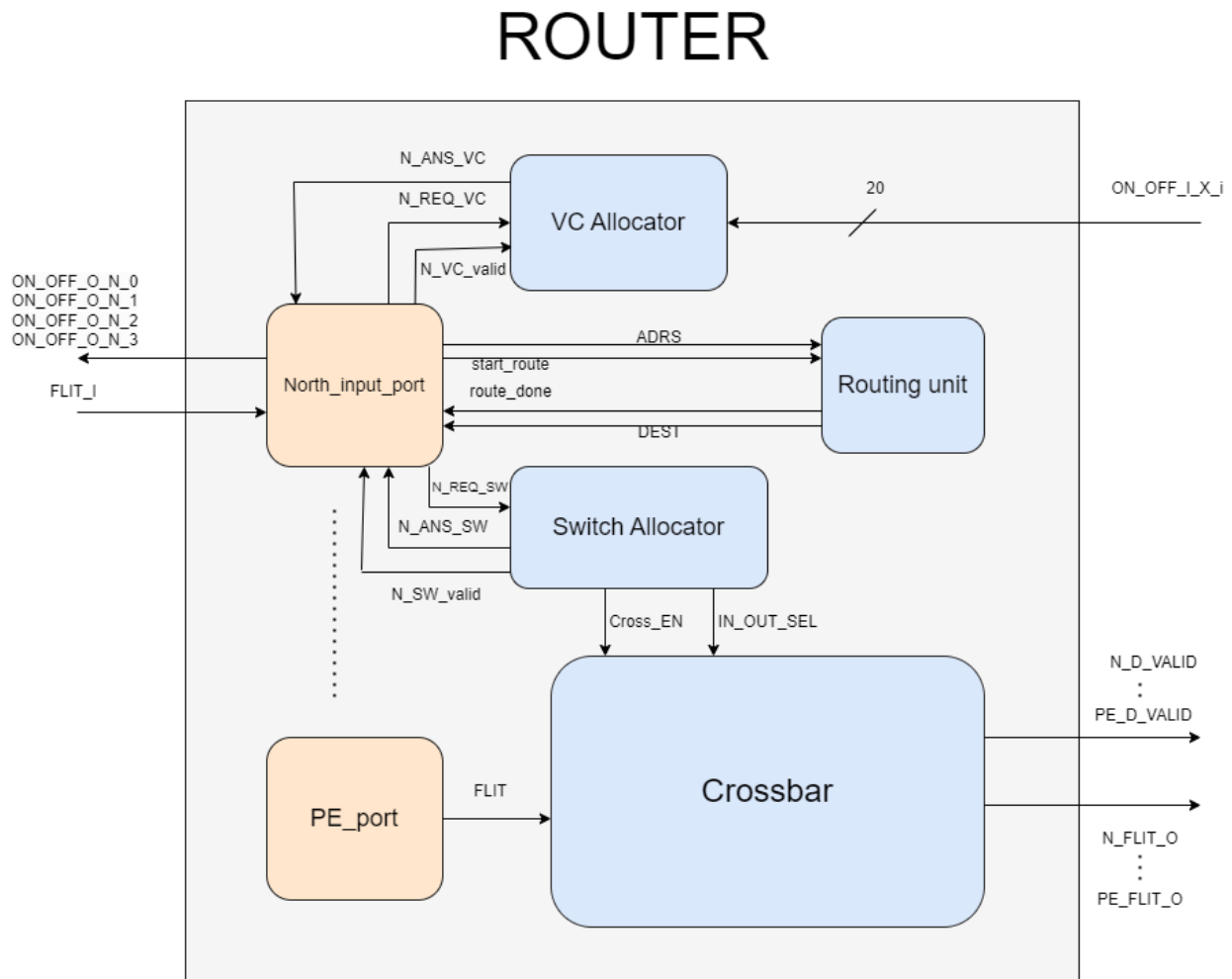
One of the main networking domains, and the subject of this project, is Network-on-Chip (NoC), in which the interconnection network is used for interconnecting micro-architecture functional units, register files, caches, compute tiles and processor and IP cores within chips or multi-chip modules; current and near future NoCs support the connection of a few tens to a few hundreds of such devices with a maximum interconnection distance on the order of centimeters.

- Specifications of design :-

- A Network-on-Chip interconnection module has been developed, with a **2D mesh topology (3X3mesh)**.
- The routers allocate data at **flit granularity**, implementing a **wormhole switching architecture** further optimized by the presence of multiple virtual channels per input, avoiding the Head of Line blocking issue and thus allowing a higher average throughput to the network.
- Packet routing is driven by **[Node-based Routing algorithm with West-first Turn Model technique]**, independently computed by each router belonging to the mesh.
- Flow control is implemented **in the switching activity management**, which is controlled by a per-router switch allocation unit, and uses the **On-Off algorithm**, easy to implement but efficient enough for a **medium level of traffic** in the network.

Design and implementation

- Router Block diagram



The router contains 5 blocks:

- INPUT_PORTS module consists of five input ports: N,S,E,W,PE.
- Routing_unit module.
- VC_Allocator module.
- Switch_allocator module.
- Crossbar module.

Packet configurations: -

- Maximum number of packets is 8. [sequence number 3-bit]
- Each packet contains 8 flits.

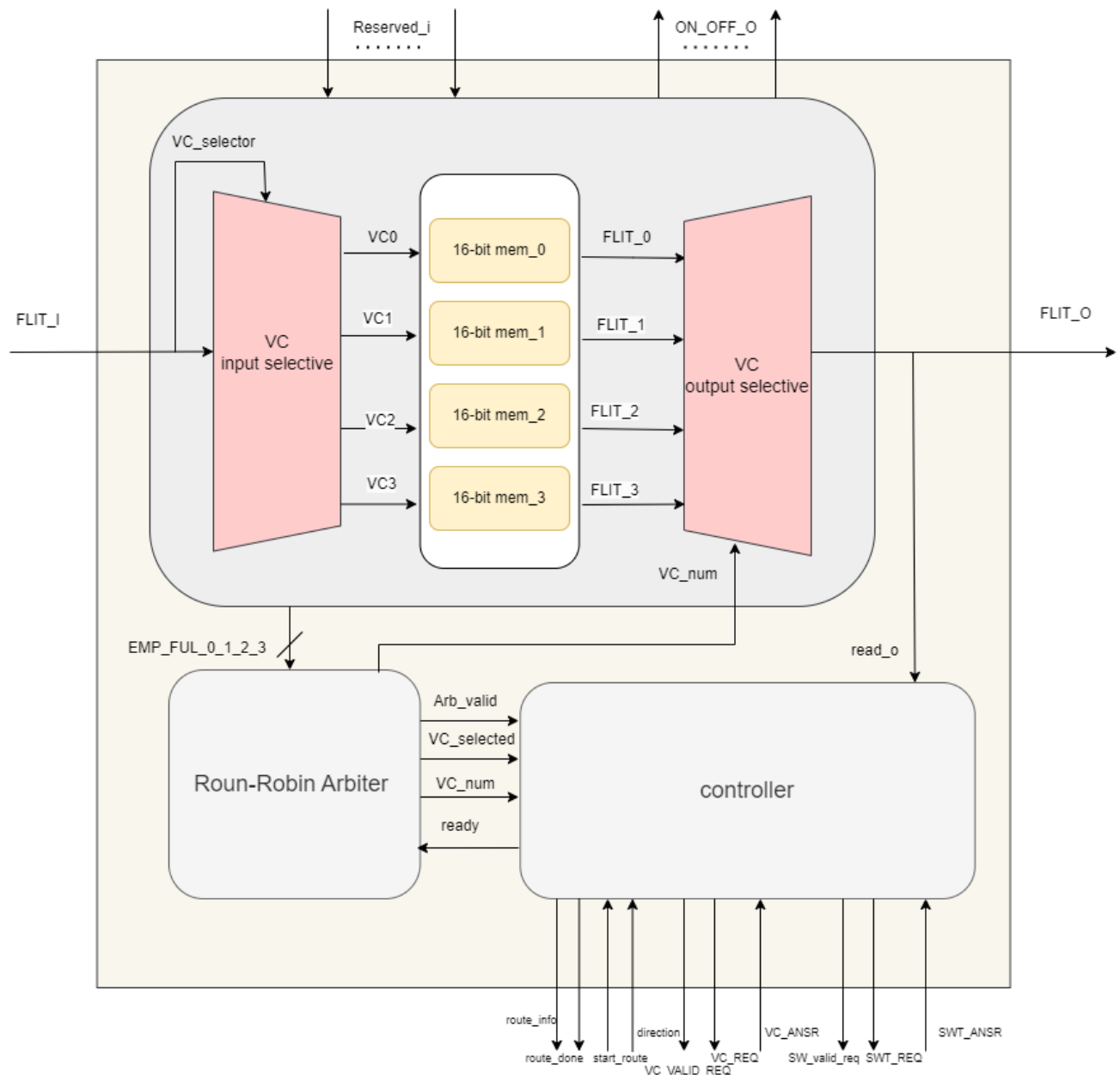
VC identifier [2-bit]	Type [2-bit]	Sequence number [3-bit]	Data [9-bit]
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- Sequence number: number of the packet which the flit belongs to.
- VC identifier: number of the VC.
 - VC0
 - VC1
 - VC2
 - VC3
- Type: the type of carried data on the flit {Header, Body, Tail}.
 - Header = 2'b00
 - Body = 2'b01
 - Tail = 2'b10

Input Port module.

- is responsible for storing the flits that comes from its input interface matching the correspondent **virtual channel id**.
- One router has exactly 5x input modules, each input module has 4 **virtual channels**.
- Each input port has Roun-Robin Arbiter to choose between VCs.

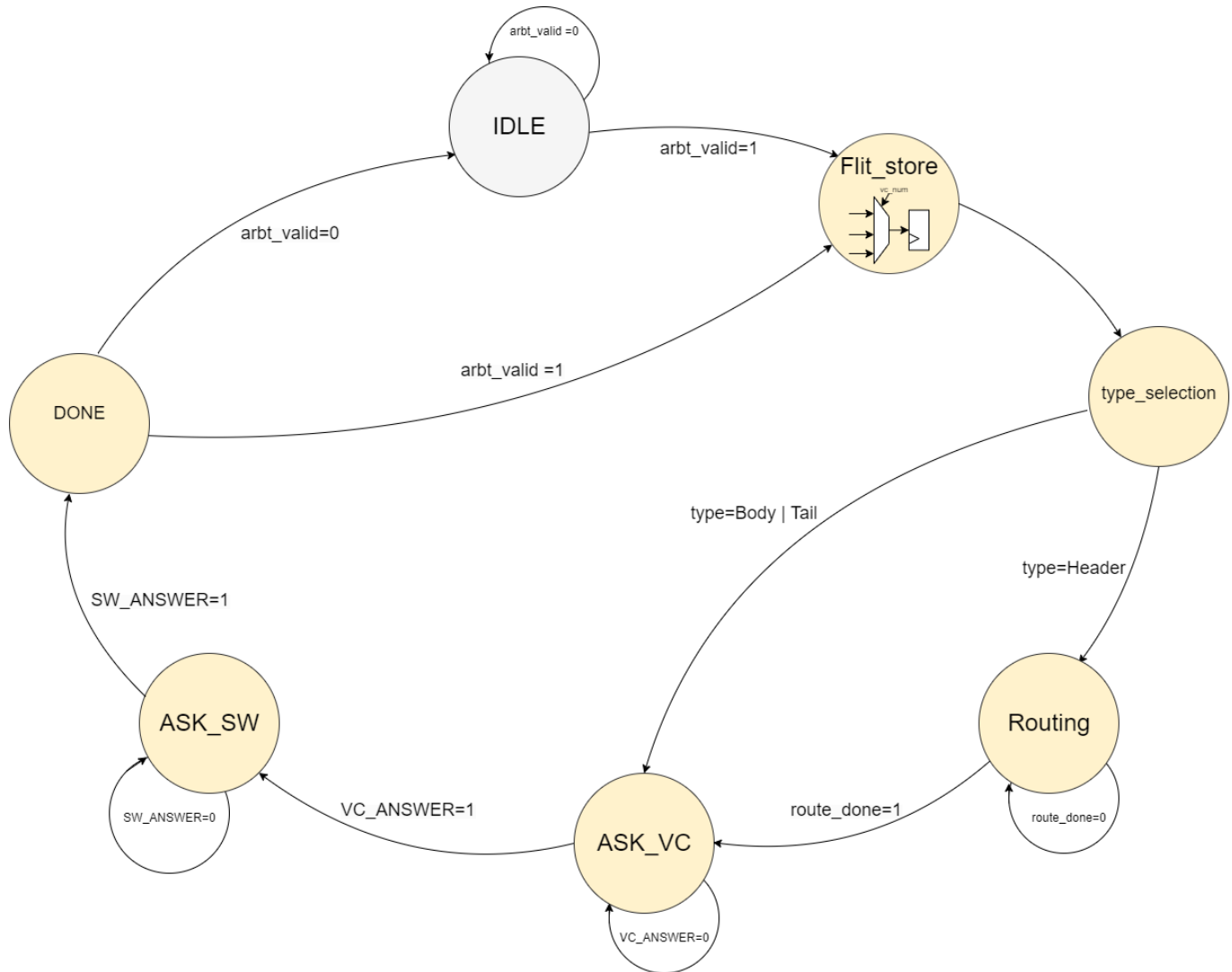
INPUT PORT MODULE



Signals description:-

Pot	width	direction	description
FLIT_I	16-bit	input	The incoming flit from the upstream router.
direction	3-bit	input	The direction which Computed by the routing unit.
VC_ANSR	1-bit	input	The evaluated signal after the VC allocation is done.
SWT_ANSR	1-bit	input	The evaluated signal after the switch allocation is done.
Route_info	4-bit	output	It contains destination node data from the incoming flit going to routing unit to compute the next direction
VC_REQ	5-bit	output	{evaluated output port , VC number} going to VC allocator to check the availability of VCs in the downstream router.
VC_valid_req	1-bit	output	This is a control signal for the VC_ALLOCATOR
SWT_REQ	3-bit	output	the evaluated output port going to switch allocator to check the availability of this output port in the current router.
SW_valid_req	1-bit	output	This is a control signal for the switch_ALLOCATOR
ON_OFF_0_1_2_3	1-bit	output	Control signals for the upstream VC allocator High when there is a valid VC and low when the VC is reserved
Reserved_0_1_2_3	1-bit	input	A control signal from the upstream vc allocator to reserve the valid VC.
FLIT_O	16-bit	output	The output flit from the input port I to the cross bar.

Input controller



IDLE state: it is the default state & reset state of the finite state machine.

Ready	This signal is high at the IDLE state and when there is no operations in the controller	Output to Arbiter
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Flit_store state: this state responsible for storing the selected flit into a register.

Type_selection state: this state selects the type-bits then decide,

If (type-bits = header):

- It will send the address-bits stored in the register to the Routing unit.

If (type-bits = body or tail):

-

- It will take the routing information which stored while Routing state, and Sending the request to the vc_allocator.

Route_info	It contains the routing informatin in the flit	Out to Routing unit
Start_route	This signal is high for one clock cycle when sending the routing information and low otherwise	Out to Routing unit
Vc_request	It contains the output port calculated from the routing unit and the vc number {out_port,vc_numb}	Out to VC Allocator
valid_vc_req	This signal is high only for one clock cycle while sending the Vc_request	Out to VC Allocator

Routing state: this state wait for the routing unite output, then store the calculated direction for the flit labeled by it's sequence number.

Vc_request	It contains the calculated output port and the VC number {out_port,vc_numb}	Out to VC Allocator
valid_vc_req	This signal is high only for one clock cycle while sending the Vc_request	Out to VC Allocator

ASK_VC state: it is responsible for waiting the answer of the VC Allocator and sending the request to the switch allocator after the VC Allocator is done.

Vc_request	This signal will be in the same data until the VC answer is positive	Out to VC Allocator
Sw_request	It contains the calculated output port and the VC number {out_port,vc_numb}	Out to switch Allocator
Valid_sw_req	This signal is high only for one clock cycle while sending the sw_request	Out to switch Allocator

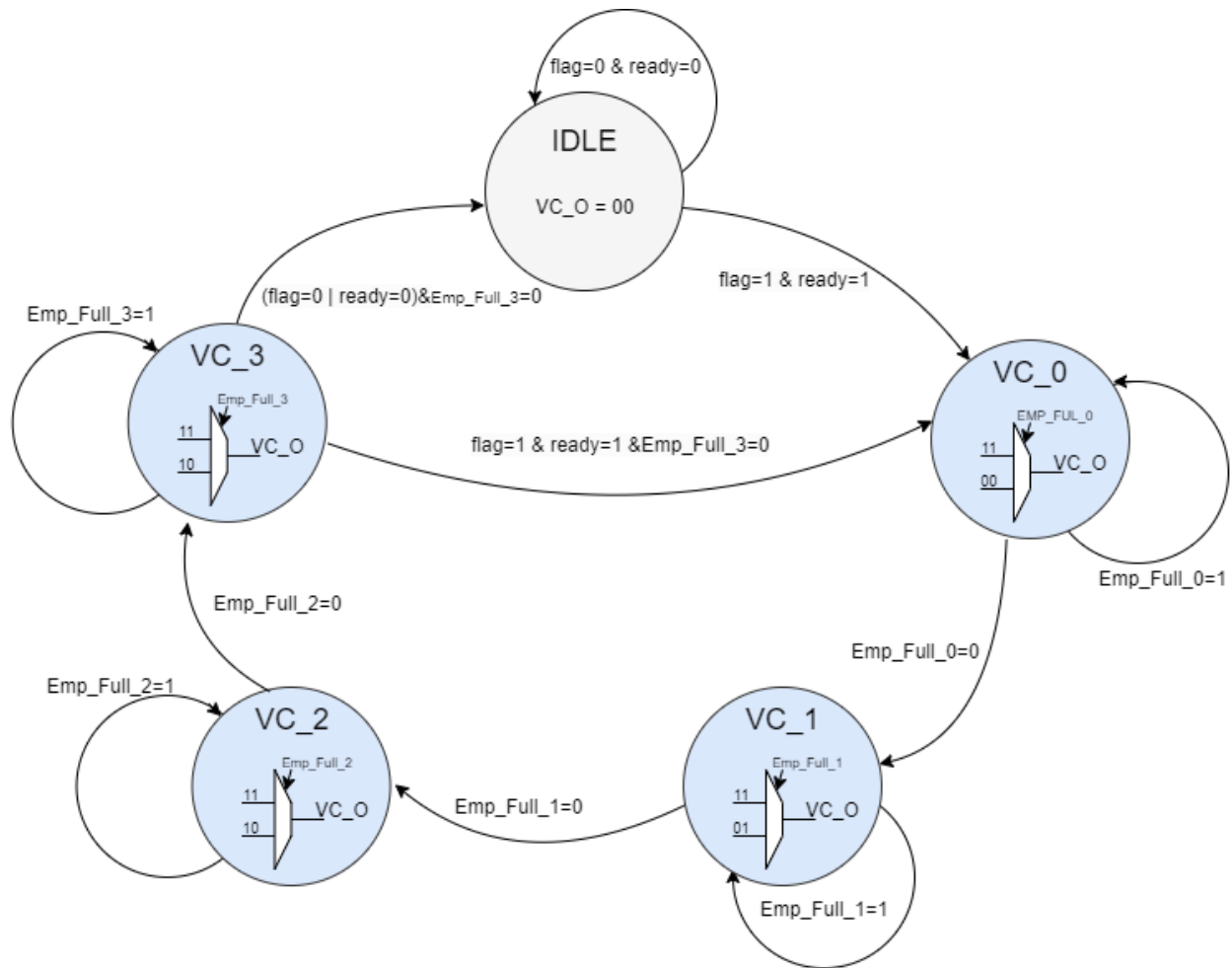
ASK_SW state: this state also waits for the answer of the switch allocator to select the output VC .

Sw_request	It contains the calculated output port and the VC number {out_port,vc_numb}	Out to switch Allocator
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DONE state: it is responsible for making the ready signal high and check if the Arbiter ready or not.

Ready	This signal is high at the IDLE state and when there is no operations in the controller	Output to Arbiter
clear	This is high for one clock to clear the vc and deactivate the empty/full signal and activate the on/off signal	Out to input buffer

Round-Robin Arbiter for input Port



- Flag signal consists of {EMP_FULL_0, EMP_FULL_1, EMP_FULL_2, EMP_FULL_3}.
- Ready signal is a control signal coming from the controller.
- VC_O signal carries the VC number to the controller.

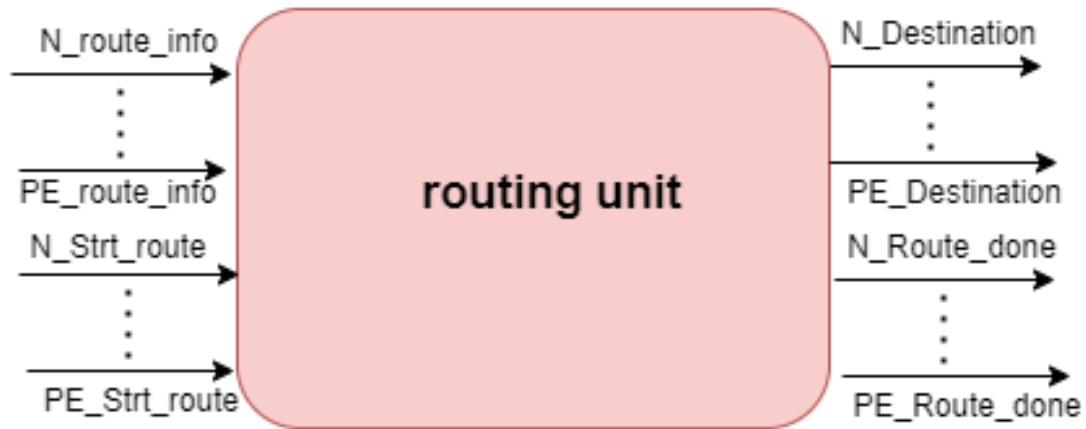
IDLE state: the default state & reset state of the finite state machine.

VC_x state: responsible for choosing the VC number x if it's VC is full and still in until the controller done of it.

Route computation Unit

- the route computation unit computes the next hop for each packet as soon as the head flit arrives to the router and sends the result to the input port unit.
- the implemented routing algorithm [**Node-based Routing with West-first Turn Model technique**] requires only information about the position of the current router and of the destination router in the 2D mesh. As the table below.

Node-based routing table for a 3×3 mesh with West-First turn model									
	00	01	02	10	11	12	20	21	22
00	X	N-	N-	E-	EN	EN	E-	EN	EN
01	S-	X	N-	ES	E-	EN	ES	E-	EN
02	S-	S-	X	ES	ES	E-	ES	ES	E-
10	W-	W-	W-	X	N-	N-	E-	EN	EN
11	W-	W-	W-	S-	X	N-	ES	E-	NE
12	W-	W-	W-	S-	S-	X	ES	ES	E-
20	W-	W-	W-	W-	W-	W-	X	N-	N-
21	W-	W-	W-	W-	W-	W-	S-	X	N-
22	W-	W-	W-	W-	W-	W-	S-	S-	X



Signals description:-

Port	width	direction	description
X_route_info	4-bit	input	It contains the destination node data from the incoming flit from the input port (X) to compute the next direction
X_Start_route	1-bit	input	This signal is high for one clock cycle when sending the routing information and low otherwise
X_ROUTE_Done	1-bit	output	This signal is high when finishing the routing computation and low otherwise.
X_Destination	4-bit	output	The direction of the packet.

(X) CORRESPONDING TO THE NAME OF THE INPUT PORT(N,S,W,E,PE)

VC Allocator

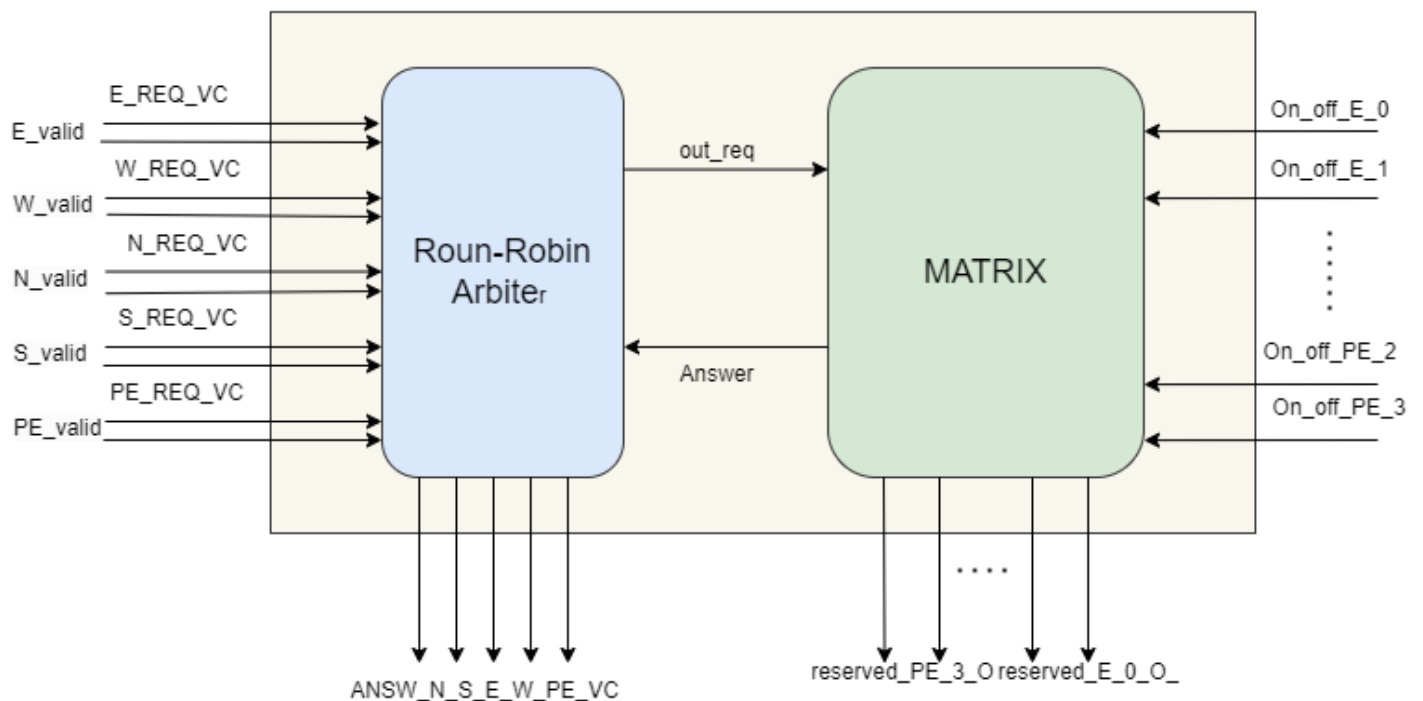
It responsible for checking the availability of VCs in the downstream router.

- A separable input-first allocator is used inside the VC allocator unit.
- It is implementation by Applying a matrix contains all resources with respective to its availability.
- Round-Robin Arbiter to choose between requests.

The available resources matrix:

VCi\PORTS	North	South	East	Weast	PE
VC_0	ON_OFF_N_0	ON_OFF_S_0	ON_OFF_E_0	ON_OFF_W_0	ON_OFF_PE_0
VC_1	ON_OFF_N_1	ON_OFF_S_1	ON_OFF_E_1	ON_OFF_W_1	ON_OFF_PE_1
VC_2	ON_OFF_N_2	ON_OFF_S_2	ON_OFF_E_2	ON_OFF_W_2	ON_OFF_PE_2
VC_3	ON_OFF_N_3	ON_OFF_S_3	ON_OFF_E_3	ON_OFF_W_3	ON_OFF_PE_3

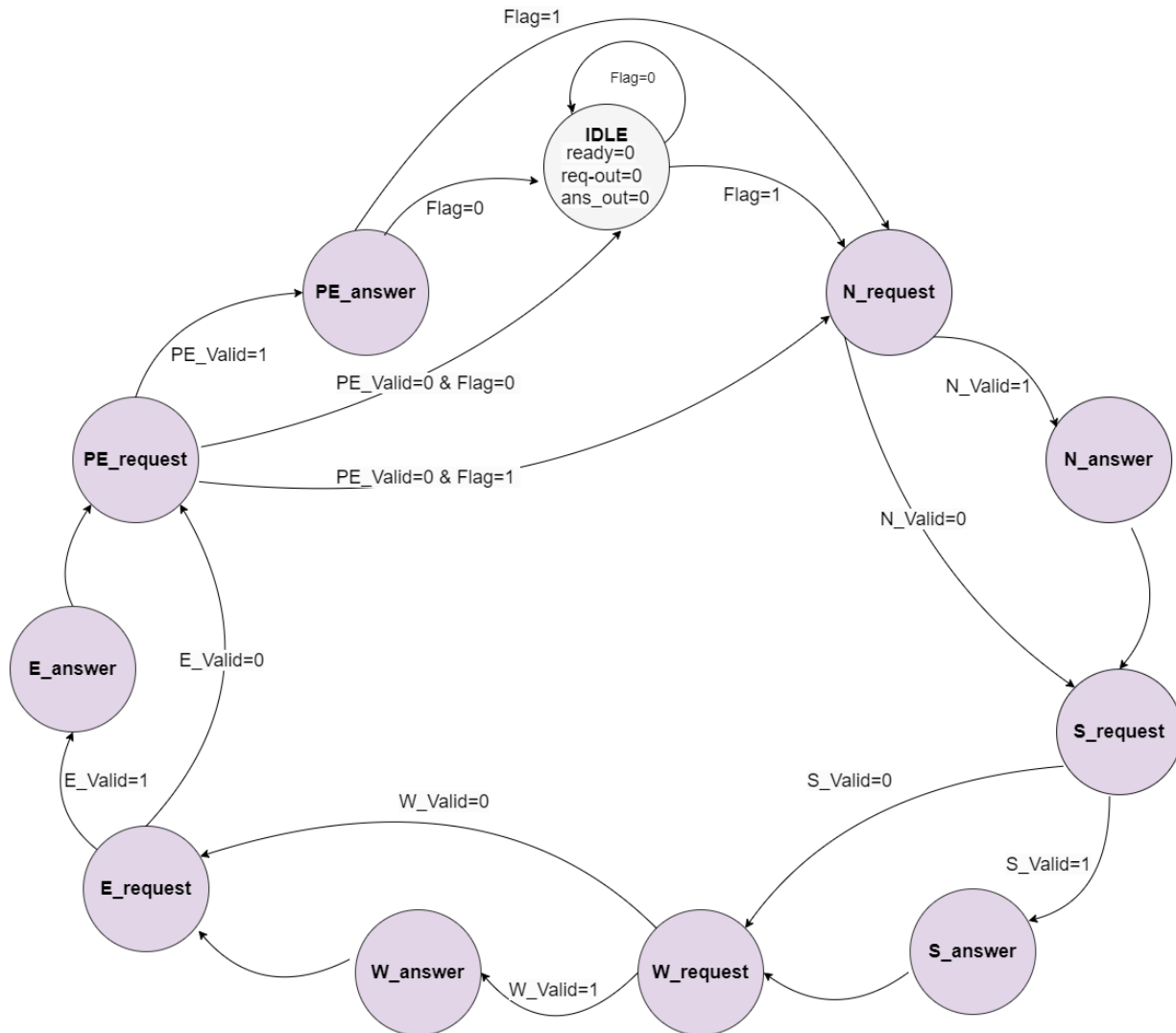
VC ALLOCATOR



Signals description:-

Port	width	direction	description
E_REQ_VC	5-bit	input	East port request consists of {evaluated output port , VC number} coming to check the availability of VCs in the downstream router.
W_REQ_VC	5-bit	input	west port request consists of {evaluated output port , VC number} coming to check the availability of VCs in the downstream router.
N_REQ_VC	5-bit	input	north port request consists of {evaluated output port , VC number} coming to check the availability of VCs in the downstream router.
S_REQ_VC	5-bit	input	south port request consists of {evaluated output port , VC number} coming to check the availability of VCs in the downstream router.
PE_REQ_VC	5-bit	input	Processing Element port request consists of {evaluated output port , VC number} coming to check the availability of VCs in the downstream router.
On_off_x_i	1-bit	input	A single bit signal coming from each VC in each input port of the downstream router, it represents it's VC empty or full if {zero} full if {1} Empty and ready to receive a flit.
:			
On_off_PE_20			
ANSW_N_VC	1-bit	output	This signal represents the acceptance of the incoming request from the North input port.
ANSW_S_VC	1-bit	output	This signal represents the acceptance of the incoming request from the South input port.
ANSW_E_VC	1-bit	output	This signal represents the acceptance of the incoming request from the East input port.
ANSW_W_VC	1-bit	output	This signal represents the acceptance of the incoming request from the West input port.
ANSW_PE_VC	1-bit	output	This signal represents the acceptance of the incoming request from the PE input port.
Reserved_x_0	1-bit	output	This signal goes out to the downstream router to announce that a specific VC is reserved and it's on_off signal must be low
:			
Reserved_x_20			

Round-Robin Arbiter for VC Allocator



_ Flag signal: consists of {N_Valid, S_Valid, E_Valid, W_Valid, PE_Valid,}.

_ req_out signal: the signal which carries the chosen request from it's state going out to the matrix.

_ ans_out signal : this signal carries the answer which comes from the matrix to get out of the VC Allocator module.

_x_reserved_i_o signals: this signal is High if the answer=1 in it's port(x) state
And low other wise.

The request states: responsible for checking if there is a valid request and send it to the matrix.

req_out	6-bit	Carries the request bits	Out to the matrix
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The answer states: responsible for capturing the answer from the matrix and make the ready signal low.

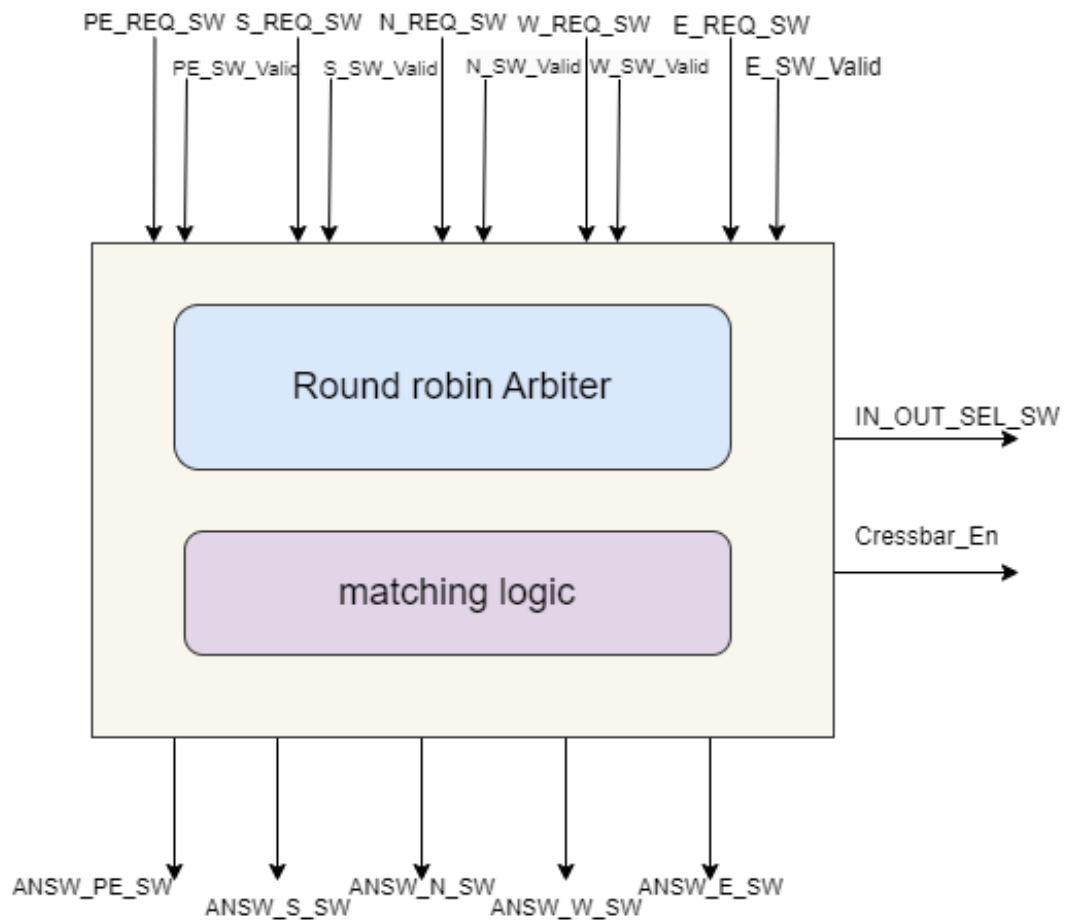
Ans_out	1-bit	Carries the answer captured from the matrix	Out to the INPUT Module
x_reserved_i_o	1-bit	It represents if the on_off signal of a specific VC is reserved or not.	Out to downstream input port

Switch Allocator

The switch allocator module solves the contention between input buffers for the access to the crossbar switch.

- By implementing a separable input-first allocator and thus sending control signals to the crossbar module and to the input buffers.
- And Round-Robin Arbiter to choose between the available output ports.

SWITCH ALLOCATOR

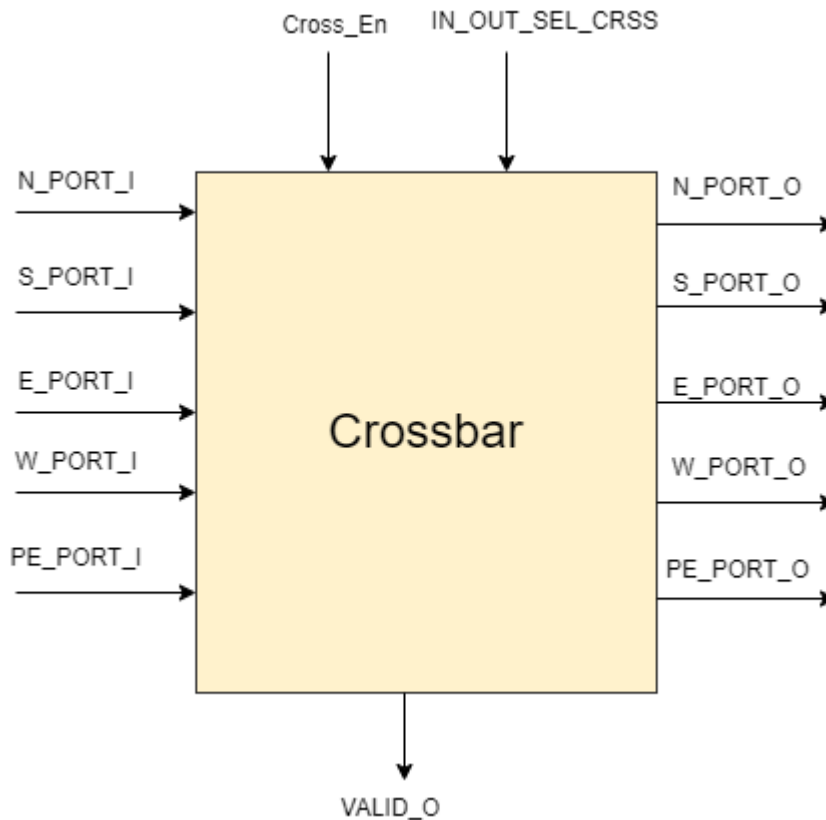


Signals description:-

Port	width	direction	description
E_REQ_SW	3-bits	input	East port request consists of {evaluated output port} coming to check the availability of this output port in the current router.
W_REQ_SW	3-bits	input	west port request consists of {evaluated output port} coming to check the availability of this output port in the current router.
N_REQ_SW	3-bits	input	north port request consists of {evaluated output port} coming to check the availability of this output port in the current router.
S_REQ_SW	3-bits	input	south port request consists of {evaluated output port} coming to check the availability of this output port in the current router.
PE_REQ_SW	3-bits	input	PE port request consists of {evaluated output port} coming to check the availability of this output port in the current router.
X_SW_Valid	1-bit	input	The valid signal is high when the request ready for the switch and low when the answer of the switch is high.
:			
X_SW_Valid			
ANSW_E_SW	1-bit	output	This signal represents the acceptance of the incoming request from the East input port.
ANSW_W_SW	1-bit	output	This signal represents the acceptance of the incoming request from the West input port.
ANSW_N_SW	1-bit	output	This signal represents the acceptance of the incoming request from the North input port.
ANSW_S_SW	1-bit	output	This signal represents the acceptance of the incoming request from the South input port.
ANSW_PE_SW	1-bit	output	This signal represents the acceptance of the incoming request from the PE input port.
IN_OUT_SEL_SW	6-bit	output	The signal which control the cross bar it's consists of {input port , output port }
Crossbar_En	1-bit	output	This enable signal is high when IN_OUT_SEL_SW signal is ready and low otherwise

Crossbar

Cross bar module allows moving flits from input Block to output ports allowing only one input to propagate at a time. And input and output selection are done through switch allocator.

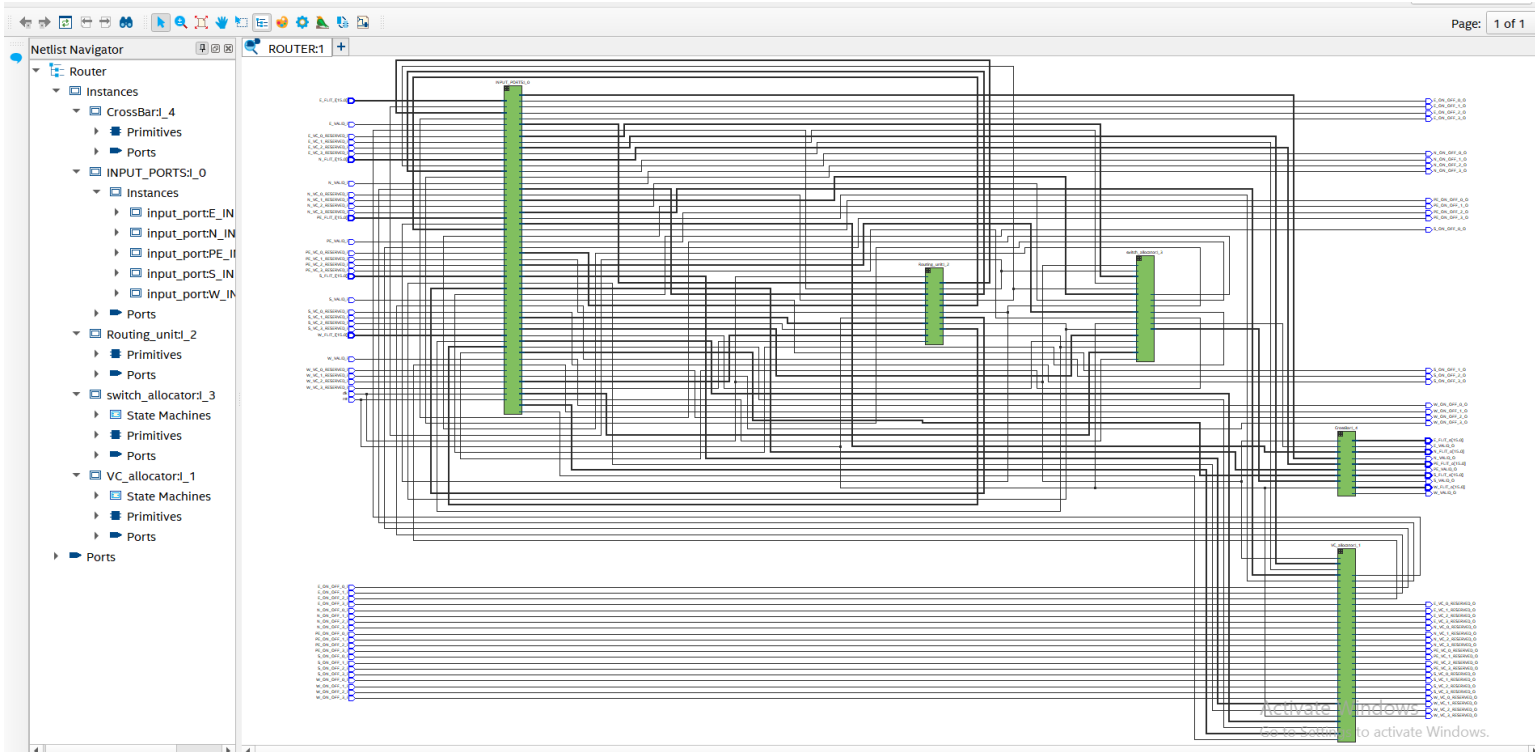


Signals description:-

Port	width	direction	description
IN_OUT_SEL_CRSS	8-bit	input	The signal which control the cross bar it's consists of {input port , output port }
N_PORT_I	16-bit	input	Input ports
S_PORT_I	16-bit	input	
E_PORT_I	16-bit	input	
W_PORT_I	16-bit	input	
PE_PORT_I	16-bit	input	

Cross_En	1-bit	input	A control signal for the crossbar from the switch allocator to take the data from input.
N_PORT_O	16-bit	output	Output ports
S_PORT_O	16-bit	output	
E_PORT_O	16-bit	output	
W_PORT_O	16-bit	output	
PE_PORT_I	16-bit	output	
Valid_O	1-bit	output	This signal is high when the data ready at the crossbar to go to the downstream router

Synthesis & RTL Netlist for Router



Analysis & Synthesis Summary

Analysis & Synthesis Status: Successful - Fri Dec 22 21:39:03 2023

Quartus Prime Version: 22.1std.2 Build 922 07/20/2023 SC Lite Edition

Revision Name: ROUTER

Top-level Entity Name: Router

Family: Cyclone V

Logic utilization (in ALMs): N/A

Total registers: 717

Total pins: 252

Total virtual pins: 0

Total block memory bits: 0

Total DSP Blocks: 0

Total HSSI RX PCSs: 0

Total HSSI PMA RX Deserializers: 0

Total HSSI TX PCSs: 0

Total HSSI PMA TX Serializers: 0

Total PLLs: 0

Total DLLs: 0

Tasks

Compilation

Compilation Report - ROUTER

Table of Contents

- Flow Summary
- Flow Settings
- Flow Monitor/Default Global Settings

Analysis & Synthesis Messages

Processing (34)

Type ID Message

- Running Quartus Prime Analysis & Synthesis
- Command: quartus_map --read_settings_files-on --write_settings_files-off ROUTER -c ROUTER
- 18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_
- 20030 Parallel compilation is enabled and will use 14 of the 14 processors detected
- 12021 Found 1 design units, including 1 entities, in source file pr_arbiter.v
- 12021 Found 1 design units, including 1 entities, in source file input_port.tb.v
- 12021 Found 1 design units, including 2 entities, in source file input_port.v
- 12021 Found 1 design units, including 1 entities, in source file input_buffers.v
- 12021 Found 1 design units, including 1 entities, in source file controller.v
- 12021 Found 1 design units, including 1 entities, in source file vc_allocator.v
- 12021 Found 1 design units, including 1 entities, in source file switch_allocator.v
- 12021 Found 1 design units, including 1 entities, in source file crossbar.v
- 12021 Found 1 design units, including 1 entities, in source file routing_unit.v
- 12021 Found 1 design units, including 1 entities, in source file router.v
- 12021 Found 1 design units, including 1 entities, in source file input_ports.v
- 12021 Found 1 design units, including 1 entities, in source file router.tb.v
- 12127 Elaborating entity "Router" for the top level hierarchy
- 12128 Elaborating entity "INPUT_PORTS" for hierarchy "INPUT_PORTS:I_0"
- 12128 Elaborating entity "input_port" for hierarchy "INPUT_PORTS:I_0input_port:N_INPUT_PORT"
- 12128 Elaborating entity "INPUT_BUFFERS" for hierarchy "INPUT_PORTS:I_0input_port:N_INPUT_PORT[INPUT_BUFFERS:I_0]"
- 10264 Verilog HDL Case Statement information at INPUT_BUFFERS.v(129): all case item expressions in this case statement are onehot
- 12128 Elaborating entity "PR_ARBITER" for hierarchy "INPUT_PORTS:I_0input_port:N_INPUT_PORT[PR_ARBITER:I_0]"
- 12128 Elaborating entity "CONTROLLER" for hierarchy "INPUT_PORTS:I_0input_port:N_INPUT_PORT[CONTROLLER:I_0]"
- 12128 Elaborating entity "VC_allocator" for hierarchy "VC_allocator:I_3"
- 12128 Elaborating entity "Routing_unit" for hierarchy "Routing_unit:I_2"
- 12128 Elaborating entity "switch_allocator" for hierarchy "switch_allocator:I_3"
- 12128 Elaborating entity "Crossbar" for hierarchy "Crossbar:I_4"
- 286030 Timing-Driven Synthesis is running
- 17049 32 registers lost all their fanouts during netlist optimizations.
- 14400 Generated suppressed messages file d:/digital_design/noe/RTL/quartus/router/output_files/ROUTER_map.smg
- 16010 Generating hard_block partition "hard_block:auto_generated_inst"
- 21057 Implemented 1468 device resources after synthesis - the final resource count might be different
- Quartus Prime Analysis & Synthesis was successful. 0 errors, 1 warning

System: Processing (34)

Filter (place&route)

The screenshot shows the Quartus Fitter Summary report for the ROUTER project. The left pane displays the Project Navigator with the 'Filter' task selected under 'Compilation'. The right pane shows the 'Fitter Summary' report, which includes a 'Table of Contents' and a 'Fitter Status' section.

Table of Contents:

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
 - Filter
 - Summary
 - Settings
 - Parallel Compilation
 - Netlist Optimizations
 - Incremental Compilation Section
 - Pin-Out File
 - Resource Section
 - I/O Rules Section
 - Device Options
 - Operating Settings and Conditions
 - Estimated Delay Added for Hold Timing
 - Messages
 - Suppressed Messages
 - Flow Messages
 - Flow Suppressed Messages

Fitter Summary:

Fitter Status: Successful - Fri Dec 22 22:01:52 2023

Quartus Prime Version: 22.1std.2 Build 922 07/20/2023 SC Lite Edition

Revision Name: ROUTER

Top-level Entity Name: Router

Family: Cyclone V

Device: 5CEBA7F27C7

Timing Models: Final

Logic utilization (in ALMs): 515 / 56,480 (< 1 %)

Total registers: 753

Total pins: 252 / 336 (75 %)

Total virtual pins: 0

Total block memory bits: 0 / 7,024,640 (0 %)

Total RAM Blocks: 0 / 686 (0 %)

Total DSP Blocks: 0 / 156 (0 %)

Total HSSI RX PCSs: 0

Total HSSI PMA RX Deserializers: 0

Total HSSI TX PCSs: 0

Total HSSI PMA TX Serializers: 0

Total PLLs: 0 / 7 (0 %)

Total DLLs: 0 / 4 (0 %)

The screenshot shows the Quartus Messages window for the ROUTER project. The left pane displays the Project Navigator with the 'Filter' task selected under 'Compilation'. The right pane shows the 'Fitter Summary' report, which includes a 'Table of Contents' and a 'Fitter Status' section.

Table of Contents:

- Flow Summary
- Flow Settings

Fitter Status: Successful - Fri Dec 22 22:01:52 2023

The Messages window displays the following messages:

- 119006 Selected device 5CEBA7F27C7 for design "ROUTER"
- 21077 Low junction temperature is 0 degrees C
- 21077 High junction temperature is 85 degrees C
- 171003 Fitter is performing an Auto Fit compilation, which may decrease Fitter effort to reduce compilation time
- 292013 Feature LogicLock is only available with a valid subscription license. You can purchase a software subscription to gain full access to this feature.
- 15714 Some pins have incomplete I/O assignments. Refer to the I/O Assignment Warnings report for details
- 169085 No exact pin location assignment(s) for 252 pins of 252 total pins. For the list of pins please refer to the I/O Assignment Warnings table in the fitter report.
- 184020 Starting Fitter peripheral placement operations
- 11191 Automatically promoted 2 clocks (2 global)
- 184021 Fitter peripheral placement operations ending: elapsed time is 00:00:00
- 176233 Starting register packing
- 332104 Reading SDC File: 'ROUTER.sdc.sdc'
- 332152 The following assignments are ignored by the derive_clock_uncertainty command
- 332129 Detected timing requirements -- optimizing circuit to achieve only the specified requirements
- 332111 Found 1 clocks
- 176235 Finished register packing
- 11798 Fitter preparation operations ending: elapsed time is 00:00:10
- 170189 Fitter placement preparation operations beginning
- 14951 The Fitter is using Advanced Physical Optimization.
- 170190 Fitter placement preparation operations ending: elapsed time is 00:01:42
- 170191 Fitter placement operations beginning
- 170137 Fitter placement was successful
- 170192 Fitter placement operations ending: elapsed time is 00:00:11
- 170193 Fitter routing operations beginning
- 170195 Router estimated average interconnect usage is 0% of the available device resources
- 170199 The Fitter performed an Auto Fit compilation. Optimizations were skipped to reduce compilation time.
- 170194 Fitter routing operations ending: elapsed time is 00:00:06
- 11888 Total time spent on timing analysis during the Fitter is 2.73 seconds.
- 334003 Started post-fitting delay annotation
- 334004 Delay annotation completed successfully
- 334003 Started post-fitting delay annotation
- 334004 Delay annotation completed successfully
- 11801 Fitter post-fit operations ending: elapsed time is 00:00:13
- 144001 Generated suppressed messages file D:\digital_design\Noc/RTL/quartus/router/output_files/ROUTER.fit.smsg
- Quartus Prime Fitter was successful. 0 errors, 4 warnings

Timing analysis

_ clock period 7.2n

_ No setup violation at all corners

Slow 1100mV 0C Model Setup Summary			
<<Filter>>			
	Clock	Slack	End Point TNS
1	clk	0.465	0.000

Fast 1100mV 0C Model Setup Summary			
<<Filter>>			
	Clock	Slack	End Point TNS
1	clk	4.168	0.000

Fast 1100mV 85C Model Setup Summary			
<<Filter>>			
	Clock	Slack	End Point TNS
1	clk	3.885	0.000

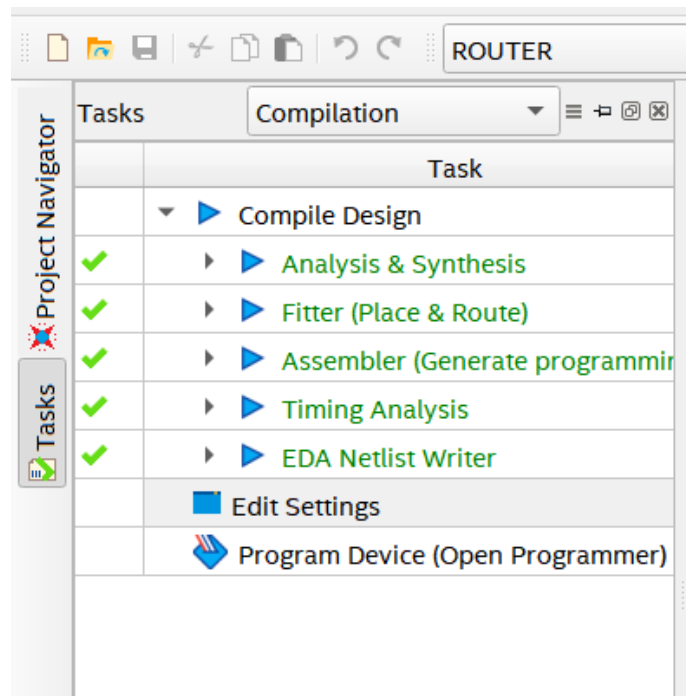
___ No Hold violation at all corners

Slow 1100mV 85C Model Hold Summary			
<<Filter>>			
	Clock	Slack	End Point TNS
1	clk	0.361	0.000

Fast 1100mV 0C Model Hold Summary			
<<Filter>>			
	Clock	Slack	End Point TNS
1	clk	0.162	0.000

Multicorner Timing Analysis Summary						
<<Filter>>						
	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	▼ Worst-case Slack	0.465	0.162	N/A	N/A	2.837
1	clk	0.465	0.162	N/A	N/A	2.837
2	▼ Design-wide TNS	0.0	0.0	0.0	0.0	0.0
1	clk	0.000	0.000	N/A	N/A	0.000

Router Flow is completed



Router simulation

Router simulation

- 1- When 5 input for 5 different input ports to five different output ports:

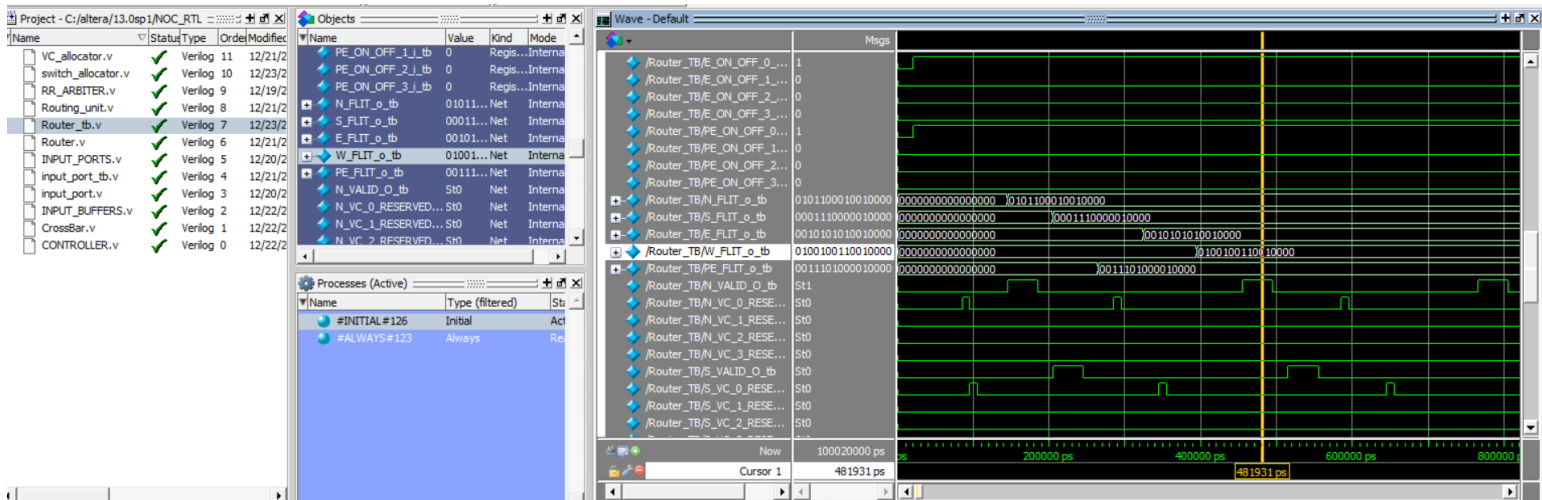


Fig. five inputs to different output ports.

- 2- When 2 different flits on 2 different input ports to same output ports:

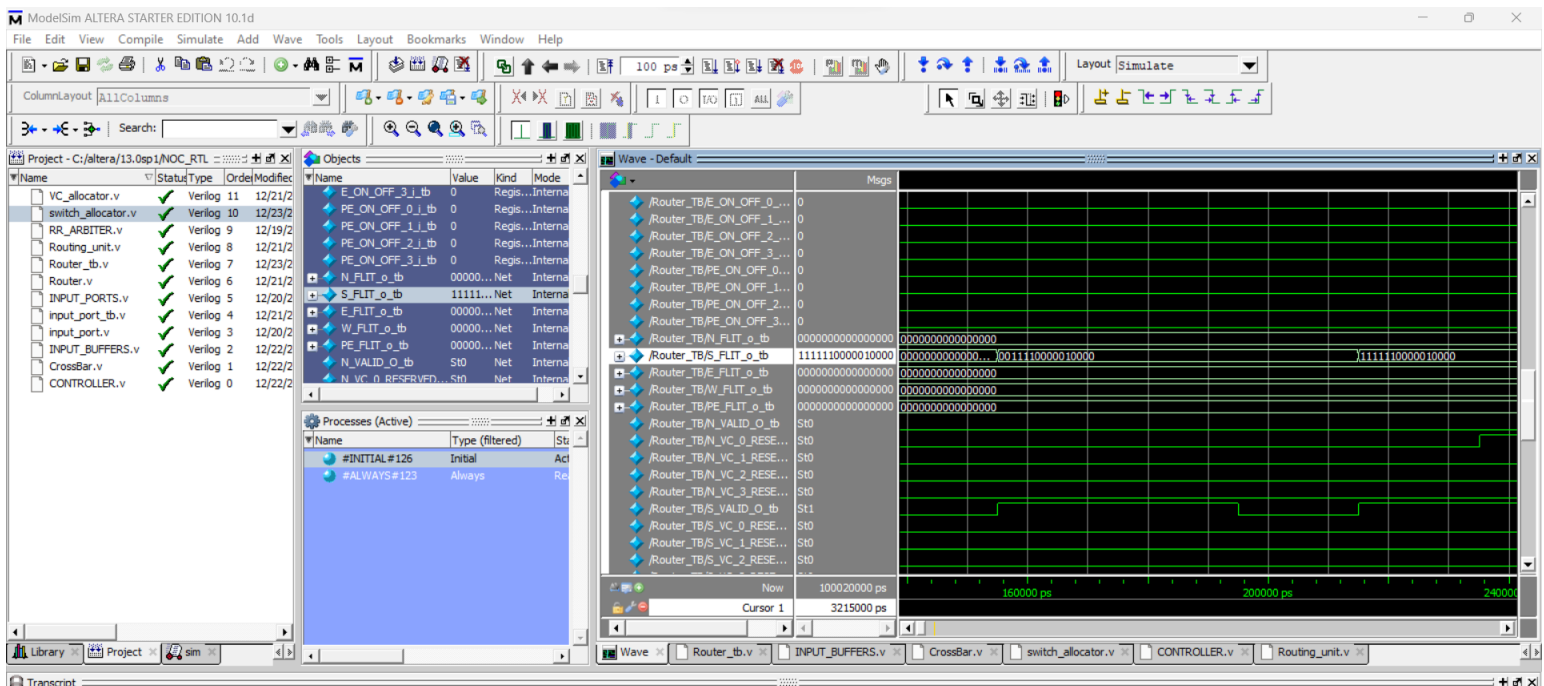
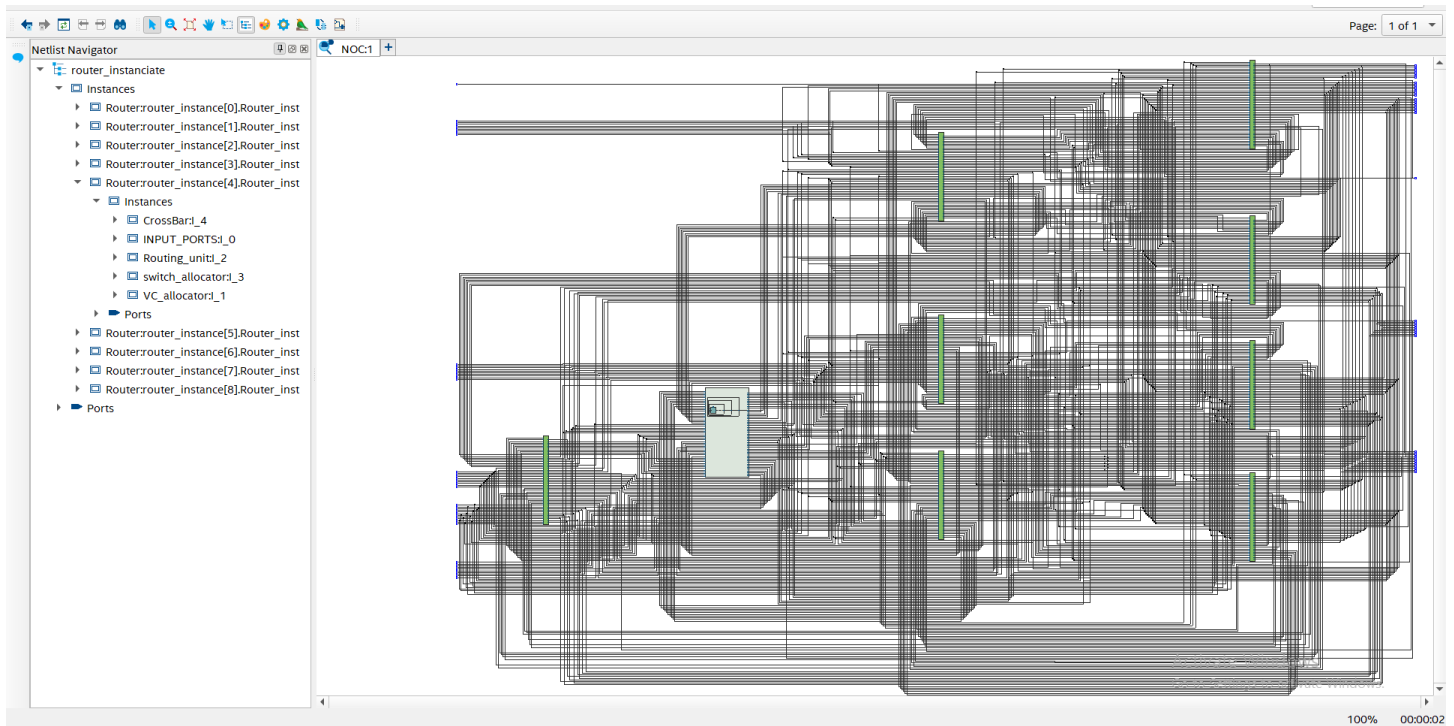


Fig. 2 different flits on 2 different input ports to same output ports

Netlist of connecting routers with each other

- We used for generate to generate 9 routers and instantiate them to the main router, then connected them to each other to generate the network.



NOC Netlist

