Signal name					200			400	ns
reset									
clk									
output	00		05				08		
nx_State							state2		
pr_state							state2		
rin_r0	05	14	03	21	70	08	70	00	
rout_r0	00		05				08		
rin_r1	05	14	03	21	70	08	70	00	
rout_r1	00				03				
rin_r2	05	14	03	21	70	08	70	00	
rout_r2	00								
rin_r3	05	14	03	21	70	08	70	00	
rout_r3	00								
pc	01	02	03	04	05		06		
rin_ir	05	14	03	21	70	08	70	00	
rout_ir	10		14		21		70		
LD0									
LD1									
LD2									
LD3									
zr0									
zr1									
zr2									
zr3									
LD_PC									
LD_IR									
inc_pc									
clr_pc									
s0					U				

Cursor 1	500 ns

1

Signal name						
			200		400	ns
⊞ s1	U					
⊞ reg_select_mux0	0	1		0		
⊞ reg_select_mux1	0		1	0		
⊞ ir_select	1		2	7		
⊞ mux0	00	05	00	03	05	08
⊞ mux1	00	05		03	08	
⊞ aluresult	00		08	0B	10	
⊞ busline	05	14	03	21	70	08	70	00
⊞ MData	05	14	03	21	70	00
bus_sel						
⊞ cmd	0		1			
⊞ data	00					
⊞ my_Rom	7F, 00, 00, 00, 00, 00, 00, 70, 21, 03, 14, 05, 10					

Cursor 1   500 ns