CS2610: Computer Organization and Architecture Lab

January-May 2023 Semester

Verilog Programming Assignment 2

Date: 13th February, 2023

Structural description method is to be used.

Design an 8-bit multiplier circuit that uses carry save addition (CSA) based 3-to-2 reducers followed by 16-bit adder using 4-bit CLAs with higher-level propagate and generate terms.

(a) Unsigned integer multiplier

(b) Signed integer multiplier

Design the logic for overflow detection.

Test cases for unsigned integer multiplier:

2 pairs of operands that do not result in overflow.

1 pair of operands that results in overflow.

Test cases for signed integer multiplier:

Following pairs of operands that do not result in overflow:

1 pair of positive operands

1 pair of positive multiplicand operand and negative multiplier operand

1 pair of negative multiplicand operand and positive multiplier operand

1 pair of negative operands

Following pairs of operands that result in overflow:

1 pair of operands of the same sign

1 pair of operands of opposite signs