CS2610: Computer Organization and Architecture Lab

January-May 2023 Semester

Verilog Programming Assignment 1

Date: 6th February, 2023

Design of 16-bit adder/subtractor for integers using the following:

1. 4-bit CLA based 16-bit adder without using higher-level propagate and generate terms
2. 4-bit CLA based 16-bit adder using higher-level propagate and generate terms

Overflow detection logic also needs to be included.

Structural description method is to be used.

Test cases for unsigned integers should include the following:

1. A pair of unsigned integer operands for addition without resulting in overflow

2. A pair of unsigned integer operands for addition resulting in overflow

3. A pair of unsigned integer operands for subtraction with a valid output

Test cases for signed integers should include the following:

1. A pair of positive integers for addition without resulting in overflow

2. A pair of positive integers for addition resulting in overflow

3. A pair of negative integers for addition without resulting in overflow

4. A pair of negative integers for addition resulting in overflow.

5. A pair of operands of opposite sign for addition. There is no overflow for this condition.

6. A pair of operands of opposite sign for subtraction without resulting in overflow

7. A pair of operands of opposite sign for subtraction resulting in overflow