



# Intel® Technology Journal

## Optical Technologies and Applications

This issue of Intel Technology Journal discusses Intel's work on optical interconnects; commercial optical transceiver products that combine leading-edge packaging and assembly technologies with advanced electronics; and collaborative research with academia focusing on bringing optical closer to and around the microprocessor.

Inside you'll find the following papers:

### Optical Technologies for Enterprise Networks

### 10 Gb/s Optical Transceivers: Fundamentals and Emerging Technologies

### Optical Interconnect System Integration for Ultra-Short- Reach Applications

### On-Chip Optical Interconnects

### Silicon Photonics

### Automated Optical Packaging Technology for 10 Gb/s Transceivers and its Application to a Low-Cost Full C-Band Tunable Transmitter

### Indium Phosphide-Based Optoelectronic Wavelength Conversion for High-Speed Optical Networks



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## Preface

By Lin Chao

Publisher, Intel Technology Journal

Optical (light-based) devices are typically used by telecom companies and long-haul fiber-optic networks for high-bandwidth communications. Optical devices direct information coded in light, or photons, the basic unit of energy associated with light. The goal for today's computing and communications networks is to deliver more data faster, so the ability to process information at the speed of light—the fastest possible speed known today at 300 million meters per second—clearly has its advantages.

Electrons flow through silicon, the common building material for today's integrated circuits. But photons can travel farther and faster. Optical devices are typically made not on silicon, but on exotic materials from the column III and column V family of elements in the periodical table, such as indium phosphide and gallium arsenide. And these III-V materials have limitations due to difficulty of manufacturing and associated higher costs.

Intel is interested in applying Intel's volume manufacturing expertise and Moore's Law to optical communications. This Intel Technology Journal (Volume 8, Issue 2) examines Intel's and collaborative academia work on optical transceivers, interconnects, and optical research.

The first paper examines the fundamentals of optical interconnect technologies, their potential to replace copper-based interconnects inside and around servers, PCs, and the devices that connect to them. The second paper details a common 10 Gb/s optical transceiver architecture, tradeoffs in designing a wavelength tunable DWDM transceiver, and technology for electronic dispersion compensation. The third paper describes the planar automated package and how it can be adapted to the practical manufacturing of tunable transmitters.

The next two papers discuss optical interconnects. Optical interconnects could be a viable solution to the predicted bandwidth limitations for copper interconnects on integrated circuits both in Ultra-Short-Reach (<10m) applications and on chip. On-chip optical interconnects can offer decreased interconnect delays and provide higher bandwidth, with lower power consumption and resistance to EMI.

The last two papers examine research underway in silicon photonics and monolithically integrated wavelength converters (WCs) made on Indium Phosphide. Silicon photonics uses silicon-based materials for the generation, guidance, control, and detection of light. The Silicon Photonics paper looks at Intel's approach to opto-electronic integration, silicon photonics, and opto-electronic integration platforms. The final paper discusses research—undertaken jointly with the University of California at Santa Barbara and Stanford University—into novel approaches for monolithically integrating Wavelength Converters (WCs) in Indium Phosphide.

These papers reveal the excitement underway as Intel and the industry research how to harness the speed of light into computers and communications that we use every day.

## Foreword

### A New Era in Optical Communications

By Mario Paniccia

Director Photonics Technology Lab, Intel Corporation

The thirst for information and the need to “always be connected” is spawning a new era of communications. This new era will drive the need for higher bandwidth technologies in order to keep pace with increasing processor performance, driven by Moore’s Law. Today, computing is often limited less by microprocessor performance than by the rate at which data can be transmitted between the processor to the outside world. As the demand for higher bandwidth continues to steadily grow, an increasing number of optical technologies are replacing copper-based interconnects to meet the needed higher bandwidth performance requirements. These optical-based technologies are not only important for the traditional long-haul telecommunications market, but are becoming increasingly more important for the connections inside and around servers, PCs and the devices that connect to them. Optical offers many advantages besides pure bandwidth; these include reduction in EMI (Electro-Magnetic Interference), reduced signal cross talk, lower weight and improved security.

Over the past decade, optical communication technologies have migrated steadily from long-haul backbones to the network edge, invading Metropolitan Area Networks (MANs) and campus-level Local Area Networks (LANs). A key inflection point will come when optical technologies are used to interconnect within and around enterprise networks and access points. One of the most important consequences of this migration has been the need to develop more efficient and lower cost optical technologies and solutions. The future of optical networks rests on the ability to bring optical communications technologies from the MAN, LAN, into the data centers, to the curb, to the home and if possible, maybe someday directly to the microprocessor. However, the cost of these optical technologies is still relatively high compared with electrical or copper-based interconnects. The transition of optical to the mass market may only happen if one can bring data-com economics, high-volume manufacturing and assembly to the optical world.

Optical systems have become, to a large extent, more strongly linked with electronics. Moore’s Law and new 90 nm fabrication technologies are enabling new electronic capabilities that add more intelligence and/or increased performance to optical systems. In addition, improved manufacturing and

packaging technologies are reducing assembly cost and producing new form factors that a few years ago were not possible. All these point to the possibility that “data-com” economical optical communication technologies may become a reality in the not-too-distant future.

In this issue of Intel Technology Journal, we discuss various optical activities within Intel, ranging from today’s commercial optical transceiver products that combine leading-edge packaging and assembly technologies with advanced electronics to some much longer range research activities focused on bringing optical closer to and around the microprocessor. These optical activities could someday revolutionize the optical communications industry and bring the benefits of optical to the mass market and most importantly to the end user.

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# Optical Technologies for Enterprise Networks

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Index words: optical interconnects, 10 Gb/s transceivers, packaging, enterprise networks

## ABSTRACT

Optical networking technologies have been over the last two decades reshaping the entire telecom infrastructure networks around the world. As network bandwidth requirements increase, optical communication and networking technologies have been moving from their telecom origin into the enterprise. For example, today in data centers, all storage area networking is based on fiber interconnects with speeds ranging from 1 Gb/s to 10 Gb/s. As the transmission bandwidth requirements increase and the costs of the emerging optical technologies become more economical, the adoption and acceptance of these optical interconnects within enterprise networks will increase. This paper, which provides the framework for the different optical interconnect technologies in this special optical issue of the *Intel Technology Journal*, is organized as follows. First, a brief overview of the fiber optics interconnects technology evolution and its current application within the enterprise, is presented. Second, various interconnect evolution paths, such as, board-to-board, chip-to-chip, and on-chip interconnects, are discussed.

## INTRODUCTION

The birth of optical communications occurred in the 1970's with two key technology breakthroughs. The first was the invention of the semiconductor laser in 1962 [1]. The laser generates a tightly focused beam of light at a single pure wavelength, a spot small enough to be connected to fiber optics. The second breakthrough happened in September 1970, when a glass fiber with an attenuation of less than 20 dB/km was developed [2, 3]. In the 1960's, glass-clad fibers had an attenuation of about 1 dB/m, which was sufficient for medical imaging applications, but was too high for telecommunications. With the development of optical fibers with an attenuation of 20 dB/km, the threshold to make fiber optics a viable technology for telecommunications was crossed. In 1977, AT&T installed the first optical fiber cables in Chicago [3]. The first field deployments of fiber

communication systems used Multimode Fibers (MMFs) with lasers operating in the 850 nm wavelength band. These systems could transmit several kilometers with optical losses in the range of 2 to 3 dB/km. A second generation of lasers operating at 1310 nm enabled transmission in the "second window" of the optical fiber where the optical loss is about 0.5 dB/km in a Single-Mode-Fiber (SMF). In the 1980's, the telecom carriers started replacing all their MMFs operating at 850 nm. Another wavelength window around 1550 nm was developed where a standard SMF has its minimum optical loss of about 0.22 dB/km. The development of fiber-based telecommunication systems in the 1990's focused on increasing their transmission capacity. This was done first by increasing the signal modulation speed from 155 Mb/s to 622 Mb/s, to 2.5 Gps, and finally to 10 Gb/s, today's modulation speed. The total available bandwidth of standard optical fibers is enormous; it is about 20 THz. Since it is impossible for a single-wavelength laser to utilize this enormous bandwidth, multiple single-wavelength laser transmitters are typically multiplexed and transmitted on a single fiber. This scheme, which was developed in the mid 1990's, is called Wavelength-Division-Multiplexing (WDM) [4]. Dense WDM (DWDM) optical communication systems with more than 60 wavelengths, where each wavelength carries 40 Gb/s data, have been demonstrated [5]. Thus, the demonstrated total transmission capacity of an SMF is more than 2.5 Tb/s.

Today, MMFs operating at 850 nm are primarily used for short distances in the enterprise as the least expensive method. An SMF at the 1310 nm wavelength band is primarily used for medium distances ranging from 2 km to 40 km. For long-haul telecommunications, WDM systems operating in the 1550 nm wavelength band windows are deployed. From 850 nm to long wavelength and WDM, higher performance is being offered, but each one comes with a higher price tag. Nowadays, all the telecom infrastructure is fiber-based with the exception of the famous last miles to homes, which is still based on coaxial cables and copper-twisted pairs. Inside enterprise

networks, fiber has been deployed since the early 1980's initially with supercomputers, and later in Local Area Networks (LANs) as well as more recently in Storage Area Networks (SANs). With continuously increasing demands for high-speed data, optical fibers and interconnects will continue to play an increasing role within the enterprise network.

In this paper, we first discuss the fundamentals of optical components for communication such as optical fibers, laser transmitters, and receivers. Second, we review the optical packaging trends for optical modules and optical transceivers. Then, after a review of the various optical interconnect topologies in the enterprise, we discuss their applications and cost trends. We then move on to discuss the next-generation optical interconnects dividing them into four main categories: box-to-box, board-to-board, chip-to-chip, and on-chip interconnects. Finally, the evolution of optical interconnects and technical challenges in enterprise networks are discussed.

## THE FUNDAMENTALS OF OPTICAL COMPONENTS

A basic optical communication link consists of three key building blocks: optical fiber, light sources, and light detectors. We discuss each one in turn.

### Optical Fibers

In 1966, Charles Kao and George Hockman predicted that purified glass loss could be reduced to below 20 dB per kilometer, and they set up a world-wide race to beat this prediction. In September 1970, Robert Maurer, Donald Keck, and Peter Schultz of Corning succeeded in developing a glass fiber with attenuation less than 20 dB/km: this was the necessary threshold to make fiber optics a viable transmission technology. The silica-based optical fiber structure consists of a cladding layer with a lower refractive index than the fiber core it surrounds. This refractive index difference causes a total internal reflection, which guides the propagating light through the fiber core. There are many types of optical fibers with different size cores and cladding. Some optical fibers are not even glass-based such as Plastic Optical Fibers (POFs), which are made for short-distance communication. For telecommunications, the fiber is glass based with two main categories: SMF and MMF. SMFs typically have a core diameter of about 9  $\mu\text{m}$  while MMFs typically have a core diameter ranging from 50 to 62.5  $\mu\text{m}$ . Optical fibers have two primary types of impairment, optical attenuation and dispersion. The fiber optical attenuation, which is mainly caused by absorption and the intrinsic Rayleigh scattering, is a wavelength-dependent

loss with optical losses as low as 0.2 dB/km around 1550 nm for conventional SMF (i.e., SMF-28\*) [6].

The optical fiber is a dispersive waveguide. The dispersion results in Inter Symbol Interference (ISI) at the receiver. There are three primary types of fiber dispersions: modal dispersion, chromatic dispersion, and polarization-mode dispersion. The fiber modal dispersion depends on both the fiber core diameter and transmitted wavelengths. For a single-mode transmission, the step-index fiber core diameter ( $D$ ) must satisfy the following condition [2]:

$$D < \left[ \frac{2.405 \cdot \lambda}{\pi} \right] \cdot (n_1^2 - n_2^2)^{-1/2}$$

where  $\lambda$  is the transmitted wavelength and  $n_1$  and  $n_2$  are the refractive indices of fiber core and cladding layer, respectively. Consequently, for a single-mode operation at 850 nm wavelength, the fiber must have a core diameter of 5  $\mu\text{m}$ . Since a conventional SMF has typically a core diameter of 9  $\mu\text{m}$ , single-mode operation can be only supported for wavelengths in the 1310 nm wavelength band or longer.

The fiber chromatic dispersion is due to the wavelength-dependent refractive index with a zero-dispersion wavelength occurring at 1310 nm in conventional SMF [6]. At 1550 nm, the fiber dispersion is about 17 ps/nm/km for SMF-28. When short duration optical pulses are launched into the fiber, they tend to broaden since different wavelengths propagate at different group velocities, due to the spectral width of the emitter. Optical transmission systems operating at rates of 10 Gb/s or higher and distances above 40 km are sensitive to this phenomenon. There are other types of SMFs such as Dispersion Shifted Fibers (DSFs) where the zero dispersion occurs at 1550 nm.

Polarization-Mode Dispersion (PMD) is caused by small amounts of asymmetry and stress in the fiber core due to the manufacturing process and environmental changes such as temperature and strains. This fiber core asymmetry and stress leads to a polarization-dependent index of refraction and propagation constant, thus limiting the transmission distance of high speed ( $\geq 10$  Gb/s) over SMF in optical communication systems. Standard SMF has a PMD value of less than 0.1 ps/ $\sqrt{\text{km}}$  [6]. Special SMFs were developed to address this issue.

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\* All other trademarks are the property of their respective owners.

Optical fiber is never bare. The fiber is coated with a thin primary coating by the fiber manufacturer; then a cable manufacturer, not necessarily the fiber manufacturer, cables the fiber. There is a wide variety of cable construction. Simplex cable has a single fiber in the center while duplex cables contain two fibers. Composite cable incorporates both single-mode and multimode fiber. Hybrid cables incorporate mixed optical fiber and copper cable. In the enterprise, the MMF is housed in a cable with an orange colored jacket, and the SMF is housed in a yellow jacket cable.

## Light Sources

The light source is often the most costly element of an optical communication system. It has the following key characteristics: (a) peak wavelength, at which the source emits most of its optical power, (b) spectral width, (c) output power, (d) threshold current, (e) light vs. current linearity, (f) and a spectral emission pattern. These characteristics are key to system performance.

There are two types of light sources in widespread use: the Laser Diode (LD) and the Light Emitting Diode (LEDs). All light emitters that convert electrical current into light are semiconductor based. They operate with the principle of the p-n semiconductor junction found in transistors. Historically, the first achievement of laser action in GaAs p-n junction was reported in 1962 by three groups [1-4]. Both LEDs and LDs use the same key materials: Gallium Aluminum Arsenide (GaAlAs) for short-wavelength devices and Indium Gallium Arsenide Phosphide (InGaAsP) for long-wavelength devices.

Semiconductor laser diode structures can be divided into the so-called edge-emitters, such as Fabry Perot (FP) and Distributed Feedback (DFB) lasers and vertical-emitters, such as Vertical Surface Emitting Lasers (VCSELs). When edge-emitters are used in optical fiber communication systems, they incorporate a rear facet photodiode to provide a means to monitor the laser output, as this output varies with temperature.

In today's optical networks, binary digital modulation is typically used, namely on (i.e., light on) and off (no light) to transmit data. These semiconductor laser devices generate output light intensity which is proportional to the current applied to them, therefore making them suitable for modulation to transmit data. Speed and linearity are therefore two important characteristics.

Modulation schemes can be divided into two main categories, namely, a direct and an external modulation. In a direct modulation scheme, modulation of the input current to the semiconductor laser directly modulates its output optical signal since the output optical power is proportional to the drive current. In an external modulation scheme, the semiconductor laser is operating

in a Continuous-Wave (CW) mode at a fixed operating point. An electrical drive signal is applied to an optical modulator, which is external to the laser. Consequently, the applied drive signal modulates the laser output light on and off without affecting the laser operation.

One important feature of the laser diode is its frequency chirp. The frequency of the output laser light changes dynamically in response to the changes in the modulation current. A typical DFB has a frequency chirp of about 100-MHz/mA. This spread of the wavelength interacts with the fiber dispersion. As previously mentioned, as the data rate is increased, this interaction limits the transmission distance of optical transmission systems due to the additional ISI generated at the receiver [1-4].

Optical back-reflection is one of key issues when coupling the output light from a laser source to a fiber. The optical back-reflection disturbs the standing wave in the laser cavity, increasing its noise floor, and thus making the laser unstable. One practical way to reduce the phenomenon of back-reflection is to place an isolator between the laser cavity and the fiber, which adds a significant additional cost to the laser [1, 4]. Temperature also affects the peak wavelength of the laser; threshold current also increases with temperature as slope efficiency decreases. For DWDM applications, which require very precise operating wavelengths, most of the current laser diode designs need to be cooled to within  $\pm 0.3$  °C.

As previously explained, the direct modulation of a laser diode has several limitations, including limited propagation distance due to the interaction between the laser frequency chirp and fiber dispersion. This is not an issue for enterprise networks which are short distance, but could be a serious limiting factor for telecommunications applications. To overcome this limitation, the laser diode is operated in a CW mode, and output light is externally modulated by an optical modulator. Intensity modulators can be divided into two main groups: Mach-Zehnder Interferometer (MZI) and Electro-Absorption (EA) modulators. In an MZI modulator, a single input waveguide is split into two optical waveguides by a 3 dB Y junction and then recombined by a second 3 dB Y junction into a single output. A Radio Frequency (RF) signal, which is applied to a pair of electrodes constructed along the waveguides, modulates the propagating optical beam. The modulator key parameters are its modulation bandwidth, linearity, and the required drive signal voltage for  $\pi$  phase shift. MZI modulators based on LiNbO<sub>3</sub> are high-performance modulators with a large form-factor (about 2.5 inches) that are not suitable for optical integration [4, 7]. EA modulators are based on a voltage-induced shift of the semiconductor bandgap so that the modulator becomes absorbing for the lasing wavelength. The advantages of an EA modulator is its low driving

voltage, high-speed operation, and suitability for optical integration with InP-based laser diodes [8].

A tunable laser is a new type of laser where its main lasing longitudinal mode can be tuned over a wide range of wavelengths such as the C band (1510–1540 nm) of an Erbium-Doped Fiber Amplifier (EDFA), which is commonly used for DWDM systems [1–4]. The use of tunable lasers is driven by the potential cost savings in DWDM transport networks since a significantly reduced inventory of fixed-wavelength lasers could be maintained for a robust network operation. The technical challenges are to provide both broad wavelength tunability and excellent wavelength accuracy over the laser life. A broadly tunable External Cavity Laser (ECL) employing micromachined, thermally tuned silicon etalons has been designed to achieve these goals.

## Light Detectors

Light detectors convert an optical signal to an electrical signal. The most common light detector is a photodiode. It operates on the principle of the p-n junction. There are two main categories of photodetectors: a p-i-n (positive, intrinsic, negative) photodiode and an Avalanche Photodiode (APD), which are typically made of InGaAs or germanium. The key parameters for photodiodes are (a) capacitance, (b) response time, (c) linearity, (d) noise, and (e) responsivity. The theoretical responsivity is 1.05 A/W at a wavelength of 1310 nm. Commercial photodiodes have responsivity around 0.8 to 0.9 A/W at the same wavelength [1–4]. The dark photo-current is a small current that flows through the photo-detector even though no light is present because of the intrinsic resistance of the photo-detector and the applied reverse voltage. It is temperature sensitive and contributes to noise. Since the output electrical current of a photodiode is typically in the range of  $\mu$ A, a Transimpedance Amplifier (TIA) is needed to amplify the electric current to a few mA [2–4].

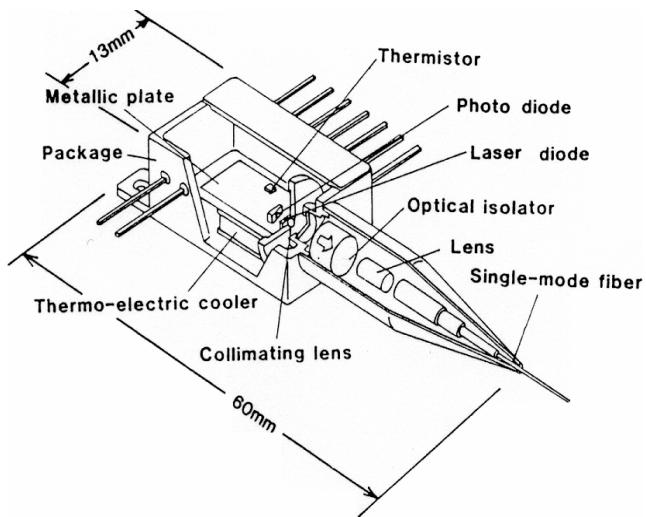
APDs provide much more gain than the pin photodiodes, but they are much more expensive and require a high voltage power to supply their operation [2]. APDs are also more temperature sensitive than pin photodiodes.

## PACKAGING: PACKAGING: OPTICAL SUB-ASSEMBLY (OSA) AND OPTICAL TRANSCEIVERS

As previously described, laser diodes and photodiodes are semiconductor devices. To enable the reliable operation of these devices, an optical package is required. In general, there are many discrete optical and electronic components, which are based on different technologies that must be optically aligned and integrated within the optical package. Optical packaging of laser diodes and

photodiodes is the primary cost driver. These packages are sometimes called Optical Sub-Assemblies (OSAs). The Transmitter OSA package is called a TOSA and the Receiver OSA package is called a ROSA.

Figure 1 shows, for example, a three-dimensional schematic view of a DFB laser diode mounted on a Thermo-Electric Cooler (TEC) inside a hermetically sealed 14-pin butterfly package with an SMF pigtail [9]. Most of the telecom-grade laser diodes are available in the so-called TO can or butterfly packages. The standard butterfly package is a stable and high-performance package, but it has a relatively large form-factor and it is costly to manufacture. These packages are typically used for applications where cooling is required using a TEC [4].



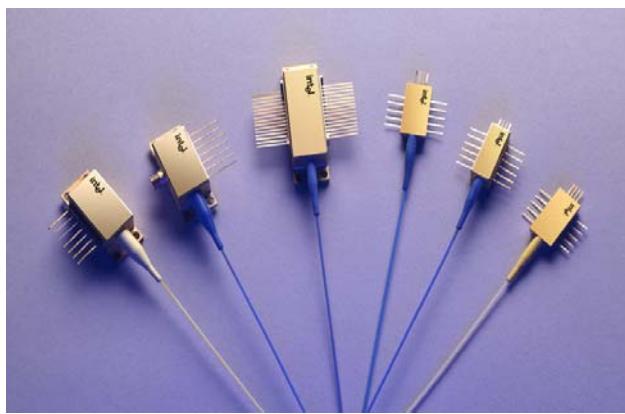
**Figure 1: Three-dimensional view of a DFB laser diode configuration with single-mode fiber pigtail  
(after Ref. [8] (© 1990 IEEE))**

The TEC requires a large amount of power to regulate the temperature of a laser inside the package. This type of optical packaging was used for the early 10 Gb/s modules. More recently, tunable 10 Gb/s lasers are using a similar butterfly optical package. The butterfly package design uses a coaxial interface for passing broadband data into the package, which requires the use of a coaxial interface to the host Printed Circuit Board (PCB). Although coaxial cables and connectors have been reduced in size, they still consume valuable real estate in the optical transceiver.

The evolution of optical module packages is toward smaller footprint packages. If relatively easy for receivers, the trend toward smaller packages is particularly challenging for laser transmitter modules due to the power and thermal dissipation constraints. Figure 2 shows the evolution of 10 Gb/s optical module packaging

technology. To operate with high-performance, uncooled designs must be implemented with more advanced control systems that can adjust the laser and driver parameters over temperature. The smaller packages utilize a coplanar approach to the broadband interface, which more closely resembles a surface-mount component and enables much smaller RF interfaces.

TO-can-based designs, which have been used extensively in lower data rate telecom and datacom systems up to 2 Gb/s as well as CD players and other high-volume consumer applications, are now maturing to support high-performance 10 Gb/s optical links. Leveraging the fact that these packages are already produced in high volume will further reduce the cost of the 10 Gb/s optical modules in optical transceiver designs.



**Figure 2: Trends in 10 Gb/s optical transmitter packaging technology. To decrease size and power dissipation, the trends are from cooled to uncooled packages, from coaxial to planar RF interfaces, and from pigtailed to pluggable optical interfaces.**

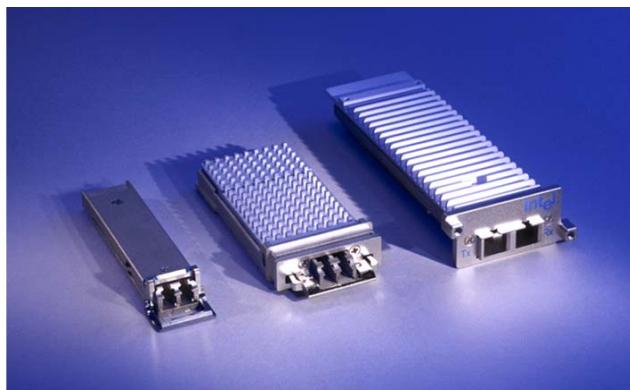
The current TOSA/ROSA package form factors are trending toward smaller packages, and it will not end at the 10 Gb/s TO-can implementation. These TOSA/ROSA form factors are still too large and too expensive to compete in the market segment where today copper interconnects dominate. Leadframe-type packages could be an attractive choice for high-speed optical modules since similar packages are already in use in the semiconductor industry [10]. Using insert molded or pre-molded thermoplastic housing, different optical components can be passively aligned in a fully automated manufacturing process. For example, integrated modules with VCSEL and photodiodes in leadframe packages have been developed for the automobile industry, but are limited today in the 20 Mb/s bit rate. Additional research and development is needed to define the packaging specifications for optoelectronic modules based on size and cost.

## Optical Transceivers

For telecommunication applications, the optical transmitter and receiver modules are usually packaged into a single package called an optical transceiver. Figure 3 shows an example of different transceivers and Figure 4 shows an example of the printed circuit board of a transceiver. There are several form factors for this optical transceiver depending on their operating speed and applications. The industry worked on a Multi-Source Agreement (MSA) document to define the properties of the optical transceivers in terms of their mechanical, optical, and electrical specifications. Optical transponders operating at 10 Gb/s, based on MSA, have been in the market since circa 2000, beginning with the 300-pin MSA, followed by XENPAK, XPAK, X2, and XFP. Table 1 summarizes the key MSA specifications for the different form-factor 10 Gb/s optical transceivers and their release dates.

### Which are the Most Popular Form-Factor Transceivers in the Enterprise?

For the 1/2/4 Gb/s transceivers, the Small Form-Factors (SFFs) and the small Form-Factor Pluggables (SFPs) are the most recently developed and the ones that are finding new sockets into systems. It should be noted, however, that the older GBIC form factors for 1 Gb/s Ethernet (GbE), despite no new development, is still shipping in large volumes due to the large installed base of this design. The SFF transceiver is used in a Network Interface Card (NIC) for the LAN or in the Host Bus Adaptor (HBA) in SANs. The SFP transceiver is typically used for enterprise switches such as Ethernet or Fiber-Channel (FC) switches. In these high-capacity switches, switching is done by electrical ICs while the optical transceivers provide optical-to-electrical (O-E) or electrical-to-optical (E-O) conversion.



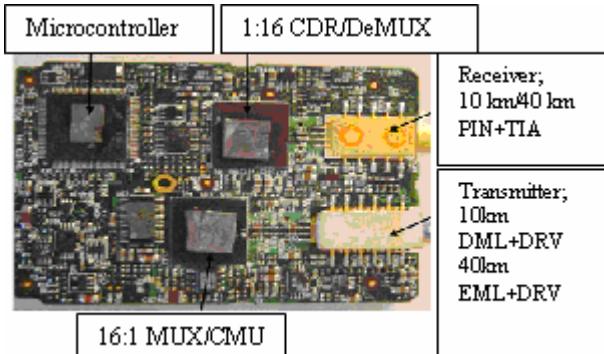
**Figure 3: Next-generation 10 Gb/s enterprise optical transceivers: (from left) XFP, XPAK/X2, XENPAK. These modules are electrically hot-pluggable and optically pluggable.**

In general, not all the switches' ports are populated with transceivers when they are shipped to customers. The customer has the option to buy these transceiver modules as the demand for ports increases. It also gives the customer the choice of optics: MMF or SMF. Therefore, these modules have been designed to be pluggable.

The choice between the different 10 Gb/s form-factor optical transceiver packages is guided by reach, cost, and thermal and size constraints and requirements.

**Table 1: Summary of different form-factor 10 Gb/s optical transceiver packages**

MSA	XENPAK	XPAK/X2	XFP
MSA Date	March 2002	March 2003	April 2003
Application	Enterprise switch	Enterprise switch NIC Storage	Telecom Datacom
Electrical Interface	4 bit XAUI	4 bit XAUI	1 bit XFI
Optical interface	SC pluggable	SC or LC pluggable	LC pluggable
Dimension	4.8x1.4x0.7	2.7x1.4x0.4	
Max Power	11W	5W	3W



**Figure 4: Intel® TXN13220 FR-4 printed circuit board showing optical modules, Mux/DeMux, and microprocessor**

## OPTICAL TECHNOLOGY TRENDS IN THE ENTERPRISE

Enterprise network topology can be divided into four main categories: horizontal cabling, vertical cabling, data center interconnects, and campus backbone. Table 2 shows the use of various technologies in each of these topologies based on distance and speed. Within a data center, the LAN, which is based on the Ethernet protocol, is based mostly on copper interconnects operating at speeds of up to 1 Gb/s for all distances below 100 m. Some MMFs at 850 nm are also used at speeds of up to 10 Gb/s. However, within a SAN, which is based on the Fiber Channel (FC) protocol, only MMFs at 850 nm are used for transmission rates ranging from 1 Gb/s to 10 Gb/s. Optical interconnects based on SMFs at 1310 nm are typically used within a campus-size network with transmission distances up to 10 km and rates of up to 10 Gb/s. All the optical interconnects used in enterprise networks today are box-to-box connections typically between a server to a switch connection and a switch to a switch connection. The most popular optical modules are SSF and SFP form-factor modules operating at speeds of up to 4 Gb/s, while the 1 Gb/s GBIC for LAN is still shipping in volume. For the 10 Gb/s modules, the XENPAK is the most commonly used today within enterprise networks. However, the new optical module designs are trending towards smaller form-factor modules such as XPAK and XFP.

**Table 2: Used technology in each of the enterprise network topologies**

Segment	Distance	Speed	Technology
Horizontal	100 m	10/100/1000 Mb/s	Copper
Vertical	300 m	10/100 Mb/s 1/10 Gb/s	Copper MMF
Data center	100 m	10/100Mb/s 1Gb/s-10Gb/s LAN 1/2/4 Gb/s SAN	Copper Copper/MMF MMF
Campus	2-10 km	1- 10 Gb/s	SMF

In today's enterprise networks, copper-based interconnects dominate the box-to-box connections due to their cost advantage over comparable optical interconnects. For example, in the 1 Gb/s LAN (i.e., Ethernet-based) market, Dell'Oro in January 2004 was forecasting the shipment volume to grow from about a total of 13 million switch ports in 2003 to 158 million ports in 2008 [11]. Out of the total number of switch

ports, the number of 1 Gb/s copper-based interconnects is expected to grow from about 7 million in 2003 to about 141 million in 2008. This anticipated growth of copper-based interconnects is driven by the deployment of 1 Gb/s to the desktop. The average selling price of copper-based switch ports is \$181 in 2003. For the lowest cost segment of the copper-based 1 Gb/s switch port market, the average selling price is forecasted to decline from about \$59 to \$9 over the same period. In comparison, out of the total number of switch ports, the 1 Gb/s optical interconnects market is expected to grow from about 6 million ports in 2003 to 17 million ports in 2008 with the average selling price about \$416 in 2003 [11]. The market for the SAN, which is based on the FC protocol standard, is planned to transition from optical interconnects operating at 2 Gb/s to 4 Gb/s during the 2005-2006 period. The forecasted volume for the FC-based switch ports is expected to grow from 1.8 million of 2 Gb/s ports in 2003 to 6.4 million of 4 Gb/s ports in 2007, according to the IDC forecast published in August 2003 [12]. Over the past year, the average selling price of optical 10 GbE switch ports has been dropping from about \$30K to about \$10K per port today. The average selling price of these 10 GbE switch ports must be below \$3K per port for a wide deployment within enterprise networks.

## NEXT-GENERATION OPTICAL INTERCONNECTS

In general, interconnects can be divided into four main categories: box-to-box, board-to-board, chip-to-chip, and on-chip interconnects. Today, optical interconnections in the enterprise are mostly used for the box-to-box interconnects. The optical transceivers are either plugged into high-capacity Ethernet or FC-based switches, or placed on a NIC/HBA, which are implemented into servers. Will optical interconnects move into the other categories? A brief overview of each optical interconnect category is provided in the next subsections.

### Board-to-Board Interconnects

The move of the communications industry, both telecom and datacom toward a Modular Communication Platform (MCP) favors the deployment of bladed architecture. Functions that were traditionally housed in a standalone box, such as between servers and switches, have started to be implemented into a board-level form-factor, which is called a blade, and they plug into a common chassis. Therefore, interconnect opportunities at the board level are becoming more important. As the transmission speed increases, copper-based interconnects are facing technical challenges in terms of speed, reach, EMI, and routing.

Backplanes are potential applications for optical interconnects. These are point-to-point or point-to-

multipoint high-speed interconnects with typical lengths of under 1m. The key advantages of optical backplane interconnects are low-crosstalk among the optical signals, and their large bandwidth. However, most of today's optical backplanes are more like patch panels rather than replacements for backplanes. Many different optical technologies have been demonstrated including polymer waveguides integrated on Si, planar light wave circuit interconnects, and fiber ribbon arrays integrated with VCSELs and photodiodes. However, none of these optical technologies today have displaced copper interconnects outside of some niche applications. The transition to optical backplanes might be induced by the accumulating technical challenges of electrical interconnects. However to be widely adopted, optical interconnects must be able to advance toward a smaller form-factor with a lower power consumption at a lower cost. Meeting these requirements is critical to the technology evolution of optical interconnects from box-to-box to board-to-board to chip-to-chip. Several new technical breakthroughs will need to occur in order to meet these challenging requirements.

### Chip-to-Chip Interconnects

Extrapolation of Moore's law shows that microprocessors are expected to be clocked at about 10 GHz by the end of the decade [13, 14]. Consequently, it is becoming extremely difficult to route enough bandwidth through a PCB or a module using the existing electrical wires. It has been shown that frequency-dependent loss for copper traces on FR4 circuit boards rapidly rises above 1 GHz, reducing the Signal-to-Noise Ratio (SNR) and introducing timing errors. In addition, the resultant high-frequency crosstalk among the different copper traces limits the wiring density on the circuit board. High-speed short-distance ( $L < 10$  cm) chip-to-chip optical interconnects have several advantages over copper interconnects. Optical interconnects are low-loss interconnects with a large transmission bandwidth. Another key advantage is their inherent immunity to Electro-Magnetic Interference (EMI). The density of copper traces on FR4 boards is constrained by these EMI and electrical crosstalk problems. Over the last 20 years, many different optical technologies were demonstrated to overcome the electrical bottleneck [14, 15]. However, their relative high costs due to implementation complexity and use of exotic materials made them unsuitable for high-volume manufacturing and thus prevented the adoption of these technologies.

### On-Chip Interconnects

The design of on-chip electrical interconnects is becoming increasingly difficult given the continuous growth in the complexity of integrated circuits operating

at multi-GHz. Can on-chip optical interconnects potentially solve these issues? On-chip point-to-point and point-to-multipoint optical interconnects with typical lengths under 1 cm are potentially attractive because of the following reasons: (a) they decrease the existing electrical interconnect delays, (b) provide a higher bandwidth to keep pace with the speed of transistors, (c) reduce electrical power consumption, and (d) minimize sensitivity to EMI. The potential primary application of on-chip optical interconnects in microprocessors, for example, are in high-speed signaling and clock distribution. For on-chip signal distribution, four key benchmark parameters are typically used: signal delay normalized by clock cycle, available bandwidth per unit area or bandwidth density, bandwidth density/delay ratio, and cost. For on-chip clock distribution, the critical parameters are timing, skew, and jitter. The primary challenges for implementing these optical interconnects is the integration of multiple VCSEL and photodiode arrays with their corresponding drivers and TIAs, and on-chip light coupling into optical waveguide arrays over the entire chip. Currently, such optoelectronic integration is not only in its early stages of development, but it is also very expensive relative to copper-based interconnects with limited or no performance advantages. In order to take advantage of on-chip optical interconnects, today's microprocessor architecture might need to evolve from a single superscalar chip to a mesh of optically interconnected processors with their associated memories. The WDM scheme could be used, for example, to send multiple wavelengths in the same optical waveguide to significantly increase the overall communication bandwidth.

### Silicon-Based Optical Interconnects

In order to enable the chip-to-chip or on-chip optical interconnects, silicon-based optical components should be developed. As previously noted, optical components such as tunable WDM filters, photodiodes, optical waveguides, and electronic components such as laser drivers and TIA circuits are all based on different materials and technologies precluding them from an optoelectronic monolithic integration. The attractiveness of silicon-based optical interconnects is the potential integration with CMOS integrated circuits for high-volume manufacturing. The first prototype of such silicon-based optical components includes thermally tunable WDM Bragg filters, high-speed optical MZI modulators and a Si/Ge high-speed photodiode [16].

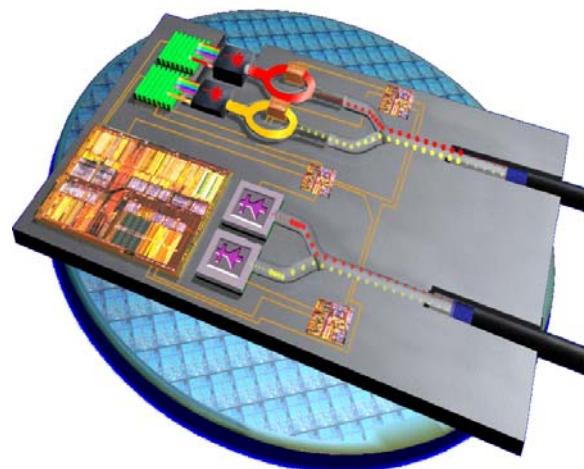
A narrow-band Bragg grating filter has been made in silicon waveguides with alternating polycrystalline/crystalline layers. The Bragg grating reflects only the wavelengths that satisfies the Bragg condition [1–4]

$$\lambda_B = 2n \cdot \Lambda / m$$

where  $n = 3.46$  in the effective refractive index of the silicon waveguide,  $\Lambda = 2.445 \mu\text{m}$  is the Bragg grating pitch, and  $m = 11$  is the Bragg grating order. Using the strong thermo-optics effect in silicon, these Bragg grating filters can be made tunable [17]. Such WDM Bragg grating filters with a 3-dB bandwidth of 100 GHz and 200 GHz, insertion loss of about 4 dB and tunability over 12 nm for 100 °C temperature variation were demonstrated. These tunable Bragg filters can be used as channel filters in a low-cost WDM communication system.

Silicon-on-Insulator (SOI) optical modulators based on current injection had a modulation bandwidth of only 20 MHz. Consequently, these devices were not suitable for today's high-speed communication networks.

Recently, an MZI silicon optical modulator with a modulation bandwidth of 2.5 GHz around 1550 nm was demonstrated [18]. The high-speed operation was achieved by using a novel phase shifter design based on a Metal-Oxide-Semiconductor (MOS) capacitor embedded in a passive silicon waveguide with doped and undoped polysilicon regions in MZI configuration. The accumulated charges in the MOS capacitor induce fast refractive index changes in the silicon waveguide due to the free carrier plasma dispersion effect [19]. The 1.5 cm long silicon MZI modulator had an extinction ratio of more than 16 dB with an applied peak-to-peak voltage of about 7.7 volts.



**Figure 5: Future vision of hybrid optical integration of a four-channel WDM optical transceiver with silicon photonic components and conventional CMOS drivers**

However, the demonstrated modulator had a total of 12 dB insertion loss, which can potentially be reduced to about 4–5 dB if the polysilicon is replaced with a single-crystal silicon and tapered waveguides are used to efficiently couple the light in and out of the modulator through a diabatic transformation of the optical mode. The development of tapered waveguide technology for this high-index contrast optical system is one of the key challenges to developing a hybrid integration of these devices.

Such SOI-based modulators and Bragg filters can lead to an integrated optical transceiver module on a single die, combining multiple wavelength sources, modulators, and WDM multiplexer/de-multiplexers with the corresponding drive electronics. This concept is illustrated through an artist vision in Figure 5 which shows a hybrid integration of a four-channel WDM optical transceiver with silicon photonic components such as modulators, filters, and multiplexer/de-multiplexers and conventional CMOS-based drivers on the same silicon die.

## TECHNICAL CHALLENGES AND CONCLUSION

The costs of high-speed optical interconnects has been reduced by more than an order of magnitude while their performance has been significantly improved over the last five years. Tremendous progress has been made in the development of cost-effective packaging technologies for optical modules operating at transmission rates up to 10 Gb/s. Four different MSA form-factor packages for 10 Gb/s optical transceivers in enterprise networks, namely, XENPAK, XPAK, X2, and XFP have been created, trending toward smaller form factors. In the meantime, the SFF and SFP, which are the smallest form-factor modules on the market, are trending to higher speed capabilities from 1/2 Gb/s today toward 4 Gb/s. In today's enterprise networks, the optical transceivers are used for box-to-box connections. The optical transceivers are either plugged into high-capacity Ethernet or FC-based switches, or placed on a NIC/HBA, which are plugged into servers. In terms of volume shipped, copper-based interconnects dominate the box-to-box connections due to their cost advantage over comparable optical interconnects until at least 2008. However, the number of either Ethernet-based or FC-based server-to-switch and switch-to-switch optical interconnects is expected to grow in the coming years.

To be widely adopted, optical interconnects must be able to advance toward a smaller form-factor with a lower power consumption at a lower cost. Meeting these requirements is critical to the technology evolution of optical interconnects from box-to-box to board-to-board,

to chip-to-chip. Several new technology breakthroughs will need to occur in order to meet these challenging requirements.

## ACKNOWLEDGMENTS

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# 10 Gb/s Optical Transceivers: Fundamentals and Emerging Technologies

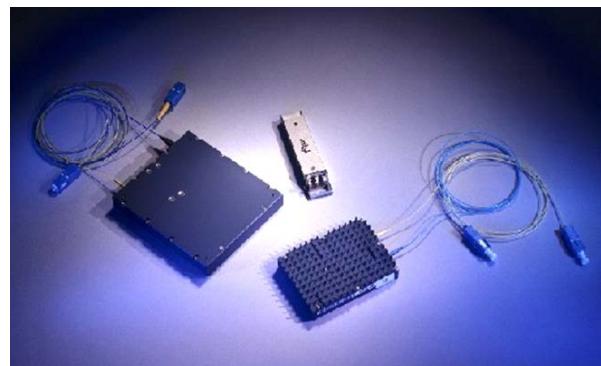
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Index words: fiber optics, optical transceiver, 10 Gb/s, Dense Wavelength Division Multiplexing (DWDM), tunable laser, Electronic Dispersion Compensation (EDC)

## ABSTRACT

Continued demand for higher bandwidth in data networks along with an industry need for standardized network components has driven the need for 10 Gb/s optical transceivers into the long haul, metro core, and enterprise/storage environments. In response to this demand, the functionality and performance of these modules have increased significantly, while the size, cost, and power consumption have been dramatically reduced. While each transceiver application has unique system-level requirements, performance criteria, and cost sensitivities, the structure of each transceiver is much the same. This paper presents a discussion of the basic transceiver architecture including analog and digital electronic ICs and process choices, optical components and packaging, and control, monitoring, and interface circuitry. With each component, the critical performance criteria and cost-reduction opportunities are highlighted. More detail is presented on a full C-band wavelength tunable long-haul optical transceiver for Dense Wavelength Division Multiplexed (DWDM) systems, including the DWDM system requirements and design issues that arise in amplified, high-power, multi-channel links. The functionality and performance of a tunable 10 Gb/s transceiver are explored in more depth with a focus on transmitter and receiver front-end design. Finally, an application of Electronic Dispersion Compensation

(EDC) is presented, and we show how it can be used to compensate for fiber limitations to enable extended 10 Gb/s links over modal bandwidth limited legacy multimode fiber in enterprise systems.



**Figure 1: 10 Gb/s optical transceivers for DWDM line side and metro client-side interfaces. Pictured from the left are the 300-pin, XFP, and small form factor 300-pin MSA modules.**

## INTRODUCTION

Optical transceivers operating at line rates of 10 Gb/s have matured rapidly over the last few years and are currently available in a wide variety of form factors, each addressing a range of link parameters and protocols. These form factors are the result of Multi-Source

Agreements (MSAs) that define common mechanical dimensions and electrical interfaces. The first MSA was the 300-pin MSA in 2000, followed by XENPAK, X2/XPAK, and XFP. Each of the transceivers defined by the MSAs have unique advantages that fit the needs of various systems, supporting different protocols, fiber reaches, and power dissipation levels. Figures 1 and 2 show 10 Gb/s transceivers for client-side telecom and enterprise interfaces, respectively. As the underlying technologies have matured, the optical and electrical performance of these modules has been significantly improved, while the power dissipation and cost have been reduced dramatically.



**Figure 2: 10 Gb/s optical transceivers for enterprise interfaces. Pictured from the left are the XFP, X2/XPAK, and XENPAK MSAs.**

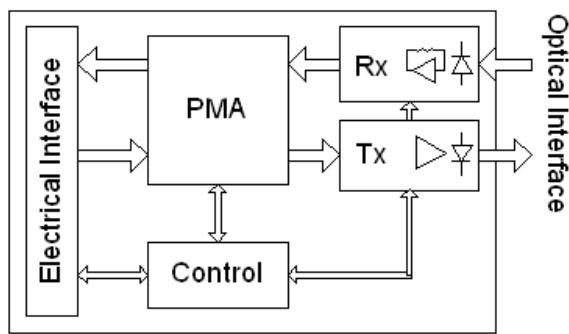
In the architecture section of this paper, the basic architecture of all 10 Gb/s transceivers is presented, highlighting the functionality and critical performance parameters of each functional block. Design considerations such as IC process and optical packaging technologies are also discussed.

In the DWDM section, details on the design challenges and performance of a 10 Gb/s full C-band wavelength tunable optical transceiver are presented. Issues that arise in amplified, high-power, multi-channel links are discussed in terms of design choices and performance criteria.

Finally, the fundamentals of Electronic Dispersion Compensation (EDC) are presented, which uses adaptive electrical filtering techniques to compensate for limitations incurred during fiber propagation. The application of EDC to the problem of extending 10 Gb/s links using 1310 nm directly modulated lasers over low-bandwidth Multi-Mode Fiber (MMF) is explored in more detail.

## 10 GB/S TRANSCEIVER ARCHITECTURE

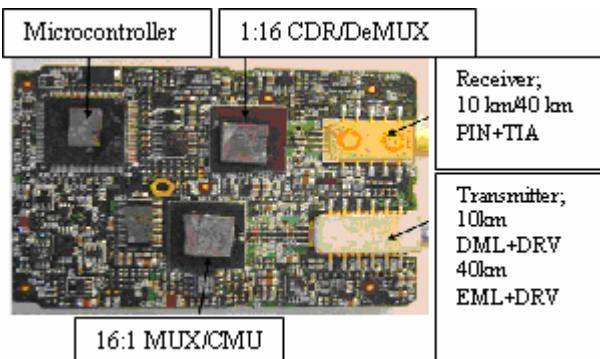
The basic architecture and interconnection between components in a 10 Gb/s optical transceiver are shown in Figure 3. This basic architecture holds for all of the 10 Gb/s transceiver Multi-Source Agreements (MSAs), independent of form factor, electrical interface, or fiber reach. Figure 4 shows the actual printed circuit board from a small form factor 300-pin MSA transceiver.



**Figure 3: 10 Gb/s optical transceiver architecture showing functional components and interconnection**

### Electrical Interface

The electrical interface provides input/output data transfer to the host card, various clocking channels, control and monitoring channels, as well as DC power and ground connections. This interface can take the form of a socket that plugs perpendicularly into the plane of the host board, as in the 300-pin MSA [1], or it can take the form of a board-edge connection that mates to a socket in the plane of the host board. The latter is the case for XENPAK [2], X2/XPAK [3,4], and XFP [5], which provide front-panel pluggability at the host system level. Along with this benefit comes the added requirement of hot-pluggability and inrush current management.



**Figure 4: Small form factor 300-pin optical transceiver PCB showing optical modules with integrated driver/TIA, PMA (1:16 Mux/DeMux), and microcontroller**

The width of the data bus varies between the different MSAs. The first to emerge was the XSBI (based on SFI-4) interface of the 300-pin MSA, with 16-bit differential buses for input and output data [6]. Each I/O channel transmits or receives data at 1/16 the line rate (e.g., 622.080 Mb/s with a SONET line rate of 9.953 Gb/s). The XAUI interface on XENPAK and X2/XPAK provides a 4-bit differential bus. In this interface, each channel operates at 3.125 Gb/s, for a total bandwidth of 12.5 Gb/s. Multiple encoding/decoding steps on the XAUI signals result in the Ethernet line rate of 10.3125 Gb/s, which we discuss further in the Physical Medium Attachment (PMA) section. Finally, for XFP, the XFI interface provides a 1-bit differential signal at the line rate, providing a truly protocol-independent interface for 10 Gb/s communication.

Clocking schemes vary between the different interfaces. The clocking used in SFI-4 systems can vary, but generally a synchronous clock (1/16 or 1/64 of the line rate) is provided with the input data, and a reference clock is provided to keep the receiver Clock and Data Recovery (CDR) within locking range of the input data rate. The clock recovered by the receiver CDR is provided along with the output data. In XAUI and XFP transceivers, the host board simply provides a reference clock to keep the CDRs in the module within locking range of the data rate.

The electrical interface also provides DC connections to the host board DC power supplies. Care must be taken to minimize power dissipation given the different voltage and current levels available in various system designs.

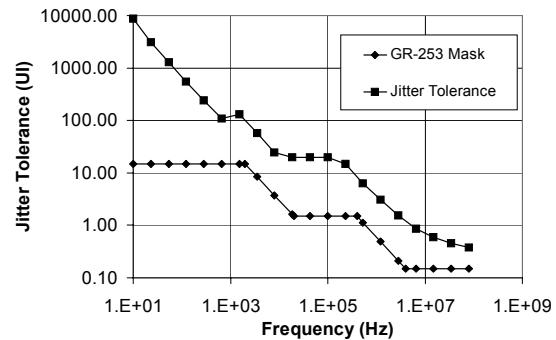
## Control System

The control systems in modern 10 Gb/s transceivers are generally implemented using a microcontroller. This device performs many functions that previously had been implemented using analog hardware. The controller sets control parameters for the Physical Medium Attachment (PMA), transmitter, and receiver, which may vary over time and temperature or when the host system changes the link configuration (i.e., loopback modes). The controller also provides a two-wire interface such as I<sup>2</sup>C so the host board can set control parameters and read the status registers where monitor values are stored.

## Physical Medium Attachment

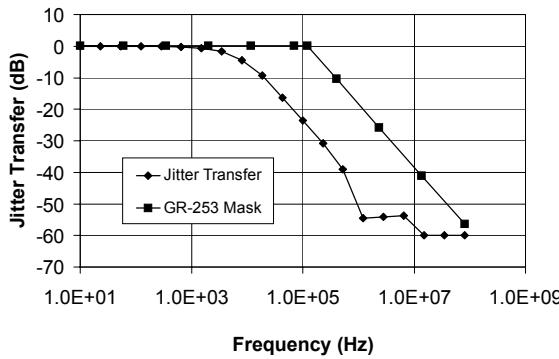
The core electrical functionality of a 10 Gb/s transceiver is contained in the PMA device. Transceivers at lower data rates generally do not include this functionality, because maintaining robust signal integrity is not as difficult at lower speeds. PMA devices take the form of clock multiplier/multiplexer (MUX/CMU) and clock and data recovery/demultiplexer (CDR/DeMUX) in the 300-pin modules. The MUX/CMU interleaves the 16-channel

data bus into a serialized data stream at the line rate, clocked by a multiplied version of the input clock. This data stream is used to modulate the optical transmitter. The CDR/DeMUX provides the complementary functionality on the receive side. For the two types of PMA, there are a wide range of features and performance parameters that are critical to system-level quality. Here, we focus on the basic functionality and jitter characteristics. The PMA output waveform quality has a large impact on optical transmit eye quality, and PMA sensitivity has a large impact on optical receive sensitivity. The system-level impacts of these characteristics are covered in the optical device section below.



**Figure 5: Jitter tolerance performance of a typical 300-pin small form factor 40 km transceiver. Note the stepped mask indicating the specification limit.**

In SONET systems [7], jitter performance is critical to maintaining error-free performance over links involving several network elements [8]. There are three jitter parameters of interest in these systems: transmitter jitter generation, receiver jitter tolerance, and receive-to-transmit jitter transfer. For all SONET network elements, the jitter generation must have significant margin on the specification limit of 100 mUIpp (UI denotes a unit interval, or one bit period), ideally 50 mUIpp. For a receiver, robust jitter tolerance is critical to performance of the network. This is the amount of sinusoidal jitter that causes a 1 dB penalty in the sensitivity of the receiver. Figure 5 shows the worst-case jitter tolerance performance of the 300-pin small form factor transceiver along with the specification mask. When a transceiver is used as a simple repeater, the jitter transfer characteristic is also important to network reliability. This is the amount of jitter transmitted at a specific frequency given a specified level of jitter into the transceiver. The worst-case jitter transfer performance of a 300-pin small form factor transceiver is shown in Figure 6. The peaking is less than 0.1 dB at low frequencies, and at higher frequencies the transfer rolls off to stay below the specification limit.



**Figure 6: Jitter transfer performance of a typical 300-pin small form factor 40 km transceiver. The specification limit is indicated on the plot.**

Although Ethernet standards do not specifically define jitter parameters, the jitter generation and tolerance of these devices are still critical in Ethernet systems [9]. Jitter generation has an impact on the Transmitter and Dispersion Penalty (TDP), where the transmission performance over a fiber link of a device under test is compared with a reference transmitter. Any degradations due to waveform imperfections or jitter generation add to this penalty. Jitter tolerance has an impact in the Stressed Receive Sensitivity (SRS) test, where receiver sensitivity is measured with an eye that contains stress from sinusoidal jitter, as well as filtering and vertical sinusoidal closure. The TDP and SRS performance of a 40 km XENPAK transceiver is shown in Table 1. As 300-pin modules are often used in Ethernet systems, the TDP and SRS performance of the 40 km 300-pin small form factor module is shown for comparison.

**Table 1: 10 Gb/s Ethernet 40 km (10GBASE-L) optical transceiver performance**

SPECIFICATION	300-PIN 40 KM		XENPAK 40 KM		
	Performance	Margin	Performance	Margin	
SRS	<-11.3 dBm	-15.1 dBm	3.8 dB	-15.4 dBm	4.2 dB
TDP	< 3 dB	0.6 dB	2.4 dB	1.1 dB	1.9 dB

Data is worst-case performance over temperature (-5..70°C) and power supply variation ( $\pm 10\%$ ).

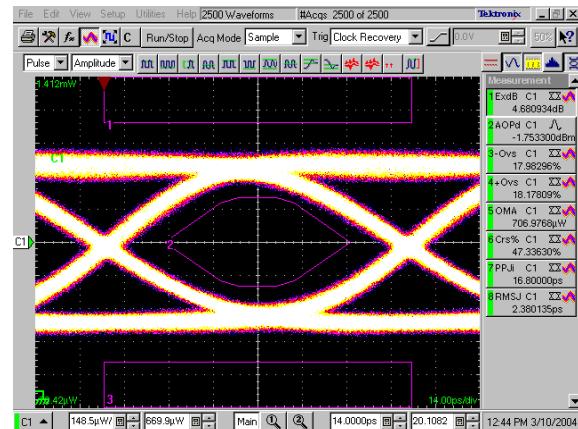
The XAUI PMA used in Ethernet and Fiber Channel systems also has MUX/CMU and CDR/DeMUX functionality for the 4-lane interface. The definition of the XAUI interface provides the additional benefits of individual CDRs on each lane as well as several bits of deskew functionality to provide robustness to layout and routing issues. The architecture also defines encoding and decoding overhead to the interface, to provide error detection, link status, and DC balance. On the 4-lane side,

each lane operates at a line rate of 3.125 Gb/s, for an aggregate bit rate of 12.5 Gb/s. The 8B/10B coding on this interface provides DC balance at a 25% overhead, for an actual datarate of 10 Gb/s. The signal is then scrambled, and 64B/66B coding is used to add link status, line/block coding, and scrambler synchronization on the optical interface, bringing the serial line rate to 10.3125 Gb/s.

For XFP transceivers, the PMA consists of simple CDRs for both the transmit and receive paths. As these modules work in both SONET and Ethernet systems, all of the performance parameters above apply. They must provide robust SONET jitter performance as well as TDP and SRS. This is particularly difficult in SONET systems as the output of an XFP transmitter must meet the 100 mUIpp jitter generation spec, while the chip providing the data signal to the XFP unit is allowed to have 50 mUIpp of jitter.

#### Optical Devices and Physical Medium Dependent ICs

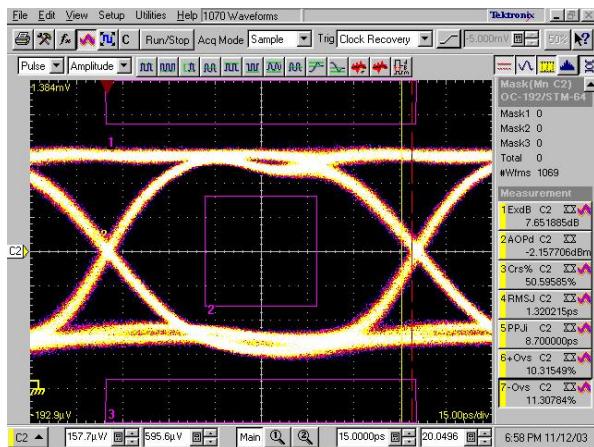
Depending on the reach requirements of a fiber link, different optical transmit and receive devices are required. Although there are alternative devices and technologies emerging, devices that are technically established and available in the market are discussed here.



**Figure 7: 850 nm multimode VCSEL optical eye diagram at 10 Gb/s from an XFP module**

For Very Short Reach (VSR) applications in the enterprise space, such as within-building or within-campus LAN and SAN connections where multimode fiber (MMF; 50 or 62.5  $\mu$ m core diameter) is present, 850 nm GaAs/AlGaAs Vertical Cavity Surface Emitting Laser (VCSEL) transmitters and GaAs pin photodetector-based receivers are sufficient for 10 Gb/s on links of 25 to 300 m, depending on fiber quality. The low drive current and high efficiency of a VCSEL enable a transceiver with very low power dissipation. As the drive current and voltages are low, generally less than 20 mA, a low-power CMOS driver can be used for direct modulation of

the VCSEL current. The bias current and driver swing may be controlled over temperature to compensate for changes in the characteristics of the device in uncooled operations. As these devices are only used in Ethernet links, they are generally operated at lower extinction ratios ( $> 3.5$  dB). A typical 850 nm VCSEL transmit eye diagram is shown in Figure 7.

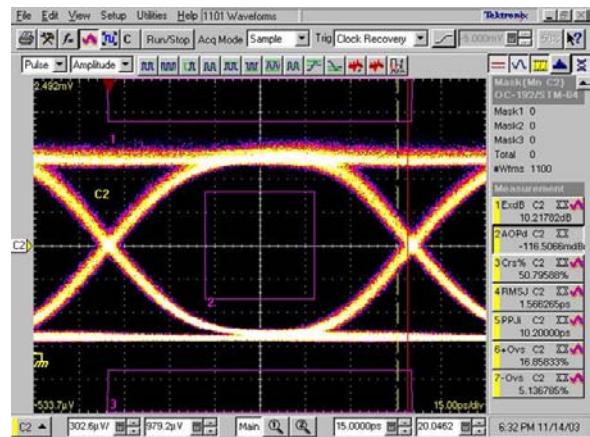


**Figure 8: 1310 nm directly modulated DFB optical eye diagram at 10 Gb/s from small form factor 300-pin 10 km module**

For Longer Reach (LR) links (7-20 km), a single-mode fiber (SMF; 9  $\mu$ m core diameter) is required, along with an InP-based single-mode Distributed Feedback Laser (DFB) operating at 1310 nm. This wavelength is chosen to match an operating region in the fiber that has close to zero chromatic dispersion (an impairment which otherwise causes pulses to expand during propagation). To satisfy SONET extinction ratio specifications ( $> 6$  dB), a DFB has higher current swing requirements than a VCSEL, which drives the need for higher current GaAs or SiGe drivers, lower impedance ( $25 \Omega$ ) interfaces, and alternative modulation schemes to save power, improve yields, and lower cost. Care must be taken to compensate for temperature variations in uncooled formats. A typical 1310 nm, 10 km DFB eye diagram is shown in Figure 8.

For metro area network access, Extended Reach (ER) links (40-80 km) may be used over SMF. These links are traditionally addressed by using externally modulated lasers, or EMLs, at 1550 nm. These devices, which monolithically combine a DFB laser with an Electro-Absorption Modulator (EAM) on an InP substrate, can be tuned to operate with low chirp (change of wavelength under modulation) to enable extended propagation in the low attenuation but higher dispersion 1550 nm window. These devices are generally modulated with GaAs or SiGe drivers to provide ample voltage swing and offset to achieve high extinction ratios ( $> 9$  dB) and high-quality eye diagrams. EMLs are operated in controlled temperature environments to ensure performance, the cost

of which is increased power dissipation from the Thermo-Electric Cooling (TEC) element and control circuit. A typical 1550 nm, 40 km EML eye diagram is shown in Figure 9.

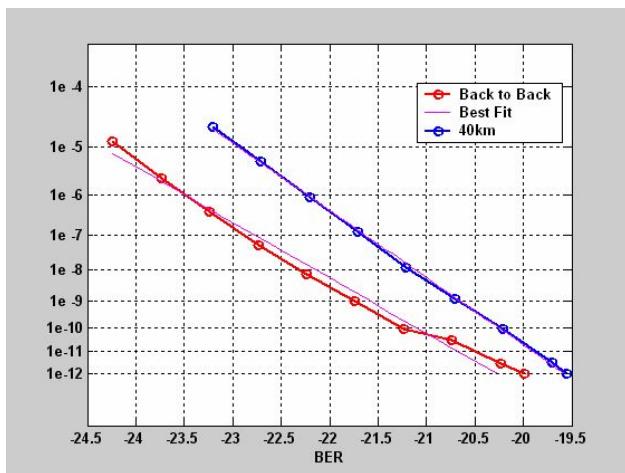


**Figure 9: Small form factor 300-pin 40 km module 1550 nm optical eye diagram at 10 Gb/s**

This type of eye quality must be achieved without sacrificing dispersion penalty performance, or difference between back-to-back sensitivity and post-dispersion sensitivity. High-quality 40-80 km transmit modules have low-dispersion penalty ( $< 1$  dB).

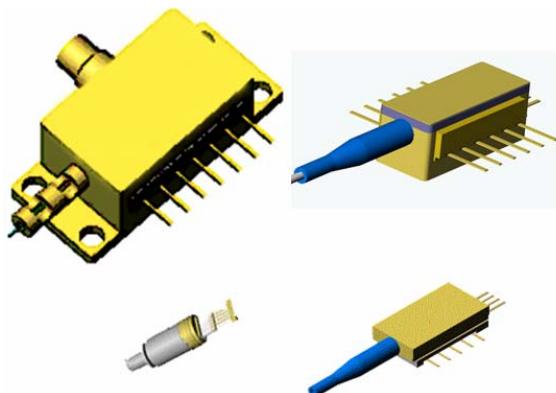
## Optical Receivers

Receivers for 10 Gb/s links are based on two types of optoelectronic devices, InP or GaAs PIN (Positive-Intrinsic-Negative doped structure) photodiodes or InP Avalanche Photodiodes (APD) that convert light into electrical current. The fundamental performance criteria for a receiver is its optical sensitivity, which is the optical power required to maintain a link Bit Error Rate (BER) of  $10^{-12}$ . A typical sensitivity curve is shown in Figure 10.



**Figure 10: Sensitivity curves from a typical 300-pin small form factor transceiver. The BER is plotted in error function space to yield a straight line.**

At these data rates, receivers integrate Transimpedance Amplifiers (TIA) to convert the photocurrent into a voltage swing that can be provided to a decision circuit such as a CDR. The shorter reach links above, from 300 m at 850 nm up to 40 km at 1550 nm, all use pin-based receivers. Unamplified links at 80 km use the additional gain of an APD to meet more stringent sensitivity requirements. Generally, a Limiting Amplifier (LIA) is integrated into the TIA to provide high gain and high sensitivity. There are cases, discussed later, where high gain is traded for linearity. Depending on the noise and gain requirements set by the sensitivity level of a particular link, TIAs can be designed in GaAs, SiGe, or CMOS processes.



**Figure 11: Optical module packaging options. Upper left shows a standard cooled “butterfly” can with coaxial RF interface. Upper and lower right show cooled and uncooled modules, respectively, with coplanar RF interface. Lower left shows uncooled TO can with coplanar RF interface.**

## Optics Packaging

Depending on the performance, cooling, and board interface requirements of a particular transceiver design, several different optical packaging technologies are employed, as shown in Figure 11. Traditionally, due to the difficult problem of achieving stable high optical coupling in a reliable manner, “butterfly” style packages have been used. Although they are large and costly, these packages provide a stable, hermetic environment for transmitters, TECs, and receivers, along with a coaxial RF interface to ensure high-quality signal integrity. Smaller, lower cost cooled packages with coplanar RF interfaces have been developed to enable smaller form factor transceivers without sacrificing performance. Uncooled designs are also smaller and cost a lot less; although, their use is limited to devices that can operate over a wide temperature range such as receiver circuitry and uncooled transmitters. Finally, coaxial TO-can-style optics with either coplanar ceramic or glass feedthrough RF interfaces are emerging to provide a very low-cost package that still provides adequate signal integrity for 10 Gb/s operation. While miniaturizing and reducing the cost of these optical modules, it is important to maintain performance and the standards of reliability that have been met by modules qualified to the Telcordia requirements in GR-468 [10]. It is critical that new optical packaging technologies increase yields and the quality of performance and reliability while decreasing the cost of the components, simplifying their manufacture, and reducing testing.

With the basic architecture of the 10 Gb/s optical transceivers presented here, optical communication system vendors have a wide array of transceivers available to meet the specific needs of individual system designs. Depending on the requirements of a particular system design, various form factors, fiber reaches, and performance levels are available in standardized modules.

Two emerging technologies that are influencing 10 Gb/s transceiver design are discussed in the following sections. The first, a wavelength tunable transceiver, enables next-generation DWDM systems. The second, EDC, can compensate for signal degradations due to fiber limitations.

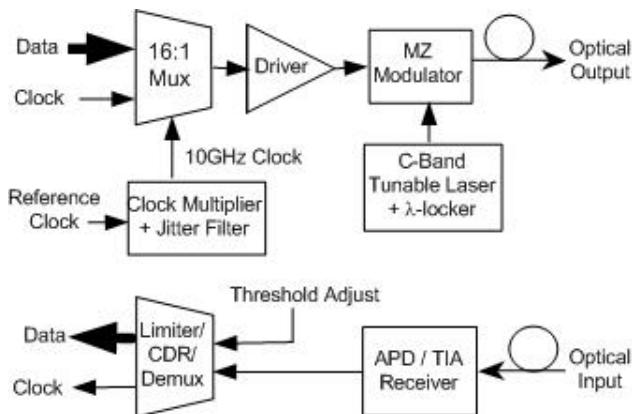
## DWDM DESIGN CHALLENGES

### Introduction

The recent downturn in the telecom market has forced telecommunications carriers to put enormous pressure on equipment providers to reduce system costs in the core backbone, where DWDM transport systems are typically employed. As a result, equipment providers are beginning to outsource their line-side optics to transceiver vendors. Cost pressures will continue to push standardized

transceiver-based solutions into next-generation products as the DWDM market continues to grow. However, standardizing DWDM line-side optics is very difficult given the very stringent and proprietary requirements specific to each system provider. Here, we present the technologies employed in a 10 Gb/s DWDM transceiver to guarantee robust transmission.

DWDM transport systems are made possible by one key invention, the Erbium-Doped Fiber Amplifier (EDFA). An EDFA boosts the optical power without the need for an electrical regeneration, and thus it manages the link losses between network nodes. It simultaneously amplifies any optical channel within its gain-bandwidth, and this is why optical transport system designers densely pack channels together. Telecommunications carriers can install EDFA at repeater sites between each fiber span, usually every 20-80 km. The benefits of EDFA include the ability to add and drop channels at intermediate nodes while allowing pass-through of other channels and the flexibility to add dispersion compensators at each repeater site to minimize transmission penalties. With these technologies, 10 Gb/s long-haul systems have extended their reach well past 1000 km, and 10 Gb/s metropolitan systems have surpassed 300 km in ring circumference.



**Figure 12: Functional block diagram of a DWDM transceiver**

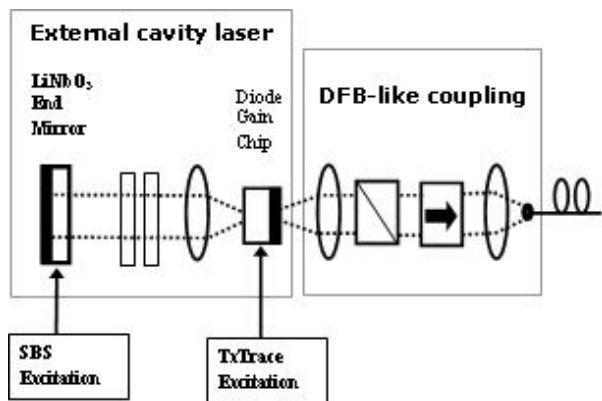
The success of DWDM systems has resulted in a number of technical and logistical challenges. Several system design strategies can mitigate the problems of DWDM transport. Specifically, for a DWDM transceiver, an effective design includes the use of tunable lasers, advanced electronic control circuitry, and high-performance modulators and receivers. Figure 12 depicts a simplified design architecture of a DWDM transceiver.

### Tunable Lasers for Channel Sparing

Traditionally, each 10 Gb/s optical channel in a DWDM system is supplied by a unique line card, which specifies

its optical carrier frequency. The large number of channels in the system puts enormous cost pressures on both the telecommunications carrier and the equipment provider when dealing with the inventory and forecasting of line cards. Tunable lasers are useful for reducing the number of inventory codes that an equipment provider must supply when deploying a DWDM system. Full-band tunable lasers can take all the channels in the EDFA bandwidth and reduce them to a common inventory code. Thus, a single tunable line card can be used as a spare for any optical channel in a DWDM system.

One example of a full-band tunable laser is the External Cavity Laser (ECL), which is shown in Figure 13. The LiNbO<sub>3</sub> crystal mirror and the gain-chip output facet, denoted by dark lines in the diagram, provide the optical boundaries (e.g., mirrors or facets) of the laser cavity. Thermally tuning the intra-cavity filters and adjusting the cavity length provide single-mode operation at a chosen channel wavelength. Coupling optics transmit the output to PM fiber and provide a power tap for output power control [11].



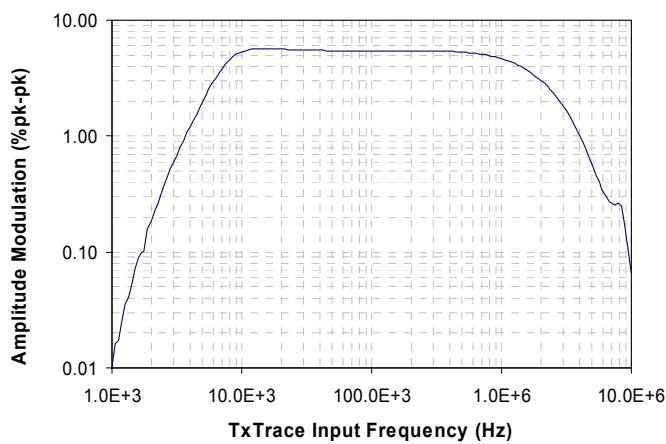
**Figure 13: Function block diagram of an ECL tunable laser**

### Channel Monitoring in DWDM Systems

Most carriers require that the DWDM system recognize the presence and absence of channels as they are added and dropped from the network. By applying low-frequency Amplitude Modulated (AM) trace tones to the transceiver output, knowledge of channel presence is established between the terminal equipment and each EDFA repeater site, without degrading other transmission performance parameters. Generally, these requirements fall within a modulation spectrum from 10 kHz to 1 MHz, with peak-to-peak modulation indices ranging from 1% to 5% of the total output power. The AM of tunable lasers is significantly more difficult than that of single wavelength lasers. This is because the DC bias current of a tunable laser varies with each channel and with output power in a complex manner. A sophisticated calibration routine is

required for modulating the tunable laser bias current. One benefit of using tunable lasers such as an ECL is that the gain of the laser can be sufficiently amplitude modulated without producing chirp or frequency modulation.

To account for the above factors, the gain of the transmitter trace circuit for a DWDM transceiver must be adjustable and flat over the AM bandwidth of operation. The circuit also filters any noise that is within the bandwidth of other control circuits, such as the servo signals used for wavelength locking. In Figure 14, the transfer function versus modulation frequency is shown for a tunable DWDM transceiver at a specific channel frequency.



**Figure 14:** Optical output modulation transfer function (%/mV) as a function of input tone frequency, for an input amplitude of 400 mV<sub>pk-pk</sub>.

## High-Power Launch Conditions

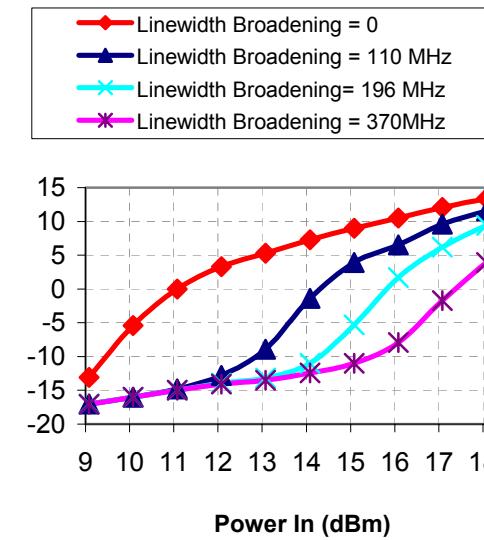
In most DWDM systems, the channel power can be well above 10 dBm for long ( $> 100$  km) fiber spans where intermediate repeater sites are not available. High optical intensities in optical fibers create a number of nonlinearities that cause transmission penalties. One such nonlinearity, which can be mitigated by the transceiver design, is the Stimulated Brillouin Scattering (SBS) of the optical carrier signal.

SBS is a nonlinear phenomenon that coherently beats the optical carrier with the acoustic phonons (i.e., molecular vibrations) of the optical fiber. As a result, the optical channel power is reflected back towards the source. This effect creates bursts of errors at the receiver as the channel power is scattered. Being nonlinear, the amount of SBS increases exponentially with the optical intensity in the fiber. The SBS threshold characterizes the launch power at which the back-scattered light becomes significant. This limits the amount of launch power that

an EDFA can provide to a DWDM system, and thus ultimately limits the transmission distance.

The most common SBS suppression technique effectively broadens the laser linewidth to reduce the power spectral density in the fiber, and thus increases the threshold at which SBS occurs [12]. For high-power applications, linewidth broadening of up to 1 GHz is common. At this linewidth, the EDFA may safely launch more than 19 dBm per channel into standard single-mode fiber.

For tunable external cavity lasers, modulation of the gain medium does not broaden the laser linewidth. This is because the phase of the cavity is dictated mostly by the end mirrors and filters, and less from the index of the gain medium. For ECLs, linewidth broadening is achieved by applying a voltage modulation to the external cavity's LiNbO<sub>3</sub> end mirror, thus producing a pure optical phase modulation [11]. Providing adequate excitation voltage amplitude to the LiNbO<sub>3</sub> crystal is a major circuit design challenge. The step-up transformer is a key component for achieving the necessary amplitude. One of the biggest difficulties regarding the transformer design is achieving high output voltage in a very small size.



**Figure 15:** Measured SBS reflected power versus launch power over 100 km of single-mode fiber. The SBS suppression scheme has increased the SBS threshold by more than 7 dB.

By applying direct FM modulation in the tunable laser, the SBS threshold of a DWDM transceiver can be increased. Figure 15 illustrates the measured power reflected back to the source as a function of input power into single-mode fiber. As the linewidth is broadened, less power is reflected. At 15 dBm of input power, for example, we observe, the reflected power drops from about 9 dBm to -12 dBm as the voltage of the end mirror

is applied. This results in an overall 7 dB increase in the SBS threshold. Meanwhile, the resultant AM due to the tone is less than a tenth of a percent of the overall output power.

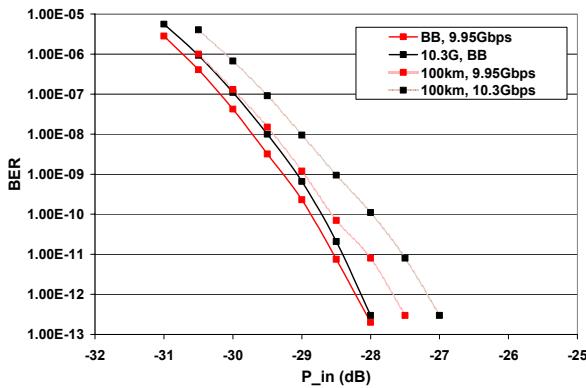
## DWDM Transmission and Optical Noise

The transmission performance of a communications link is typically characterized by its system BER, which is defined as the ratio of errored bits to the total number of bits transmitted. The BER is equal to the complementary error function,  $\text{erfc}$ , of the quality factor,  $Q$ , where

$$Q = V_{\text{sig}} / \sigma = (\mu_1 - \mu_0) / (\sigma_1 + \sigma_0), \quad (1)$$

and  $V_{\text{sig}}$  and  $\sigma$  are the received signal and noise levels, respectively [13]. The complementary error function decreases logarithmically as  $Q$  increases. In an optical transceiver, the received signal is proportional to the peak-to-peak voltage across the input of the CDR unit, as shown in Figure 15, and we define  $\mu_1$  and  $\mu_0$  as the mean voltages of the one and zero bits, respectively. The received noise level consists of the mean (rms) noise voltages of the one and zero bits,  $\sigma_1$  and  $\sigma_0$ , respectively. In thermally noise limited systems,  $\sigma_1$  and  $\sigma_0$  are equal in value. This is not true in amplified DWDM systems.

For optical communication systems, the system BER is a function of the transmitter extinction ratio, the transmitted eye quality, and the receiver tolerance to noise sources. The BER is also a function of several system parameters, such as the input power to the receiver, the amount of dispersion penalty in the fiber, the nonlinear penalty due to high launch powers, and the Optical Signal to Noise Ratio (OSNR). Both the transmitter and receiver portions of a DWDM transceiver can be optimized to improve system BER.



**Figure 16: BER vs. received optical power for back to back and after 100 km of single-mode fiber. The data rate is 10.7 Gb/s. The receiver sensitivity is about -28 dBm at a BER of 1E-12.**

## DWDM Transmitter Design

Equation (1) shows that the Q can be optimized by increasing the transmitter extinction ratio, which is defined by the ratio of the mean one and zero bits. In addition, the Q increases with received signal power. After transmission through fiber, the received signal levels may decrease due to fiber loss and dispersion penalty. For this reason, a high-performance transmitter must output a high optical power and yield a high extinction ratio. As shown in Figure 12, a typical DWDM transceiver employs a high-power tunable laser with a low-loss external LiNbO<sub>3</sub> Mach-Zehnder Modulator (MZM). This combination can result in an output power of greater than 6 dBm.

MZM modulators provide much higher extinction ratios than the electroabsorption modulators that are commonly used in shorter reach applications. Also, they have a well-defined chirp. By properly controlling the modulator chirp, longer transmission distances may be achieved without dispersion compensation. Figure 16 shows the BER as a function of received optical power for a negatively chirped DWDM transceiver before and after 100 km of single-mode fiber. The high transmitter extinction ratio produces an extremely sensitive (-28 dBm) recovery of data using an APD receiver, and the well-controlled chirp only causes 1 dB of dispersion penalty after fiber. The total link loss budget for this DWDM transceiver is more than 33 dB, assuming a 6 dBm launch power.

## Optical Noise

In amplified DWDM systems, the loss from the fiber span does not limit the system BER performance because the gain from an EDFA equals the fiber loss. In other words, the  $V_{\text{sig}}$  into the receiver can be maintained constant as long as amplification is available. As a result, amplified DWDM systems are typically noise limited due to the accumulation of optical noise after a chain of EDFAs. This noise is present at the receiver, and it is often referred to as Amplified Spontaneous Emission (ASE) noise. DWDM system designers characterize this noise in terms of an OSNR, where power of the signal in a channel is compared to the optical noise floor. The design of a DWDM transceiver must be able to adapt and optimize the system to various OSNR levels. An approximate expression for OSNR at the end of an optically amplified link with  $N_{\text{amp}}$  fiber spans preceding each amplifier is given by

$$\text{OSNR (dB)} = 58 + P_{\text{out}} - L_{\text{span}} - NF - 10 \log (N_{\text{amp}}) \quad (2)$$

where  $P_{\text{out}}$  is launch power per channel in dBm,  $L_{\text{span}}$  is fiber loss in dB of the fiber span, and  $NF$  is the EDFA noise figure in dB [14].

At the receiver, the noise from a DWDM system is given by the statistical sum of the electrical and optical noise sources. The electrical noise sources within a receiver itself is composed of dark current, shot noise, and thermal noise. The noise levels for the one and zero bits can be described as

$$\sigma_1^2 = \sigma_{dark}^2 + \sigma_{shot}^2 + \sigma_{thermal}^2 + \sigma_{ASE}^2 + \sigma_{sig-ASE}^2 \quad (3)$$

$$\sigma_0^2 = \sigma_{dark}^2 + \sigma_{shot}^2 + \sigma_{thermal}^2 + \sigma_{ASE}^2 \quad (4)$$

where  $\sigma_{dark}$  is the dark current noise;  $\sigma_{shot}$  is the shot noise;  $\sigma_{thermal}$  is the thermal noise;  $\sigma_{ASE}$  is the noise due to ASE from the EDFA; and  $\sigma_{sig-ASE}$  is the noise due the beating between the ASE and the optical signal.

### DWDM Receiver Design

When the noise levels are different on the one and zero bits, a more detailed derivation for the system BER is needed [15]. This is given as

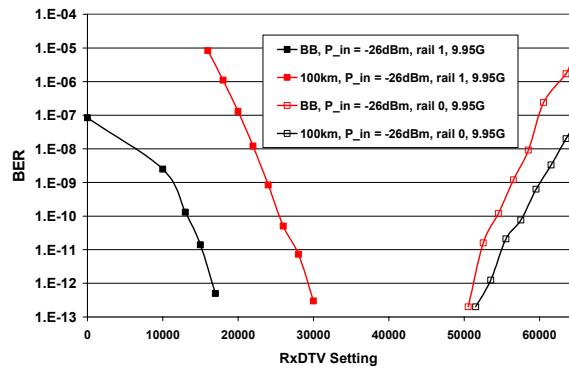
$$\begin{aligned} BER(V) &= (1/2) erfc [(\mu_1 - V) / \sigma_1] \\ &+ (1/2) erfc [(V - \mu_0) / \sigma_0], \end{aligned} \quad (5)$$

where  $V$  is the receiver decision threshold voltage. The maximum system performance is achieved when the BER is minimized, and this occurs when the decision threshold is at its optimum, or

$$V_{opt} = (\sigma_0 \mu_1 + \sigma_1 \mu_0) / (\sigma_1 + \sigma_0). \quad (6)$$

In unamplified systems, the dominant noise term in the receive path is receiver thermal noise because ASE noise is nonexistent. According to Equations (3-4), this implies that the noise is symmetric on the ones and zeroes, and the optimum decision threshold is halfway between the ones and zeroes level (e.g., fifty percent of the signal amplitude) using Equation (6).

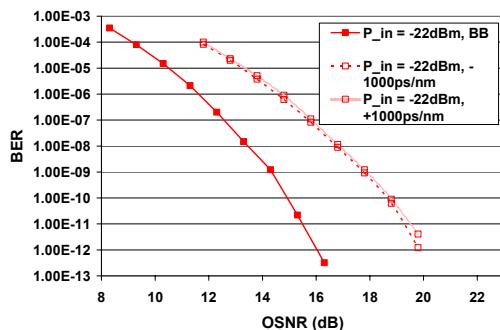
The optimum threshold will change in amplified systems where the OSNR is low (about 10 dB) and the ASE noise is dominant. This primarily occurs in long-haul DWDM systems where many EDFA are used to maximize the transmission distance. As shown in Equations (3-4), the ASE noise from the EDFA is present on both the one and zero bits. However, the noise on the one bit consists of an additional noise term due to beating between the signal and ASE ( $\sigma_{sig-ASE}$ ). This leads to an asymmetry in the noise levels on the one and zero bits. Because the noise on the ones level is larger than that on the zero, the optimum decision threshold level is skewed toward the zero level, as expected, by Equation (6). Note that the  $\sigma_{sig-ASE}$  beating noise is also dependent upon the received signal power.



**Figure 17: System BER vs. decision threshold setting**

For these reasons, long-haul DWDM systems actively control the receiver decision threshold level to minimize the recovered BER under all possible conditions. DWDM receivers are equipped with an external input for adjusting the decision threshold level before the CDR, as shown in Figure 12. An example of the system BER as a function of receiver decision threshold voltage is shown in Figure 17. The BER is minimized at the optimum voltage (near the middle of the range), and it increases as the voltage approaches both the one and zero levels (towards the ends of the range). It is evident that the BER varies asymmetrically as the decision voltage approaches the one and zero levels. This is due to the different noise elements for each level. It is also noted that the threshold moves closer to the zero level after transmission through 100 km of fiber. This is primarily due to chromatic dispersion and the resultant interference on the ones level.

The tolerance of a receiver to optical noise at low system OSNR values is a key figure of merit. This is usually measured at the optimum decision threshold. In Figure 18, the optimum BER for each OSNR level is plotted for a DWDM transceiver with and without transmission through fiber. As shown, the transceiver can recover a BER of 1E-12 in a DWDM system that provides only 17 dB of OSNR. At higher BER levels, such as 6E-5, the system OSNR can be as low as 12 dB. DWDM systems using Forward Error Correction (FEC) will typically operate at these high BER levels.



**Figure 18: BER performance versus OSNR for a typical tunable DWDM transceiver operating at 11.3 Gb/s. As the system OSNR increases, the BER improves (decreases). The receiver decision threshold is optimized at each condition.**

## Summary of DWDM Transceivers

The design of DWDM line-side optics is primarily driven by stringent system requirements that have been developed over the last several years based upon the limitations of optically amplified transmission. These optics must be able to satisfy the basic functionality for DWDM metropolitan and long-haul systems, including the ability to provide excellent transmitter extinction ratio, high launch power, and optical noise tolerance. These transceivers must also have several additional features in order to provide a high quality of service to the telecommunications carrier. These include the use of tunable lasers, channel trace tones, and adjustable receiver thresholds. By combining these attributes into a standardized modular interface, the DWDM transceiver will be able to penetrate an existing proprietary market space.

## ELECTRONIC DISPERSION COMPENSATION

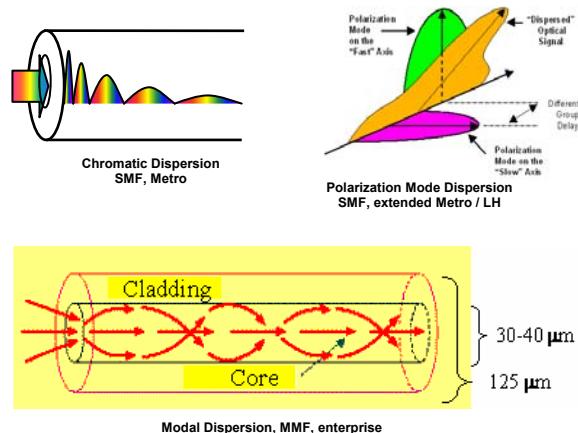
We now begin a discussion of a technology that can apply to several variations on the basic 10 Gb/s transceivers discussed thus far. Electronic Dispersion Compensation (EDC) is a technology that can be realized in an integrated circuit and thus implemented as an enhancement to various transceivers, enhancing the performance of existing designs and enabling new applications.

Although optical communication is among the fastest high-capacity data transport means available, there are various impairments that limit the capacity per fiber further than the capabilities of the active devices transmitting and receiving light at the ends of the fiber. Besides simple attenuation of the transmitted signal,

various dispersion phenomena affect the ability to recover the signal because of Intersymbol Interference (ISI). In general all dispersion phenomena lead to optical pulse broadening and ISI through different optical properties of the fiber. Recent improvements in the speed of silicon enable deployment of electronic filtering techniques, widely used in lower speed systems such as disk drives and wireless applications. The filter technology applied to optical impairments is known as EDC.

## Fiber Dispersion

The most common types of optical dispersion are shown in Figure 19. Chromatic Dispersion (CD) is significant for 10 Gb/s transmission at 1550 nm and distances above 40 km. The modulated spectrum (spread) of the light carrying information and the fact that CD causes light at different wavelengths to propagate at different speeds in fibers causes a broadening of the transmitted light pulses when transmitted over longer distance. The typical means to overcome CD in the optical domain are by reducing unwanted spectrum spread of the transmitter, by inserting sections of fiber with inverse dispersion behavior compared to the standard fiber, or by manipulating the index profile and hence the dispersion coefficient (ps/nm/km) of the fibers. However, all these means are costly and attractive only in long-haul systems. Due to the rather static nature of CD, optical compensation techniques are mostly stationary, set once during installation.

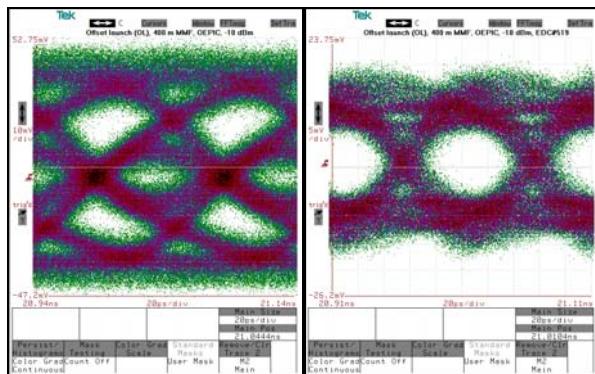


**Figure 19: The most important optical dispersion impairments and their relation to markets/applications**

Polarization Mode Dispersion (PMD) is a phenomenon occurring from the propagation of polarized light through fiber or optical components. In a polarized environment, the light traveling down the fiber can be split into two orthogonal directions or axes. If the fiber geometry is not exactly circular the light in the two axes will not travel at equal speed (birefringence), and the transmitted pulse will be broadened at the receiver end of the fiber. PMD is

secondary to CD and of less importance in today's fibers due to better control of the geometries in the manufacturing process. This reduces the importance to long-haul systems where CD is compensated in the optical domain; however, PMD can be significant in legacy single-mode fibers as they are upgraded from 2.5 Gb/s to 10 Gb/s transmission. PMD is problematic since it is difficult to compensate for due to its mechanically sensitive nature. Bending the fiber, vibrations, and thermal expansions will all change the actual PMD, and therefore compensation systems have to be adaptive.

Modal dispersion is significant in Multimode Fibers (MMF), widely used in shorter reach applications up to a few hundred meters. It is caused by the fact that the optical pulse splits into several paths (modes) traveling at different speeds down the fiber. The problem is somewhat identical to multi-path fading of wireless signals due to echoes from buildings etc. The use of MMF in enterprise systems has been traditionally related to the cost of connectorizing cables. When dealing with short distances the cost of adding connectors to cables, patch cords, etc. dominates, so there are significant savings in using MMF since the splicing and connectorization processes are more robust and tolerant to misalignments. The availability of low-cost 850 nm multimode VCSEL sources has also lowered the effective cost of multimode links. The penalty paid is modal dispersion, which is significant at speeds beyond 4 Gb/s.

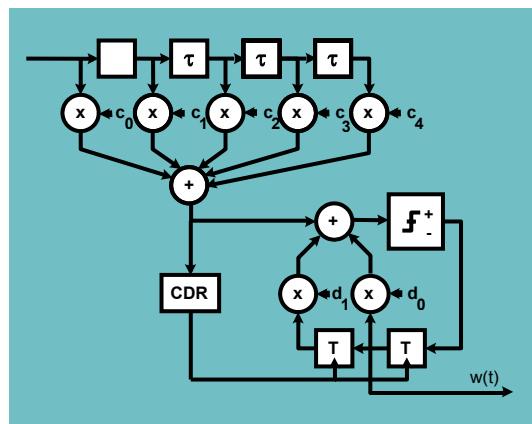


**Figure 20: Offset launch eye diagram after 400 m MMF (left), equalized eye diagram (right)**

Although the types of dispersion described above can be compensated or controlled in the optical domain, they can with some approximation also be dealt with in the electrical domain. When optical pulses are received by a photodetector, the signal is squared, and phase information of the transmitted signal is lost, leaving only a time continuous power distribution of the received optical pulses.

Applying techniques developed for recovery of information from disk drives, wired communication

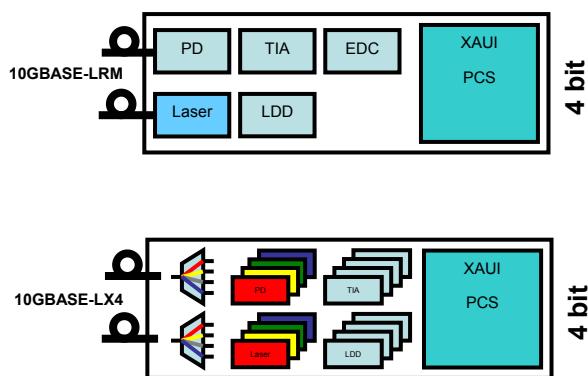
systems such as DSL, and wireless systems, the signal can be recovered from a signal that looks totally distorted at a first glance, as shown in Figure 20. This technology, when applied to optical dispersion, is known as EDC.



**Figure 21: Conceptual block diagram of an electronic dispersion compensation solution, consisting of an FFE, FBE/DFE, and CDR**

Adaptive filter techniques are widely described in the literature and can be implemented in a variety of ways. The Finite Impulse Response (FIR) method restores the original signal by reorganizing the received signal from a finite number of time-dispersed weighted partitions that, when correctly adjusted to perform the inverse function of the dispersive channel, will recover the transmitted pulse. The filter consists of a combination of feed forward taps providing linear filtering and feed back taps dealing with the non-linear portion of the pulse reshaping, as shown in Figure 21. Choosing an FIR filtering technique allows the use of adaptive algorithms used to automatically align the filter coefficients to minimize the error relative to an ideal signal. Various adaptation algorithms are possible, among them the Least Mean Square (LMS) approach, which continually compares the filtered output to that of an ideal signal and adjusts the filter coefficients to minimize the square of the error.

Although silicon technology speeds are exceeding the base requirement to operate a 10 Gb/s optical link, carefully architected solutions are needed to best optimize for the lowest possible power consumption. Choosing the right architecture with the optimum balance of FFE and FBE taps to form the optimal combination for the application is critical. Architecting the adaptation control function with the right set of characteristics is an important step to provide the EDC function with the right profile for the given task.

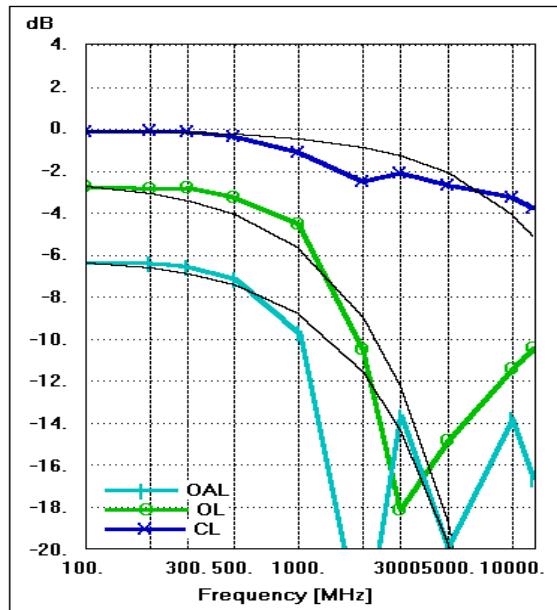


**Figure 22: Optical module examples showing the physical content of an EDC-based and a 4-wavelength-based module for 10 Gb/s Ethernet**

### EDC for Modal Dispersion

The enterprise market is one area of optical transmission that will greatly benefit from the use of filtering techniques. This market is typically Ethernet oriented, and the increments of speed from one generation to the next are one order of magnitude, 10 Mb/s – 100 Mb/s – 1 Gb/s – 10 Gb/s. The market is cost-sensitive and requires robust and reliable solutions that operate under office environment conditions with plug-and-play capabilities. The use of MMF is widespread from the early introduction of 1 Gigabit Ethernet (GbE). Because they offered a good combination of longer distance and higher speed enabled by optical transmission, these fibers were installed as backbone connections in networks, vertical risers in large buildings, campuses and other applications spanning up to 300 m distances. As desktop and server connections increase in speed from 100 Mb/s to 1 Gb/s, interest has increased in upgrading backbone fiber links from 1 GbE to 10 GbE.

Upgrading existing fibers originally installed for 1 GbE to run 10 GbE is not easily done, since the modal dispersion is significant and unless properly compensated, could prevent error-free transmission at 10 Gb/s. The current solution to overcome modal dispersion at 10 Gb/s in 300 m legacy multimode links is to multiplex 4 individual data streams at  $\frac{1}{4}$  of the datarate onto a fiber at individual optical wavelengths. However, this solution is relatively expensive and is not scalable to smaller form factors (notably XFP). Electronic dispersion compensation offers a cost-effective alternative. As there are no added system blocks, over time the EDC feature will be integrated with the PCS block as shown in Figure 22.

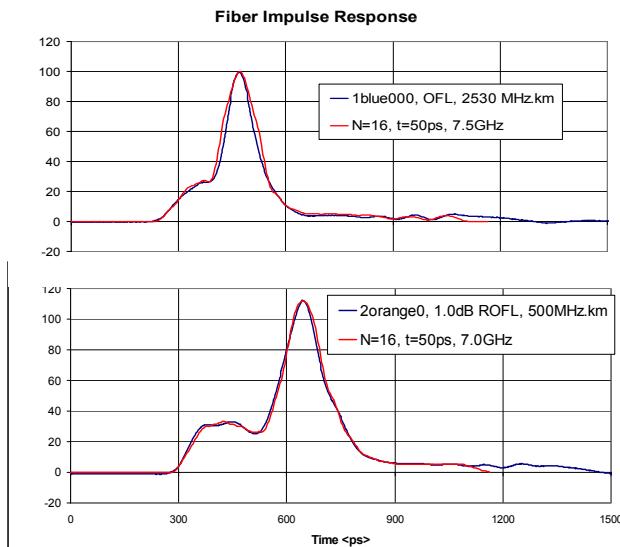


**Figure 23: Modal bandwidth measurement of 400 m of low BW multimode fiber under different launch conditions, center launch, offset launch, and overfilled launch with added modes**

### IEEE Task Force, 10GBASE-LRM

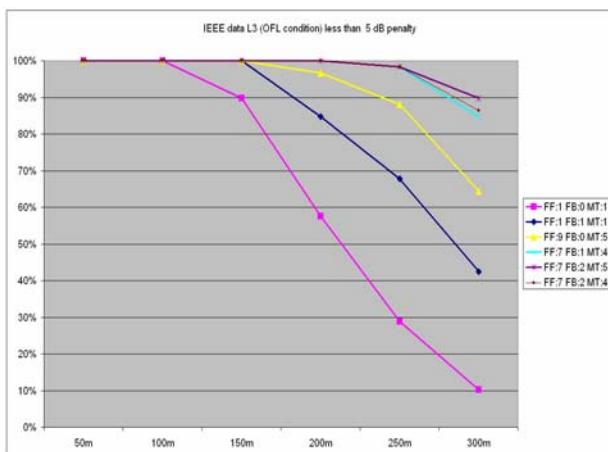
A solution based on established filter theory and implemented in silicon is being pursued by development teams throughout the industry. The IEEE has recently established a task force, 10GBASE-LRM, working to standardize the application space defined by a channel description and a required minimum probability of correctly compensating a worst-case fiber based on statistically collected data describing the base of installed fibers in today's network. This is not a trivial task since modal dispersion is very dependent on the mechanical and optical characteristics of the fiber, including the index profile, where fibers installed in the early 1990's exhibit worse behavior than new fibers. So far, fibers have been characterized using a simple bandwidth measurement, but when dealing with dispersion compensation this is an inaccurate method. Two fibers exhibiting the same modal bandwidth may exhibit very different dispersion patterns of which one could be significantly more complex to compensate than the other.

In Figure 23 the three measured curves show the modal bandwidth of one fiber under different transmitter launch conditions (the way light is coupled into the transmit end of the fiber). Launch conditions are important characteristics that are also covered by the IEEE 10GBASE-LRM task force, which will eventually specify launch condition requirements for 10 Gb/s transmission over multimode fibers.



**Figure 24: Example of realistic impulse response from multimode fibers of 300 m length**

A better way to characterize multimode fibers is by means of its impulse response or by recording a bit pattern from which the pulse response can be obtained, as shown in Figure 24. Once the impulse response of the channel (the fiber with a given launch condition) is known, it is a simple mathematical task to compute the required filter combination that exhibits the inverse function of the fiber and therefore would compensate the dispersion.



**Figure 25: Analysis of a selected set of worst-case fibers and the ability to compensate the modal dispersion at a optical power penalty of 5 dB. The individual curves plot particular filter combinations, with the number of FFE taps and FBE taps listed.**

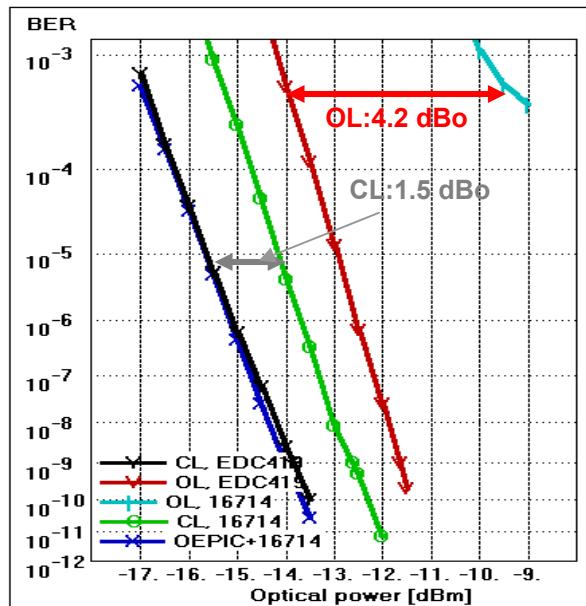
Because the requirement to compensate modal dispersion is related to all existing fibers installed, there are requirements to cover a sufficiently large portion of these fibers with the chosen adaptive solution. This allows the

EDC to adapt to any fiber within a defined set of characterized fibers, representing all existing fibers. Extensive modeling of filter combinations and their ability to restore signals from representative worst-case fibers are used in architecting the required solution. In Figure 25 a set of curves, each representing a specific filter combination, shows the percentage of fiber responses successfully compensated to a BER of  $10^{-12}$  at a given optical power penalty.

## Test Circuit Development

Although the raw speed of silicon technology has increased and allows more signal-processing circuit techniques in 10 Gb/s systems, there is no room for complex techniques to compensate dispersion in enterprise applications. This is because sophisticated filtering would require strong parallel approaches to provide the required performance, with excess power consumption that is incompatible with existing power budgets for optical modules. The challenge therefore lies in the circuit designer's ability to provide circuits fulfilling the requirements of the defined channels while at the same time accommodating the power budget by integrating the EDC feature into a transceiver building block in the enterprise optical transceiver module. As pictured in Figure 21, the block can be described using filter block terminology such as number of taps, tap weight range, feed forward equalizer, feed back equalizer, etc. The individual block characteristics and tradeoffs are all measured in conventional metrics such as linearity, bandwidth, resolution, and sensitivity. Breaking down the circuit into these well-defined equivalent blocks help the circuit designer to choose the optimal filter combination required for the application while at the same time optimizing the circuit.

Measurements from experimental circuits exhibit predicted performance improvement when applied to modal dispersion. Figure 26 shows the performance improvement at different launch conditions of a 400 m fiber link using a test device with a 5-tap FFE. The graph plots BER vs. receiver Optical Input Power (ROP), a common way to express the performance of optical systems. With Center Launch (CL) conditions the modal dispersion is limited, which explains the low relative improvement. With Offset Launch (OL) the eye diagram of the received signal and the equalized signal are those of Figure 20 resulting in a 4.2 dB improvement in ROP at  $\text{BER} = 10^{-3}$  and a dramatically higher improvement at lower BER (not measured due to limitations in setup). From the diagram, it can also be seen that the residual dispersion penalty (for offset launch) is 2.5 dB compared to the back-to-back reference measurement (transmitter coupled directly to receiver with 1-2 m fiber).



**Figure 26: Optical penalty comparisons to unequalized link. Center launch improvement, 1.5 dBo; offset launch improvement, 4.2 dBo (400 m MMF).**

Intel has had a long-standing interest in adaptive filter technology and has benefited from a strong knowledge pool derived in dealing with DSL and wireless applications. This has been used in the technology development providing fundamental building blocks for EDC to be integrated into products directed at the enterprise and metro market segments. The proven technology has demonstrated superior performance and helped set the expectations in the industry. Intel has contributed to the work on multimode EDC in the IEEE standards effort and has provided strong data, based on both modeling and experimental work, paving the way for an industry-wide acceptance of EDC-enabled transmission of 10 Gb Ethernet over legacy multimode fibers.

## CONCLUSION

The state of the art in 10 Gb/s optical transceiver design has been presented, with the architecture, functionality, and performance criteria for each of the major functional elements. Based on this basic structure, many different standardized products are available, with various form factors, fiber reaches, performance levels, and costs to satisfy the needs of optical communication system-level designs. Two emerging technologies that are pushing performance to new levels while reducing the cost of implementing modern designs were also explored. The wavelength tunable transceiver allows system vendors who had previously built DWDM solutions at the board

level to use modularized transceivers in their systems. The promising technology of electronic dispersion compensation is expanding link budgets and margins while driving new thinking about the capability of fiber systems. While the application to compensate for modal dispersion in multimode fiber links was discussed here, the technology lends itself to a variety of systems where dispersion and bandwidth limitations are present. As bandwidth demands continue to increase and 10 Gb/s links are adopted more widely in the industry, technologies such as these will play a significant role in satisfying that demand.

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We acknowledge the hard work and innovations of the engineers of Intel's Optical Platform Division (OPD) and Optical Networking Components Division (OND). Special thanks to Scott Schube for insights and editing. Much of the work in this paper would not be possible without the knowledge, insight, and patience of Steve Buchheit.

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# Automated Optical Packaging Technology for 10 Gb/s Transceivers and its Application to a Low-Cost Full C-Band Tunable Transmitter

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Index words: optical packaging, tunable laser, transceiver, automation, Dense Wavelength Division Multiplexing (DWDM), Micro Electro-Mechanical system (MEMs)

## ABSTRACT

Intel's quasi-planar optical packaging technology upon which multiple 10 Gb/s transponders and transceiver products are based is presented. This packaging technology has been applied to a low-cost, broadly tunable, high-output power laser, optimized for Dense Wavelength Division Multiplexing (DWDM) transport networks. The laser uses an external cavity design with intracavity thermally tuned filters fabricated from silicon wafers with optical Micro Electro-Mechanical System (MEMs) technology. Optical performance exceeds incumbent technologies and industry standards in all areas while little or no cost premium over non-tunable products is expected. The density of optical components and the alignment precision required presented challenges for the development of scalable component placement processes and packaging. Excellent performance has been obtained as evidenced by short-term stability under thermal and mechanical stress tests and long-term stability under accelerated stress tests.

## INTRODUCTION

The development of cost-effective optical component technology is critical for the continued penetration of optical high-bandwidth solutions in telecommunications, data networks, and computing. Development of

packaging methods suitable for mass production is a key enabler whose importance is magnified since standard electronics packaging methods are not suitable for optical components. Indeed in most practical cases to date, packaging is the primary cost driver of the optical components. Many packaging advances have been made or are currently in development at Intel, including silicon hybrid packaging, Micro Electro-Mechanical System (MEMs)-based alignment, and more recently, an adaptation of high-volume CD-ROM laser diode packaging technology commonly called "TO-cans." In the first part of this paper we describe planar automated packaging technology, one of Intel's automated packaging technologies that is currently used in our high-end 10 Gb/s transponders, and which has resulted in a dramatic reduction in the cost of 10 Gb/s transceivers sold on the market. In the second part of this paper, we present its recent adaptation to the practical manufacturing of an industry-leading, high-performance, yet low-cost tunable transmitter.

## AUTOMATED OPTICAL PACKAGING TECHNOLOGY

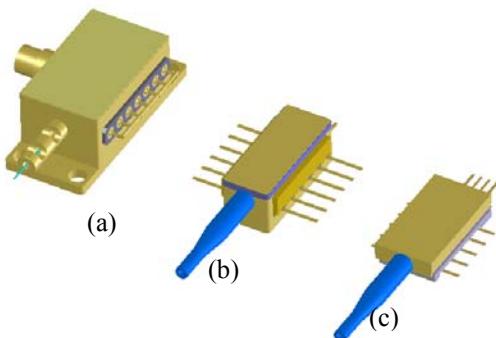
Intel's Optical Platform Division has been developing optical packaging technologies to meet the challenges of the design and manufacturing of high-volume and high-end optical components. The required attributes are as

follows: low cost and therefore highly scalable processes, high yields, excellent high-frequency performance for 10 Gb/s applications, low-power dissipation, small footprint for small form factor transceivers, and high reliability to ensure robustness under environmental stresses.

## Key Engineering Building Blocks

To respond to these design and manufacturing constraints, Intel's quasi-planar packaging technology has been developed using the following key engineering building blocks:

- Quasi-planar technology for the leverage of standard surface mount technology processes such as pick-and-place machines, reflow ovens, and wirebonding systems for non critically aligned components.
- Deformable metallic flexure technology to enable automated and robust active alignments of micro-optics to achieve high coupling efficiency (described in detail in the following section).
- Small form factor designs utilizing the flexure technology and ceramic substrates for an optimized electrical interface.
- Integration of microelectronics (transimpedance amplifier, laser diode driver) into the optical package to minimize transceiver form factor and optimize the Radio Frequency (RF) performance.
- Hermetic design enabled by manufacturing process developed using resistive seam sealing or laser seam sealing.



**Figure 1: Examples of Intel's optical modules: (a) iBTx platform for DFB and EA-DFB 10 GB/s transmitters, (b) sBTx platform, and (c) iMTx platform**

These technologies have been applied for a broad range of products illustrated in Figure 1 and reviewed in previous articles [1-4]. The initial applications were two standard butterfly can-based 10 Gb/s transmitters. The first one incorporated a distributed feedback laser for

7- and 10-km applications (iBTx010), and the second design for a 40-km transmitter incorporated an electro-modulated laser (iBTx040). These 10 Gb/s transmitters were integrated into multiple 10 Gb/s optical serial transceivers.

Subsequent product families making use of these technologies included a small uncooled transmitter iMTx007 and two small semi-cooled butterfly transmitters: sBTx-012 and sBTx-040. These products integrated a laser driver into the package to enable the design of small form factor 10 Gb/s optical serial transceivers such as the XENPAK compliant transceivers. This technology was also applied to a range of high-end optical receivers integrated into these transceivers as well.

The manufacturing advantages of this packaging technology were also incorporated into the design of Intel's Full C-Band Tunable Laser, which is in turn used as the laser source of Intel's Tunable Optical Transceiver.

In the following sections, general details are presented on two key engineering blocks, the flexure alignment technology and the component population using standard surface mount technology. A specific application of these technologies to fabricate Intel's tunable laser is described at the end of this paper.

## Optical Alignment of Components

In the past, optical components were produced on a small scale. The high demand for capacity in the last ten years, however, has driven the telecom industry to develop technologies that could be used in large volumes at low cost. Hence, Intel has developed a quasi-planar welding alignment technology by using a compliant clip, colloquially referred to as a flexure. This technology enables the automation of high-coupling, stable, and reliable optical platforms compatible with high-volume manufacturing. Figure 2 shows the design of a micro-machined flexure.



**Figure 2: Metallic micro-machined 6-mm long flexure**

Micro-optical components such as lenses, isolators, and fibers are mounted on the etched and formed flexible clips that allow for the building of different and complex free-space optical trains.

The clip is designed so it can be easily picked, placed, and aligned by an automated machine. The clip is first picked and placed on the substrate and released to stand freely on its feet. A second machine vision-guided tool then interlocks with the clip from above and compresses it, causing the flexible legs to be in intimate contact with the substrate at all times. Alignment in the plane of the substrate is performed by sliding the clip under constant pressure. Vertical alignment is accomplished by changing the pressure on the clip. This deforms the clip elastically by moving its legs apart. Once the optimal alignment is found, the feet are laser welded on the substrate. Since the legs are always in intimate contact with the substrate, play is kept to a minimum, and the usually problematic weld shift can be reduced during the attachment process. With proper clip and feet design, the tool can then be lifted up after the feet are welded without the flexure springing back up. With proper clip, tooling and process design, it is possible to achieve final positioning accuracies down to the few tenths of a micron necessary for high coupling efficiency.



**Figure 3: Automated welding system developed at Intel for high-throughput alignment processes**

Intel developed state-of-the-art automated alignment and laser welding stations, as shown in Figure 3. These automated tools perform active alignment, based on a variety of different feedback mechanisms, and securely laser weld the flexures in place to ensure excellent long-term reliability. To accommodate modularity and flexibility in the production lines, the assembly stations have been designed to process many different optical elements with minimum hardware and software changes.

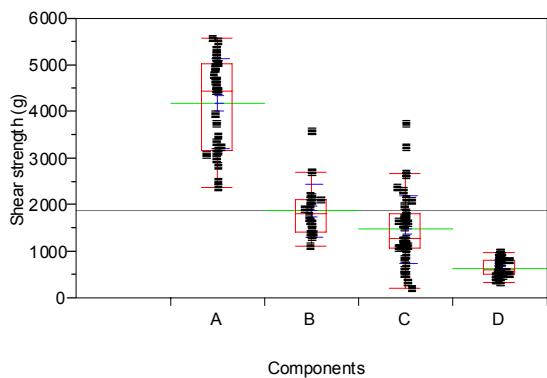
The alignment process starts with picking and coarsely placing the pre-assembly on a metallic platform using a machine vision algorithm. If a “first light” or feedback signal is not detected, a scanning algorithm is launched to drive the optical element to a position where an initial

feedback monitor can be sensed. A second algorithm, based on hill climbing or simplex schema, is launched to find the optimum optical alignment. After completion of the alignment, the process uses a pre-compensation to anticipate the post-attachment-shifts common in laser welding applications. The compensation is computed as a function of criteria such as weld pool shrinkage shift, the history of the alignment algorithm, motorized stage backlash, and the friction coefficient between the flexure and platform. The flexure feet are then laser welded to the metallic platform. Finally the gripper is released with no significant shifts.

## Component Population

Many of the components that are attached to the optical platform do not demand the fine alignment that most optical components require. Electrical components and weld plates can be placed with a precision commonly achieved with commercial electronic pick and place tools. The Intel optical platform technology uses these standard tools to pre-populate the substrate with these components using hard solders. Die shear tests were used to qualify the die attach per the MIL2019.5 standard as shown in Figure 4. SAM, X-ray image, and SEM/EDS techniques were used to detect the solder voids. Void-free die attach is critical for reliable packages.

For high-power devices such as laser diodes, heat dissipation and elimination of hot spots are key issues. Eutectic die attach is a common technique and has been used extensively in the industry [7-9]. For devices bonded using hard solders such as Au-Ge, Au-Sn, and Au-Si, the bonding layer generally has adequate mechanical strength to endure the induced stress without plastic deformation and thus would not become fatigued during thermal cycling. However, voids in the hard solder layer tend to generate localized stress on the backside of the chip, which may initiate cracking either during the die attach process or during thermal cycling. The voids could also cause hot spots due to poor local heat flow. On the other hand, when a softer solder is used for die attach, most of the stress would occur in the bonding layer, since it is much softer than the die and substrate. As a result, the bonding layer is degraded during thermal cycling due to thermal fatigue. If voids exist in the bonding layer, they will initiate the crack during thermal cycling. Therefore, in either hard solders or soft solders, void-free die attachment is important for achieving highly reliable packages.



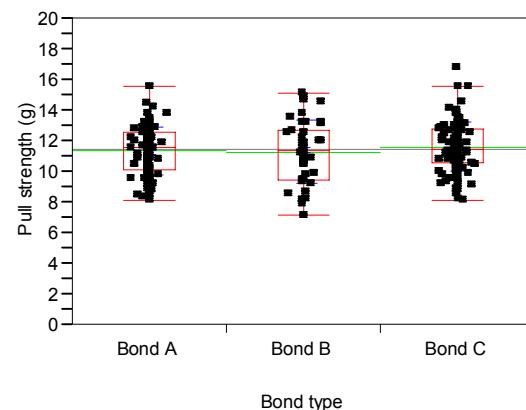
**Figure 4: One-way analysis of shear strength by components (A to D). Due to the different size of the components, the shear strength criterion is specific to the component.**

AuSn solder has been used for die attach in opto-electronic packages over the last decade. 80Au20Sn is a primary choice because of its favorable mechanical properties. This solder can be used as either preforms or pre-deposited solder. The melting point of 80/20 eutectic AuSn solder is 278°C, and it consists of two phases: 64.3% Au5Sn and 35.7% AuSn. When the molten 80/20 AuSn solder contacts the gold layer during reflow, the pure gold on the die and the substrate surface reacts with the solder constituent to form the Au5Sn phase. As a result, the Au5Sn phase content is increased and the AuSn phase content is decreased. The solder becomes more gold rich resulting in a higher melting temperature. The 80Au20Sn eutectic solder is characterized by steep liquid lines on both sides of the eutectic. The consequence of this is that a deviation of 1 wt% Au from the eutectic composition towards the Au-rich side will result in an approximate 30°C increase in the temperature of the liquid. Thus, careful attention should be paid to control the composition and reflow temperature.

### Automatic Wire Bonding

Challenges in the wire bonding for high-performance small footprint butterfly packages are 1) multiple surface metallizations within a package, 2) large bonding height differential, 3) short wire length for RF interconnection, 4) low bonding temperature, and 5) narrow space for deep access [13]. There are three types of commercial wire bonding methods: ball bonding, wedge bonding, and ribbon bonding. All of these methods use ultrasonic energy to enhance the welding joint of the bonding wire to the device and the substrate. In ball bonding, the first bond is made by connecting a ball formed by flaming off the gold wire that is threaded through a capillary tool. The second bond is a crescent shape formed by the imprint of the capillary on the joint. With wedge bonding, both the

first and second bonds look the same because the bonding occurs under the foot of the wedge tool in both instances. The second bond of the ball bond has less surface contact than that of the wedge bond. Therefore, the wedge bond exhibits higher pull strength for the same size wire diameter. This enables wedge bonded devices to achieve higher reliability and yield. Selection of the bonding methods should be based on the package structure, RF performance requirements, materials, metallization, and cycle time. For example, ball bonding is commonly used for laser diode to submount interconnection, but wedge bonding also has been successfully used.



**Figure 5: Wire pull strength versus bonding types**

When there are many types of metallizations within a package, it is important to consider each metallization separately with multi-variation of the bonding parameters [13]. This is easily achieved by an automatic wire bonder but difficult for a manual bonder. Figure 5 shows wire pull strength on the different surfaces' metallization after process optimization of an automatic wire bonder. The profiles used had to balance the requirement, the different metallization, height differential, and low temperature. The optimum bonding parameters are different from location to location and from device to device.

Understanding the electro-magnetic interactions is important for designing and selecting the wire bonding methods [14], especially for these 10 Gb/s applications. At these high frequencies, current flows closer to the surface of the conductor. The higher the frequency, the more current moves toward the surface. As a result, the bond wire's internal inductance is decreased as the square root of the frequency, while the external inductance is increased. Conductor layers couple to nearby conductors, and the coupled electric field induces current. The induced current leads to more electro-magnetic fields elsewhere. Ribbon wire bonding provides better high-frequency electrical performance than round wire bonding because of the lower mutual inductance and crosstalk between adjacent ribbons. Ribbon bonding uses thermosonic wedge-wedge bonding with the flattened

wire having rectangular cross sections. It requires lower bonding parameters (ultrasonic power and bond force) than for an equivalent diameter round wire [15]. Stiffness of the thin ribbon cross section is also significantly lower than for the equivalent diameter round wire, allowing the ribbon to bend and form a loop with less force than with an equivalent round wire.

The extreme range of heights within a butterfly package requires deep access equipment and tooling. In order to accurately and repeatably locate and bond components whose surfaces are at different heights, the wire bonder must have a pattern recognition system with a clearly focused image while the bonding tool moves over a large range in the vertical direction. Another feature of the opto-electronic package is that the wire bonding occurs at the end of the assembly process, after the lowest melting temperature solder alloy has already reflowed, thus limiting bonding temperature. Leads or feed-throughs that could vibrate and attenuate ultrasonic energy require special consideration [9]. Research has shown that when the vibration frequency of the leads is over half of the ultrasonic frequency, weak bonding will occur. One solution is to reduce the overhang of the leads; another is to increase the ultrasonic frequency.

## Reliability and Qualification

These products are designed primarily for Sonet and Ethernet applications in the telecom and datacom industry. Lifetime expectations of 20 years or more for these products demand that stringent reliability specifications be met. Extensive qualification under severe environmental conditions is required.

To reduce program risks as early as possible in the development of the product, a knowledge-based reliability assessment approach [16-18] is chosen to evaluate the critical areas of the design and to maximize the robustness of the product under environmental stresses. Our methodology is to understand the possible failure modes associated with the different functionality area of the design and to evaluate as early as possible the failure mechanisms associated with these modes by using specially designed test vehicles. We discuss an example of this methodology for the tunable laser product in a later section.

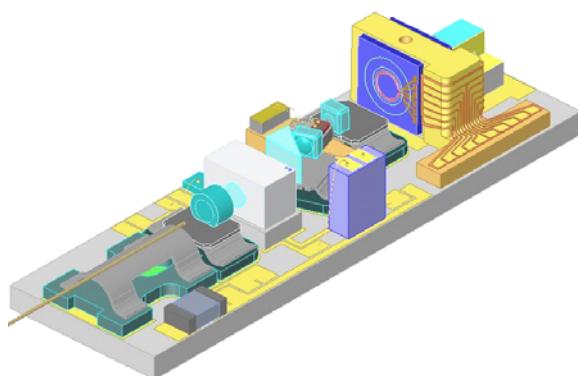
**Table 1: Telcordia requirements**

Test	Reference	Conditions
Aging	GR-468 Section 5.18	T=85°C, 2000 hours, 5000 hours for information
High temperature storage	GR-468 Section 4.3.2	T=85°C, 2000 hours
Low temperature storage	GR-468 Section 4.3.2	T=-40°C, 2000 hours
Damp Heat	MIL-STD-202 Method 103	85% / 85°C, 1000h
Thermal Cycling	GR-468 Section 5.2	100 cycles -40°C to 85°C, 40 min cycles. 500 for info.
Fiber pull test	GR-468 Section 4.3.2	3 times 1kg for 5s
Shock	MIL-STD-883 Method 2002.	500g, 1ms 5 times/axis, condition B
Vibration	MIL-STD-883 Method 2007	20g, 20-2000 Hz 4 min/cycle, 4 cycles/axis condition A
Operational test	Multiple	Vibration, shock, thermal cycling
Thermal shock	MIL-STD-883 Method 1011	ΔT = 100°C
ESD – Threshold measurement	GR-468, Section 5.22	5 discharges, 500V, all pins
Internal moisture	MIL-STD-883 Method 1018	Max. 5000 ppm water vapor

Finally, full qualification is evaluated in compliance with the GR-368. Telcordia requirements are summarized in Table 1.

## APPLICATION TO THE TUNABLE LASER

Tunable lasers help achieve cost savings for carriers operating Dense Wavelength Division Multiplexing (DWDM) transport networks by reducing the number of spare lasers that must be kept on site. Similarly, they greatly reduce the inventory of lasers that must be maintained by system vendors. The value of tunability is greatest in systems using the densest channel spacing.



**Figure 6: Solid model of the temperature-tuned external cavity laser assembled on the Intel quasi-planar laser welded manufacturing platform. Visible are welded flexures supporting the optical fiber, collimating lenses and a prism that sends a small fraction of the output beam power to a monitor photodiode. At upper right are the tunable filters and the partially obscured lithium niobate end mirror.**

However, closer channel spacing requires more stringent wavelength accuracy. The technical challenge is to provide both broad tunability and excellent wavelength accuracy over product life. We present here the key design characteristics of a broadly tunable External Cavity Laser (ECL) employing micromachined, thermally tuned silicon etalons designed to achieve these goals. To achieve a cost-effective solution, we utilized the efficient, high-yield manufacturing processes described earlier for Intel's 10 Gb/s transmitters, extending them for the tunable laser application, and we developed fast calibration methods for the tunable laser. Knowledge-based reliability assessment was conducted to demonstrate the robustness of the design.

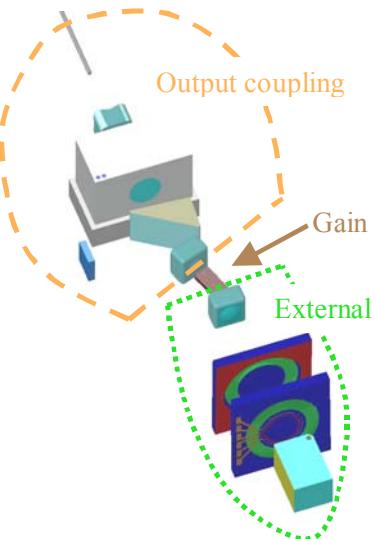
### Design of the External Cavity Laser

The design of the tunable laser module, shown in Figure 6, is based on Intel's quasi-planar manufacturing technology. The output optics of the tunable ECL are similar to those found in the single-channel lasers and the cavity side optical element attachment processes have also been adapted from those existing products.

The optical layout of the Intel C-Band tunable laser comprises three general sections (see Figure 7)

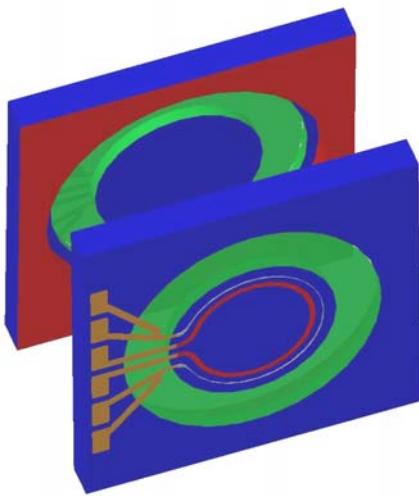
- 1) An external cavity to provide wavelength reference, tuning, and locking.
- 2) A gain medium.
- 3) Coupling optics to transfer the laser power to the single-mode fiber output.

The coupling optics provide efficient matching of the lasing mode to the fiber mode, isolation of the laser from optical feedback originating in the network, and power monitoring. The gain medium is similar in material and general structure to that used in single wavelength telecom lasers. Management of the facet reflectivity for the gain medium is important for proper operation, as it is for other telecom lasers. The ECL is bounded by the front facet of the gain chip at the front and the lithium niobate mirror at the back. The undesired reflectivity of the interior facet of the gain chip is reduced by a bent waveguide path, which ensures low feedback by design. Conventional anti-reflection coatings are used to further reduce feedback.



**Figure 7: Schematic of the optical train with the external cavity laser and the front-end output fiber coupling**

The unique aspects of the Intel tunable laser are realized by hybrid assembly techniques. Narrowly tunable-DFB and widely tunable-SG-DBR designs are often considered to be monolithic devices; however, for DWDM applications, these ostensibly monolithic devices require an external wavelength reference and an external power monitor, each realized by hybrid assembly. The Intel tunable laser separates wavelength selection and tuning from the gain medium, in addition to the wavelength reference and power monitor.



**Figure 8: Optical etalon composed by two thermally tuned Si filters**

The ECL does entail an increase in the number of components. The apparent mechanical complexity of the ECL is managed at the time of manufacture by use of the established Intel quasi-planar technology described earlier. As well, the Intel ECL essentially retains immunity to shock and vibration, as afforded by its no-moving-parts design and packaging implementation.

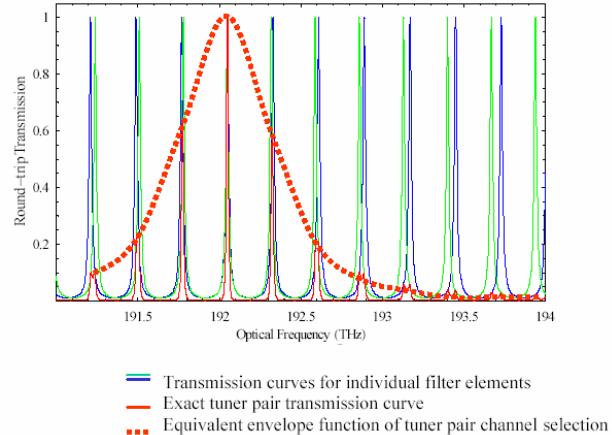
This separation of optical functionalities permitted by hybrid assembly avoids loss by replacing absorptive regions of the InP used for wavelength selection with equivalent implementations in low loss materials. One result of this overall structure is that required telecom power levels can be achieved without the need for subsequent amplification. More important, this separation results in actuators (e.g., for tuning and power control) with minimal crosstalk. The independent nature of the actuators significantly simplifies the control of the laser. The various control functions in the Intel ECL operations are as follows:

1. Maintaining the intracavity wavelength reference.
2. Wavelength tuning.
3. Locking the laser wavelength to the wavelength reference.
4. Locking the output power to a calibrated photodiode.

Locking the lasing wavelength is achieved by recovering a servo error-signal from the electro-optical dithering of the lithium niobate substrate for the ECL cavity mirror and by using a peak-locking algorithm to fix the cavity length. Locking the output power is implemented with an error signal generated in the coupling optics.

The intracavity tunable filter serves also as the wavelength reference. Hence, the control functions of

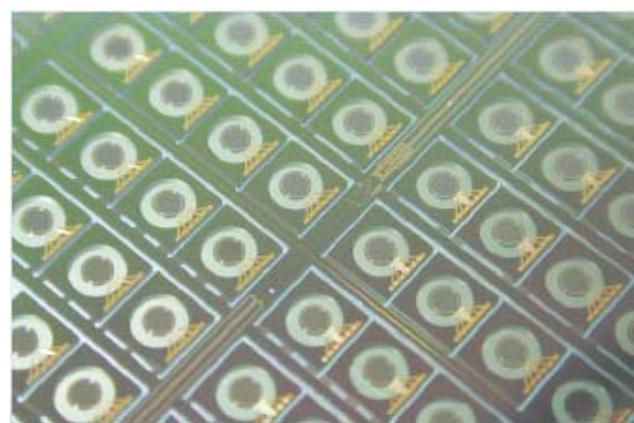
setting the wavelength reference and wavelength tuning are unified, eliminating control conflicts. The wavelength filter selectivity is created by the Vernier effect, which is caused by the transmission through a pair of silicon etalons with slightly differing periods (see Figure 8).



**Figure 9: Illustration of the Vernier effect. The laser is tuned by shifting the spectrum of each filter to have the transmission peak at the desired wavelength.**

The net transmission of the pair is at a maximum for the wavelength for which both etalons have a peak in transmission (see Figure 9).

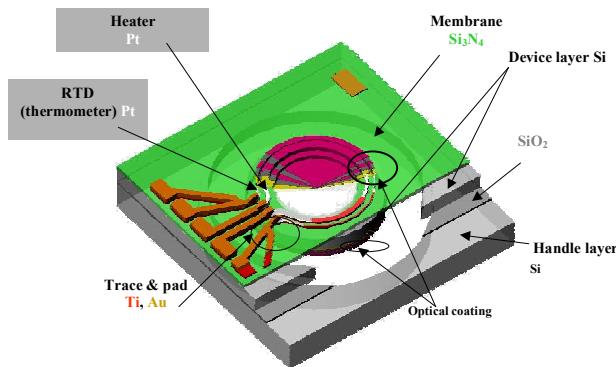
The composite periodicity of the pair of filters is greatly increased compared to that of the individual etalon by the Vernier effect, providing a unique transmission peak in the telecom band of interest.



**Figure 10: Wafer of the MEMS filters**

Changing the temperature of a given filter spectrally translates the transmission function, with a sensitivity driven by silicon's thermo-optic coefficient. In the Vernier implementation, any wavelength in the C-Band can be addressed with a small temperature adjustment of the individual etalons. To tune to a target wavelength, a temperature is chosen for the first etalon that places a

transmission peak at the target wavelength. Simultaneously, a second temperature is chosen for the second etalon so that it also has a transmission peak at the same target wavelength. This achieves the filter configuration shown with a joint maximum at the new target wavelength. Owing to the microfabrication, local heating, and local temperature sensing, the filters can slew across their entire operating range within one second. The independent nature of the tunable filter control permits wavelength tuning while current to the gain medium is turned off. This operation avoids laser emission at any wavelength other than the final target wavelength.



**Figure 11: Details of the Si thermally tuned filter**

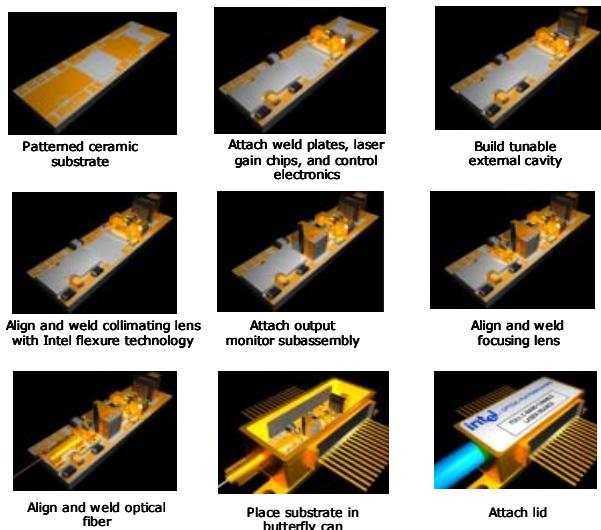
In addition to silicon's optical and thermal properties, silicon is also amenable to microfabrication techniques (see Figure 10). Microfabrication allows for low cost, and permits integration of features to maximize utility. In particular, microfabrication is used to create thermal isolation by a silicon nitride suspension, and for electrical connectivity for local heating and temperature monitoring. Similar micromachined Si microstructures with SiN membranes are being used for other applications such as thermal sensors, accelerometers, and anemometers [5-6].

The temperature monitoring of the etalon's optical clear aperture is critical, as the calibrated etalon temperatures are used as the proxies for optical wavelength. The integrated Resistive Thermal Device (RTD) thermometer uses a platinum sensing element (see Figure 11).

The thermal conductivity of the silicon etalon suppresses temperature gradients improving accuracy in temperature monitoring, and avoiding complications in control for standard (e.g., fused silica) etalons traditionally used in external wavelength lockers. A four-wire probe is created by microfabrication to isolate the RTD function from stray series resistance from wire-bonding and other sources. The temperature control achieved by these measures supports, in conjunction with factory calibration, the role of the wavelength filter as a stable and accurate wavelength reference.

## Process and Manufacturability

To achieve a cost-effective solution, the quasi-planar optical packaging technology described earlier in this paper was implemented to achieve efficient, high-yield manufacturing processes.



**Figure 12: Manufacturing process steps to build the tunable laser**

The module is assembled on a flat ceramic substrate upon which is deposited a patterned metallic layer as illustrated in Figure 12. Optical chips (laser, photodiodes) and electronic components are mounted with an accuracy of approximately 10 microns by pick and place automation using machine vision, as commonly employed in the electronics industry.

Optical components such as lenses and fibers are mounted on etched and formed flexible metallic elements (flexures) as shown in Figure 2. This module optical alignment consists of four active alignments with the flexure technology (two collimating lenses, one focusing lens, and one optical fiber) and two active alignment components that require special thermal conductivity management, which are epoxied down (back cavity mirror and tunable filter subassembly).

Leveraging of the alignment technologies developed for previous products [1-4] has allowed the reduction of the development time. Another benefit is our ability to reuse our high-volume manufacturing capability that is already in place.

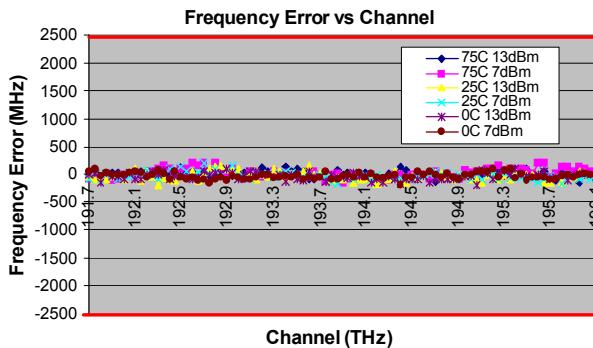
Part of the manufacturing cost is the testing and calibration time to ensure the frequency and power accuracy on 88 channels. Tuning and calibration of these lasers is simple and fast because the tuning curves are determined by known, predictable physical attributes of

stable materials, i.e., the change in the length of the optical path in single crystal silicon and the change in resistance of Pt as a function of temperature. By using accurate physical models to interpolate between wavelength channels, the Intel tunable ECL can be calibrated across the whole C-Band with very few parameters.

## Performance

After the tunable ECL device is assembled, it goes through a rigorous test suite to evaluate its performance. The intracavity locking technique using the thermally controlled etalons provides excellent performance. Frequency accuracy at two power levels and several case temperatures, shown in Figure 13, demonstrate the tight etalon temperature control and hence the frequency accuracy of the design. The lasers exhibit day-to-day optical frequency stability of +/-100 MHz, which is well below the +/-2500 MHz specification, and they are able to maintain this stability independent of case temperature. Furthermore, this stability over case temperature is obtained without any compensation. Table 2 illustrates the key specification of the TTx1150 C-Band Tunable Laser.

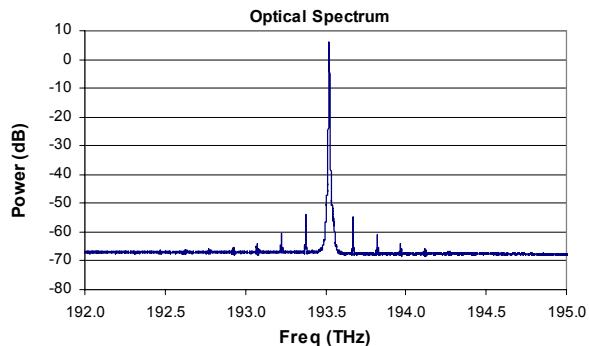
The optical spectrum of the laser at the center of the tunable range (193.5 THz) is shown in Figure 14. This spectrum is very consistent across the whole tuning range, as illustrated by the distribution of the Side Mode Suppression Ratio (SMSR) between 191.7 THz and 196.1 THz shown in Figure 15.



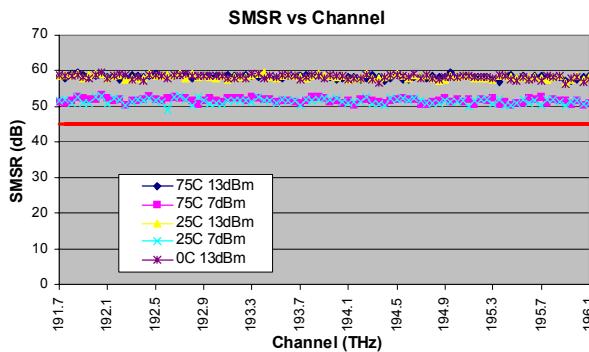
**Figure 13: Frequency accuracy of the temperature-controlled-etalon-based ECL. Accuracy is plotted vs. laser output frequency from 191.7 to 196.1 THz. Results for two different power levels and three different case temperatures are shown.**

**Table 2: Specification of the TTX1150 Full C-Band Tunable Laser**

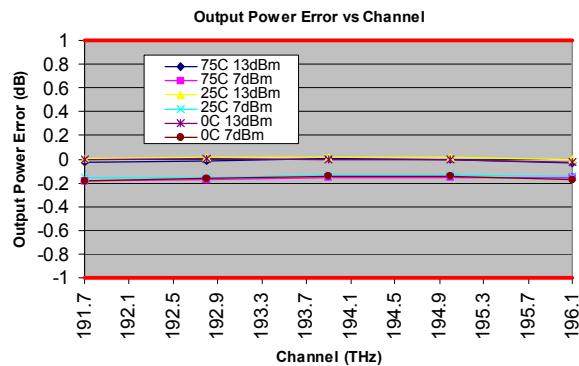
Parameter	unit	Min	Typical	Max
Operating temperature	°C	-5		75
Tuning range	THz	191.7		196.1
Output power	dBm		13	
Wavelength accuracy	GHz	-2.5	$\pm 0.1$	2.5
Wavelength stability		-2.5	$\pm 0.1$	2.5
Power accuracy	dB	-0.5	$\pm 0.1$	0.5
Power stability	dB	-0.5	$\pm 0.3$	0.5
SMSR	dB	45	55	
RIN, 1 MHz to 10 GHz	dB/Hz	-140		
PER	dB	20	30	
Tuning speed	sec		10	25
Module power consumption	W		2	4



**Figure 14: Optical spectrum of the temperature-controlled-etalon-based ECL locked at 193.5 THz**



**Figure 15: SMSR of the temperature-controlled-etalon-based ECL is plotted vs. laser output frequency from 191.7 to 196.2 THz at two different power levels and three different case temperatures**



**Figure 16: Power accuracy of the temperature-controlled-etalon-based ECL is plotted vs. laser output frequency from 191.7 to 196.2 THz. Results for two different power levels and three different case temperatures are shown.**

Figure 16 shows the power accuracy vs. the frequency range from 191.7 to 196.2 THz. The power variation is within 0.2 dB across the frequency range and the case temperature ranges from 0 to 75°C. This excellent power stability results from the quasi-planar design, which provides very good temperature stability of the optical train and isolation from the case temperature variation.

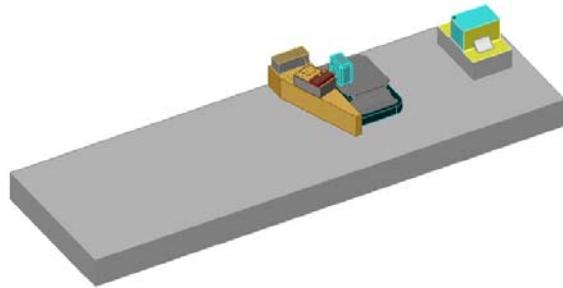
## Reliability Assessment

To reduce risk as early as possible in the development of the product, a knowledge-based reliability assessment approach has been chosen to evaluate and maximize the robustness of the product under environmental stresses. The system has been analyzed using multiple test vehicles to isolate failure mechanisms associated with each of the functionality areas:

- Laser chip on submount: This subassembly is the critical active component of the design and provides the gain media for the external cavity. High-temperature and high-biased stress tests were conducted to assess the degradation mechanisms (power, optical spectrum) and the failure rate.
- Front optics test vehicle: This test vehicle was used to evaluate the robustness of the coupling efficiency between the laser output and the fiber output. The main metric was the coupling efficiency and the monitor photodiode responsivity. This test vehicle had the tunable ECL completely replaced by a Fabry-Perot laser chip that isolated the front optics reliability from external cavity reliability.
- External cavity test vehicle: This test vehicle was used to evaluate the robustness of the external cavity end mirror and the collimating lens stability (Figure 17). The main metrics were the threshold of the laser

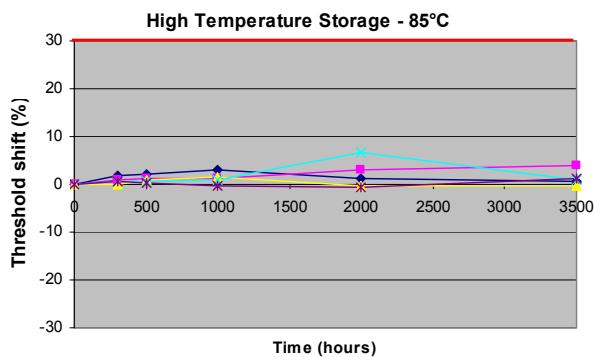
and the end mirror tilt (measured independently with an external probe). This test vehicle had no filters or tuning mechanism so as to provide a direct evaluation of only the mechanical stability of the external cavity.

- Tuner subassembly test vehicle: This test vehicle was used to test the robustness of the two thermally tuned etalons attached to a carrier. The metrics of this test vehicle were the resistance of the thermal detector, the optical transmission, and the angle tuning of the etalon.



**Figure 17: Example of test vehicles used to isolate failure mechanisms. This figure shows the external cavity laser including the end mirror, a collimating lens, and the gain chip.**

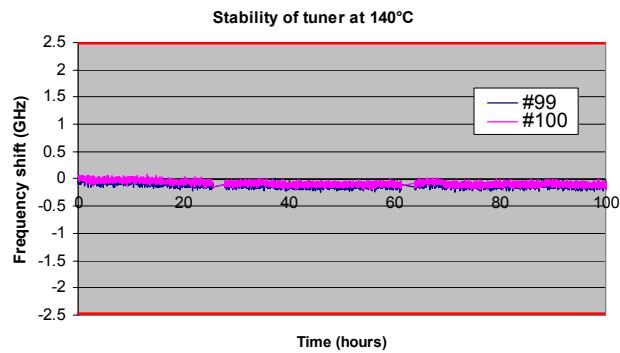
Figure 18 shows the threshold variation of the external cavity test vehicle during a 3500-hour test at 85°C. The maximum threshold variation was around 4% which is far smaller than the budget of threshold increase over the lifetime of the product.



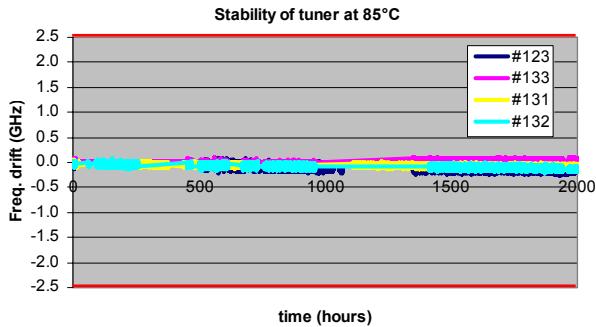
**Figure 18: Shift of the threshold of external cavity during a 3500-hour stress test at 85°C**

Since the primary novelty of the laser design is the use of the micromachined thermally tuned silicon etalons, (see Figure 8), extensive tests have been conducted to analyze the failure modes associated with this subassembly. Highly accelerated testing has been conducted to analyze the time to failure and the acceleration factors. Using the integrated heater and temperature detector in the filter, it was possible to run the two filters at very high

temperatures while precisely monitoring the frequency stability of the tuner. Figure 19 and Figure 20 show the frequency stability of tuners during a 100-hour test at 140°C and a 2000-hour test at 85°C. The observed drift was below 200 MHz.

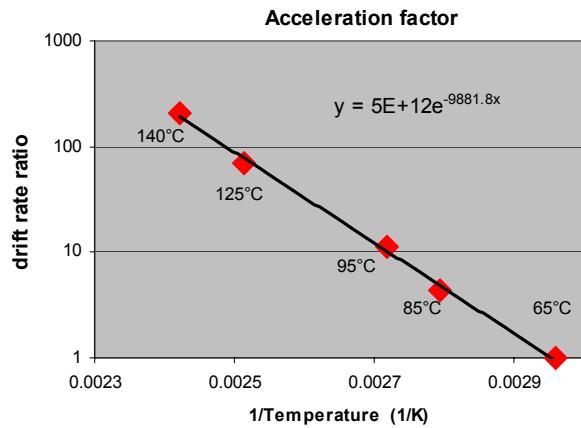


**Figure 19: Highly accelerated stress test on tuners at 140°C over 100 hours. The frequency drift is below 150 MHz after 100 hours.**



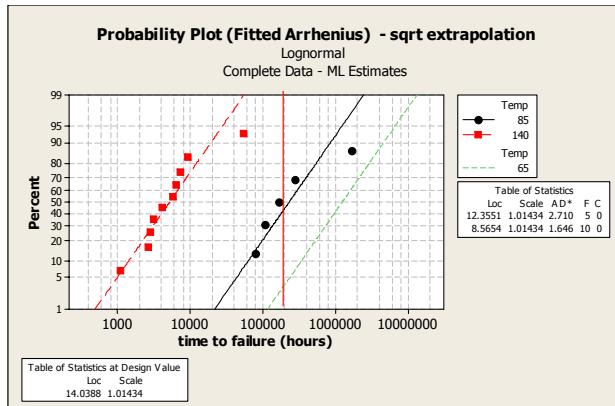
**Figure 20: Accelerated stress test on tuners at 85°C for 2000 hours**

This stress test enables the evaluation of the acceleration factor with temperature for the change in frequency of the tuners (Figure 21). An activation energy of around 0.85 eV was measured.

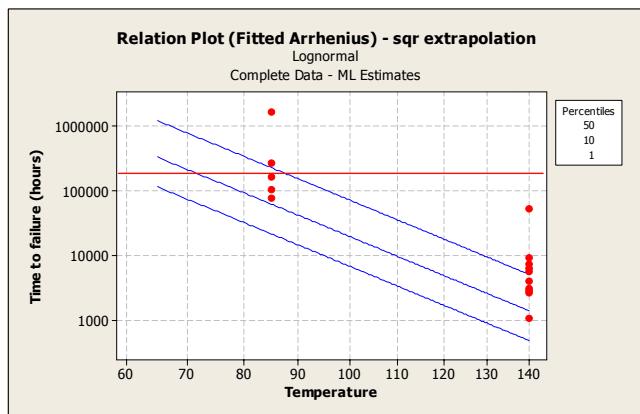


**Figure 21: Arrhenius plot of the frequency shift rate ratio vs. temperature to compute the activation energy of the failure mechanism associated to frequency stability at elevated temperatures**

Based on the distribution of time to failure at multiple temperatures, we computed the median time to failure for nominal conditions as shown in Figure 22 and Figure 23. The median time to failure was found to be beyond 130 years in this initial reliability assessment.



**Figure 22: Computation of the expected median time to failure based on a lognormal failure distribution at different temperatures**



**Figure 23: Prediction of the time to failure as a function of temperature. The three curves correspond to the predictions for 1%, 10%, and 50% failure.**

In addition to the failure mode isolation and risk analysis on the subcomponents and test vehicles, extensive stress tests were conducted on the completed product.

The results of the prequalification demonstrated the robustness of the design and highlighted the advantages of a non-moving part design for a tunable laser. For example, the frequency stability during the mechanical stress tests was excellent (max 300 MHz of frequency shift out of a 2.5 GHz specification), as shown in Table 3.

**Table 3: Results of the frequency shift during operational vibration and shock test**

Condition	Number Failure	Max. Power variation (dB)	Max. Frequency fluctuation (GHz)
2 G, 5-500Hz, Sweep Sine Vibration Test	0	0.15	0.2
40 G with 1 ms Shock pulse	0	0.17	0.3
50 G, 5 ms, 5 impacts	0	0.23	0.3

## CONCLUSION

To respond to the challenge of the manufacturing of high-end optical components, Intel has developed a set of key engineering technologies based on quasi-planar technology and alignment flexures. This technology has been successfully applied to a broad range of optical modules from small footprint butterfly transmitters using cooled EML and DML to high-end, low-cost, tunable lasers. High performance and low cost are concurrently demonstrated in a broadly tunable external cavity laser design employing micromachined, thermally tuned, silicon etalons and Intel's laser-welding manufacturing

platform. Integral wavelength locking and efficient calibration procedures further enable the essential combination of wavelength accuracy, power stability, and low-cost required for metropolitan, regional, and long-haul DWDM applications. Initial reliability testing has confirmed the very good design margins that are inherently expected from a "no moving parts" design.

## ACKNOWLEDGMENTS

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# Optical Interconnect System Integration for Ultra-Short-Reach Applications

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**Index words:** optical interconnect, hybrid integration, silicon optical bench, VCSEL arrays, Ultra-Short-Reach

## ABSTRACT

It is predicted that the increase in microprocessor clock frequency will create bandwidth limitations for copper interconnects on Printed Circuit Boards (PCB) due to signal attenuation, Electromagnetic Interference (EMI) and crosstalk [1]. Optical interconnects could be a viable solution to these problems. This paper explores the potential and challenges for optical interconnects in Ultra-Short-Reach (USR), <10 m, applications. We discuss two designs for implementing high-performance and cost-effective optical interconnect solutions. The first architecture uses the Silicon Optical Bench (SiOB) approach and is primarily focused on the board-to-board and rack-to-rack solutions. The second architecture implements hybrid integration on a standard microprocessor package in order to address issues in chip-to-chip data transmission. Using the latter method we demonstrate a 3 Gb/s optical eye for the transmitter and 1 Gb/s error-free transmission.

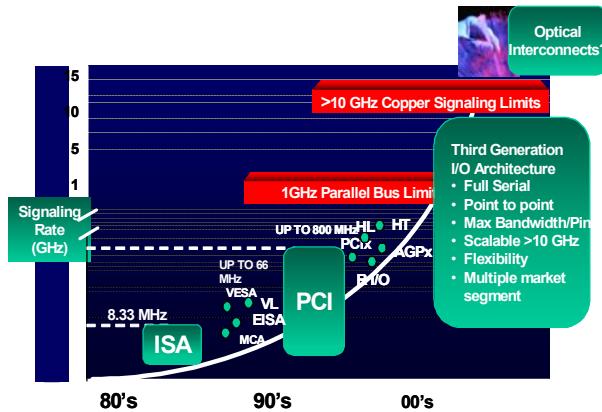
## INTRODUCTION

Fiber optic communication links dominate over copper wire electrical signaling in high-speed communication networks for distances over several hundred meters in length due to the superior bandwidth distance performance of the optical channel. However, as distances become shorter, copper-based interconnects

become the dominant solution because they are simpler, cheaper, and reliable. Intel's commitment to the extension of Moore's law well into the future will help drive the ever-increasing processing power of computer and communication systems, placing increasing demands on the bandwidth of copper interconnects. One particular formulation of Rent's Law states that the bandwidth requirement of a module with processing capability C increases in proportion to  $C^\alpha$ , where  $0.5 < \alpha < 0.75$  [2]. Although the bandwidth requirements aren't accelerating at the rate of Moore's law, they undoubtedly are increasing.

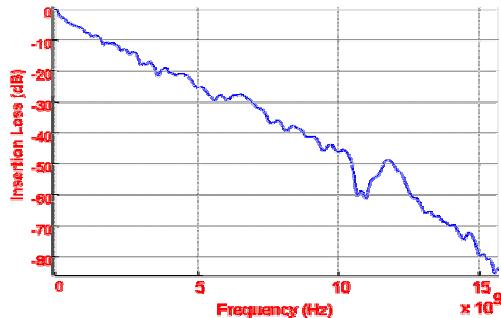
Figure 1 shows the history of computer Input/Output (I/O) protocols and the corresponding signaling rates in copper interconnects on Printed Circuit Boards (PCBs). Industry Standard Architecture (ISA) and Peripheral Component Interconnect (PCI) communication protocols dominated the 1980s and 1990s, respectively. PCI uses multi-drop bus architecture to communicate to multiple peripheral devices in computers. To comply with the increase in bandwidth through the 1990s PCI bus architecture has developed into faster and wider buses; however, wider buses not only increase silicon cost, but they also constrain space. Currently, the third-generation I/O protocol called PCI Express, developed by the Signal Interest Group (SIG) consortium, is becoming an industry standard [3]. PCI Express is expected to have a significant impact on interconnects in desktop computers since it

uses a point-to-point bus architecture along with a substantial increase in the data transfer rate, queuing technology, and transaction management. PCI Express is expected to increase transfer rates up to 10 GHz in the next 7-10 years. Beyond 10 GHz, copper interconnects on PCB made of FR4 material, become bandwidth limited due to frequency-dependent losses such as the skin effect in the conductors and the dielectric loss from the substrate material.



**Figure 1: Computer I/O architecture history and I/O roadmap**

Above 1 GHz, dielectric losses rapidly become larger than skin effect losses. Figure 2 shows simulated data of frequency-dependent loss for a 20-inch long electrical interconnect link for a situation found in a blade-based server configuration. The result includes the effect of packages, pad capacitance, via inductance, and connectors, in addition to the loss associated with the traces in FR4 material.



**Figure 2: Projected channel loss for electrical link**

At 10 GHz the simulation for this link predicts an insertion loss of ~50 dB in a standard FR4 material. It has been reported that replacing the FR4 material with newer laminates such as Rogers 4000 can extend the bandwidth of electrical interconnects by over two times, but also increase the cost by five times [4]. Alternatively, the insertion loss can be countered by using equalization, pre-emphasis, and multi-level encoding techniques [5]. For the situation in Figure 2, equalization implemented at the

transmitter extended the bandwidth from 4.5 Gb/s to 7.7 Gb/s. More complex equalization techniques are expected to extend the bandwidth limitation of electrical interconnects, but at the cost of increased transistor count for each of the I/O ports. The cost benefits of Moore's law, however, allow greater levels of processing complexity in each new generation of technology with no additional cost, making these solutions more easily implemented and ultimately cheaper in the near term. While frequency-dependent loss is considered the primary problem, the effects of reflections and crosstalk on the performance of electrical interconnect can pose other challenges for interconnect designers as the data rate increases beyond 10 GHz.

Optical solutions have been proposed for the upcoming electrical interconnect bottleneck for over 20 years [6]. If we focus on high-speed point-to-point computer I/O links, however, there are several important constraints on solving the problem. The primary and overriding constraint to solving the problem revolves around the cost of the optical components and packaging. The paramount importance of cost in the decision to implement an optical link, coupled with the focus on high-volume markets, leads naturally to the conclusion that high-performance, energy-efficient and low-cost optical and electronic components are crucial. Vertical Cavity Surface Emitting Lasers (VCSELs) have become the choice for optical interconnects due to their performance (high-modulation bandwidth, low power consumption, high efficiency) and manufacturing advantages (amenable to high-volume production, wafer-level testing, and ease of integration). The low power requirement of these VCSELs allows simple Complementary Metal-Oxide-Semiconductor (CMOS) driver circuits to be used, and as CMOS scaling continues, it is expected that CMOS-based optical interconnect driver and receiver circuits will improve in every aspect [7].

A widely accepted rule of thumb in the optical communications industry is that the cost of a module is roughly 33% components, 33% testing, and 33% packaging. In practice the assembly cost usually becomes the dominant cost of the link. Low-cost, reliable VCSELs must be complimented with very low-cost, highly manufacturable packaging processes, if the optical link cost is to be kept low.

In this paper we discuss two implementations of VCSEL-based optical interconnect technology that we are developing to address the packaging related costs. The first approach uses the Silicon Optical Bench (SiOB) technology and the second approach incorporates optical components onto a microprocessor style package. We discuss the benefits and challenges of each approach and discuss the results of the latter approach. We begin by

discussing several important considerations of optical link design in order to highlight some of the performance issues for Ultra-Short-Reach (USR) optical links.

## OPTOELECTRONIC SYSTEM DESIGN CONSIDERATIONS

The optical system incorporates the performance of the transmitter, the receiver, and the waveguide. Key considerations in any optical link system design are transmission distance, the optical transport medium (waveguide loss, dispersion, operating wavelength), coupling loss, Bit-Error Rate (BER), number of connectors in the system, source type, and receiver sensitivity. However, for USR applications, the transmission distance, which is normally the performance limiting factor in longer distance links, is of less importance since waveguide loss and dispersion are minimal. Therefore, for a given BER, optimum system design in USR applications focuses on the source power, coupling loss, connector loss, and receiver sensitivity. The cost/performance tradeoff for these links requires that the system be carefully designed to maximize performance while enabling low-cost packaging.

In the following two sections we describe in some detail the elements of the optical power budget, the factors affecting the receiver sensitivity, and the rise time budget for USR applications.

### Optical Power Budget

Calculating the optical link power budget is the first step towards designing an optical link. It is sum of the end-to-end optical loss in which the channel operates and meets all specifications. In the absence of significant waveguide propagation loss, Vertical Cavity Surface Emitting Lasers (VCSELs)/photodiodes to waveguides/fibers coupling loss and waveguide/fiber connectorization loss are dominant. Therefore, minimizing these losses has a significant impact on the system design cost since these losses are always counted relative to the VCSEL output power, and they affect the required input power at the receiver. Coupling losses are mainly affected by the mismatch of the VCSEL divergence angle and the numerical aperture (acceptance angle) of the waveguide or the fiber in order for most of the optical power to be imaged on the waveguide/fiber core. Detailed discussions of such optimization involving simulations and measurement are discussed later for the two proposed architectures. Typical connector losses for multimode fibers range from 0.5-1 dB whereas the connectorization loss for waveguide arrays used in the CPU-style package ranges from 1-2 dB. This means the connectorization of the small form factor Multi-Terminal (MT) connectors still needs optimization. If we succeed in minimizing the

coupling and connector losses, then we will be able to use VCSELs with very low output power (100s of  $\mu\text{W}$ ). As the bandwidth requirement of VCSELs increases, their apertures (Oxide) need to be reduced to minimize their capacitance. A consequence of this is the use of lower bias current and therefore lower output power, which not only lowers the transmitter's power consumption but also increases the reliability of VCSELs.

### Receiver Sensitivity

The minimum signal necessary to achieve a given BER is called sensitivity. Ultimately the sensitivity of the optical receiver is the key determining factor for the design of optical links; greater sensitivity yields longer links or lower launch power or a better BER. In order to calculate the sensitivity of an optical receiver, we have to choose a target BER or Signal to Noise Ratio (SNR). All possible noises in the system, including noise from the transmitter, waveguide, or fiber and noise generated in the photodiode and receiver circuitry, must be included in the SNR analysis. Relative Intensity Noise (RIN) from the VCSEL, modal, or mode selective noise due to the multimode behavior of the optical channel, as well as receiver electrical noise, are the major sources of noise. Here we estimate that the receiver circuit noise is the primary source of the overall noise and we discuss it in some detail using parameters relevant to the microprocessor style package. Analytically the receiver sensitivity is given by

$$10 \log \left( \frac{\left( i_n \text{SNR} + \left( \frac{V_{Th}}{Z_{TIA}} \right) (r_e + 1) \right)}{2R(r_e - 1)} \times 1000 \right) \quad \text{Equation 1}$$

where  $i_n$  is the input referred noise of the receiver,  $\text{SNR}$  is the digital signal to noise ratio,  $V_{Th}$  is the threshold voltage of the decision circuit,  $Z_{TIA}$  is the transimpedance gain,  $R$  is the responsivity of the photodiode, and  $r_e$  is the extinction ration of the VCSEL. The analytical calculation of sensitivity provides an understanding of the main noise contributors such as the photodetector and the Transimpedance Amplifier (TIA). Equation 3 is an analytical expression for the input referred noise in a CMOS-based receiver system [8].

$$\bar{i}_{n,TIA}^2 = \frac{4kT}{R_F} \cdot BW_1 + 2qI_G \cdot BW_1 + 4kT\Gamma \frac{(2\pi C_T)^2}{g_m} \cdot \frac{BW_2^3}{3} + \dots \quad \text{Equation 2}$$

This expression neglects 1/f as well other noises as these noise contributions have negligible effect at high-data-rate optical transmission.  $BW_1$  and  $BW_2$  are integrals related to the so called Personick bandwidth integrals [8].

In this equation,  $R_F$  is the feedback resistor of the TIA,  $I_G$  is the gate leakage current of the receiver front-end,  $\Gamma$  is the channel noise factor of the transistor associated to the short channel effects of transistors,  $C_T$  is the total front-end capacitance which is the sum of the photodetector, TIA, and any stray capacitance ( $C_T = C_{PD} + C_{TIA} + C_S$ ), and  $g_m$  is the transconductance of the front-end transistor. The capacitance of the receiver is a key factor affecting its performance. It can be shown easily that for optimized noise performance  $C_{PD} = C_{TIA}$  [8]. For a given data rate, noise optimization can also be obtained by manipulating the parameters ( $R_F$ ,  $g_m$ ,  $I_G$  and  $C_T$ ) involved in Equation 2. However, this is not easy as these quantities depend upon factors specific to CMOS technology. For the microprocessor-style package we estimate the receiver sensitivity for targeted BER of  $10^{-14}$  to be  $\sim 20$  dBm. This value allowed the data to be received error-free for the worst-case optical loss of -12 dB at >1 Gb/s. The system bandwidth is the convolution of the bandwidths of the transmitter ( $B_{Tx}$ ), the waveguide ( $B_{wg}$ ), and the receiver ( $B_{Rx}$ ), and it determines the maximum system response or bandwidth; it is described by Equation 3 below.

$$B_{Sys} = \frac{1}{1.1 \sqrt{\frac{1}{B_{Tx}^2} + \frac{1}{B_{wg}^2} + \frac{1}{B_{Rx}^2}}} \quad \text{Equation 3}$$

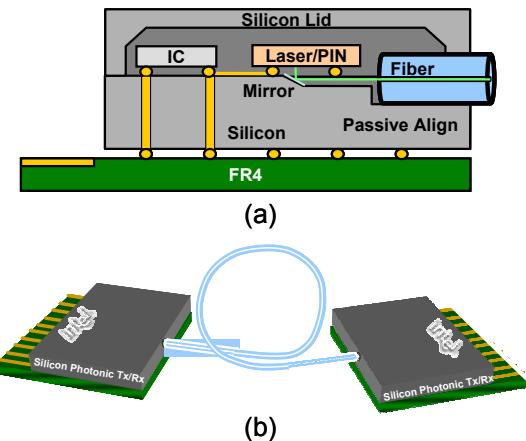
Due to the shorter distance of USR links, the system bandwidth is dominated by the bandwidth of the driver and the receiver.

## SILICON OPTICAL BENCH SOLUTION

The SiOB approach that we propose consists primarily of a patterned and etched silicon substrate as the assembly template for the integration of VCSELs, pin photodiodes, fibers, integrated electronics, and potentially a quasi-hermetic sealing lid. Variations on this theme have been proposed [9-11]. The advantage of a silicon optical bench approach is the ability to incorporate lithographically defined structures on the silicon substrate that can be used to enable passive alignment of various optical components, most especially the fiber. A passive alignment packaging technique eliminates the need for a precise, time-consuming, and ultimately expensive closed-loop procedure for the alignment of optical components. Coupled with the inherently low-cost manufacturing of silicon, due to both the built-in infrastructure and also the economies of scale, the use of passive alignment techniques to assemble optical modules creates the ability to package very low-cost optical assemblies. An additional advantage of the silicon optical bench approach, is the ability to integrate other silicon functionality onto the substrate. As shown in Figure 3

below, our proposal is to use the silicon as a packaging substrate for VCSEL and pin photodiode optical modules.

We envision the silicon substrate containing driver and receiver ICs with high-speed microstrip or co-planar transmission lines to operate at high frequency, and thru vias to connect to the FR4 board underneath. In this configuration, connectorization is created by mating the FR4 board with a connector on the server blade. This IC block could eventually become the network processor itself, although this is a large departure from current techniques and the integrated approach in the next section might be more amenable to CPU integration.



**Figure 3: Silicon optical bench approach**

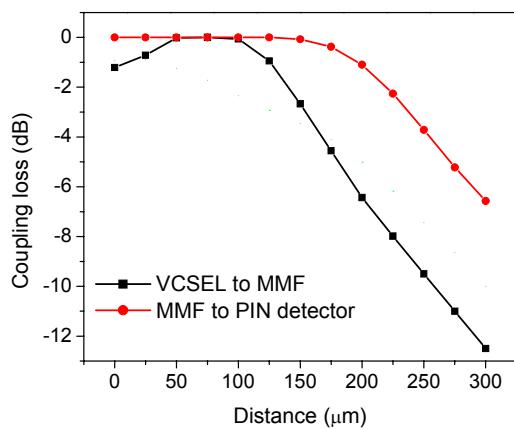
## Technical Considerations

The most important technical concern that must be addressed in order to make this SiOB vision a reality is to ensure low loss coupling between the VCSEL and fiber and between the fiber and photodiode. There are two factors involved in this technical evaluation: the inherent coupling loss associated with the mode profile in the constituent components and the tolerance to misalignment of the optical system. In order to keep the cost low, the required alignment precision must be kept at an easily achievable value.

### Optical Mode Matching

There are three prime candidates for the optical channel; Single-Mode glass Fiber (SMF), Multi-Mode glass Fiber (MMF), and Plastic Optical Fiber (POF). Representative dimensions of core and cladding are approximately 8  $\mu\text{m}$  / 125  $\mu\text{m}$  for SMF, 50  $\mu\text{m}$  / 125  $\mu\text{m}$  for MMF, and 125  $\mu\text{m}$  / 500  $\mu\text{m}$  for POF. If the aperture of the multi-mode VCSEL is assumed to be 10  $\mu\text{m}$ , and some other simplifying assumptions are made regarding the mode profile, then the coupling loss associated with each of these fibers can be calculated. If the laser aperture to fiber aperture distance is  $\sim 150$   $\mu\text{m}$ , then the associated coupling loss is  $\sim 14$  dB for SMF,  $\sim 3$  dB for MMF and

~0 dB for POF. In the case of fiber coupling to the pin photodiode, the coupling loss for both SMF and MMF are <1 dB until ~150 μm, while the coupling loss for the POF could be as large as 4 dB even for butt coupling. Here we assume that the pin photodiode aperture is circular and 80 μm in diameter. Clearly there is a tradeoff in fiber aperture between the coupling efficiency at the transmitter and receiver sides of the link, and MMF is the best choice. Figure 4 shows the simulated coupling loss versus optical path length for the case where MMF is used for the link. The VCSEL coupling loss is ~1.2 dB for butt coupling due to the mode mismatch since the MMF can support only a limited number of guided modes. As the distance increases, the coupling loss decreases because the VCSEL mode size becomes larger and the overlap between the VCSEL modes and MMF modes is better. At an optimal distance of ~75 μm between the VCSEL and the MMF, the coupling loss is almost zero. As the distance is further increased, the coupling loss increases as the VCSEL mode size exceeds the MMF core.



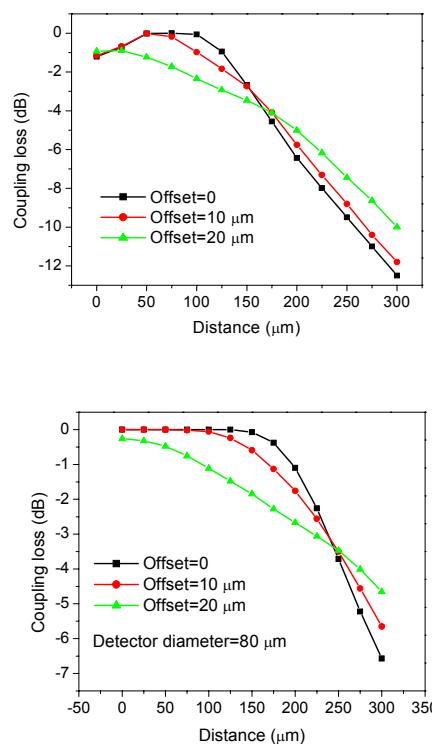
**Figure 4: Simulated coupling loss for VCSEL to multi-mode fiber and multi-mode fiber to pin photodiode**

#### Optical Alignment Tolerance

The other technical issue that must be addressed is the tolerance to misalignment of the optical components, which depends strongly upon the physical distance between the components. In this optical system the beams will diverge quickly, and low coupling losses require short distances between components as well as tightly parallel apertures. The length of the optical path has two primary components: the horizontal and vertical distance. The vertical distance is primarily determined in this system by the divergence of the optical beam in order to alleviate shadowing of the light path by the die. The horizontal distance is determined both by the location of the optical aperture with respect to the die edge and also

by the assembly tolerance for distance between the die edge and the fiber facet. For a 45-degree coupling mirror and a VCSEL with a divergence angle of ~14° (typical for an 850 nm MM VCSEL), the optical path length will be ~150 μm; with a similar length for the receive path. Using these values, the sensitivity of the optical path to both angular and lateral misalignment, due to either the die and fiber placement process or the cleave angle of the glass fiber, can be calculated. Our analysis shows that at 150 μm, a tilt angle of ±2° results in < 1 dB of excess loss.

Figure 5a shows the sensitivity of the VCSEL-MMF system to lateral misalignment and Figure 5b the sensitivity of the MMF to photodiode misalignment. In both cases, the modeling shows that lateral misalignment of 10 μm or less results in < 1 dB of additional coupling loss.



**Figure 5: The effect of lateral misalignment upon the coupling loss for a) a 10 μm aperture MM 850 nm VCSEL to a MMF, and b) a MMF to an 80 μm diameter pin photodiode**

The nominal coupling loss will then be ~4 dB for the transmitter (3 dB mode-matching + 1 dB misalignment) and ~1 dB at the receiver (0.5 dB mode-matching + 0.5 dB misalignment) for a total coupling loss of 5 dB.

Electrical design of the connection between either the driver IC or the TIA will not be considered here, as these issues are addressable with standard electrical routing

techniques, such as microstrip lines and ground planes to isolate highly sensitive signals from any EMI that may be present in the environment. Silicon optical bench components have been shown to operate at frequencies greater than 20 GHz [10], and there is a potential to scale them to higher frequencies.

## Processing Challenges

There are two processing challenges that will be considered: the formation of the 45 degree coupling mirror and the formation and integration of the trench for passive alignment of the fiber to the optical axis.

There are several techniques for the formation of these mirrors on a silicon surface, the two most likely candidates are grey scale mask formation followed by dry etching [12] and wet etching to expose crystallographic planes [13]. The advantage of the wet etch approach is that the variation of mirror angle due to process variation is expected to be very small, < 0.5 degrees, whereas the grey scale approach, while capable of creating complex mirror surfaces to focus the light and lower the coupling loss, will have a greater process variation.

The creation of the fiber alignment trench can also be done by either dry or wet etch methods. For a dry etch depth of 80  $\mu\text{m}$ , the approximate sum of  $\frac{1}{2}$  the fiber diameter + vertical spacing, a 10% etch uniformity would be only 8  $\mu\text{m}$ , well within the required tolerance. As shown in the previous section, our analysis shows that the lateral placement tolerance of both the transmit and receive sub-assemblies show minimal degradation of coupling efficiency for misalignment of  $\leq 10 \mu\text{m}$ . A wet etch can be designed that will create both the 45-degree coupling mirror and an alignment trench for the fiber simultaneously, reducing the required processing steps and hence the cost.

## Assembly Challenges

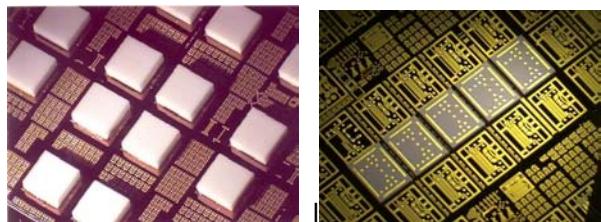
The assembly of these modules has five distinct phases: VCSEL/photodiode attach, passive fiber attach, lid attach, integrated circuit physical/electrical attach, and FR4 board mounting. We do not address the IC attach and electrical connection nor the FR4 mounting as they are similar to currently used techniques.

The VCSEL/photodiode die attach is done active side down with either of two approaches: Au thermo-compression bonding [14] or a AuSn solder approach [15]. Either system relies upon the alignment of fiducials on both the die and the substrate in order to achieve the desired placement accuracy. While the solder approach has the advantage of an aligning restorative force under certain conditions, in order to remove surface oxide, the solder re-flow must be done in a controlled atmosphere, which requires a more expensive pick and place machine.

Placement accuracies below 1  $\mu\text{m}$   $3\sigma$  have been reported, although with very expensive and slow pick and place machines. Die placement accuracies of  $\pm 5 \mu\text{m}$  are all that should be required for this application.

The placement accuracy of the fiber is determined by the etched dimensions of the alignment trench and can be determined to at least  $\pm 1 \mu\text{m}$  in a dry etch process and to a much higher degree of precision in a crystallographic wet etch process. Since the fiber will be held in place by UV or thermal cured epoxy with no active alignment necessary, the alignment tolerance will be completely determined in the transverse dimension by the etched trench. The alignment of the fiber aperture along the optical axis will be accomplished with the use of an etch stop; initial results indicate placement tolerances of  $\leq 10 \mu\text{m}$ .

Recently, two types of Mechanical Electro-Mechanical Systems (MEMS) package lids have been demonstrated by Intel that may be applicable to silicon photonics. The first is a ceramic lid with a glass frit seal ring, as shown in Figure 6a. In this case, a ceramic lid was placed over the MEMS component and heated to 350°C in order to reflow the glass frit ring, thereby sealing the devices in a hermetic cavity. The signal feedthroughs are lateral (i.e., in the plane of the wafer) and extend to the perimeter of the die for wirebonding. The second package, Figure 6b, is a ceramic lid containing metal-filled vias and a solder seal ring. In this case, the die was mounted by a flip-chip process rather than wirebonding.



**Figure 6: A photograph of a ceramic lid package onto a MEMS wafer a) for lateral electrical contact, and b) for through lid electrical contact**

Either of these packages may potentially be suitable for packaging optical devices. They are considered hermetic, since low-permeability and low-outgassing materials were used. Because of the thickness and reflowing property of the sealing materials, they are capable of sealing over underlying topography on the MEMS wafer (6  $\mu\text{m}$ ) and may be able to accommodate larger topographies. The costs for the individual ceramic packages range from five to ten cents apiece, which is very competitive when compared to other MEMS products on the market. The placement accuracy of the lid can be extremely coarse, with the only limitation on the process being the potential

impact on the previous optical alignments and the process thermal stack-up.

## Next Steps

The great flexibility of silicon allows the potential future integration of additional functionality onto a similar silicon substrate. This functionality could incorporate either or both MEMS and optical devices resulting in Coarse Wavelength Division Multiplexing (CWDM) or Wavelength Division Multiplexing (WDM) transmitters and receivers or even remote access to highly sensitive Radio-Frequency (RF) MEMS components.

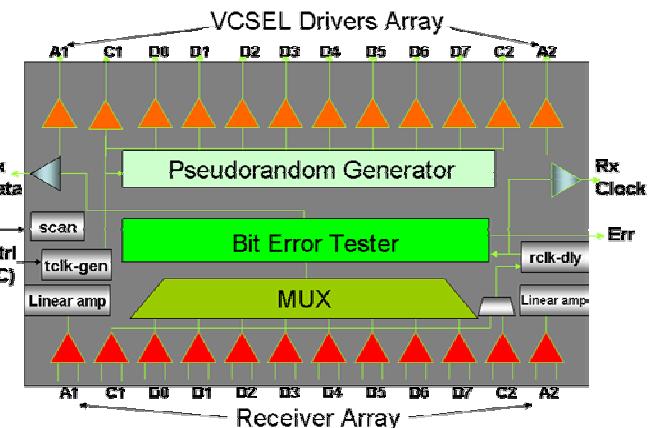
## MICROPROCESSOR PACKAGE INTEGRATED OPTICAL SOLUTION

In this section we describe the development of a high-speed, 12-channel parallel optical transceiver package used to demonstrate the viability of chip-to-chip optical I/O in Very Large Scale Integration (VLSI) circuits. The package concept has been developed to be compatible with the current microprocessor package technology and at the same time allow the integration of low-cost, high-performance optical components. VCSELs, pin photodetectors, polymer waveguide arrays with Multi-Terminal (MT) connectors as well as CMOS transceiver chips were heterogeneously integrated on a standard microprocessor Flip-Chip Pin Grid Array (FCPGA) substrate. The main advantages of this approach include (1) compatibility with the IC packaging industry, (2) parallel transmission architecture that increases throughput, (3) an MT optical port that alleviates distance limitations between two packages (multiple applications), (4) passive alignment, and (5) contains self-testing capability circuit. We discuss the CMOS chip architecture and the package design and assembly as well as the characterization results.

## Transceiver Chip Architecture

The optoelectronic transceiver chip circuit was designed and fabricated in a  $0.18\text{ }\mu\text{m}$  CMOS process technology, and it contains all the circuits needed for use in optical link communication. Figure 7 shows the schematic of the chip architecture. The key units of the test chip are VCSEL drivers, TIAs and Limiting Amplifiers (LIAs), a clock unit, a tester unit and a scan chain for testing. The signal and bias currents of the VCSEL driver are separately programmable through the scan chain. The two outer most channels in Figure 7 (Ch-A1 and Ch-A2) provide DC signals that were intended to be used for optical alignment of optoelectronic chips with waveguide arrays. Two inner channels (Ch-C1 and Ch-C2) generate clock signals, and the remaining eight channels were used to transmit  $2^{15}-1$  Pseudo-Random Bit Sequence (PRBS) Non-Return-to-Zero (NRZ) data signals to drive the

VCSEL arrays. The VCSEL drivers are capable of sourcing up to a  $16\text{mA}/\text{channel}$ .



**Figure 7: CMOS transceiver chip architecture**

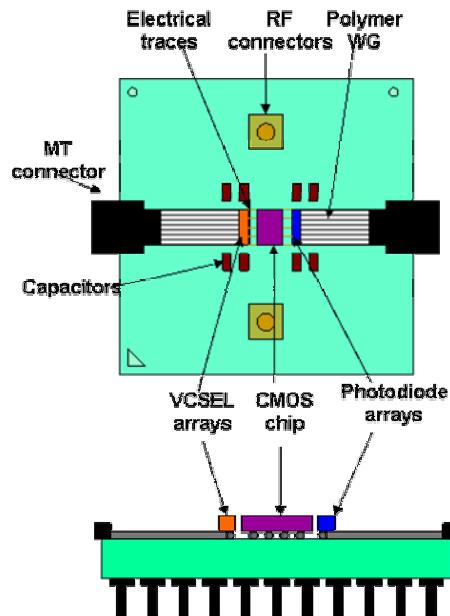
The 12-channel receiver array circuitry consists of TIAs and LIAs. The TIA has a  $2.5\text{ k}\Omega$  feedback resistor and it was designed to handle a  $500\text{ fF}$  total capacitance, which comes from the bumps, Electrostatic Discharge (ESD) diodes, and parasitic capacitance of the photodetector.

## Package Architecture and Design

The package design includes the mechanical, electrical, and optical design of the package. Figure 8 shows a cartoon for the architecture and physical layout of the top side of FCPGA transceiver package. The 6-layer organic substrate has a dimension of  $35\times 35\text{ mm}^2$ . The physical layout of the package includes VCSEL and photodiode array chips, MT connectorized polymer waveguide arrays, decoupling capacitors, and miniature RF connectors, all attached to a common organic substrate. MT fiber optic connectors at the edge of the package are used for easy interface with other modules and system-level testing.

## Electrical

The electrical design of the package involves the routing of signal and power lines as well the use of decoupling capacitors for noise reduction. All the electrical lines on the substrate are routed as controlled impedance ( $50\text{ ohm}$ ,  $2.5\text{ GHz}$ , microstrip lines). The Cu traces used to interface with optoelectronic chips were routed on the top surface of the FCPGA package to maintain signal integrity.



**Figure 8: Top and side view of the physical placements of optical and electrical components on FCPGA package**

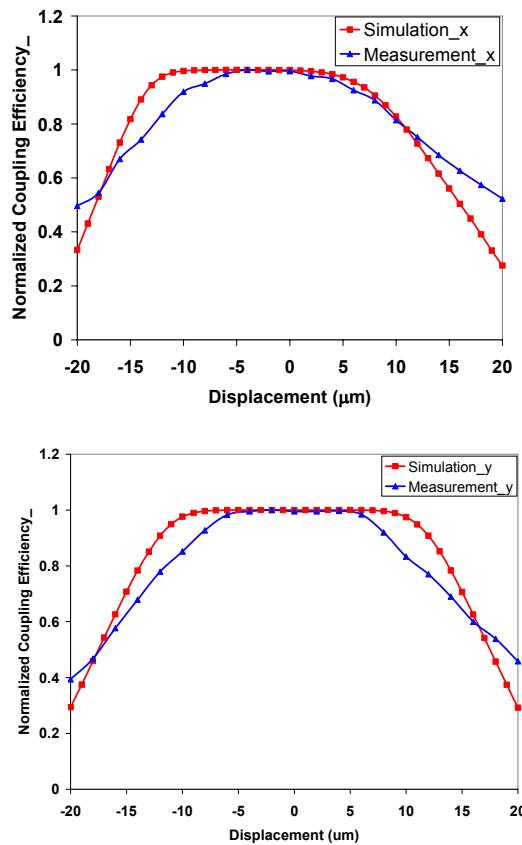
The microstrip lines originating from the driver and receiver section of the CMOS chip were equalized to avoid skew between clock and data for the source synchronous architecture. The CMOS transceiver chip is in close proximity to the optoelectronic array chips to minimize frequency-dependent loss on the microstrip traces.

### Optical

The optical assembly on the FCPGA substrate has a transmitter and a receiver portion that are symmetrically situated with respect to the CMOS transceiver chip at the center of the substrate, as shown in Figure 8. This arrangement allows more than two chips to communicate simultaneously in a cascaded manner. We used GaAs-based, oxide-confined, top-emitting VCSELs and GaAs pin photodiode arrays with coplanar contacts. The polymer waveguide device consists of a 45 degree coupling mirror on one end and a modified MT connector on the other. The waveguide array has a core dimension of  $35 \times 35 \mu\text{m}^2$  and was fabricated from acrylate, using photobleach processing. We used polymer waveguides due to their potential for high-volume, low-cost production. The acrylate-based multimode polymer waveguides are known for their low loss (0.08 dB/cm), ease of integration, best system performance, and manufacturability. The detailed processing can be found in [16]. The transmitter includes a VCSEL optical source array and a polymer waveguide array. VCSEL arrays are flip-chip bonded on the substrate and coupled to polymer waveguides with 45-degree metal mirrors to direct light at

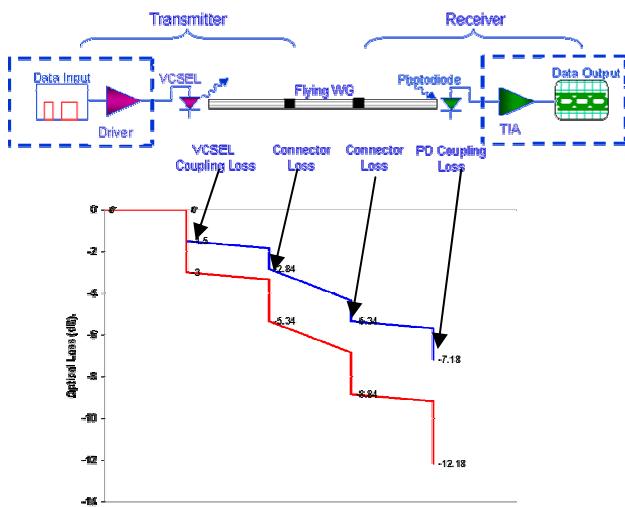
right angles for transmission through the waveguide. Similarly, the receiver consists of identical optical waveguide assembly to the transmitter section, with a high-speed GaAs photodiode array replacing the VCSEL array.

As described earlier, the optical coupling efficiencies at the ends of the polymer waveguides are critical parameters. Therefore, we conducted experiments and simulations to determine the optical misalignment tolerance of the system in the lateral x (transverse to the waveguide) and y (along the axis of the waveguide) directions. Figure 9 shows these results. The rectangular and triangular plots are simulation and measured data, respectively. During the experiment, the waveguide was scanned over the VCSEL along both the x and y directions of the waveguide. The simulation results are in reasonable agreement with the experimental data. For 1 dB half-width ( $\sim 80\%$  efficiency from maximum coupling), a misalignment tolerance in excess of  $\pm 10 \mu\text{m}$  was simulated and measured for both x and y directions. This tolerance range allowed passive alignment of the VCSEL and photodiode dies to the waveguide arrays.



**Figure 9: VCSEL-waveguide misalignment tolerances in the transverse (x) and axial (y) directions**

Figure 10a is a schematic of the end-to-end optical link from the transmitter to the receiver showing the interfaces where optical losses occurred. Figure 10b details the optical losses at each interface of the optical link. The largest loss contributor in this optical link is a coupling loss from/to VCSELs/photodiodes to waveguides, which ranges from 1.5-3 dB, and the smallest contributor is the waveguide loss which, for the current case, is 0.11 dB/cm @850 nm. In a CPU package where the distances involved are less than two centimeters, such waveguide loss is minimal. MT connectorized multimode fiber array jumpers could be used to reduce the propagation loss in the polymer waveguide jumper used for the measurement. Based on various parameters of individual optical components and optical simulations, the total optical loss budget for the complete link was calculated to be between 7 (best case) and 12 dB (worst case) as shown in Figure 10b.

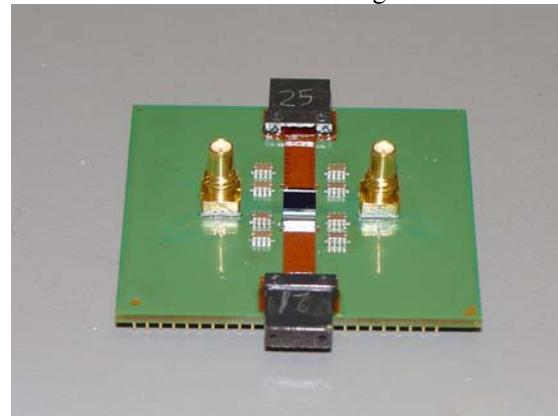


**Figure 10: (a) Schematic showing the optical transmission link and (b) optical power loss of the link**

## Optoelectronic Assembly

The process flow for the assembly of the optical package was important because of the temperature sensitivity of individual optical components. The flow starts with a bare fabricated FCPGA substrate that contains all routed signal and power lines as well as all the electrical contact pads at the surface of the substrate. Electrical and optical components were picked up and aligned with fiducial marks on the substrate and bonded. First, the decoupling capacitors and the silicon die were soldered onto the substrate using a flux. Then the package was de-fluxed and cleaned to prevent contamination of the waveguide. The preassembled polymer waveguide arrays with 45-degree mirrors and MT connectors were mounted on to the substrate and attached using an ultraviolet (UV) curable epoxy. Flux-less bonding was used to attach the

optoelectronic chips such as the VCSEL and photodiode arrays. Flux-less bonding has been widely used in the optoelectronics industry because flux residues will contaminate optical paths and cause optical loss and possible reliability problems. A gold stud bumping technique was used to form Au stud bumps on the optoelectronic dies. The active areas of optoelectronic chips were aligned to the waveguide cores on the substrate and bonded on the substrate. The completed transceiver module is shown in Figure 11.



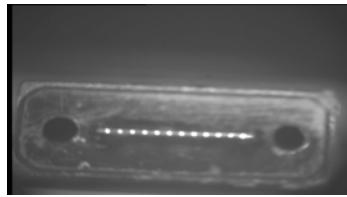
**Figure 11: Completed prototype package for chip-to-chip optical data communication**

## Optical Characterization

Characterization of the optical link was performed by mounting two optical packages on a test board and connecting them with a polymer waveguide jumper. Optical transmission tests were performed using programmable settings of signal and bias currents in the VCSEL drivers. These high-speed output data and clock signals were read out from RF connectors on the top of the package and displayed on oscilloscope. Also, bit-error signals were displayed on Liquid Crystal Displays (LCD).

### Optical DC Characterization

Optical DC characterization was performed on 20 prototype samples out of which more than 90% were fully functional. Figure 12 shows a photograph of the actual MT connector output taken using an Infrared (IR) camera where all 12 channels are functional. The average threshold current for all the channels was 1.5 mA with a slope efficiency of 0.2 W/A for the waveguide coupled optical power.



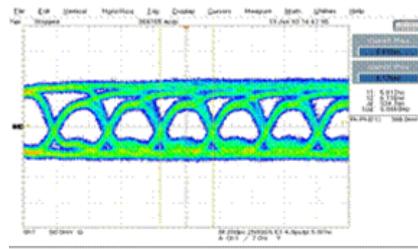
**Figure 12: Light output from 1x12 MT connector for fully assembled package**

The average optical loss and crosstalk measured for transmitter channels were -6 dB and -25 dB, respectively, and it was within the calculated power budget range. The crosstalk is primarily caused by light coupled to the waveguide from adjacent VCSELs in the array. The kind of crosstalk can be eliminated by using VCSELs that have a low divergence angle. In fact, experiments indicated that polymer waveguides of the type used here have shown an impressive crosstalk of -30 dB for 10  $\mu\text{m}$  waveguide spacing [16]. Typical crosstalk values for 250  $\mu\text{m}$  spacing waveguides is better than -40 dB.

### High-speed Optical Characterization

#### Transmitter

VCSELs were biased above threshold to avoid turn on delay and overshoot. The bias current,  $I_{\text{Bias}}$ , was selected within 1 mA above the threshold current,  $I_{\text{Th}}$ , and the modulation current,  $I_{\text{Mod}}$ , was selected within the linear region of the LI curve. Higher modulation currents were chosen to maximize the extinction ratio. On the average, typical  $I_{\text{Bias}}$  and  $I_{\text{Mod}}$  were 2.5 mA and 6 mA, respectively. Figure 13 shows the optical eye diagram of the transmitter at 3 Gb/s data rate using a  $2^{15}-1$  PRBS data pattern that is generated by the on-chip test circuits. The measurement showed a rise and fall time of 110 ps and 130 ps, respectively with a peak-to-peak jitter of 100 ps. The power consumption for a single transmitter channel was 13 mW. The received electrical power was -11 dBm, and it is consistent with the calculated optical power budget.



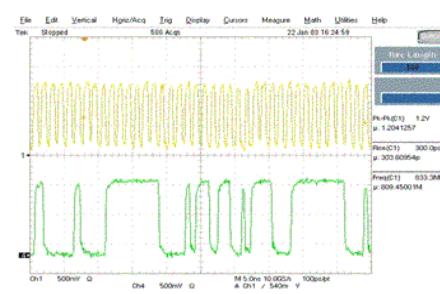
**Figure 13: Transmitter eye at 3 Gb/s**

The eye patterns showed asymmetry and increased jitter. The asymmetry is a result of the difference in rise and fall times that may have been caused by the driver circuit, and the increased jitter is a combination of reflection from impedance mismatch and reduced SNR for the data rate. The slow tail observed in the optical eye pattern is likely

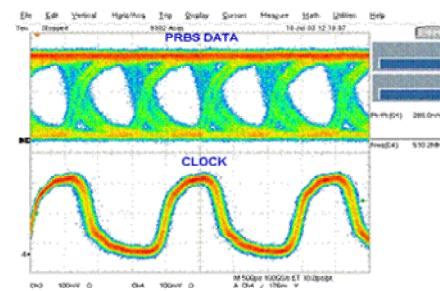
to be caused by long recombination lifetime (spontaneous emission) of carriers diffusing laterally during turn off.

#### Optical Transmission Link

The complete optical transmission link involves the transmitter and receiver packages connected with flying polymer waveguides through their respective MT-type connector optical ports. Including the waveguide jumper used to connect the two chips, the total optical link length was about 20 cm. However, this distance could be extended significantly using standard multimode fibers without affecting the integrity of the received optical signal.



(a)



(b)

**Figure: 14 (a) received clock and data waveforms at 1.7 Gb/s, and (b) received clock and eye diagram data at 1 Gb/s**

Figure 14a shows the received clock and  $2^{15}-1$  PRBS data waveforms at 1.7 Gb/s, and Figure 14b shows the eye diagram measurement for the complete link. In both cases the Oscilloscope display shows received data along with a clock for triggering, since source synchronous architecture is used. As the clock speed increases even the smallest difference in path length between clock and data causes misalignment between clock and data, deteriorating the received data. As a result, the rise and fall times as well as the peak-to-peak jitter for the received waveform increased to 220 ps, 260 ps, and 330 ps, respectively. The overall BER at 1 Gb/s was estimated to be less than  $10^{-14}$ .

## Future Directions

The package concept implemented in this section is developed to have the minimum impact on the current CPU packaging technology. In the current architecture, the transceiver chip used an integrated driver and receiver circuitry to reduce power that would have been lost in the output buffers of each component. Similarly, the optical-to-electrical interface of the current approach will benefit from the integration of optoelectronic components on the CMOS chip. Heterogeneous integration of efficient materials such as GaAs and Ge with CMOS chips is an attractive solution, if it can be implemented successfully. Approaches such as epitaxial liftoff and waferbonding are gaining more popularity since they have the potential for wafer-level manufacturing. Integration of the polymer waveguides onto the substrate will also be investigated in future work.

## SUMMARY

In this paper, we addressed the issues that electrical interconnects will encounter as the data transfer rate increases beyond 10 GHz. We discussed two possible options for high-performance and cost-effective optical interconnect solutions. The optical design, processing and assembly challenges of the SiOB approach were discussed in some detail. This approach allows passive alignment of optical components using lithographic definition of fine structures on the Si substrate and therefore is expected to be low cost. We also discussed the system architecture and design of a 1x12 optical transceiver recently developed at Intel using a hybrid integration of components on a microprocessor-style package. Such an approach will have minimum impact on the existing motherboard technology and therefore reduces cost. Using the latter approach we demonstrated 3 Gb/s transmitter optical eye and 1 Gb/s error-free transmission.

We believe that the cost of optical interconnects for USR applications is the most significant impediment to their implementation. In addition to cost reduction in optical components and packaging, there is also a cost associated with altering the microprocessor package. An entire infrastructure of suppliers, vendors, and sub-contractors would need to be developed, and standard parts would need to be agreed upon—an enormous undertaking. The economics of the market would dictate that in order to implement this new and unproven technology it would not only have to provide a current performance benefit, it would have to be a sustainable one and cost less than existing solutions in already proven technology. We believe that these two approaches show promise to overcome these significant market hurdles.

## ACKNOWLEDGMENTS

We gratefully acknowledge Douglas Stunkard for developing testing software and Julie Mckenney for layout design. We also acknowledge Assia Barkai and Rami Cohen for all of their understanding and insight into SiOB processing-related issues. Guoying Ding, Hai-Feng Liu, and Ruolin Li have been helpful for various discussions on the SiOB approach.

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# On-Chip Optical Interconnects

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Index words: interconnect, integrated circuit, optical

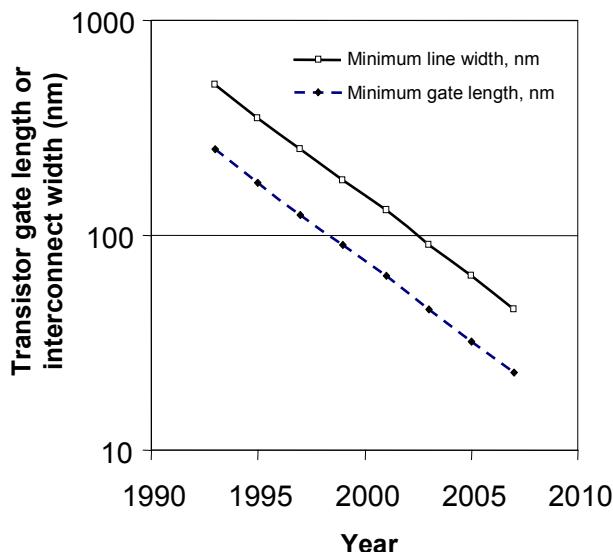
## ABSTRACT

Gordon Moore's prediction over thirty years ago that the number of transistors per Integrated Circuit (IC) would double every two years has driven a dramatic scaling in feature sizes, which has had a negative impact on the resistance of metal interconnects. The recent conversion of the IC industry from aluminum to copper interconnects provided a one-time improvement of resistivity and electromigration, but it does not resolve the degradation of interconnect delay with further scaling. Furthermore, numerous other issues still remain with metal interconnects, such as power consumption and Electromagnetic Interference (EMI). Consequently, several researchers are considering the possibility of using photonics to replace metal interconnects. Optical interconnects offer the promise of decreasing interconnect delays and providing higher bandwidth to keep pace with transistor speed improvements, while potentially lowering power consumption and being resistant to EMI.

In this paper, potential on-chip applications of optical interconnects to mitigate the limitations of metal interconnects are discussed. In particular, we compare the performance and cost of optical interconnects and Cu interconnects for clock distribution and intrachip global signaling. Our analysis did not reveal significant advantages for on-die clock distribution using optical interconnects as compared to conventional clock distribution. For signaling, it was found that optical interconnects, in conjunction with wavelength division multiplexing, can potentially provide a low latency-high bandwidth option.

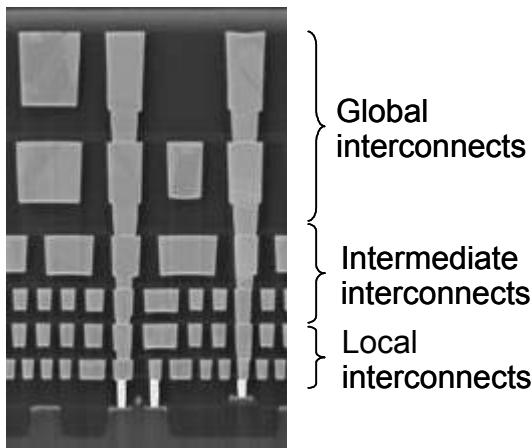
## INTRODUCTION

In 1965 Gordon Moore observed that the number of transistors in an Integrated Circuit (IC) was doubling every two years [1]. He predicted that this trend would continue, and it is now clear that what has become known as Moore's Law has been remarkably accurate. Recently, Sery [2] has estimated that for Intel architecture microprocessors, the transistor count will exceed one billion between the years 2005 and 2007. The dramatic increase in the number of transistors in microprocessors of approximately constant size has been enabled by the shrinkage of transistor and interconnect dimensions over time. Figure 1 shows the minimum interconnect width and the smallest transistor gate length for the last ten years, as well as the expected values for the near future. It can be observed that both physical dimensions scale maintaining their ratio approximately constant.



**Figure 1: Comparison of the trends for the smallest transistor gate length and minimum interconnect width**

Today, all leading-edge Intel architecture microprocessors have transistor gate lengths and minimum line widths that are smaller than 100 nm. Interconnect scaling has been insufficient to provide the necessary connections required by an exponentially growing transistor count, which has resulted in an increasing number of metal layers. Figure 2 shows a cross-sectional micrograph of an IC with 6 metal layers manufactured on 0.13 µm technology.

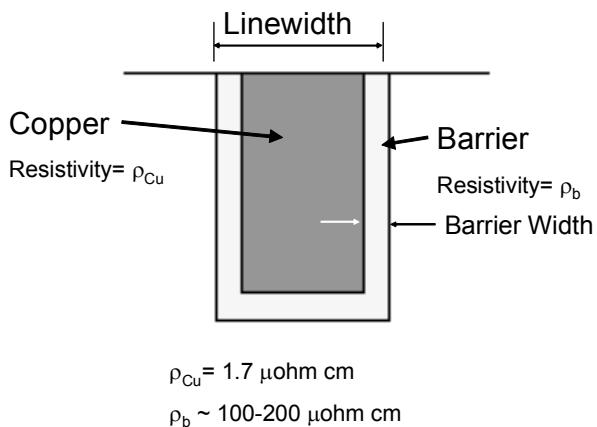


**Figure 2: Cross-sectional micrograph of a 6-metal layer IC manufactured on 0.13 µm technology showing the typical decrease of interconnect dimensions for the layers that are closer to the Si devices**

Unlike transistors, for which performance improves with scaling [3], the delay of interconnects increases with scaling, which is discussed later in this paper. For the copper interconnects used in today's microprocessors,

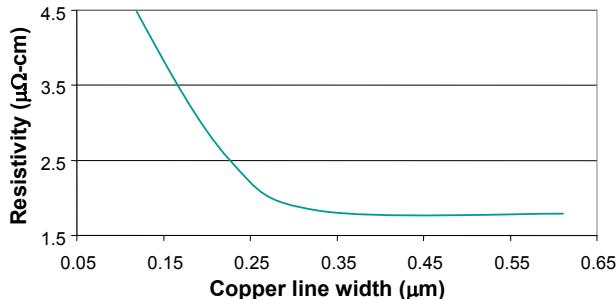
delay increases with increasing resistance and capacitance, which explains the industry-wide efforts towards decreasing the dielectric constant of the dielectrics and the resistance of the metals that form the interconnect.

A schematic of an interconnect cross section is shown in Figure 3. Since the barrier layer has a high resistance compared to Cu, it is desirable to decrease its thickness to maximize the Cu cross-sectional area. Scaling the dimensions of the interconnects while the barrier thickness remains constant would result in an increase in the effective resistivity, which would degrade the delay of the interconnects. The effective resistivity is defined as the resistance per unit length times the total cross-sectional area (i.e., including the areas used by the Cu and the barrier). In this scenario, the resistance of the line will eventually be dominated by that of the high-resistivity barrier. If the barrier thickness is scaled proportionally to the line width, then the effective resistivity of interconnects is not further affected by the barrier (notwithstanding the effects of the barrier on surface scattering), which is the motivation for the significant efforts to scale the barrier thickness.



**Figure 3: Schematic cross-section of a Cu interconnect showing the metal and the barrier. Presently, the width of the Cu line scales, but the barrier thickness is approximately constant.**

In addition, as the width of the copper line shrinks, the resistivity of copper starts to increase due to increased scattering at interfaces [4], which appears to be dominated by surface scattering. The effect of scattering typically becomes important below 50 nm widths and is strongly dependent on deposition techniques [4,5]. The overall impact of scattering on the effective resistivity is shown in Figure 4. It is relevant to note that even in the case of a scaled barrier, the resistivity increases as dimensions decrease.



**Figure 4: Schematic diagram showing the increase in the effective resistivity of copper as a function of Cu width (i.e., not including the barrier thickness)**

In principle, if the effective resistivity of interconnects is maintained constant, scaling all their dimensions (width, thickness, and length) by the same factor would result in a constant point-to-point latency. Even in this idealized case, since the clock frequencies are increasing, a constant interconnect latency would be equivalent to a decreasing interconnect performance.

Interconnects are typically divided into three groups: global, intermediate, and local interconnects (Figure 2). Global interconnects have the largest pitch and provide communication between large functional blocks, while local interconnects have the smallest pitch and are typically dedicated to interconnections within logic units. Intermediate interconnects have dimensions that are between those of global and local interconnects. A key difference between local and global interconnects is that the length of the former scales with technology node, while for the latter the length is approximately constant. Global interconnect lengths are linked to the die size, which has remained nearly constant at approximately 1 cm<sup>2</sup> for desktop microprocessors. Because local interconnects have smaller dimensions than intermediate and global ones, they are more adversely affected by scattering-induced resistivity increases and non-scaling barriers. On the other hand, global interconnects are also adversely affected by scaling because their lengths do not decrease with technology node. Decreases in the dielectric constant will partially mitigate the resistivity-related degradation of interconnect delay. In summary, the delay of both global and local interconnects is degrading in absolute and relative terms with technology node.

To offset the decrease in interconnect performance with scaling, there are several options. The latency of interconnects can be reduced by decreasing the distance between repeaters (simple one- or two-stage drivers) along the interconnect lengths. The drawback of repeaters is that they take up die area, consume power, and make wire routing increasingly more difficult. Another option is to not scale the upper metal layers in the interconnect

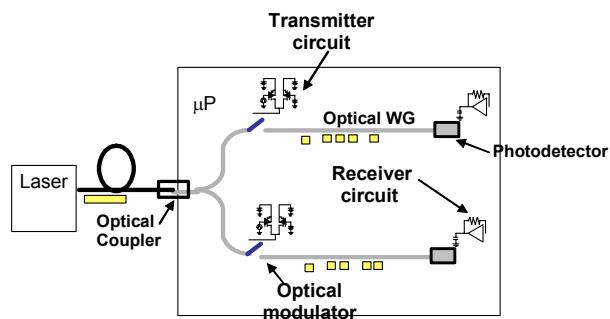
stack. The consequence of this would be poor bandwidth density compared to scaled interconnects, which would result in a rapid increase in the number of metal layers. The additional metal layers add processing steps, which increase cost and decrease the die yield. Additionally, it is unknown how the addition of a significant number of metal layers will affect the reliability of the package/chip interface and other thermal-mechanical issues.

Two of the most important and performance-demanding applications of interconnects in microprocessors are signaling and clock distribution, for which optical interconnects have been considered by researchers both in industry and in academia. In order to compare interconnect schemes, we developed simple benchmark metrics. The comparison for clock distribution is based on the results presented in Reference 6; in this paper we focus on skew and jitter as metrics. For signaling, four areas were benchmarked: signal delay normalized by clock cycle, available bandwidth per unit area or bandwidth density, bandwidth density/delay ratio, and cost.

## CONCEPTUAL OPTICAL SYSTEM

### Optical Signaling

In order to model the expected performance of an optical system used for signaling, a hypothetical optical system is proposed in Figure 5. In this system, an external continuous wave laser is used as the optical power supply.



**Figure 5: Hypothetical on-chip optical system for signaling**

The light is then coupled into an on-die waveguide that distributes light over the entire die. Light is split and routed into a given optical interconnect and converted into data using an optical modulator that is controlled by an electrical signal generated by a driver. This architecture produces optical pulses (signals) driven by a standard Complementary Metal-Oxide-Semiconductor (CMOS) driver. Light is then routed to a CMOS photodetector on the other end of the interconnect that converts the light into a photocurrent. The photocurrent is

then transformed into a conventional digital voltage signal by a Transimpedance Amplifier (TIA). Many such interconnects would be fabricated on the chip, but their number is limited by available optical power, waveguide spacing limitations, detector and modulator area, as well as routing constraints.

There are several important requirements for such an optical interconnect system to be feasible. The main requirements are performance related and include signal delays and high bandwidths that can compete with Cu interconnects in all future technology nodes. It is important to mention that the delay of optical interconnects has several contributions, including those arising from the modulator, the propagation delay in the waveguide, the detector, and the TIA.

Although these components have not all been fully realized, considerable efforts have been reported in the literature. Our intent is not to present details of the components necessary to build a working system, but to evaluate the potential performance of a conceptual optical system. In addition, we present a limited number of experimental results to demonstrate the feasibility of some of the key components.

To evaluate our proposed optical system, several assumptions have to be made. The first is that the active optical elements have the necessary bandwidth to perform their function; i.e., we assumed that the transistor performance in the transmitter and receiver was the system limiter and not the detector or modulator. To meet this requirement, the devices must have low parasitic capacitance. We have chosen 5 fF as the capacitance of the detector and 7.5 fF for the modulator. Although these values have not been reported in the literature, they can be considered as aggressive goals that have to be met in the future for optical interconnects to be competitive with Cu interconnects. We assumed that the waveguides must have a high index contrast to meet the routing requirement such as tight turn radii and high packing density. High index contrast waveguides with a difference in refractive index between the core and the cladding,  $\Delta n$ , larger than 0.5, can be fabricated using a Si or silicon nitride core, and  $\text{SiO}_2$  cladding [7,8]. A high index waveguide, however, will have a longer time of flight because the speed of light in the waveguide is  $c/n_{\text{eff}}$ , where  $n_{\text{eff}}$  is the effective index of the waveguide's mode. The effective index of a single-mode waveguide will be between the core and cladding index. This delay could be significant because the  $n_{\text{eff}}$  for a Si waveguide could be larger than 3, thus the time of flight is increased by a factor of 3 compared to the speed of light. The minimum optical line width is based on the optical mode size and does not scale with process generation since it is not expected that the wavelength can be scaled. For the

analysis, we will assume nitride waveguides that have an effective index of approximately 1.7 for a single mode waveguide. This is a good compromise between mode size, turning radii, and speed of light in the guide. Additionally, nitride waveguides can be used at all the telecom/datacom wavelengths.

For signaling, it is imperative to have as small a delay as possible. The key to building a fast receiver is to have a high photocurrent per unit of photodetector capacitance. A large ratio between the photocurrent and the dark current is also of paramount importance. One way to achieve this is to use a lateral waveguide coupled Metal-Semiconductor-Metal (MSM) photodetector [9]. Ge, Si, and SiGe have been studied as potential CMOS-compatible detector materials [10,11,12,13]. Close electrode spacings, less than 1  $\mu\text{m}$  apart, are necessary for low-voltage operation because the detector speed is proportional to the field the carriers in the detectors experience. However, capacitance increases with decreasing distances between the electrodes. A small detector area is therefore necessary to lower the device capacitance, which makes coupling light to the detector quite challenging.

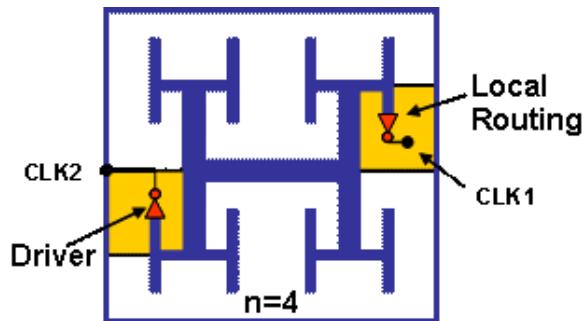
The amount of photocurrent is determined by the fraction of optical power that eventually reaches the detector and is converted into current. Thus the coupling efficiency from the laser into the on-chip waveguide, and the responsivity of the photodetector are key factors to achieving a power-efficient system. In addition, the losses in the waveguide, splitters, and from the coupling between the waveguide and photodetector, need to be minimized. An inexpensive coupling solution has to be developed to efficiently couple light from large waveguides to the small high-index contrast waveguides that will be needed for signaling. In this analysis, we assumed 100  $\mu\text{A}$  of photocurrent provided by 5 fF detectors.

The delay associated with the TIAs will decrease with each process generation. We assumed the detector and modulator performance remains constant and does not scale with process technology, since there is no intrinsic advantage to scaling these components.

A potential approach to utilize the large bandwidths of optical interconnects is to use a Wavelength Division Multiplexing (WDM) scheme to enable multiple signals of different wavelengths in the same waveguide (at the same time), which would generate an improvement in bandwidth density. WDM could be implemented using multiple laser sources or a broadband laser and on-chip filters. Considering that not all the components are currently available for on-chip optical signaling, this is a highly speculative option. In particular mux and demux technology need to be developed for on-die applications.

## Optical Clocking

An optical clocking scheme is shown in Figure 6. A mode-locked laser with short pulse width can be used as the clocking source. The light is coupled into an on-chip waveguide and distributed across the chip using an H-tree formed by waveguides. A photodetector and a TIA are placed at the end of each branch of the H-tree to convert the optical clock signal into a conventional electrical clock signal. The TIA drives a local buffer that in turn drives a local grid. This case is similar to optical signaling in that it can use the same type of waveguides, couplers, and detectors.



**Figure 6:** Schematic diagram of an on-chip clock distribution system

## COMPARISON OF Cu AND OPTICAL INTERCONNECTS

### Signaling

Copper interconnects are currently being used to enable the communication of different logic units, which is referred to as signaling. The most important metrics for signaling are latency, power, bandwidth, and cost. It is important to mention that these metrics are not completely independent of each other. For example, often a power-latency tradeoff exists, while bandwidth and cost are related to each other. As was already mentioned, the complexity of advanced microprocessors requires several layers of metallization. Global layers have the largest pitch and include the longest signal interconnects that provide communication between large functional blocks, while the local layers have the smallest pitch and are typically dedicated to interconnections within logic units. The pitches that optical interconnects can provide are only consistent with global “metallization” layers.

For Cu interconnects, latency is decreased by introducing repeaters along its length. The distance and size of the repeaters are typically optimized to minimize the point-to-point latency or a latency-power figure of merit. Several analytical expressions exist to calculate the latency of a repeatered metallic interconnect, and in this work we followed the approach provided in References 14 and 15,

which models the interconnects as a simple RC element. In the case of an optimally repeatered interconnect to minimize latency

$$T = 2.5 \sqrt{\tau_0 r c} L \quad [1]$$

where  $T$  is the point-to-point interconnect delay,  $L$  is the interconnect length,  $\tau_0$  is the minimum-size inverter delay, and  $r$  and  $c$  are the resistance and capacitance per unit length of interconnect, respectively. As shown in Equation 1, the interconnect delay increases with  $r$  and  $c$ . The increase in resistance per unit length of Cu interconnects with technology node is partially mitigated by decreasing repeater delay and by scaling the dielectric constants.

To validate our conclusions, we also conducted detailed simulations using Intel's internal simulation tools in which the repeaters were evaluated using compact models that include non-idealities, and the interconnects were modeled as transmission lines that take into account inductive effects that become important at high frequencies in wide Cu lines. The results obtained with simple analytical expressions are similar to our more accurate simulations, and the trends and conclusions are unchanged.

Finally, it is important to include in our analysis the fact that on-die communication over long distances (i.e., comparable with die sizes of 1 cm) requires multiple clock periods. In practice, the signal information is temporarily stored in latches near the end of each clock cycle, which enables the transmission of several signal bits at the same time in a particular Cu line (pipelining). In this paper, we assume that electrical signals travel for 80% of the clock period and are stored in latches during the remaining 20%. It is relevant to mention that interconnects with latencies up to 0.8 of the clock cycle do not have this time overhead. A straightforward correction was included in Equation 1 to account for this pipelining overhead.

We consider two extreme scenarios for Cu interconnects to explore their potential. In one scenario, we assume that Cu interconnect dimensions will be scaled following the International Technology Roadmap for Semiconductors (ITRS), and we will refer to them as scaled Cu interconnects. The ITRS scaling factor for interconnects is roughly 0.7. Another alternative is to maintain the dimensions of Cu interconnects constant, and we will refer to these interconnects as non-scaled Cu interconnects. The data used to obtain the results reported in this paper were obtained from the 2001 ITRS roadmap; including Cu interconnect pitches, dimensions (including aspect ratio), dielectric constants, resistivity, transistor delay and drive current, and clock frequency.

In the case of optical interconnects, there are four contributions to the latency arising from the modulator, the time of flight in the waveguide, the detector, and the TIA. For the detector we assumed a capacitance of 5 fF and a photocurrent of 100  $\mu$ A. For the TIA, we used a design based on the ones proposed in Reference 16, which we optimized for our detector assumptions using numerical simulations. For example, for the 90 nm technology node, the detector+TIA delay was found to be 39.5 ps, which is already 16% of the clock cycle assuming the ITRS frequency of 4 GHz for the node. The faster transistors that will be available in future nodes will decrease the TIA contribution to the delay, but it is not expected that the detector delay will be reduced by scaling. Consequently, the detector+TIA delay was found to decrease with technology node, but at a pace that is slower than that of repeaters. The waveguide delay,  $T_{wg}$ , is the time of flight for a given length, which was calculated using

$$T_{wg} = \frac{n_{eff}}{c} L \quad [2]$$

where  $n_{eff}$  is the effective refraction index of the relevant optical mode,  $c$  is the speed of light in vacuum, and  $L$  is the length of the interconnect (i.e., the waveguide). To assess the delay contribution of the modulator, we assumed a capacitance of 7.5 fF that does not scale with process technology. We used a two-stage buffer to drive the modulator, which we optimized for each technology node. Since optical interconnects behave as transmission lines, they can sustain several different bits of information without the need for the pipeline latches required by Cu interconnects. The total latency of optical interconnects is given by the sum of the modulator, waveguide, detector, and TIA delays. The latency of optical interconnects with and without WDM is assumed to be identical.

The number and length distribution of interconnects is a function of the number of transistors, and is generally described using the well-known Rent's rule [14]. The interconnect supply depends on the number of interconnect layers and on the number of interconnects that each of them can provide. Transistor scaling enables a growing number of transistors per die (for example, at constant die size), which causes an increasing demand of interconnects with technology node. We will use the bandwidth density per interconnect layer, BW, to characterize the wire supply provided by optical and Cu interconnects, which is given by:

$$BW = \frac{1}{\tau_{clk}} \frac{D}{p} \quad [3]$$

where  $\tau_{clk}$  is the clock period,  $D$  is the die size, and  $p$  is the pitch. In Equation 3, it was assumed that for Cu

interconnects, pipelining enables sending one signal per clock cycle in each interconnect, even if the latency is larger than a clock cycle (i.e., ideal pipelining is assumed). In practice, pipelining introduces additional latency and power. In the case of optical interconnects with WDM, an effective pitch,  $p_{eff}$ , was defined to account for an increasing number of signaling channels per waveguide as

$$p_{eff} = \frac{p}{N} \quad [4]$$

where  $N$  is the number of channels per waveguide, which was assumed to increase by one every two technology nodes.

Our metric to capture the cost of the different alternatives is the number of layers that are necessary to replace one interconnect layer with scaled Cu interconnects. Although the cost of an optical interconnect layer is likely to be larger than that of a Cu layer, most of the cost impact can be captured by considering the number of layers. Since signaling using Cu interconnects requires dedicated returns between signal lines to minimize crosstalk, it was assumed that the wire efficiency of the optical interconnects was higher than that of Cu interconnects by a factor of 1.6, which is likely to be an optimistic assumption for optical interconnects.

## Clock Distribution

Because modern microprocessors are synchronous, it is necessary to deliver a high-quality clock signal over the entire die, which ideally has to be received at the same time by all sequential elements. The most important performance metrics for clock distribution are skew, jitter, power, and cost. Skew refers to the time difference between the arrival of a given clock edge in different physical locations, while jitter is a measure of the variations in the arrival time between consecutive clock edges at a given location. The requirements are typically defined as a skew and jitter budget that is tied to the clock period (e.g., 20% of the clock cycle). Since the clock frequency is increasing with each technology node, clock distribution is becoming more challenging. Clock power increases linearly with frequency, and it accounts for a large and growing share of the total power. Finally, "clock cost" can be measured by the amount of metallization that is consumed by the clock interconnections, which is directly related to the pitch that is provided by the interconnects used for the clock distribution.

In present microprocessors, clock distribution is done using Cu interconnects, and can be divided into a global component that takes the clock signal from the Phase Locked Loop (PLL) to a few large regions of the die, and

a local part that delivers the clock signal to each sequential. There are several techniques for clock distribution such as grids, buffered H-trees, serpentines, and combinations of them [17,18]. The rapid increase of resistance of Cu interconnects resulting from scaling their dimensions increases their latency, which is known to increase skew and jitter. In summary, lower skew and jitter targets have to be met with lower quality interconnects, which increases clock design complexity. The pitch of the optical waveguides and the area used by the optical-to-electrical conversion makes the permeation of optical interconnects to intermediate or local metallization layers unlikely. Consequently, optical interconnects would only replace the global part of the clock distribution, which is done in the upper metal layers.

The approach to comparing the performance for global clock distribution of Cu and optical interconnects is already presented in Reference 6 and will be referenced in this paper. The 2001 ITRS roadmap was used as the source of data.

## RESULTS AND DISCUSSION

### Signaling

In optical interconnects, high speeds of propagation are achieved in the waveguides, but significant time overheads are associated with the electrical-optical-electrical conversion. For sufficiently long interconnects in which most of the latency is associated with the waveguides, it is expected that optical interconnects will be faster than Cu ones. To identify potential on-die uses of optical interconnects, it is convenient to define a critical interconnect length,  $L_c$ , above which the latency of optical interconnects is less than that of repeatered Cu wires. Figure 7 shows  $L_c$  both for scaled Cu wires and non-scaled Cu wires as a function of the technology node. The critical length that compares scaled Cu with optical interconnects decreases with technology node (Figure 7a), which is an indication that optical interconnects will become “better” with respect to their scaled Cu counterparts. However, even for the 22 nm node,  $L_c$  remains larger than 500  $\mu$ m, which implies that optical interconnects would not replace local Cu wires. On the other hand, if non-scaled Cu interconnects are compared against optical interconnects, Figure 7b shows that  $L_c$  increases with technology node, and at the 22 nm node, non-scaled Cu wires would be faster than optical ones for all possible lengths for die sizes on the order of 1cm (desktop microprocessors).

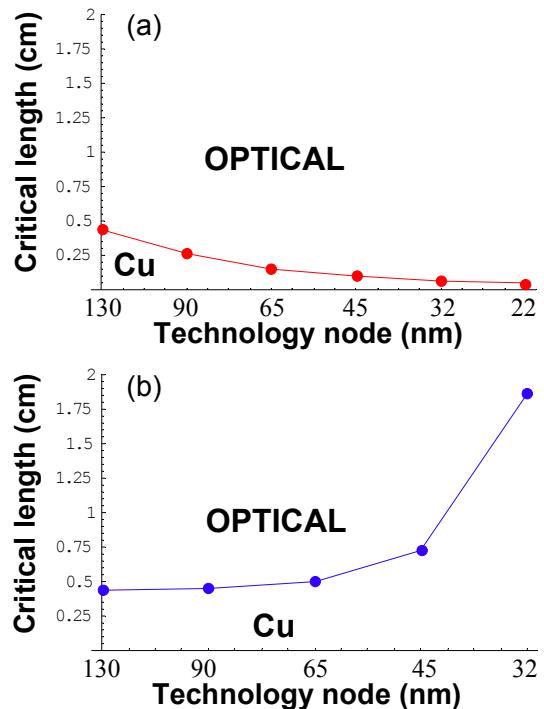


Figure 7: Critical length for optical interconnects: (a) optical interconnects compared against scaled Cu interconnects, (b) optical interconnects compared against non-scaled Cu interconnects

Based on the results of Figure 7, the longer the interconnects, the better the performance of optical interconnects with respect to their Cu counterpart. Since desktop microprocessor die sizes are approximately 1  $\text{cm}^2$ , most of the interconnects will be shorter than 1 cm. Our analysis in this paper is based on 1 cm-long interconnects, which is a relatively favorable approach for optical interconnects. Figures 8a and 8b show, respectively, the latency and latency normalized by the clock cycle of 1 cm-long conventional scaled Cu, non-scaled Cu and optical interconnects as a function of technology node. The latency rapidly increases for scaled Cu interconnects (Figure 8a), but it decreases for non-scaled Cu interconnects and optical interconnects. In the case of non-scaled Cu interconnects, the decrease of the absolute value of the latency is a consequence of the expected decrease in dielectric constant with technology node, as well as the decrease in repeater delay. Unfortunately, since the natural time unit in microprocessors is the clock cycle, an approximately constant latency is equivalent to a decreasing relative delay performance. Figure 8b shows that the normalized delay increases with technology node for all cases. The normalized delay of scaled Cu interconnects is increasingly degraded with respect to non-scaled Cu and optical interconnects. It is relevant to mention that the

normalized optical signal delay is comparable with that of non-scaled Cu interconnects.

While delay provides information on how fast the signal can travel across the die, this is not the only important metric. A microprocessor requires a large number of connections, and bandwidth is a measure of how many of these connections are completed. Since, in our analysis, pipelining is assumed, the bandwidth density for the interconnect options considered in this paper result mainly from the line pitch (see Equation 3). A plot of bandwidth density vs. process generation is shown in Figure 9. As was mentioned earlier, the minimum optical line width does not scale with process generation since it is not expected that the wavelength can be scaled. The non-scaled Cu by definition also does not scale. Clearly from a bandwidth perspective, the scaled Cu is the superior solution. However, the latency penalties for such a system would be significant. To meet the wire demand using optical or non-scaled Cu interconnects, additional metal layers would be required, as shown in Figure 10. Clearly this trend has already begun as the 0.13  $\mu\text{m}$  technology node for Intel microprocessors has six metal layers, and the 90 nm node has seven. This trend is likely to continue with the number of additional layers possibly increasing by more than one per generation since the global interconnect layers are not being scaled as aggressively as the local and intermediate layers. As mentioned earlier, the additional metal layers required will certainly add cost to the processor and may add additional thermomechanical challenges to building microprocessors with more than ten metal layers.

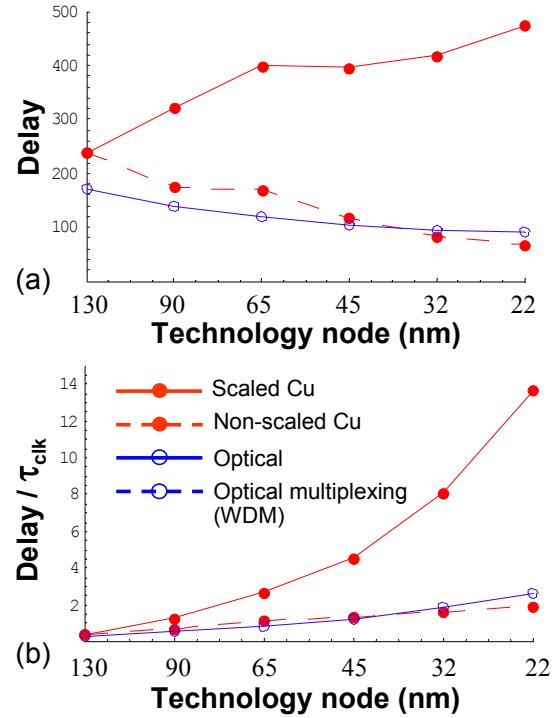


Figure 8: (a) Delay and (b) delay normalized by the clock cycle, as a function of technology node for optical, optical with WDM, scaled and non-scaled Cu interconnects

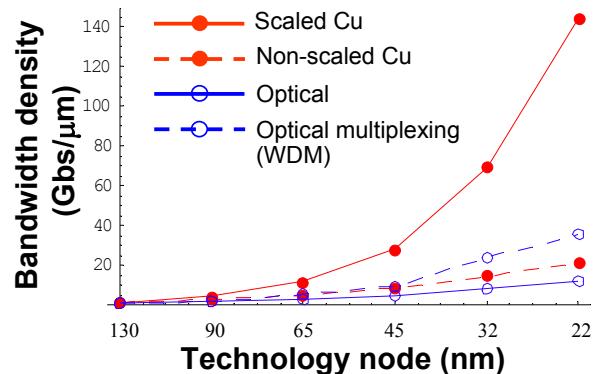
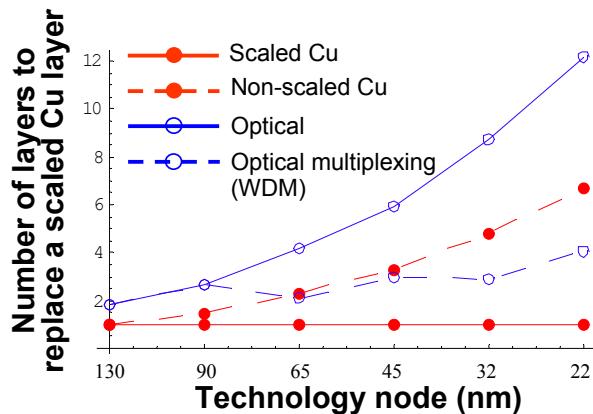


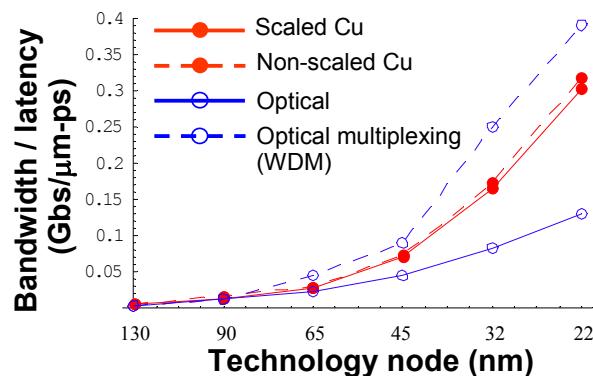
Figure 9: Bandwidth density as a function of technology node for optical, optical with WDM, scaled and non-scaled Cu interconnects

In summary, optical and non-scaled Cu interconnects have the best latency performance and the worst bandwidth density. On the other hand, scaled Cu interconnects are affected by large delays, but deliver the best bandwidth density (and lowest cost). In order to capture the tradeoff between latency and bandwidth density, Figure 11 shows the ratio of bandwidth density to latency for 1 cm-long interconnects. It is interesting to notice that scaled and non-scaled Cu interconnects have

almost identical BW-latency ratios. Optical interconnects without WDM have the poorest performance for this particular metric. However, optical interconnects with WDM show the best bandwidth-latency tradeoff, even under the assumption that the number of channels per bandwidth would only increase by one every two technology nodes.



**Figure 10:** Number of back-end layers that would be necessary to provide a bandwidth equivalent to that of a metallization layer with scaled Cu interconnects

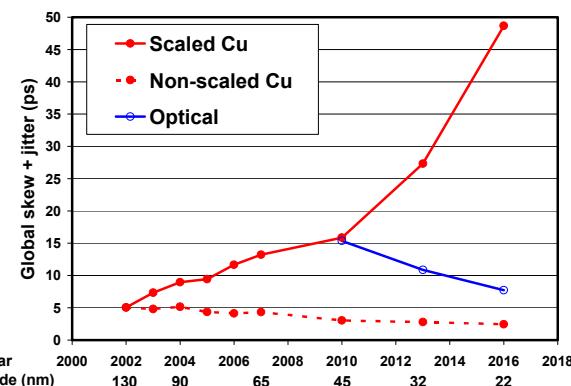


**Figure 11:** Bandwidth/latency ratio as a function of technology node for optical, optical with WDM, scaled and non-scaled Cu interconnects

## Clocking

The benchmarking of optical, scaled Cu, and non-scaled Cu interconnects for clock distribution has already been reported in Reference 6 and will be briefly summarized here. The general observation is that global optical clocks do not provide significant power savings or jitter and skew improvements because the global clock is only a small contributor to these issues. Furthermore, we found that optical interconnects do not have an advantage over non-scaled Cu interconnects for skew and jitter. Figure 12 shows the calculated skew and jitter at the global clock distribution for optical, scaled, and non-scaled Cu

interconnects as a function of technology node. It is observed that although optical interconnects show a better performance than scaled Cu interconnects, they do not offer improvements with respect to non-scaled Cu interconnects, which are an option with lower cost and less technological risk. Consequently, clocking does not seem to motivate the implementation of a disruptive technology such as optical interconnects. Other benefits of optical clocking such as electromagnetic interference immunity would not warrant implementation because conventional technology solutions exist and are less costly. Negative aspects of optical clocking include additional processing cost and the decoupling of the power level and the clock signal.



**Figure 12:** Comparison of the global skew and jitter as a function of technology node for clock distribution using optical, scaled, and non-scaled Cu interconnects

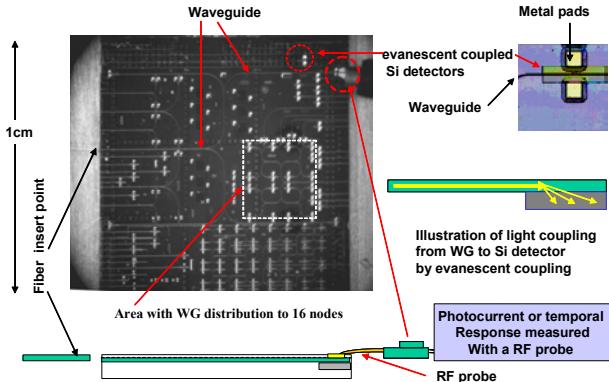
## Experimental Results

On-chip photonics is enabled by the fact that many CMOS-compatible materials can be used to build integrated photonic systems. For example, Si,  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ , and  $\text{SiO}_x\text{N}_y$  can be used as a waveguide and cladding at wavelengths where these materials are transparent and the refractive index indices enable cladding. In addition, semiconductors such as Si and Ge can be used as detectors at wavelengths where they absorb light.

Whether we are developing optical interconnects for signaling or clocking, the building blocks for on-chip applications remain essentially the same. The only exception is that an optical modulator and a CW light source is needed for signaling, while a pulsed clocking light source is needed for clocking.

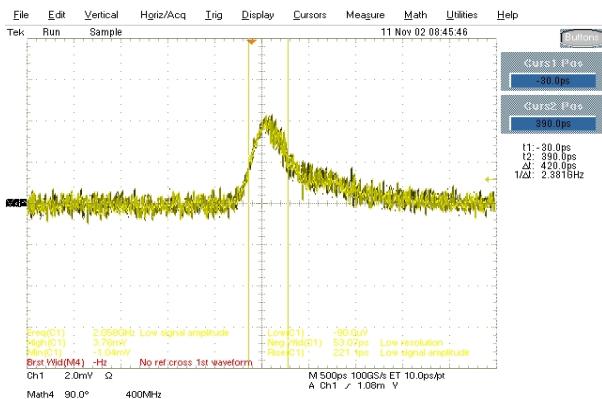
Our early work focused on building waveguides from  $\text{SiO}_x\text{N}_y$  cladded with  $\text{SiO}_2$ . The waveguide design was based on single-mode propagation of optical signals with a wavelength,  $\lambda$ , of 850 nm. The index contrast between core and cladding was designed to be at 0.07 to allow bending radii as small as 120  $\mu\text{m}$ . The waveguide core

size was  $1.2 \mu\text{m} \times 1.2 \mu\text{m}$ . The loss at 850 nm was 2 dB/cm. These waveguides were fabricated on an SOI wafer and evanescently coupled to Si pin photodetectors. A photograph of this device with a schematic explanation of various components is shown in Figure 13.



**Figure 13: Photograph of a 1 cm x 1 cm size chip with a waveguide-based H-Tree and integrated Si detectors. Si-based pin photodetectors were monolithically integrated with the waveguide. The light is transferred from the waveguide to the detectors by evanescent coupling.**

The photodetectors used in this testchip were made by doping interdigitated fingers 2  $\mu\text{m}$  wide and spaced at 2  $\mu\text{m}$  in the 1- $\mu\text{m}$  thick intrinsic Si layer, and then forming contacts to the fingers with Al. Conversion of light coupled into the waveguide by an objective lens was measured electrically by probing the detectors, which were biased at -3V. The impulse response of one of these detectors to a fiber-coupled Ti:Sapphire laser is shown in Figure 14. This particular detector has an active area of 6  $\mu\text{m} \times 400 \mu\text{m}$  and a capacitance of 250 fF. The impulse response of the pulse in Figure 14 has a Full-Width Half-Maximum (FWHM) value of 420 ps.

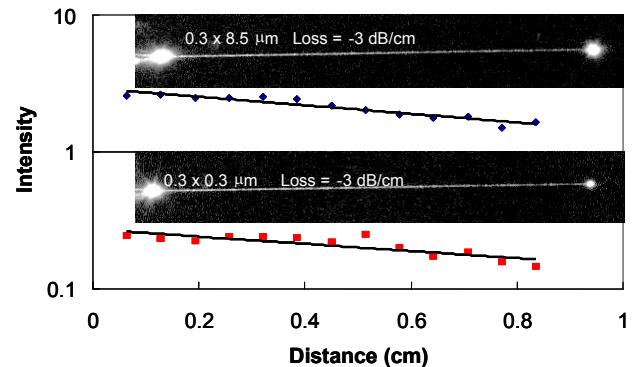


**Figure 14: Impulse response of an evanescently coupled Si pin photodetector from Figure 13**

While these results demonstrate early learning, they would not be practical for realistic on-chip systems. Detector performance needs to be improved. This can be accomplished by using Ge, for instance, because it has a higher absorption coefficient. The higher absorption coefficient can allow for the detector size to be reduced compared to Si, thus lowering the capacitance. The choice of Ge as the photodetector material would make it possible to choose any of the widely used "communications" wavelengths, while silicon would limit the choice to the short-haul wavelength (850 nm). Finally, making photodetectors out of Ge provides more options for waveguide materials to couple to the photodetectors, as Si as well as silicon nitride and silicon oxynitrides can be considered.

In the Si detector described above, speed can be increased by decreasing the width of the intrinsic region, assuming the size is reduced to minimize capacitance. However, since the waveguide dimension and optical mode size is on order of the width of the intrinsic region, further narrowing of the gap will result in loss of responsivity because light will be absorbed in the doped regions and will not be collected as photocurrent. Decreasing the optical mode size of the waveguide could allow for closer spacing without loss of detector responsivity and could therefore reduce transport times and increase speed.

In an effort to reduce the optical mode size, we have made smaller  $\text{Si}_3\text{N}_4$  waveguides ( $0.3 \mu\text{m} \times 0.3 \mu\text{m}$ ) with oxide cladding. The loss at 850 nm has been measured at 3 dB/cm and is not degraded from multimode guides with much wider widths (up to 10  $\mu\text{m}$ ) where edge scattering would not be expected to be dominant, as shown in Figure 15.



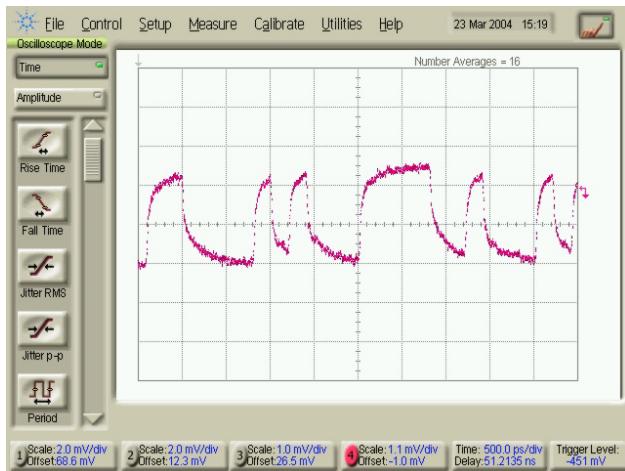
**Figure 15:  $\text{Si}_3\text{N}_4$  waveguide on loss at 850 nm**

These high-index contrast waveguides, with a  $\Delta n$  of approximately 0.5, are ideal for a practical on-chip interconnect system, because they should allow for high-density optical wiring and good compatibility with high-speed detectors and modulators. The effective index of the optical mode is approximately 1.7.

The optical components, such as photodetectors and modulators (for signaling) need to operate at high speeds and low voltages. In our development of the key building blocks for optical systems, we have also made good progress on building high-speed CMOS-compatible photodetectors. These detectors have exhibited GHz speeds even at relatively low bias voltages. An eye diagram and data trace for a detector biased at 1 V and excited by a 1550 nm light source modulated by random data at 5 Gb/s are shown in Figures 16a and b, respectively. Impulse response measurements at both 850 nm and 1550 nm indicate these structures have the potential to run at faster than 20 GHz.



**Figure 16a:** Eye diagram of a CMOS-compatible detector built on Si, measured at 5 Gb/s, biased at 1 V



**Figure 16b:** Data from the above detector at 5 Gb/s

### Signaling Challenges

The waveguides and photodetectors described above are applicable to both signaling and clocking. Signaling, however, offers much greater challenges. These challenges include fabricating waveguide modulators that not only can operate at GHz speeds, but can be driven by

CMOS circuits that will only have approximately a 1 V drive voltage available and must be very small to accommodate the large bandwidth required by the microprocessor. In addition, the modulator must be CMOS compatible. To date, there are no such modulators that meet all of these requirements. This area will require innovation in materials and devices to meet the aggressive requirements for on-chip optical signaling.

Another requirement/challenge for signaling is WDM. There are several potential options for accomplishing this. Each channel can have an independent laser. Passive filters or wavelength-sensitive modulators would be needed as additional components.

### CONCLUSION

Our analysis, performed in the 2002-2016 timeframe, did not reveal significant advantages for using on-die optical clock distribution, since the pitches of the waveguides and the Si area consumed by the optical-electrical conversion would prevent them from permeating into the local clock distribution, where most of the power, skew, and jitter are associated. For on-chip signaling, we found that non-scaled Cu and optical interconnects have the lowest latency, but the worst bandwidth density and cost, while non-scaled Cu interconnects provide the lowest cost and highest bandwidth density at the expense of the highest latency. Consequently, a tradeoff between latency and bandwidth (and cost) is necessary. Since multiplexed optical interconnects deliver the best bandwidth/latency ratio, there are considerable potential benefits for optical signaling if the large bandwidth of the waveguides can be utilized by using, for example, WDM.

The major challenges for realizing on-chip optical interconnects are the development of high-speed and low-capacitance CMOS-compatible modulators and detectors. In addition, for on-chip signaling to be competitive with Cu interconnects, and to be cost effective, a practical approach for implementing WDM has yet to be identified and tested.

### ACKNOWLEDGMENTS

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# Silicon Photonics

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## ABSTRACT

We introduce our approach to opto-electronic integration, silicon photonics, and outline the key functions required for an opto-electronic integration platform: generation, control, and detection of light. Recent research results for silicon-based optical components are discussed including a tunable external cavity laser, a 2.5 GHz optical modulator and a silicon-germanium waveguide-based photodetector. Lastly, optical packaging challenges and potential next-generation designs are presented.

## INTRODUCTION

Silicon photonics at Intel can be defined as the utilization of silicon-based materials for the generation (electrical-to-optical conversion), guidance, control, and detection (optical-to-electrical conversion) of light to communicate information over distance. The most advanced extension of this concept is to have a comprehensive set of optical and electronic functions available to the designer as monolithically integrated building blocks upon a single silicon substrate.

### Silicon in the Optical Domain

Both the wavelength of light and the transport medium used vary with the application. Our current research is aimed at developing devices and proving functionality in the optical domain for infrared wavelengths common to silica fiber-optic telecommunications systems ( $1.3\text{ }\mu\text{m}$  to  $1.6\text{ }\mu\text{m}$ ). Within this range of wavelengths, silicon is nearly transparent and generally does not interact with the light, making it an exceptional medium for guiding optical data streams between active components. With appropriate design, the introduction of additional

materials such as silicon dioxide, standard electronic dopants, and SiGe alloys selectively enhances the electronic-to-optical interactions, allowing for the creation of active devices such as a light intensity modulator and a photodetector. Notwithstanding this flexibility, no practical modification to silicon has yet been conceived which gives efficient generation of light. Thus, the Intel Silicon Photonics platform requires the light source as an external component.

### Silicon Electronics in Optical Communications

In the electrical domain, silicon integrated circuits have been widely adopted in all layers of the network, including physical media drivers, media access controls, and for complex network intelligence functions. In principal, monolithic integration of electronics and optics is possible, can reduce unwanted electrical parasitics, and can allow for a reduction in overall size. There are numerous theoretical and practical obstacles to achieving full monolithic opto-electronic integration. We are currently pursuing two parallel approaches to opto-electronic integration in silicon. The first is to achieve a high level of photonic integration with the goal of maximizing the level of optical functionality and optical performance. The second is to look for specific cases where close integration of an optical component and an electronic circuit can improve overall system performance. One such case would be to integrate a SiGe photodetector with a Complementary Metal-Oxide-Semiconductor (CMOS) transimpedance amplifier.

## Integration: The Challenge and the Value

An optical transceiver module (sometimes called a transponder) is to be found at the terminations of virtually all optical communications links and the general functionality and architecture of the transceivers in service are similar regardless of performance requirements, communications protocols, and end-user applications. One vision of the future of optical communications links is one in which the drive for lower costs for higher performance (smaller size, lower power, higher data rate, greater transmit distance, expanded functionality, and expanded flexibility) will occur through an increased complexity in the optical domain. Some examples would be multiple wavelengths in one fiber from one ingress point, adaptive or reconfigurable optical components capable of recovering signal integrity under changing external conditions, all-optical packet switching, all-optical signal regeneration, and the use of shared optical media in so-called Passive Optical Networks (PONs) and optical Code Division Multiple Access networks (optical-CDMA). Such increased complexity in the optical domain will require increasingly sophisticated electronic control solutions, and at high data rates, there will be pressure to more closely integrate optical and electronic components. Monolithic integration of a suite of optical and electronic capabilities in one substrate is the natural progression of an integrated photonics vision.

However, in the foreseeable future, the vast majority of improvements at the cost-sensitive (high-volume) applications can be expected almost exclusively in the electronic domain (electronic dispersion compensation, electronic equalization, and electronic means of recovering signal integrity under changing external conditions). Furthermore, the past decade has shown that the simplicity of single-wavelength transceivers with serial On-Off-Key data encoding (OOK) have consistently been chosen over more complex optical solutions (e.g., parallel-optical and CWDM). This does not mean that there are not steady technical improvements in the optical domain, such as recent introductions of long-wavelength Vertical Cavity Surface Emitting Lasers (VCSELs), and deployments of InP Externally Modulated Lasers (EMLs) for mid-performance links. However, these improvements generally are not changing the external architecture of the link for cost-sensitive applications (still single-wavelength, one direction per fiber, etc.).

Thus, it is fair to say that a future with wide-scale deployment of highly integrated photonic and opto-electronic components will be one with a great many changes to the “where and how” light is used to transmit information. The most likely insertion points for integrated photonics will be in places where an extreme

amount of data (aggregate bandwidth) is required in a very small space. Two such applications would be microprocessor data busses (i.e., from microprocessor to memory or between multiple processors in a server) and in the backplane of server racks. Paradoxically, these applications violate a widely held axiom that says that optics is the best choice for long-distance transmission (hundreds of meters to hundreds of kilometers) whereas copper traces and copper cables own the application space for shorter distances. The key assumption that allows us to violate this axiom is that the aggregate bandwidth will be too large for a cost-effective copper-based solution. Present-day estimates indicate that a copper-based point-to-point serial link will become prohibitively expensive above 20 Gbps.

Identifying the potential insertion point for integrated photonics is one thing, but gaining insight into the details of the implementation is quite another matter. The architecture (point-to-point or shared media, encoding scheme, etc.), the transmission medium (polymer waveguide, silica fiber), the integration platform (silicon, GaAs, InP, polymer, silica), and finally the level of integration (monolithic opto-electronic, monolithic photonic integration with separate electronics, or optical platform with hybrid electronic and optical components) are all issues of active investigation in the research community.

## Silicon Photonics at Intel

In the first section of this paper we explore Intel's ongoing research to define one particular technology platform for integrated photonics, namely Silicon Photonics. We introduce the building blocks of the technology and explore the technical advancements and critical challenges to making high-performance components for the integrated platform. The cornerstone technologies being developed at Intel are the tunable External Cavity Laser (ECL), the Silicon Modulator, Silicon-Germanium (SiGe) photodetector, and low-cost interconnection techniques.

A single mode, tunable ECL has been demonstrated by coupling an AR coated III-V semiconductor laser diode to a silicon-based waveguide Bragg grating. The lasing wavelength is selected by the grating and can be tuned by using the thermo-optic effect and simply heating the grating, producing a tuning rate of 12.5 nm/100° C.

Until recently, waveguide-based silicon optical modulators have been limited to relatively moderate speeds, the fastest reported being around 20 MHz. We have made a breakthrough by moving away from the conventional current injection-based devices to a novel MOS capacitor-based architecture. This has allowed us to achieve a 2.5 GHz phase modulation with modeling

predicting bandwidth scaling to beyond 10 GHz. This means that silicon could quickly become a viable alternative to the more conventional III-V or LiNbO<sub>3</sub> modulators currently used for optical communications.

Detection of light for wavelengths typically used for optical communications (1.310-1.550  $\mu\text{m}$ ) is not possible in silicon, which is naturally transparent in this region. We are therefore developing photodetectors based on SiGe alloys in order to push the responsivity out to longer wavelengths to achieve efficient operation.

Interconnecting the Silicon Photonic platform, such as to the transmission medium (e.g., silica fiber), is not trivial. To address high-volume applications it is imperative to have simple and low-cost coupling and packaging procedures.

In this next section we highlight waveguide tapering, passive fiber alignment, and passive hybrid alignment techniques.

## SILICON LIGHT SOURCE

In this section the use of silicon photonics applied to the light source is discussed. While a silicon laser is still out of reach, work is being done worldwide on silicon light emitters that emit both visible and infrared radiation. A silicon emitter is the missing piece for monolithic integration as it would enable all optical elements and drive electronics to be fabricated on a common substrate. Because we are using silicon waveguides to guide light, the emitter must be in the infrared region of the wavelength spectrum ( $> 1.1 \mu\text{m}$ ) where optical absorption loss is low.

We first summarize the different paths researchers are investigating to achieve electrically pumped light emission, known as Electro Luminescence (EL), from silicon. Until a reliable and efficient silicon emitter can be produced, hybrid integration must be considered (i.e., using a non-silicon-based light source coupled to silicon waveguides). In such a hybrid integrated approach, we show how a simple gain element (III-V gain chip) coupled to a silicon-based Bragg filter can be used to form an ECL. Proof of principal of this tunable, single-mode laser is discussed.

The difficulty in making a silicon light emitter arises from silicon's indirect band-gap. This indirect bandgap results in radiative (light emitting) decay being less likely compared to other non-radiative (e.g., Auger recombination) routes, and thus in a less-efficient corresponding light emission. Forming a laser or even a light emitter from silicon is therefore difficult, although not impossible, and research worldwide has shown light emission from silicon and silicon-based materials by a wide variety of different methods; see, for example, the

summary in [i]. These range from photo-luminescence in textured bulk silicon [ii], to fabrication of nano-scale [iii] or porous silicon [iv] to doping with exotic ions [vii], to Raman emission [v].

To achieve infrared light emission from silicon, the silicon must be doped with a suitable material, such as  $\beta$ -FeSi<sub>2</sub> [vi], or Erbium [vii]. Erbium-doped silicon waveguides have shown infrared light emission when the silicon is co-doped with oxygen to produce optically active ions in the lattice [vii]. A PN junction can be formed and the erbium ions pumped electrically to form EL. These kind of doped bulk silicon devices suffer from a major problem: although emission can be relatively strong below 100 K, the emission intensity falls rapidly when the device is heated to room temperature [viii]. This greatly limits the application of these devices.

A different approach to enhance the efficiency of light emission in silicon is to reduce the other non-radiative mechanisms for electron hole recombination. This can be done by restricting carrier diffusion to the non-radiative recombination centers in the lattice. This increases the probability for radiative transitions and hence increases light emission efficiency. A Very Large Scale Integration (VLSI) compatible means to achieve this carrier confinement is to use nano-crystals. Silicon nano-crystals suspended in silicon-rich oxide restrict carrier movement while still allowing electrical pumping [ix]. Pavesi has shown optical gain in these structures [iii] and Franzo et al. have doped silicon nano-crystals with erbium to achieve EL in the infrared region of the spectrum [x]. Other means to obtain carrier confinement and efficient emission of infrared wavelengths include using Ge/Si quantum dots [xi] or crystalline defects [xii].

In all these approaches the use of erbium as the dopant can be changed to allow emission at other wavelengths; e.g., ytterbium or terbium allows emission at 0.980 and 0.540  $\mu\text{m}$  in resonant cavity silicon LEDs [xiii]. For these devices to be used in practical applications, however, their lifetimes and reliability still need to be optimized.

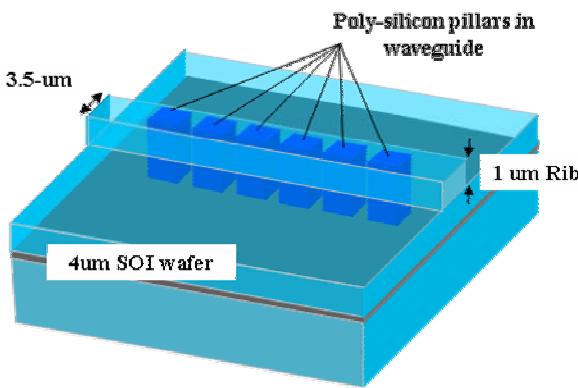
Another limitation for all forward-biased silicon light emitters is their low direct modulation speeds (~1 MHz) [xiv]. This means that realistically this kind of silicon emitter will require an external modulator for high-speed communication links. Reverse biasing has the potential for achieving higher direct modulation speeds (~200 MHz), but at the moment this comes at the expense of light emission efficiency [xv].

## Device Architecture

The work towards a silicon-based emitter is ongoing but still far from mature. Until an efficient, reliable silicon-based light source is available, a photonic integrated system will need to use a conventional III-V material light

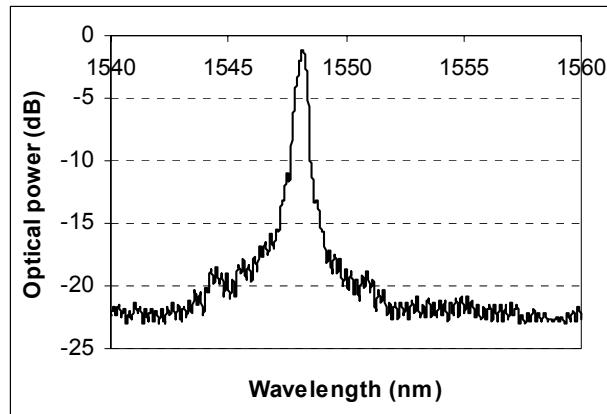
emitter. This section describes how a silicon waveguide-based Bragg grating [xvi] can be used in an external cavity to alter the lasing properties of a III-V gain chip to produce a useful source for optical communications. The strong thermo-optic effect in silicon [xvii] can be used to tune the lasing wavelength by heating the silicon grating. The driving force behind this is to produce an inexpensive narrow line-width source suitable for optical communications.

The Bragg grating is fabricated by etching a set of  $1.2 \times 2.3 \mu\text{m}$ ,  $3.4 \mu\text{m}$  deep, trenches into a  $4 \mu\text{m}$  thick Silicon-on-Insulator (SOI) wafer. One thousand of these trenches are laid out in a line along the waveguide with a range of periods around  $2.445 \mu\text{m}$  (although these were laid out as rectangular trenches, due to litho resolution, they were rounded after processing). These trenches are then filled with poly-silicon and annealed to reduce the loss due to the poly-silicon [xviii]. The poly-silicon is then chemically/mechanically polished to obtain a planar surface and the  $3.5 \mu\text{m}$  wide,  $0.9 \mu\text{m}$  deep rib is patterned using standard lithography and etching. The last step in the fabrication is to deposit a final,  $0.5 \mu\text{m}$  thick, low-temperature layer of oxide to provide the necessary upper cladding for the rib waveguides [xvi]. A schematic of the Bragg grating is shown in Figure 1.



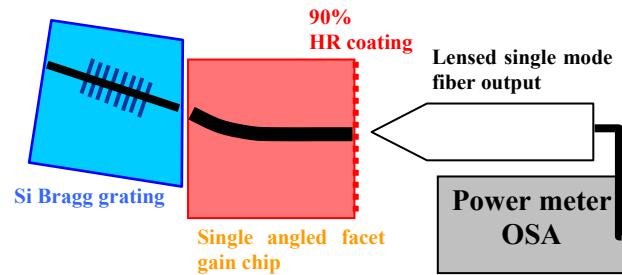
**Figure 1: Schematic of polycrystalline-silicon grating in SOI**

The novel property of this Bragg grating is that it only reflects a narrow,  $0.5 \text{ nm}$  wide range of wavelengths back through the waveguide with a reflectivity of 70% [see xvi]. An example of a reflection spectrum from a 1500-trench grating filter is shown in Figure 2. As a separate component these Bragg filters can be used in optical communication networks as channel filters for wavelength division multiplexed systems.



**Figure 2: Reflection spectrum of grating filter with 1500 periods at a pitch of  $2.455 \mu\text{m}$**

The ECL is formed by butt coupling a Single Angled Facet (SAF) gain chip to a waveguide containing the polycrystalline/crystalline silicon Bragg grating. The laser cavity is formed between the Bragg grating as one end mirror, and a 90% high-reflection coating of the gain chip as the other mirror. The  $8^\circ$  angled facet between the two chips decreased the effective reflectivity of that facet to  $\sim 10^{-3}$ . Combining an angled facet with a 1% anti-reflection coating resulted in an effective facet reflectivity of  $\sim 10^{-5}$  [xix]. The output of the laser was taken from the 90% high-reflectivity coated side of the laser diode with a conical polished ( $140^\circ$ ) lensed single-mode fiber [Figure 3]. The purpose of this lensed optical fiber was to increase the coupling between the laser and the optical fiber.

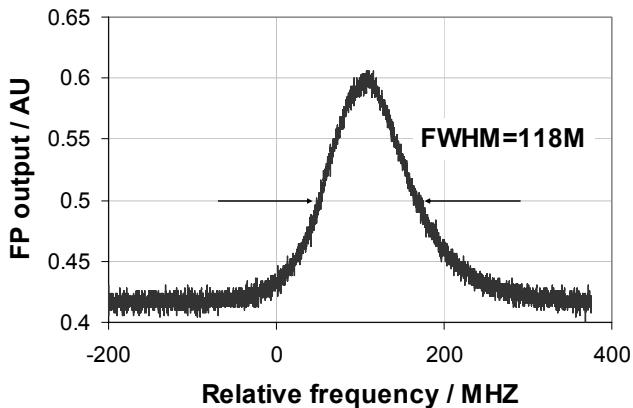


**Figure 3: Schematic of the external cavity laser**

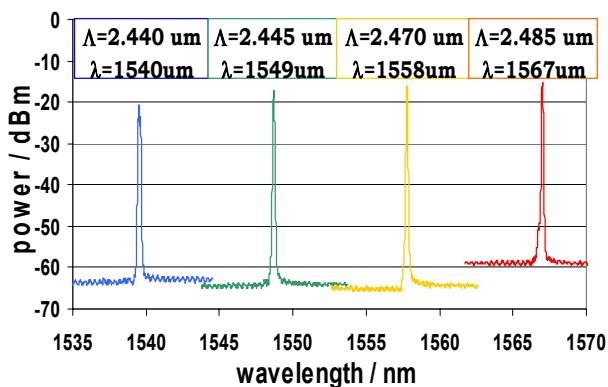
## Technical Results

With the SAF gain chip butt coupled to the Bragg grating, the ECL runs single mode with a line width of  $118 \text{ MHz}$ , as shown in Figure 4. The optimized output power of the ECL, when the gain chip was driven at  $250 \text{ mA}$ , as measured out of the single-mode fiber was  $450 \mu\text{W}$ . The output power is limited by a number of factors: the coupling of the gain chip to the waveguide, the 90% HR coating, and the coupling of the gain chip to the fiber. The 90% output coating can be optimized for increased output

power at the expense of the laser threshold, while the coupling can be enhanced by tapering the silicon waveguide so that its optical mode better matches the mode of the gain chip.

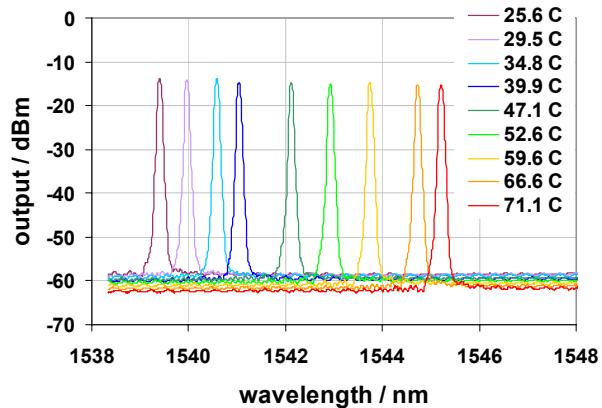


**Figure 4:** The line-width of the ECL is 118 MHz at 1.539  $\mu\text{m}$



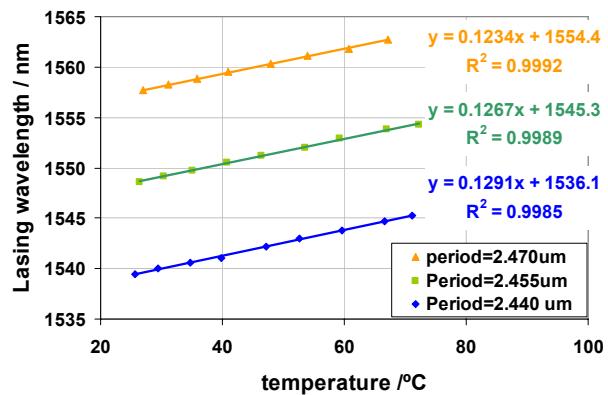
**Figure 5:** The lasing wavelength ( $\lambda$ ) for different periods ( $\Lambda$ ) of poly grating

By altering the period of the grating, different wavelengths can be fed back into the gain chip. This allows the lasing wavelength of the ECL to be changed. Figure 5 shows the spectra of the ECL for four different grating pitches. The wavelength range here is limited by the selection of gratings fabricated rather than the gain spectra of the SAF gain chip. The side-mode suppression ratio (ratio of peak emission to background) of the ECL can be seen to be over 40 dB.



**Figure 6:** The variation of the output spectra of the ECL with temperature (2.440  $\mu\text{m}$  period Bragg chip)

The refractive index of silicon can be altered by using the thermo-optic effect [xvii]. This means that the Bragg wavelength of the polycrystalline/crystalline silicon grating can be tuned by heating the silicon substrate. This was done by placing the silicon die on a thermo-electric cooler and monitoring its temperature with a thermocouple. As can be seen in Figure 6, heating the 2.440  $\mu\text{m}$  Bragg chip from 27°C to 71°C resulted in a tuning of the ECL from 1.5395  $\mu\text{m}$  to 1.5455  $\mu\text{m}$ . A plot of lasing wavelength vs. die temperature is shown in Figure 7 for three different period gratings. The tuning is linear with die temperature with a rate of 12.6 nm/100°C.



**Figure 7:** The variation of lasing wavelength with temperature for three different period Bragg gratings

### Challenges/Technical Hurdles

In this section the various means of obtaining EL from silicon are discussed. Given the current limited lifetime and efficiency of silicon light emitters, a hybrid integration approach has been taken of coupling a III-V gain chip to an SOI waveguide. The proof of concept of an external cavity, single-mode laser that can be tuned

using the thermo-optic effect at the rate of 12.6 nm/100° C has been demonstrated.

Of course there is still some device optimization that needs to take place to make this ECL a useful building block for silicon photonics. Future work will focus on optimizing the coupling between the silicon waveguide and both the InP gain chip and the output fiber to achieve the 5 mW output power needed for a viable communications system. One approach to achieving this would be to taper the silicon waveguide, which is discussed more in the optical coupling and packaging section.

Tuning speed is another issue. While the thermo-optic effect is relatively large in silicon, it is also rather slow providing tuning speeds between 1 ms and 1 s [xx]. By using other device architectures, e.g., ring resonator structures [xxi], tuning can be achieved by using faster effects, e.g., the plasma dispersion effect. This could provide much faster tuning and potentially allow for more intelligent communication systems.

For photonic integrated circuit applications, the ECL architecture described here, where the tuning is done on one side of the ECL and the output taken from the other side, involves coupling to both sides of the gain medium. This is complicated from a device assembly point-of-view, and different laser geometries are being investigated where both tuning and the laser output can be done by coupling to just one side of the ECL without degrading its output performance.

## SI MODULATOR

### Background

In the previous section we discussed our approach of coupling a silicon-based Bragg grating filter to an III-V compound semiconductor laser diode to build a narrow line-width, tunable laser. The laser output is a continuous wave, meaning it carries no data or information. To encode data onto this continuous wave of light, for use in an optical communications link, we need an optical modulator. Optical modulator devices with speeds greater than 1 GHz are typically fabricated from either the electro-optic crystal LiNbO<sub>3</sub> [xxii, xxiii] or III-V semiconductor compounds and multiple quantum wells such as GaAs/AlGaAs and InGaAsP-InP, which utilize the quantum confined Stark effect [xxiv xxv xxvi] or the electro-absorption effect [xxvii]. These devices have shown modulation frequencies in excess of 40 GHz [xxiii,xxvii].

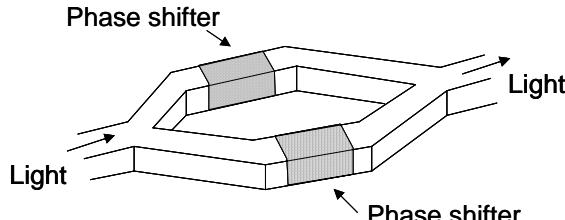
The demand for low-cost solutions has prompted studies of silicon-based modulators. These are attractive from a cost standpoint because mature silicon processing technology and manufacturing infrastructure already exist

and can be used to build cost-effective devices in volume. In addition, silicon photonics technology provides the possibility of monolithically integrating optical elements and advanced electronics on silicon using bipolar or CMOS technology [xxviii].

Numerous silicon waveguide-based optical modulators have been proposed and demonstrated [xxix, xxx]. The majority of research has focused on using the free carrier plasma dispersion effect in a forward-biased pin diode geometry. This is because unstrained pure crystalline silicon exhibits no linear electro-optic effect, and the refractive index changes due to the Franz-Keldysh and Kerr effects are also small [xxx]. Since the modulation speed due to the free carrier plasma dispersion effect is determined by the rate at which carriers can be injected and removed, the long recombination carrier lifetime in the intrinsic silicon region generally limits the modulation frequency of these silicon-based devices. Although there is literature showing theoretically that ~1 GHz modulation frequency might be achievable by reducing the waveguide dimensions to sub-micrometer range [xxxii], the previous fastest demonstrated speed of an optical modulator based on current injection in SOI is approximately 20 MHz [xxix, xxx]. These devices are of little practical interest because today's communication networks are demanding GHz performance.

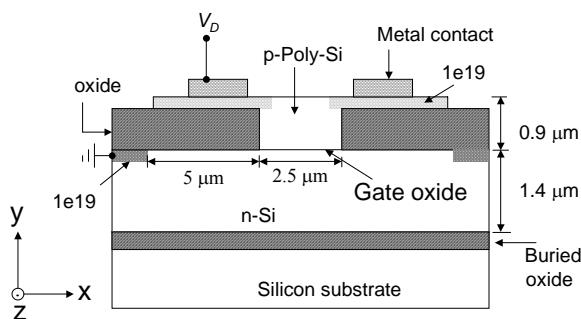
### Architecture

Here we present an experimental demonstration of a silicon optical intensity modulator with a modulation bandwidth of 2.5 GHz at optical wavelengths of around 1.55 μm [xxxiii]. This modulation frequency is two orders of magnitude higher than has been demonstrated by any silicon waveguide modulator to date. The high-speed modulation is achieved by using a novel phase shifter design based on a metal-oxide-semiconductor (MOS) capacitor embedded in a passive silicon waveguide Mach-Zehnder Interferometer (MZI). **Figure 8** is a schematic representation of one MZI modulator discussed in this paper. Light wave coupled into the MZI is split equally into the two arms, each of which may contain an active section which converts an applied voltage into a small modification in the propagation velocity of light in the waveguide. Over the length of the active section(s), the velocity differences result in a phase difference in the two waves. Depending on the relative phase of the two waves after passing through the arms, the recombined wave will experience an intensity modulation.



**Figure 8: Schematic of a Mach-Zehnder interferometer modulator with two phase shifter sections**

The novel component, as well as the essence, of our silicon MZI modulator is the MOS capacitor phase shifter. Figure 9 is a schematic of its cross-sectional view. It comprises a  $\sim 1.4 \mu\text{m}$  n-type doped crystalline silicon slab (the silicon layer of the SOI wafer) and a p-type doped poly-silicon rib with a  $120 \text{ \AA}$  gate oxide sandwiched between them. The poly-silicon rib and the gate oxide widths are both  $\sim 2.5 \mu\text{m}$ , and the total poly-silicon thickness at the centre of the waveguide is  $\sim 0.9 \mu\text{m}$ . In order to minimize the metal contact loss, we designed a wide ( $\sim 10.5 \mu\text{m}$ ) top poly-silicon layer on top of the oxide layers on both sides of the poly-silicon rib. Aluminum contacts are deposited on top of this poly-silicon layer as shown in Figure 9. The oxide regions on either side of the rib maintain horizontal optical confinement and prevent the optical field from penetrating into the metal contact areas. Vertical optical confinement is provided by the  $\sim 0.375 \mu\text{m}$  buried oxide and an oxide cover (not shown in Figure 9). Modeling and testing confirm that the waveguide phase shifter is a single-mode device at wavelengths around  $1.55 \mu\text{m}$ .



**Figure 9: Schematic diagram showing the cross-sectional view of a MOS capacitor waveguide phase shifter in SOI. Optical mode propagates along the z direction.**

In accumulation, the n-type silicon in the MOS capacitor phase shifter is grounded and a positive drive voltage,  $V_D$ , is applied to the p-type poly-silicon causing a thin charge layer to accumulate on both sides of the gate oxide. The voltage-induced charge density change  $\Delta N_e$  (for electrons)

and  $\Delta N_h$  (for holes) is related to the drive voltage by [xxxiv]

$$\Delta N_e = \Delta N_h = \frac{\epsilon_0 \epsilon_r}{et_{ox} t} [V_D - V_{FB}] \quad (1)$$

where  $\epsilon_0$  and  $\epsilon_r$  are the vacuum permittivity and low-frequency relative permittivity of the oxide,  $e$  is the electron charge,  $t_{ox}$  is the gate oxide thickness,  $t$  is the effective charge layer thickness, and  $V_{FB}$  is the flat band voltage of the MOS capacitor. Due to the free carrier plasma dispersion effect, the accumulated charges induce a refractive index change in the silicon. At a wavelength of  $1.55 \mu\text{m}$ , the index changes caused by electrons and holes, which were obtained from experimental absorption spectra through Kramers-Kronig analysis [xxxv], are given by

$$\Delta n_e = -8.8 \times 10^{-22} \Delta N_e \quad (2)$$

$$\Delta n_h = -8.5 \times 10^{-18} (\Delta N_h)^{0.8} \quad (3)$$

where electron and hole density changes are in units of  $\text{cm}^{-3}$ . The change in refractive index results in a phase shift  $\Delta\phi$  in the optical mode given by

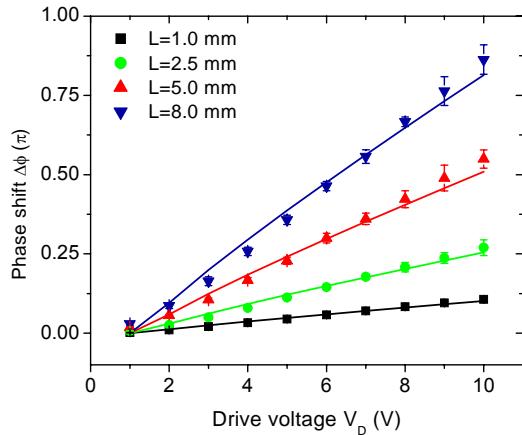
$$\Delta\phi = \frac{2\pi}{\lambda} \Delta n_{eff} L \quad (4)$$

where  $L$  is the length of the phase shifter,  $\lambda$  is the wavelength of light in free space, and  $\Delta n_{eff}$  is the effective index change in the waveguide, which is the difference between the effective indices of the waveguide phase shifter before and after charge accumulation. Because charge transport in the MOS capacitor is governed by majority carriers, device bandwidth is not limited by the relatively slow carrier recombination processes of pin diode devices. As a result, this capacitor-based design has allowed us to demonstrate bandwidth that is unprecedented in a silicon-based modulator.

## Technical Results

Phase shifter performance was evaluated in detail. Figure 10 shows the measured and modeled phase shift as a function of the drive voltage for different phase shifter lengths,  $L=1, 2.5, 5$ , and  $8 \text{ mm}$ . The phase measurement was performed in a free space interferometer. The data show good agreement between simulation and measurement for all phase shifter lengths. The measured phase shift is almost linearly dependent on the drive voltage. The data also confirm the linear dependence of the phase shift on the phase shifter length for a given drive voltage, as expected from equation (4). As a figure of merit, the product  $V_\pi L$  can be determined from the measured phase shift, where  $V_\pi$  is the drive voltage swing (or  $V_D - V_{FB}$ ) required for  $\pi$  phase shift and  $L$  is the device length. Using data in Figure 10, and taking into account the flat band voltage of  $V_{FB}=1.25 \text{ V}$ , we obtain a  $V_\pi L$

product for our current device of  $8 \text{ V cm}$ . The accumulation capacitance of the MOS structure was measured to be  $7 \text{ pF/mm}$  using an RF impedance analyzer.

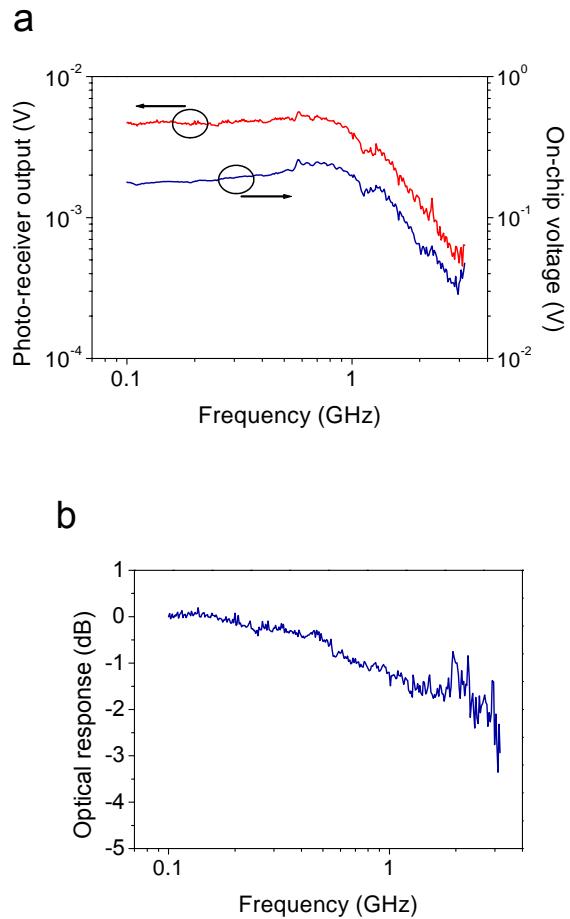


**Figure 10:** Phase shift  $\Delta\phi$  versus drive voltage  $V_D$  of the MOS capacitor phase shifter in Figure 9 at a wavelength of  $\lambda = 1.55 \mu\text{m}$  for different phase shifter lengths. The symbols represent the measured phase shifts, and the solid lines are the simulated phase shifts.

To facilitate laboratory testing, the arm lengths of the MZI of Figure 8 have been mismatched by  $\sim 16.7 \mu\text{m}$  allowing for tuning of the interferometer bias point via small adjustments to the input laser wavelength. For these asymmetric devices, wavelength adjustments of  $20 \text{ nm}$  or less are sufficient to tune the MZI bias but do not significantly affect other properties of the devices. Y junctions are used to split and combine the optical wave in the MZI, which has an overall length of  $1.5 \text{ cm}$ . To characterize the performance of our silicon MZI modulator, we measured the optical output intensity as a function of drive voltage for an MZI having a  $10 \text{ mm}$  phase shifter, in each arm. A slow voltage ramp was applied to one of the two phase shifters. The modulator showed an extinction ratio of more than  $16 \text{ dB}$  with an applied peak-to-trough voltage of  $\sim 7.7 \text{ V}$  which is close to the value of  $8 \text{ V.cm}$  predicted by the  $V_\pi L$  measurements. This device has an on-chip loss of  $\sim 6.7 \text{ dB}$ , which is mainly attributed to the doped polysilicon phase shifter and undoped polysilicon waveguide. The waveguide loss was measured using the cutback method [xxxvi].

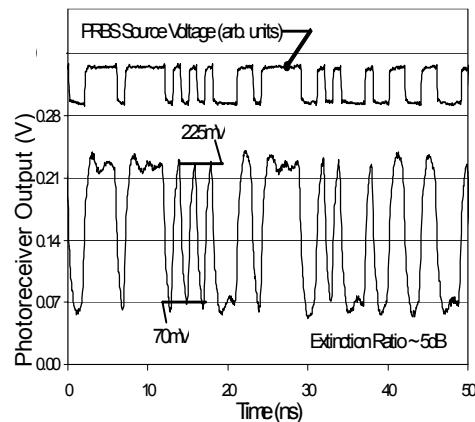
To determine the intrinsic bandwidth of the modulator, we performed a small-signal measurement using an MZI with a single  $2.5 \text{ mm}$  phase shifter. To ensure the MZI operates in a high-sensitivity region, an input wavelength of  $1.558 \mu\text{m}$  was chosen and the MOS capacitor was

biased into accumulation with  $3 \text{ V}_{\text{DC}}$ . A constant amplitude AC source was delivered to the  $17\text{pF}$  MOS capacitor through  $50\text{-ohm}$  coax cable, a short section of  $50\text{-ohm}$  PCB trace, and a simple network of resistors near the phase-shifter to form an approximate broadband  $50\text{-ohm}$  termination. Because of the non-ideal source termination, the voltage arriving at the phase shifter bond pad was monitored with a  $6 \text{ GHz}$  high-impedance oscilloscope probe. The output light was collected into a  $15 \text{ GHz}$  high-frequency photo-receiver and measured on an electrical spectrum analyzer. Figure 11(a) shows these measured values. The normalized response of the device (photo-receiver output/on-chip voltage) is presented in Figure 11(b) and shows that the phase shifter has an intrinsic bandwidth of approximately  $2.5 \text{ GHz}$  (as determined from the  $-3\text{dB}$  point).



**Figure 11 (a):** On-chip modulation voltage ( $V_{\text{RMS}}$ ) and photo-receiver output of an MZI containing a single  $2.5 \text{ mm}$  phase shifter (b): Phase shifter normalized response (photo-receiver output/on-chip voltage) showing an intrinsic bandwidth of approximately  $2.5 \text{ GHz}$ . The device was biased into accumulation with a  $3 \text{ V DC}$  bias.

To create a large-signal modulation, we used the MZI that has two 10 mm phase shifters. The MOS capacitor is again biased into accumulation with 3V<sub>DC</sub>. With an applied single-ended voltage swing of 1.6 V (3.2 V differential swing), the phase shifters should provide sufficient phase shift for the modulator to exhibit an extinction ratio of 5.8 dB when it is biased at quadrature. Figure 12 shows the optical response of the modulator driven with a 2<sup>32</sup>-1 pseudorandom bit sequence at 1 Gbps. The data show that the optical signal faithfully reproduces the electrical data stream. Furthermore, the measured high-frequency extinction ratio is 5 dB, which is close to the expected value.



**Figure 12: Output signal of a MZI driven with a 2<sup>32</sup>-1 pseudorandom bit sequence (PRBS) at 1 Gbps. The**

**MZI has two 1 cm phase shifters and is driven differentially with a total amplitude of 3.2 V (1.6 V single-ended). The RF extinction ratio is 5 dB. The input wavelength was chosen to bias the MZI at quadrature.**

### Challenges/Technical Hurdles

Our modulator with MOS capacitor phase shifters has demonstrated bandwidth performance previously unseen in silicon modulators, and modeling suggests that high-speed modulation at 10 GHz is achievable with design optimization. To realize such performance improvement, we need to overcome a number of technical challenges, two of which are discussed below.

As mentioned above, our current MZI modulator has an on-chip loss of ~6.7 dB, which is primarily due to the doped and undoped polysilicon regions in the waveguide. Because the polysilicon has a much larger optical loss than single-crystal silicon [xxxv], we can significantly reduce the present modulator loss by replacing the polysilicon region with single-crystal silicon. Modeling suggests that we can reduce the on-chip loss to ~2 dB by this method. Another approach to lowering on-chip loss is

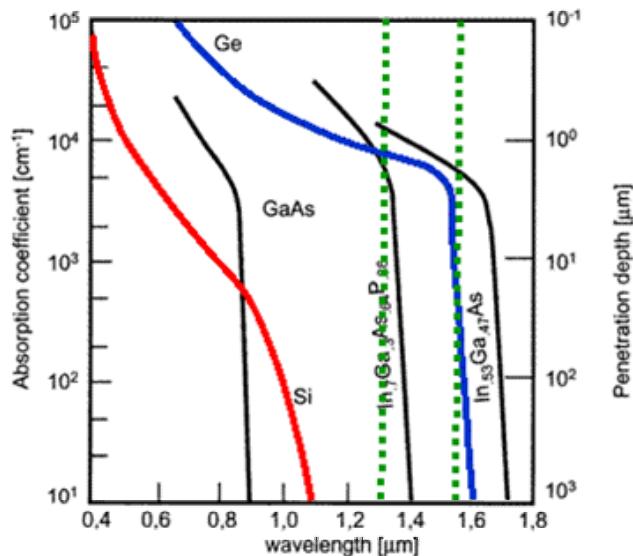
to create a graded doping profile in the *y* direction (Figure 9) in the waveguide phase shifter, while still maintaining the device speed. For example, we can design a phase shifter with higher doping densities in the areas close to the gate oxide and metal contacts, but with lower doping concentrations in the rest of the waveguide. Yet another approach is to reduce the active waveguide length required for  $\pi$  phase shift; in other words, increase the phase modulation efficiency. This can be done by reducing the waveguide dimensions, which will increase the interaction between the optical mode and the accumulated charges.

To improve bandwidth performance, the obvious thing to do is to lower device RC. This can be done by increasing the doping levels in the MOS capacitor and reducing the device size. For the moment, however, frequency response of our modulator is limited by other factors, which can be identified by taking another look at the data in Figure 11. The on-chip drive voltage drops to <50% of its low-frequency value at 1.5 GHz, despite the fact that the intrinsic bandwidth of the optical device is 2.5 GHz. Besides phase shifter capacitance, other contributors to this effect are the output impedance of the drive circuit used and interconnect parasitics. We have been actively engaged with circuit designers to tackle these driver issues. Furthermore, we are reducing the gate oxide thickness of our MOS capacitor to reduce the drive voltage requirements and high-frequency power dissipation.

### SI-BASED PHOTODETECTORS

The final active optical component that would need to be integrated onto an all-silicon optical platform is the photodetector. Silicon photodetectors have already found wide acceptance for visible light (0.400-0.700  $\mu\text{m}$ ) applications because of their near perfect efficiency at those wavelengths. However, most communication-grade semiconductor lasers are operating in the near infrared wavelength (usually 0.850, 1.310, and 1.550  $\mu\text{m}$ ), a region where silicon is a poor detector. In order to improve the performance of silicon-based detectors, the most common approach is to introduce germanium to reduce the bandgap and extend the maximum detectable wavelength. The effect on the absorption coefficient and penetration depth, defined as distance that light travels before the intensity falls to 36% (1/e), is clearly shown in Figure 13. The InGaAs material is typical of that used for commercial detectors at 1.310 and 1.550  $\mu\text{m}$ . Note that the data in Figure 13 represent unstrained bulk material with no voltage applied. By introducing strain or electrical bias, it is possible to shift the curves slightly to a higher wavelength due to a reduction in the effective bandgap. This could be critical for detection at 1.550  $\mu\text{m}$ , where a pure Ge film with the appropriate strain or bias

could potentially be shifted to reduce the penetration depth to acceptable values.



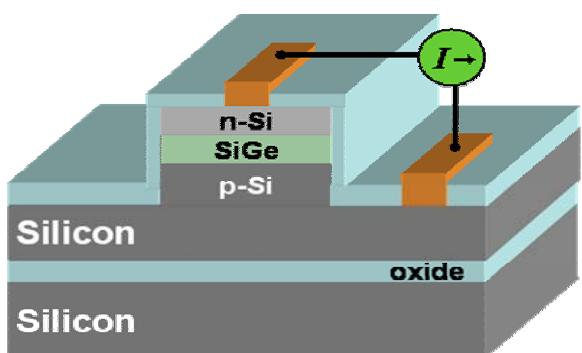
**Figure 13: Absorption coefficient and penetration depth of various bulk materials as a function of wavelength. The green lines mark the important wavelengths for telecommunications of 1.310 and 1.550  $\mu\text{m}$ .**

Two critical benchmarks for a photodetector are directly related to the absorption coefficient or penetration depth of the light; responsivity, and bandwidth. The responsivity is the ratio of collected photocurrent to the optical power incident on the detector. Responsivities for commercial III-V photodetectors are typically close to 0.8 A/W. Unless the detector is poorly designed, the responsivity should clearly increase as the absorption coefficient increases. The bandwidth of a photodetector can be limited by the transit time required for the photocarriers to travel to the contacts or the RC time constant. If the light penetrates 10  $\mu\text{m}$  into the material, for example, some photocarriers might have to travel 10  $\mu\text{m}$  back to the surface to be collected by a top contact. Typical photodetectors do not have an electric field extending that deep, so the carriers will slowly diffuse up, causing a significant low frequency component to the response. Good detector design eliminates the lethargic diffusion current by using very thin films that can be fully depleted to prevent the generation of diffusion current or effectively reducing the diffusion length of minority carriers. This has been done by using a second (and deeper) p-n junction to siphon off the slow carriers before they can reach the “real” collection junction or by introducing recombination sites near the depletion region to eliminate the carriers. The collection of the much faster drift current is then optimized by keeping the depletion

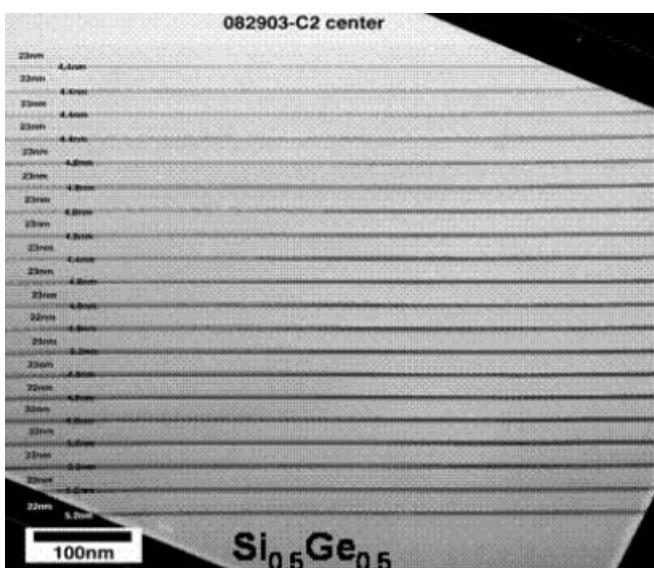
width as thin as possible as determined by the penetration depth. If the penetration depth can be kept to below 2  $\mu\text{m}$ , the transit time alone could support a bandwidth of 10 Gb/s.

The inherent tradeoff that is made in these devices when the light is incident from above them is that the electrical and optical distances are coupled. Maximizing the light absorption by making the layers thicker results in a reduction of bandwidth due to transit time issues. The way around this problem is to illuminate the device from the side. By doing this, the transit time can be kept low while the effective length of the detector is increased from a few micrometers to as long as a few millimeters. This is the approach used for waveguide-based photodetectors. Another advantage of the waveguide detector is its planar nature, which lends itself to integration with other optical devices.

We are using the same SOI platform as the modulator work to make SiGe waveguide-based photodetectors. A cross-section of this structure is shown in Figure 14 where the SiGe layer is directly on top of a silicon rib waveguide. Our initial detectors used 18  $\text{Si}_{0.5}\text{Ge}_{0.5}$  multiple quantum wells as the absorbing material, with a well thickness of 4 nm separated by 25 nm of silicon Figure 15. They were made on 2.5 and 4  $\mu\text{m}$  thick SOI wafers with waveguide widths varying between 2.5 and 15  $\mu\text{m}$ , and silicon rib etch depths sufficient to achieve multimode operation. The responsivity was as high as approximately 0.1 A/W at 1.319  $\mu\text{m}$  for some devices. We believe that this can be increased to 0.5 A/W through a combination of increasing the number of quantum wells, and changing the placement of the SiGe in the waveguide, among others. Further improvements to responsivity would entail increasing the germanium concentration in the quantum wells, forcing them to even thinner structures to prevent relaxation. This reduced area counters the higher absorption coefficient, pushing any performance gain into the region of diminishing returns. The bandwidth of the devices was limited to below 500 MHz due to a large offset in the valence band that hindered the transport of holes. This can be fixed by altering the film composition, and modeling predicts that data rates approaching 10 Gb/s could be possible. The advantage of this device structure is that it is fully strained, meaning that few, if any, defects are formed in the active SiGe material. These defects are known to increase the dark current of the device that reduce the Signal to Noise Ratio (SNR). Higher optical power would then be needed to compensate and achieve acceptable Bit Error Rates (BER). Our best devices had a dark current of less than 1  $\mu\text{A}$  ( $<1 \text{nA}/\mu\text{m}^2$ ) at 3 V, which is acceptable for most applications. For comparison, InGaAs pin photodetectors typically have dark currents close to 1 nA.



**Figure 14:**  $\text{Si}_{1-x}\text{Ge}_x$  waveguide-based photodetector on a SOI wafer. The waveguide is formed by the ridge of p-Si material and is running perpendicular to the cross-section. The SiGe MQW are inside the region labeled SiGe in the picture.



**Figure 15:** TEM cross-section of a  $\text{Si}_{1-x}\text{Ge}_x$  MQW film. The dark regions are the SiGe multiple quantum wells.

### Integration Issues with Germanium

The amount of germanium required for efficient photodetection is dependent on the wavelength. If detection at 1.310 or 1.550  $\mu\text{m}$  is desired, then very high (>40%) germanium concentrations are needed. This is much higher than that found in SiGe Heterojunction Bipolar Transistors (HBTs) or strained silicon, and as a result new integration issues have to be dealt with in the fab, including strain and stability.

Since most useful strained  $\text{Si}_{1-x}\text{Ge}_x$  films are metastable with respect to defect formation, exposing the wafer to high temperatures after growth can be problematic. Certainly, long times at temperatures above the growth

temperature (550-650° C) should be avoided. Higher temperatures might be possible for short times, such as in rapid thermal annealing, but this is conditional on the film quality. Amorphous, poly-crystalline, or relaxed single crystal films will not have this temperature limitation.

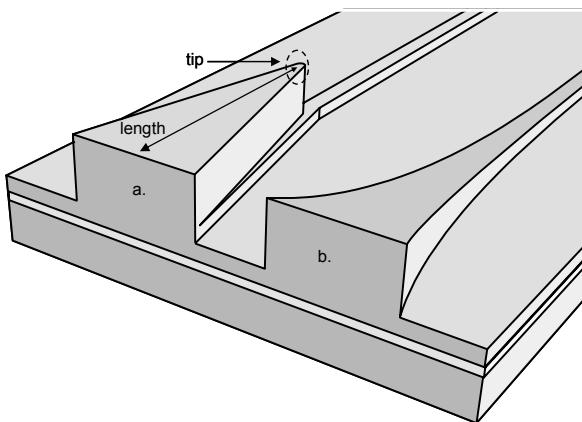
Chemical stability is also an issue for films with high germanium concentration. Since germanium does not form a stable oxide like silicon does when exposed to oxidizing chemicals, the SiGe films tend to be susceptible to corrosion during wet cleans or Chemo-Mechanical Polishing (CMP). We have developed alternate processing modules to accommodate for the difference and maintain the integrity of the SiGe films.

### OPTICAL COUPLING AND PACKAGING

One of the most difficult challenges facing high-index contrast optical systems is efficiently coupling light into and out of the chip. Particularly difficult is the coupling of light from a standard optical fiber or external light source to a silicon waveguide. Overcoming these challenges requires the development of processes and structures in addition to the core device.

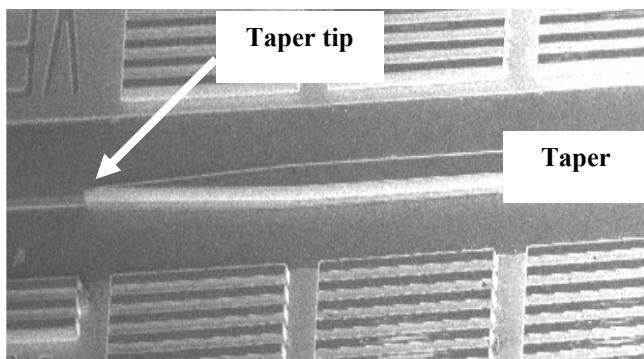
### Tapers

A single-mode fiber core ( $n = 1.5$ ) usually has a diameter of 8  $\mu\text{m}$  with a symmetric mode while a silicon waveguide ( $n = 3.45$ ) is typically only a few micrometers in width with an asymmetric mode. To overcome these large differences in effective index, core size, and symmetry, one frequently used method is to employ a waveguide taper. Tapers allow for a reduction in coupling loss through an adiabatic modal transformation and can also be used to increase the alignment tolerance of other optical devices, such as III-V lasers. Several taper methods have been proposed and have demonstrated efficient coupling from a relatively large silicon waveguide into an optical fiber. Two of these methods are (1) pseudo-vertical tapering and (2) gradual horizontal and vertical modal tapering using gray-scale lithography. Figure 16 is a schematic depiction of these two mode transform designs. Pseudo-vertical tapering from a 12  $\mu\text{m}$  by 12  $\mu\text{m}$  input to 4-5  $\mu\text{m}$  waveguides has demonstrated losses as low as 0.5 dB/facet [xxxvii].



**Figure 16: Schematic of (a) pseudo-vertical tapering and (b) 3D gray-scale taper into an SOI-based waveguide**

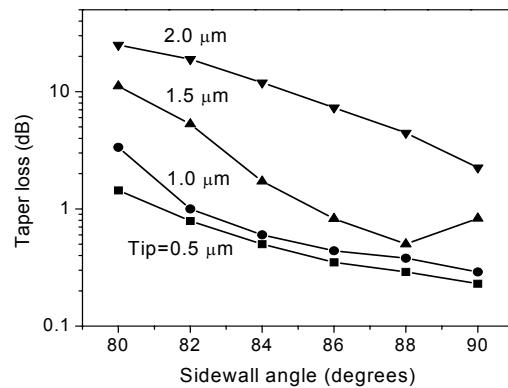
The key processing parameters essential to the success of either mode-transfer device are the lithography and etching processes. For pseudo-vertical tapering, a horizontally tapered waveguide is patterned on top of another waveguide and the optical mode is gradually squeezed from the top taper to the smaller, lower waveguide. The most important parameters for this transition are the length of the taper (the longer the length the more slowly one can transform the mode resulting in lower loss) and the taper tip width (see Figure 16a). In order to reduce optical losses associated with the finite size of the tip width, the tip should be designed such that the minimum width is substantially smaller than the wavelength of light transmitted in the waveguide. Figure 17 shows a Scanning Electron Micrograph (SEM) image of a pseudo-vertical taper patterned onto a Si waveguide at Intel Corporation.



**Figure 17: Scanning Electron Micrograph of a pseudo-vertical taper patterned on top of a silicon waveguide**

Optimally, the tip width should be small enough to not support an optical mode in the tip region. For

wavelengths of interest around  $\lambda_o \approx 1.550 \mu\text{m}$ , this corresponds to a wavelength in silicon of about  $\lambda \approx 0.450 \mu\text{m}$ . This final tip dependency is very critical, and the effect of tip width variation on taper loss is shown in Figure 18.



**Figure 18: Plot of pseudo-vertical taper loss as a function of sidewall angle for several tip widths**

The plot shows results of simulation of a pseudo-vertical taper design starting from 10 μm by 10 μm and tapering down to 2.5 μm by 2.3 μm, performed by using a commercial software package called BeamPROP [xxxviii], which incorporates finite-difference beam propagation techniques. For this simulation, the loss due to sidewall roughness was assumed to be zero, the taper length was set equal to 1 mm, and a free space wavelength of 1.550 μm was used. One can see from Figure 18 that for a fixed side wall angle of 80°, a change in tip width from 2 μm to 0.5 μm improves the total taper loss by more than 20 dB. Unfortunately, to fabricate such a taper, lithographic patterning and photo resist capabilities are not enough. In order to complete the process, etching these taper devices invariably leads to some rounding of all sharp edges, which inhibits processing the designed sharp point.

In the case of gray-scale techniques, appropriate resists and etch recipes must be created and controlled to provide smooth surfaces and a slow variation of the height of the taper from the input down to the final waveguide dimension. The technique of gray-scale lithography has been known for several years and is widely used in optical Micro Electrical Mechanical Systems (MEMS) to create lenses, prisms, and various other structures [xxxix]. However, gray-scale-based lithography adds additional complexity and cost. A gray-scale reticle is several times more expensive than a standard lithography reticle, and process tweaking to develop and pattern the resist is more complicated than standard processing. Although,

fundamentally, tapers based on gray-scale should result in much lower loss, these types of tapers have not been as prominent as top (pseudo-vertical) tapers.

Another key parameter for processing tapers is that of sidewall roughness and sidewall angle as a result of the silicon etch. Creating taper devices usually relies on significant etching away of silicon material in order to produce the final taper design. Although one can use wet-chemistry for etching, it is often difficult to control and not practical, especially if one would like to obtain vertical sidewalls or more exotic profiles, such as a parabolic design. Thus the most common approach is Reactive Ion Etching (RIE). RIE also has its drawbacks, however, as it produces surface roughness on the exposed sidewall. Since the optical loss due to surface roughness is strongly dependent on waveguide size, the loss due to roughness should be minimal at the beginning of the taper since the taper dimension is large. At the taper end, however, the waveguide becomes smaller and the loss contribution from the roughness becomes larger. Therefore, it is critical to control the surface roughness at the smaller end of the taper. Techniques to reduce loss have been proposed and demonstrated, which involve smoothing waveguides by use of repeated oxidation and stripping steps [xl,xli]. However, oxide smoothing also results in rounding of sharp points which could add additional loss due to tip width rounding.

Another approach to reduce the effect due to surface roughness would be to pattern the taper into a thick Low Temperature Oxide (LTO) layer and then grow the taper using an epitaxial growth step. This may result in lower loss due to the reduction of the silicon etch step but adds complexity into the process which may jeopardize the entire process flow, as discussed previously.

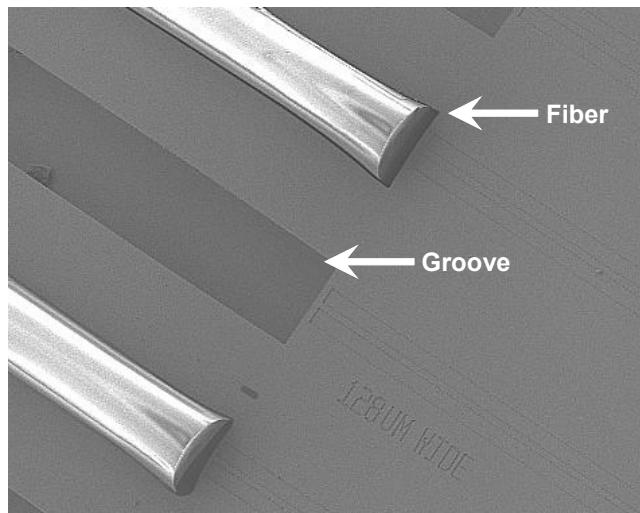
In addition to surface roughness one must monitor the resulting sidewall angle of the pseudo-vertical taper after silicon etching is complete. Figure 19 shows the effect of the sidewall angle variation from 90° to 80° can increase the loss by up to 20 dB for a given tip width.

Top tapers have been successful for coupling to waveguides with cross-sectional dimensions of 4-5  $\mu\text{m}$ , but modeling suggests that these designs may not work well when the waveguides are smaller than 2  $\mu\text{m}$ . This is true even with a tip width as small as 0.05  $\mu\text{m}$  and a tapering length of 5.2 mm. Thus a different approach must be used for coupling to very small waveguides (on the order of 1  $\mu\text{m}$  or less) to standard optical fibers. Alternative approaches have recently been proposed for coupling to sub-micron waveguides, including the use of grating assisted couplers [xlii] and inverted tapers [xliii].

## Fiber Attach

In order to integrate the optical devices, discussed in this paper, into optical networks, they must be integrated with fibers. As discussed in the previous section, the small waveguide dimensions and high index contrast of the silicon system lead to a fundamental difference in the optical mode profile between the waveguide and fiber. The integration of waveguide tapers at the waveguide/fiber interface can solve this problem.

Current fiber attach techniques are “active,” relying upon the closed loop optimization of fiber position in order to ensure low loss coupling. This technique is time consuming however and hence costly. Passive alignment techniques for fiber attachment remove the need for closed-loop optimization by creating highly precise lithographically defined structures on the silicon surface in order to align the fiber to the waveguide aperture. A photograph of passively aligned fibers using an etched U-shaped groove processed by Intel is shown below in Figure 19.



**Figure 19: Scanning Electron Micrograph of several U-grooves, two of which are populated with optical fibers and aligned to silicon waveguides**

Active alignment techniques are typically capable of placement tolerances better than 1  $\mu\text{m}$ . The accuracy required of a passive alignment technique will depend upon the mode field overlap of the fiber and waveguide modes, which can be controlled by the waveguide tapers, discussed in the earlier section. As an example, the lateral alignment tolerance of an 8  $\mu\text{m}$  single-mode fiber core to a 13  $\mu\text{m} \times$  13  $\mu\text{m}$  square waveguide input facet was modeled using FIMMPROP<sup>®</sup>[xliv]. The modeled results, based on film mode matching and local mode expansion methods, indicate that the lateral alignment tolerance is ~1.7  $\mu\text{m}$  for 1 dB excess loss. By increasing the input taper to 15  $\mu\text{m}$  by 15  $\mu\text{m}$ , the alignment tolerance is

increased by over 50% to  $\sim 2.6 \mu\text{m}$ . The achievable accuracy of the passive alignment technique will depend upon both the processing tolerance of the etched U-groove and also upon the manufacturing tolerance of the fiber. Widely accepted fiber specifications define the fiber diameter to  $\pm 1 \mu\text{m}$  of accuracy; newer fibers are specified to  $\sim \pm 0.3 \mu\text{m}$  of accuracy. The combination of the waveguide tapers and tightly specified fiber will require that the trench dimensions be defined to  $\sim 1\text{-}2 \mu\text{m}$  of accuracy, a challenging although not unrealizable goal. Additionally the large index contrast of the silicon waveguide will result in a reflection of  $\sim 30\%$  at each silicon/air interface unless an anti-reflection (AR) coating is used. The etched facets created in the passive alignment process for fiber attachment are readily amenable to wafer scale AR coating using standard dielectric films available in a CMOS fab.

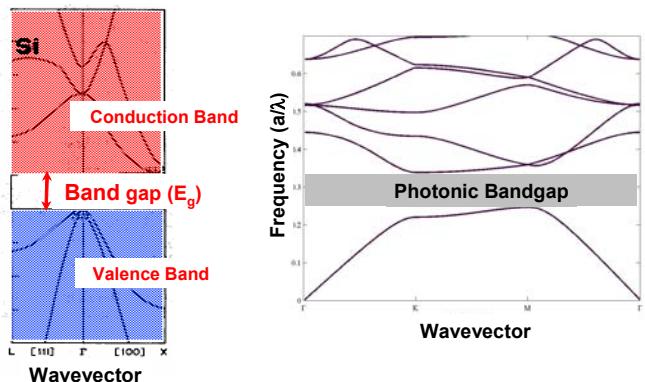
## FUTURE POSSIBILITIES

We now look ahead at two next-generation optical devices in silicon, examining opportunities for additional miniaturization and functionality of optical components.

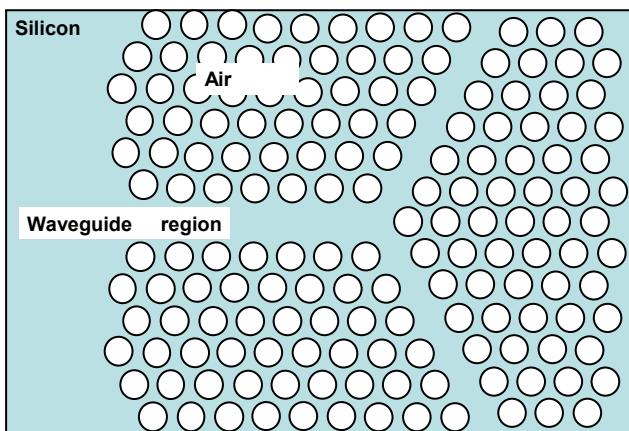
Unlike the case for silicon electronics, significant changes to silicon photonics cannot be brought about through direct scaling and reduction of Critical Dimensions (CDs). Rather, changes to the underlying physics of operation will be needed to radically change optical device designs. Some of the more recent developments in materials processing have helped develop an area of research focused on devices using critical dimensions on the order of nanometers. In the current landscape of silicon photonics, two “nano-photonics” technologies are of particular interest: Photonic Crystals (PCs) and Ring Resonators (RRs).

### Photonic Crystals

Photonic crystals are the optical analog to electronic semiconductor crystals. Through the periodic arrangement of two materials with dissimilar dielectric constants, a PC will exhibit a band of forbidden frequencies of propagation (Photonic Band Gap (PBG)). This PBG is analogous to the forbidden energy gap of semiconductors; just as forbidden electronic states are due to the periodic arrangement of atoms in a crystalline lattice, the periodic arrangement of dielectrics on the order of the wavelength of light creates an optical gap (see Figure 20). The most common example of a PC is a 1-dimensional Bragg grating for which a forbidden optical gap or “stop-band” is achieved. For most 2-dimensional planar SOI-based PBG waveguides, a triangular lattice of holes in silicon is used (see Figure 21).



**Figure 20:** Examples of (a) electrical energy band gap for a semiconductor (silicon), and (b) a photonic band gap for a photonic crystal, where  $a$  is the pitch of the lattice



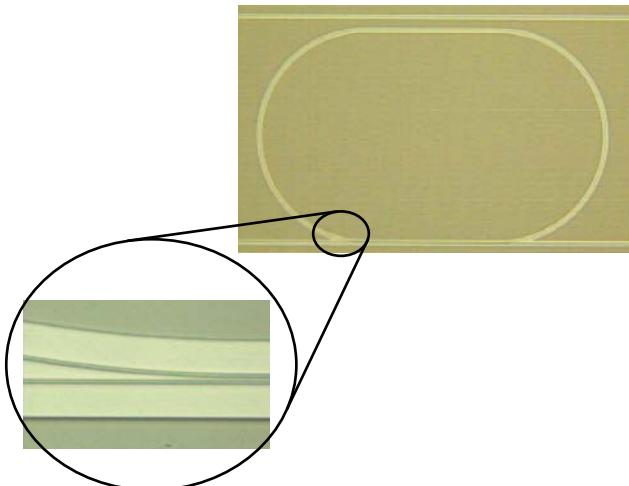
**Figure 21:** Schematic (plan view) of a Photonic crystal comprised of holes arranged in a triangular lattice in silicon

Photonic crystals have been gaining considerable research attention since reports by researchers working in silicon were brought to mainstream attention. Their dispersive properties and nonlinear optical effects, combined with the promise to drastically reduce the dimensions of common optical designs are fueling many of the PC research efforts found in literature today, such as super prisms [xlv,xlvi,xlvii] and ultra-low threshold lasers [xlviii,xlix]. Almost all research conducted in 2-dimensional planar PCs designed for  $1.55 \mu\text{m}$  and  $1.31 \mu\text{m}$  light are processed using e-beam lithography. Several advantages of research e-beam lithography systems (e.g., Raith 150) are their relatively low cost, ability to pattern  $< 20 \text{ nm}$  features, and their ease of use for processing pieces of wafers. The same e-beam system can have patterning times of 30 minutes or more for a  $10 \mu\text{m m}^2$  field with a 50% pattern density of 100 nm minimum feature sizes. Most PC structures (holes) designed for  $1.55$  and  $1.31 \mu\text{m}$

light are of similar dimensions/design rules as those for 0.130  $\mu\text{m}$  and 0.090  $\mu\text{m}$  CMOS transistor designs. One group at the Interuniversity Micro-Electronics Center (IMEC) in Belgium has fabricated PCs with conventional Deep-UV Lithography and Reactive Ion Etch techniques [I]. Their successes with 0.18  $\mu\text{m}$  technology node tools have demonstrated a compatibility with PC designs. This in turn has brought increased attention to the possibility of pursuing PC research in a modern high-volume fab. The only additional complexity to optical lithography-based patterning of PCs vs. e-beam patterning is that for 1.55 and 1.31  $\mu\text{m}$  PC designs, CD control requires Optical Proximity Correction (OPC) to design layouts. Overall, standard optical lithography can deliver equal or better results than most research e-beam systems for today's planar optical designs. In addition, by using standard fab equipment, PC designs-of-experiments can be dramatically expanded by skewing lithography and etch parameters across one experimental run. The most challenging processing problems that face PCs, whether fabricated using e-beam or DUV lithography, are coupling losses and optical loss through the waveguides. Several groups have managed to demonstrate relatively low-loss couplers to these small waveguide designs [Ii, Iii]. Recently, researchers at IBM managed to create PC waveguides in SOI with transmission losses as low as 20 dB/cm [Iiii].

## Ring Resonators

Optical Ring Resonators (RRs) are useful components for wavelength filtering, multiplexing, switching, and modulation. The key performance characteristics of the RR includes the Free-Spectral Range (FSR), the finesse (or Q factor), the resonance transmission, and the extinction ratio. These quantities depend not only on the device design but also on the fabrication tolerance. Although state-of-the-art lithography may not be required for most conventional waveguide designs, RR and PC designs require CD values at or below 100 nm.



**Figure 22: Example of a Ring Resonator device fabricated in silicon. The expanded region in the inset shows the separation between the straight “bus” and the resonator “ring.”**

For such designs, resolution and CD control are both important to the success of the devices. In the case of Si-based ring resonators, one of the critical parameters to control is the coupling efficiency between the RR and the input/output waveguide. As a compact waveguide (for example, 220 nm x 500 nm strip waveguide) is usually used in the RR to obtain a large FSR, the gap between the ring and bus waveguide is 100-200 nm (inset of Figure 22). Since the device operates through evanescent coupling, the coupling is exponentially dependent on the size of the separating gap. Thus, in order to reliably process high-Q RR devices, control of a few nm demands CD control readily achieved by modern 0.18  $\mu\text{m}$  or 0.13  $\mu\text{m}$  lithography.

## CONCLUSION

Although research in the area of planar optics in silicon has been underway for several decades, recent efforts at Intel Corporation have provided better understanding of the capabilities of such devices as silicon modulators, ECLs, and SiGe detectors. Incorporating silicon in an ECL opens a path towards hybrid silicon photonic integration, or even a Silicon Optical Bench (SiOB) platform for silicon photonics. Silicon modulators operating at 2.5 GHz have demonstrated two orders of magnitude improvement over other known si-based modulators, with theoretical modeling indicating performance capabilities beyond 10 GHz. And initial results from SiGe photodetectors have shown the feasibility of monolithically integrated waveguide detectors. Through further research and demonstration of novel silicon photonics devices, we hope to continue bringing the vision of integrated silicon photonics into focus as a viable future for commercial opto-electronics.

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# Indium Phosphide-Based Optoelectronic Wavelength Conversion for High-Speed Optical Networks

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Index words: optical, wavelength conversion, monolithic, indium phosphide, tunable

## ABSTRACT

Monolithic approaches to wavelength converters have been demonstrated and show promise to allow for the high-speed conversion of one wavelength to another without requiring the signal to pass through off-chip electronics. In this paper, we describe our research, undertaken jointly with the University of California at Santa Barbara and with Stanford University, into novel approaches for monolithically integrating Wavelength Converters (WCs) in Indium Phosphide.

In the first approach, undertaken jointly with the University of California at Santa Barbara, we describe Photonic-IC (PIC) tunable wavelength converters that are based on a photodiode receiver integrated with a tunable laser transmitter. Devices are fabricated on a robust InP ridge/InGaAsP waveguide platform. The photodiode receiver consists of an integrated optical pre-amplifier and a pin photodiode to improve sensitivity. The laser transmitter consists of a 1550 nm widely tunable Sampled Grating Distributed Bragg Reflector (SGDBR) laser modulated either directly or via an integrated modulator outside the laser cavity. An optical post-amplifier provides high output power. The Photonic-IC (PIC) tunable WC (PIC-WC) device allows signal monitoring,

transmits at 2.5 Gb/s, and removes the requirements for filtering the input wavelength at the output. Integrating the widely tunable laser on-chip yields a compact wavelength agile source that requires only two fiber connections, and no off-chip high-speed electrical connections.

In the second approach, undertaken jointly with Stanford University, we present a compact, low-power, dual-diode photonic switch architecture that allows for scalable multi-channel wavelength conversion. These photonic switches are scaled into a two-dimensional array to construct the first wavelength-converting crossbar switch on a single chip. Each of the wavelength-converting switches in the crossbar consists of an InGaAsP/InP quantum-well waveguide modulator monolithically integrated with a surface-normal InGaAs photodiode in its close vicinity as a part of a novel integrated optoelectronic circuit. The confinement of optically induced high-speed electrical signals within the lumped circuit elements of each switch node leads to efficient wavelength conversion, requiring low optical input power (mW range) for high extinction ratio (>10 dB), and eliminating the need for on-chip transmission lines and off-chip high-speed electrical connections. In addition to optical switching, the ability to enable and disable the

switch nodes electrically further allows for the electrical reconfiguration of the wavelength-converting crossbar switch as necessary. Experimental demonstrations include unlimited wavelength conversion at 2.5 Gb/s using single switch elements and multi-channel wavelength conversion at 1.25 Gb/s using 2x2 crossbar switches, all exhibiting >10 dB extinction ratio and spanning the entire C-band. Theoretical analysis predicts the feasibility of operation at 10 Gb/s with a 10 dB extinction ratio.

## INTRODUCTION

The high-speed fiber optic network of today forms the backbone of the Internet. As the Internet data bandwidth continues to climb, the optical devices used to manipulate these data must demonstrate increased line data rates, functionality, and efficiency while maintaining small size and low cost. Wavelength Converters (WC) represent a novel class of highly sophisticated photonic integrated circuits that are crucial in the function of future optical networks [1]. They allow for the manipulation of wavelengths in Wavelength Division Multiplexing (WDM) optical switches, routers, and add/drop multiplexers.

A key application of WCs is in all-optical “wavelength continuous” networks. In such networks, the interconnection between two nodes (typically optical fiber) is fixed to a given wavelength that cannot be changed along the route. Any new connection to the network must use a different wavelength; if a new connection uses a wavelength already allocated to another connection, it is blocked. Two connections cannot use the same wavelength on a given portion of the same fiber. Wavelength conversion at the nodes of the networks enables the network to avoid this “wavelength-continuity constraint” improving efficiency and flexibility.

The lowest risk and also the most expensive and bulky implementation of wavelength conversion is the use of an Optical/Electrical/Optical (O/E/O) line card that incorporates a tunable laser for its output. The additional problem with this approach is that because of the digital regeneration circuits, the line card typically only functions at a particular data rate. Such O/E/O line cards may be undesirable, because they are one of the major high-cost items that have thwarted the scaling down of system costs as needed to bring optical networking, especially WDM networking, into the metropolitan and local area distribution networks.

Many different implementations of non-tunable WCs have been proposed: using Cross-Phase Modulation (XPM) in Semiconductor Optical Amplifiers (SOAs), fiber [2,3], and Cross Absorption Modulation (XAM) in Electro-Absorption Modulators (EAMs) [4,5]. In our previous work, we have demonstrated photocurrent-

driven WCs utilizing a photodiode driving a laser or a modulator [5,6,7]. High-speed integrated photodiodes and EAMs suitable for wavelength conversion have also been previously proposed [8]. Many of these architectures have been demonstrated to perform digital signal regeneration—including improvements in extinction ratio, signal to noise ratio, pulse width control, etc. The SOA Mach-Zehnder interferometer (SOA-MZI) WC is another important class of tunable integrated WC that also implements the significant feature of digital signal regeneration [9,10]. Instead of being photocurrent driven, the SOA-MZI WC is based upon the XPM, where all of the light interaction between the original data and the new signal takes place in the one arm of an MZI. These previous demonstrations of WCs exhibited promising results for a single-channel operation [2-8]; however, a multi-channel wavelength conversion system has not been previously proposed.

In this paper, we first describe our work at the University of California at Santa Barbara on *tunable* photocurrent driven WCs made by monolithically integrating a widely tunable laser source with detectors and modulators. Next, we discuss our work at Stanford University based on a scalable, compact, dual-diode optical switch suitable for reconfigurable multi-channel wavelength conversion.

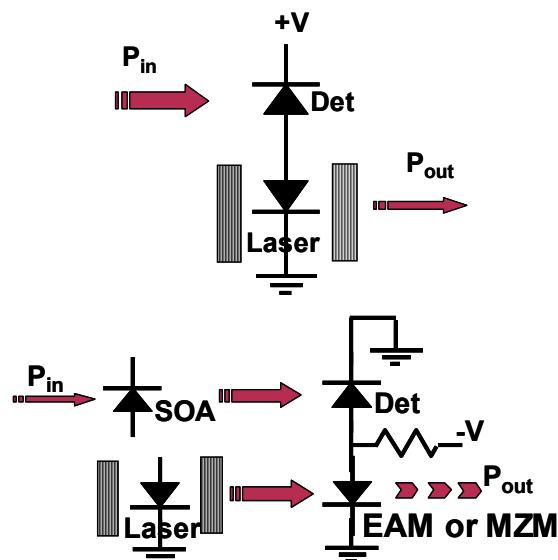
## WIDELY TUNABLE APPROACH (UCSB)

### Design

The simplest photocurrent-driven wavelength converter (PD-WC) consists of a photodiode receiver directly modulating a laser diode (Figure 1 top). Optical input is incident upon a reverse-biased photodiode, which generates a photocurrent directly modulating the gain section of an integrated tunable laser. The Sampled Grating Distributed Bragg Reflector (SGDBR) tunable laser is a four-section device consisting of SGDBR front and rear mirrors and phase and gain sections [11]. A separate DC electrode connected to the gain section can bias the laser to a level suitable for high output extinction. Above threshold, the directly modulated design affords linear operation, which is important for applications in analog links. In this approach, the extinction ratio of the converted output is proportional to the photocurrent, and the laser differential efficiency. In order to improve the extinction ratio, we implement integrated optical pre-amplifiers with on-chip Semiconductor Optical Amplifiers (SOAs) to generate increased photocurrent.

Modulation bandwidth of the directly modulated PD-WC is limited by the relaxation resonance frequency of the laser, typically ~6 GHz. External modulation of the laser, via an Electro-Absorption Modulator (EAM) or a Mach-Zehnder Modulator (MZM), represents a second important class of tunable photocurrent-driven WC

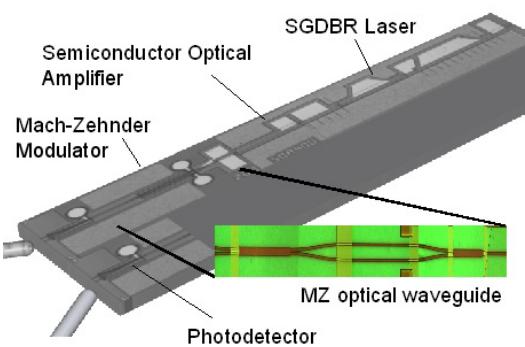
approaches (Figure 1 bottom). In these configurations, the photocurrent generates a voltage via a load resistor, which in turn modulates the transmission of the light through an EAM or MZM. Utilizing either EAMs or MZMs may lower the photocurrent requirements and offer reduced (and perhaps tunable) chirp, suitable for higher data rates.



**Figure 1: Schematic of UCSB Tunable WCs in direct modulation (top) and external modulation (bottom) implementations**

## Fabrication

The UCSB design uses a quaternary InGaAsP waveguide structure for the laser, modulator, amplifier, and photodetector sections grown on a semi-insulating Fe-doped InP substrate. Removing conducting semiconductor down to the semi-insulating substrate between the two ridges electrically isolates the ridge waveguides for the photodetector and laser sections. An N+ InGaAs layer underneath the quaternary waveguide material provides contacts to the n side of the diodes. The optically passive sections are formed by etching off the offset quantum wells down to the 10nm InP stop-etch layer prior to blanket InP regrowth. Completed devices vary in size depending on the specific design and are typically 0.5 mm wide and 2.5 to 3.5 mm long. An example micrograph of a fabricated wavelength converter with an SGDBR laser, MZM, and receiver is shown in Figure 2. More details on fabrication can be found in Reference 12.

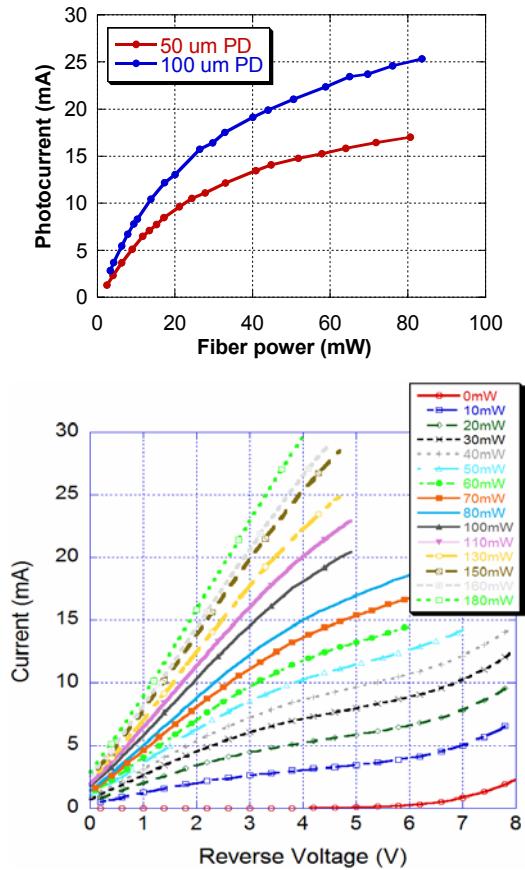


**Figure 2: Fabricated MZM WC ( $\sim 0.5$  mm x 3 mm)**

## RESULTS

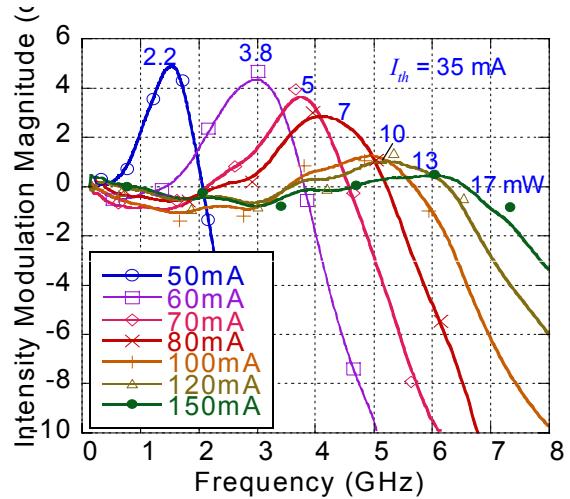
### Laser, Receivers, and Modulators

Crucial to the operation of photocurrent-driven WCs is a high-efficiency receiver. Two types of photodiodes have been investigated: bulk absorbers, utilizing the Franz-Keldysh (FK) effect, and Quantum Well (QW) absorbers, utilizing the quantum confined Stark effect. Figure 3 (top) shows the detected photocurrent of an optically pre-amplified QW photodiode of 50 and 100  $\mu\text{m}$  length. Current saturation is observed and is due to both power saturation in the SOA and QW band filling. An improved saturation photodetector can be fabricated using FK effect absorption. Figure 3 (bottom) shows the detected photocurrent vs. reverse bias for different fiber optical power levels for such a device, without any optical pre-amplification on chip. No saturation is observed up to photocurrents of at least 30 mA. Others using the same structure have observed even higher saturation currents, up to 70 mA [13]. Coupling efficiency from the lensed fiber to the waveguide mode was  $\sim 25\%$ . Note that the QW photodiodes incorporate an on-chip SOA preamp, and the bulk photodiodes do not.



**Figure 3: Photodiode optical response for quantum-well photodiodes of 2 lengths with 350  $\mu\text{m}$  SOA preamp (top) and bulk photodiodes (200  $\mu\text{m}$  long, No SOA preamp)**

Figure 4 shows the modulation bandwidth of the directly modulated SGDBR tunable laser. The relaxation resonance frequency of the laser limits the modulation bandwidth to a few GHz. To obtain a flat bandwidth response to above 2.5 GHz, the laser must be DC biased at least to 100 mA. For directly modulated wavelength converters, the resulting extinction ratio is limited by the available photocurrent from the receiver.

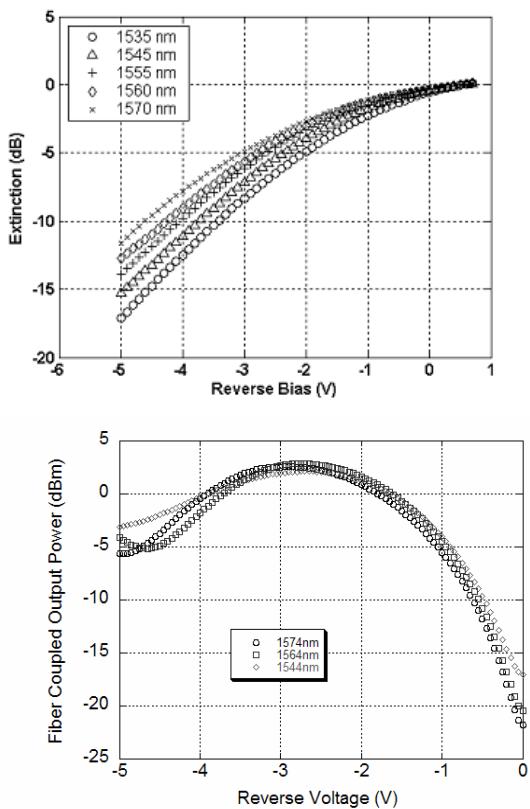


**Figure 4: SGDBR laser direct modulation bandwidth**

For improved chirp and larger extinction, WCs incorporating external modulators become attractive. In our implementation, we achieve external modulation in the WC with a DC-biased SGDBR laser followed by an EAM or MZM. The transmission of the modulator is varied through an applied voltage that is developed across a  $50 \Omega$  load resistor connected in parallel with the EAM/MZM and the photodetector. As discrete components, one crucial figure of merit for modulators is modulation efficiency in dB/Volt. Figure 5 (top) shows the extinction of a bulk FK EAM and Figure 5 (bottom) shows the extinction vs. bias for an MZM. The maximum obtained EAM efficiency for a 10 dB transmission loss is  $\sim 5 \text{ dB/V}$  at 1535 nm for a 200  $\mu\text{m}$  long EAM; the efficiency drops as the wavelength moves away from the waveguide absorption edge. Higher modulation efficiencies can be achieved, but at the expense of a larger insertion loss. The MZM exhibits an increased  $\sim 15 \text{ dB/V}$  modulation efficiency, at the expense of device area and complexity, compared to the EAM.

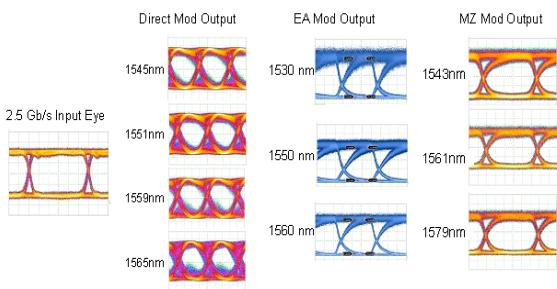
## 2.5 Gb/s Wavelength Conversion

All of the WC implementations were successfully fabricated and were tested using a 2.5 Gb/s Non-Return to Zero (NRZ) optical input signal. Figure 6 shows input and output eye diagrams at 2.5 Gb/s for the directly modulated WC, the EAM WC, and the MZM WC. All three demonstrated clearly open eyes at 2.5 Gb/s NRZ data rates across at least a 20 nm SGDBR laser tuning range. Extinction ratio for the directly modulated WC was  $\sim 3 \text{ dB}$  as the photocurrent was limited in fully integrated devices, due to a fabrication error resulting in higher than expected contact resistance. The extinction ratio for the EAM WC and MZM-WC devices was  $> 10 \text{ dB}$  for all wavelengths.



**Figure 5:** Extinction vs. bias for a 200  $\mu\text{m}$  long EAM (top) and a MZM with 200  $\mu\text{m}$  long electrodes (bottom)

All of the WC approaches fabricated demonstrated error-free operation at 10<sup>-9</sup> Bit-Error Rate (BER) with a 2.5 Gb/s 2<sup>31</sup>-1 Pseudo Random Bit Stream (PRBS) signal. Power penalties compared to back-to-back operation without a WC were 6 dB, 1-2 dB, and < 1 dB for the directly modulated WC, EAM, and MZM WC, respectively. The larger power penalty for the directly modulated WC was due to the lower than expected photocurrent and consequently extinction, due to undesirable heating resulting from a fabrication error.

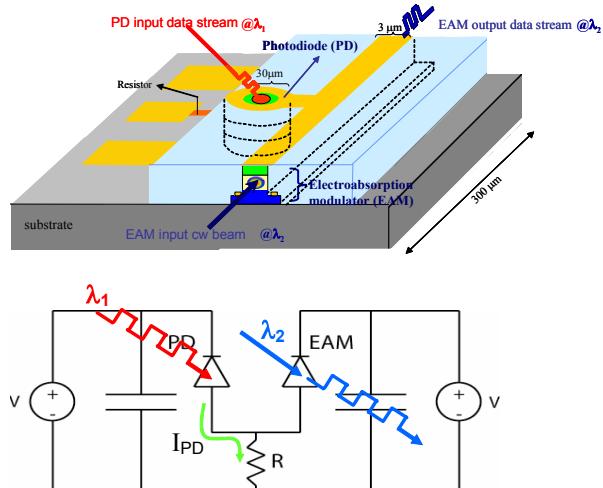


**Figure 6:** WC output eye diagrams with 2.5 Gb/s NRZ input signal

## SCALABLE APPROACH (STANFORD)

### Design and Fabrication

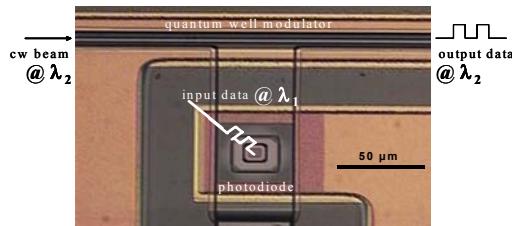
The approach taken by the Stanford team is based on the *intimate* integration of an electroabsorption modulator with a photodiode into a compact wavelength-converting switch [8]. Figure 7a illustrates such a dual-diode switch structure that incorporates a waveguide modulator diode and a surface-illuminated photodiode integrated as a part of the novel on-chip lumped optoelectronic circuit shown in Figure 7b. This dual-diode switch is designed to confine the optically generated high-speed electrical signals within its integrated circuit. The localization of the optical switching yields efficient wavelength conversion with a low optical input power requirement (mW range) to achieve high extinction ratios (> 10 dB). Furthermore, this photonic switch architecture naturally leads to a two-dimensional integrated array of these photonic switches to implement a reconfigurable wavelength-converting crossbar switch [14]. Such a photonic switch architecture also provides a convenient photonic integration platform; for example, a (tunable) laser diode and an optical semiconductor amplifier could be conveniently incorporated into the switch because of the fabrication compatibility, if desired [15].



**Figure 7 (a):** A schematic of dual-diode photonic switch, and (b) its simplified circuit diagram

These wavelength-converting switches are completely insensitive to input signal polarization due to the surface-normal input configuration. They operate over a wide range of wavelengths (e.g., over the C-band) because of the broad-band absorption of the InGaAs photodiode and because of the electroabsorption of the InGaAsP/InP quantum-well modulator that is shifted and broadened with the application of DC bias. These switches provide unconstrained, bi-directional wavelength conversion and multi-wavelength broadcasting in the C-band.

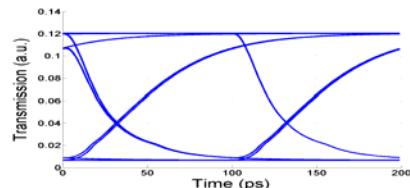
Figure 7b shows a simplified circuit diagram of the integrated photodiode-modulator structure including a local resistor and a pair of bypass capacitors. Because of the lumped circuit operation of the integrated parts, transmission lines are not necessary. In operation, the high-speed optical input signal at  $\lambda_1$  incident on the photodiode, PD, generates a photocurrent,  $I_{PD}$ , that creates a voltage drop across the resistor, R, and swings the voltage across the electroabsorption modulator. Such an optically-induced voltage change across EAM changes the transmission of the EAM quantum wells at  $\lambda_2$ . Thus, the input data at  $\lambda_1$  is bit-by-bit transferred to the output at  $\lambda_2$ , which thus converts the carrier wavelength from  $\lambda_1$  to  $\lambda_2$ . The DC biases applied to the EAM and PD can further be used to electrically enable or disable the wavelength conversion.



**Figure 8: A picture of fabricated dual-diode device**

Figure 8 is a part of the optical micrograph of a fabricated wavelength-converting switch that consists of an InGaAsP/InP waveguide quantum-well modulator and an InGaAs surface-normal pin photodiode monolithically integrated through two-step epitaxial growths. The switch is 300  $\mu\text{m}$  x 300  $\mu\text{m}$  in size. It comprises a waveguide modulator with a width of 2  $\mu\text{m}$ , a length of 300  $\mu\text{m}$  and a 0.37  $\mu\text{m}$  thick i-region; a photodiode with a 30  $\mu\text{m}$  x 30  $\mu\text{m}$  mesa and a 1.25  $\mu\text{m}$  thick i-region; and a local resistor with values from 340 to 650 Ohms depending the designed speed of operation. The device is built on a semi-insulator InP substrate to lower parasitic capacitance and to isolate the individual switches. For monolithic integration, a new selective area regrowth technique is used [16]. For the further reduction of the parasitic capacitance and leakage current, a self-aligning polymer planarization and passivation method is developed [17].

The switch simulation that includes the on-chip, integrated optoelectronic circuit and off-chip, biasing circuit predicts optical switching requiring < 10 mW absorbed optical power for > 10 dB extinction ratio at 10 Gb/s. The RC time constant of the integrated optoelectronic circuit determines the operation speed. Figure 9 shows the simulated eye diagram at 10 Gb/s with > 10 dB extinction ratio [17].

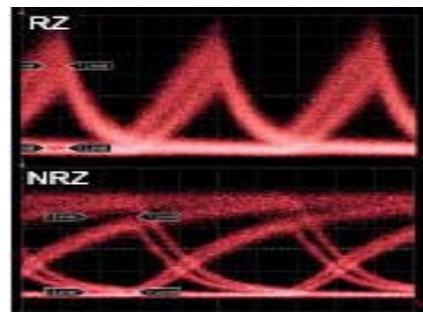


**Figure 9: Simulation of 10 Gb/s operation**

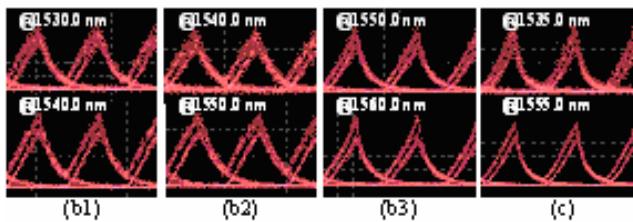
## RESULTS

Figure 10 shows two open eye diagrams from the modulator output in (a) Return-to-Zero (RZ) and (b) NRZ schemes from the WC with a designed operation speed of 2.5 Gb/s. These diagrams exhibit RF-extinction ratios of > 10 dB with absorbed average optical power of < 8 mW at 2.5 Gb/s [18]. In both cases, the input wavelength is 1550 nm, and the output wavelength is 1530.0 nm. With the input beam photogenerating ~5 mA of current, an electric field swing of ~6.5 V/ $\mu\text{m}$  is optically induced across the modulator, comparable to the field swing typically required by an electrically driven, conventional EAM. These wavelength-converting switches cover an operation range of 45 nm, from 1525 nm to 1570 nm, centered on the C-band [17].

The switches also allow for multi-channel broadcasting across the entire C-band [17]. For dual-wavelength broadcasting, two CW beams at different wavelengths are coupled into the EAM to be simultaneously modulated by the same optical input signal incident on the PD. Figure 11 (b1-b3 and c) shows the two output optical signals from the EAM with channel spacings of 10 nm and 20 nm, respectively in C-band at 1.25Gb/s [17].

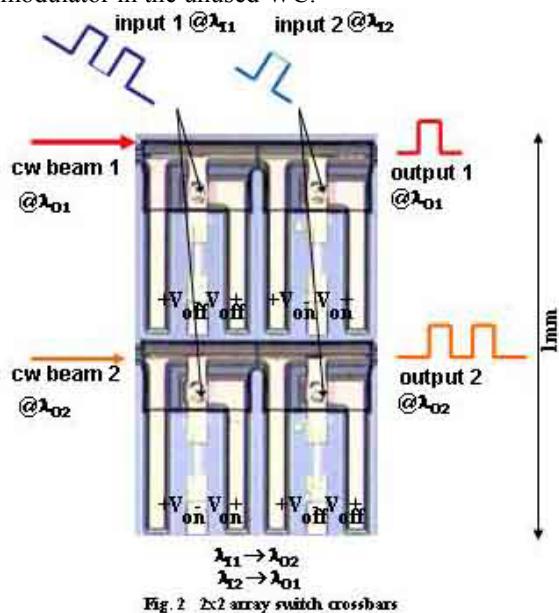


**Figure 10: Optical switching in (a1) NRZ and (a2) RZ formats with >10 dB RF-extinction ratios at 2.5 Gb/s**

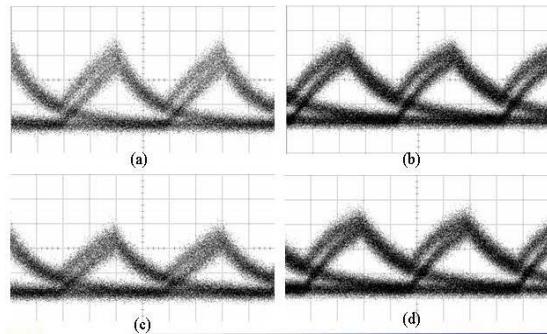


**Figure 11:** C-band dual-wavelength broadcasting with channel spacings of 10 nm in (b1)-(b3) and 20 nm in (c)

Figure 12 shows a fabricated 2x2 wavelength-converting crossbar switch [13]. Figure 13 depicts the eye diagrams taken from each of the four switch elements at 1.25 Gb/s, all measured with > 10dB extinction ratio. While one of the switch elements is tested, the unused switch along the same waveguide is disabled by slightly forward-biasing its photodiode and modulator. This removes the potential crosstalk between the two input channels and eliminates the background absorption of the quantum-well modulator in the unused WC.



**Figure 12:** 2x2 wavelength-converting crossbar switch.  
The size is 1 mm x 600  $\mu$ m



**Figure 13:** Eye diagrams from each of the four switch elements in a 2x2 array

## DISCUSSION

We presented our design and experimental results on a wide variety of wavelength-converter implementations, and showed how these approaches can achieve the desired wavelength-conversion functionality at high bit rates and extinction ratio.

The Directly Modulated (DM) laser approach to wavelength conversion remains the most compact device incorporating an on-chip tunable optical source, but is ultimately limited by the modulation bandwidth of SGDBR lasers, and would achieve bit rates of 10 Gb/s or higher only with significant redesign. In addition, “chirping” in directly modulated lasers would result in an undesirable dispersion penalty.

For bit rates of 10 Gb/s and above, the externally modulated approach, utilizing an EAM or MZM to modulate the laser output, becomes more attractive. Both modulator types have been implemented by the UCSB project, and demonstrate higher extinction at 2.5 Gb/s compared to the direct modulated approach. Our EAM approach utilizes FK absorption. The EAM WC and MZM WC designs incorporate FK photodiodes, in order to take advantage of their improved linearity.

Modulator-type WCs will benefit from increased modulator extinction efficiency (dB/V). Longer EAMs provide increased extinction efficiency at the expense of increasing capacitance (hence lower bandwidth) and on-state transmission. The MZM, by utilizing phase change-induced interference, exhibits higher extinction efficiency than the EAM of similar electrode length allowing it to maintain high bandwidth.

The photonic switch architecture based on the intimate integration of a quantum-well waveguide modulator with a surface-normal photodiode allows for the two-dimensional scalability of the wavelength-converting switches to realize the first reconfigurable wavelength-converting crossbar switches. This technology relies on the tight confinement of optically induced high-speed

electrical signals in a single, compact, integrated optoelectronic chip for efficient wavelength conversion with low switching power for high extinction ratios in high-speed operations. Experimental results include unconstrained wavelength conversion up to 2.5 Gb/s and across 45 nm around the C-band, multi-wavelength broadcasting over 20 nm across the C-band, and multi-channel wavelength conversion with a 2x2 wavelength-converter array. Theoretical simulations predict 10 Gb/s operation.

## CONCLUSION

In this paper, we described our research into novel approaches for monolithically integrating WCs in InP. The first approach, undertaken with UCSB, consists of an integrated widely tunable laser-transmitter and waveguide photodiode receiver. Several implementations have been designed, fabricated, and tested to exhibit modulation up to 2.5 Gb/s with high extinction ratio and error-free operation. The second approach, undertaken with Stanford University, consists of a scalable, compact, low-power, dual-diode photonic switch architecture that confines high-speed electrical signals in its novel photodiode-modulator integrated optoelectronic circuit. This technology enables reconfigurable multi-channel wavelength conversion. Both approaches are scalable to 10 Gb/s and higher bit rates, crucial for the implementation of advanced optical networking and the continuing explosion of Internet data bandwidth.

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