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THE INSIDER'S GUIDE TO MICROPROCESSOR HARDWARE

INTEL CANCELS 4GHz P4

Focus Shifts to System Features

By Kevin Krewell {11/1/04-01}

Intel's changing processor roadmap this year has provided one surprise after another. The normally steadfast company has inspired some observers to now view Intel as flying by the seat of its pants—a role normally attributed to long-time competitor AMD. Just two days after

its quarterly earnings report, Intel announced it had canceled the previously delayed 4.0GHz speed grade for the Pentium 4 processor and will instead increase the Pentium 4 processor's L2 cache size from 1MB to 2MB. Earlier this year, Intel had announced it was delaying the 4.0GHz speed grade from 4Q04 to 1Q05. It is now apparent that even delaying production did not solve a more fundamental problem with the design. With Intel chip designers moving away from frequency for performance scaling, it no longer made sense for Intel to continue sinking resources into additional Prescott development just to obtain one last speed grade—even if the company (and specifically, its president and COO Paul Ottelini, at the Intel 2003 analyst meeting) had promised it would.

Although, given the situation the company faced, not sinking further resources into a dead-end strategy is clearly the right decision, the roadmap change still brings into question Intel's ability to predict its processor roadmaps reliably. With all the simulation tools at its disposal, how did Intel not know of this problem much earlier? The 90nm process has been in production for about a year, and the Prescott design was well known. Intel could have canceled 4.0GHz earlier instead of postponing it. Could there have been resistance to the new direction—that a faction existed with the belief that, with just a bit more work, they could reach 4.0GHz? Unfortunately it turned out to be 200MHz too far to reach.

Intel had already pushed the thermal limits to 115W for the thermal design power (TDP) of the 3.4GHz (model

550) and 3.6GHz (model 560) Pentium 4 processors in the 775-pin LGA package. At this power level, Intel's highest-performing processors are well above the AMD Athlon 64

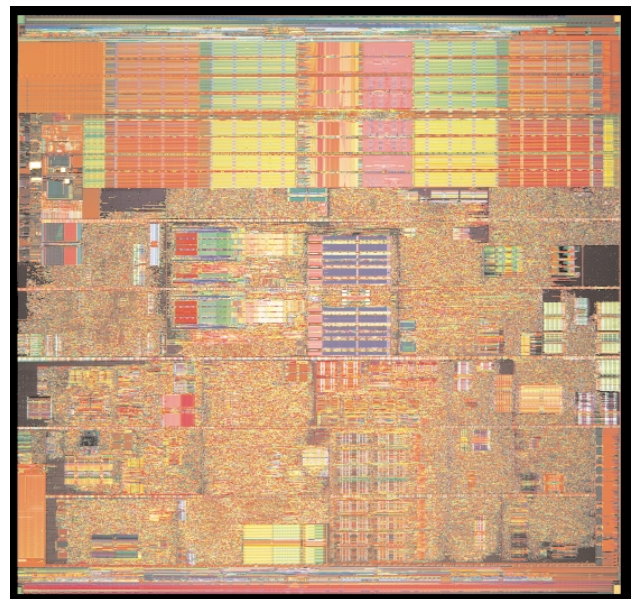


Figure 1. The 90nm Prescott die with 1MB of L2 cache is 112mm². Approximately 27% of the die appears to be the L2 cache. Adding another 1MB of L2 cache should increase the die size by 31mm², to about 143mm².

Microsoft Announces Multicore Licensing Model

In a big win for both AMD and Intel, Microsoft announced its server licensing policy for multicore processors:

"Microsoft Corp. today (October 19, 2004) announced its decision on how the company will license server software on new servers with multicore processors expected in the market next year. Microsoft software that is currently licensed on a per-processor model will continue to be licensed per processor, not per core, for hardware that contains dual-core and multicore processors. This policy is effective today and applies to several products in the Windows Server System family, including Microsoft SQL Server, Microsoft BizTalk Server and others. Microsoft is approaching this decision with

the goal of driving high volume and high value to standards-based computing through logical licensing and more cost-effective adoption of multicore processors."

Microsoft's position statement on licensing is exactly what the hardware vendors of multicore processors are looking for from the software industry in general. The hardware vendors hope Microsoft will lead the way, and others will follow. If software vendors for Unix applications also move to this model, it will help multicore server vendors IBM and Sun as well. These licensing issues regarding multicore processors largely reflect business decisions, not technical limitations.

89W TDP. To feed enough electrical power into the processor, 523 of the 775 socket connections are used for power and grounds and are needed to deliver up to 119A into the packaged processor. Even with all this power, Intel said it couldn't produce enough Prescott 4.0GHz processors without some redesign. Under some revised specifications, Intel might have reached the 4.0GHz target; at least one niche PC manufacturer (Alienware) has introduced an overclocked Prescott at 4GHz, using water cooling.

Intel hasn't said how big the new Prescott die (with the 2MB L2 cache) is, but a quick estimate can be made by taking the 112mm² Prescott die (shown in Figure 1) and estimating the extra die area required to double the L2 cache. The Prescott die photo shows that the die area is dominated by the logic and not the L2 cache. A review of the die photo reveals that about 27% of the die area contains the L2 cache. Increasing the L2 cache to 2MB would add another 31mm² to the die, for a total of 143mm².

The Good Side of Overcapacity

With three 300mm wafer fabs producing more wafers than the company can sell, owing to softened demand for desktop processors and already high inventory levels, Intel announced at its 3Q04 earnings call that it is cutting wafer production. Intel admitted overcapacity in wafer production,

and although this is not good news if one's goals are to maximize revenue per fab and absolutely minimize die cost, it can help Intel in other ways. As Intel heads toward multicore processors, this move will lead to larger dies, and larger dies lead to fewer gross die per wafer. Fewer die per wafer is not normally considered a good thing, but it is better when the larger die can return higher prices and more revenue per wafer. Without frequency as a selling point for high-margin processors, the larger cache and dual core will help.

The new Prescott/2M will not replace the Pentium 4 Extreme Edition (P4EE), marketed to PC gamers and enthusiasts (see Table 1). Intel still plans to continue the product on the basis of system improvements, such as a faster front-side bus, not on frequency. It is unclear whether Intel will continue the practice of using larger-cache server processors for the Extreme Edition parts. Intel now offers a 3.0GHz XeonMP with a 4MB L3 cache.

Next Stop Is Dual Core

Intel has confirmed that the dual-core Pentium processor has taped out and, in fact, has booted A0 silicon. This means the engineering prototype Intel showed at the fall 2004 Intel Developer Forum in September was unlikely to have been production silicon. As Intel rolls out dual-core processors in mid-2005, it expects to ramp them quickly throughout the desktop and server markets. As we've indicated previously, given the time-to-market constraints for this first dual-core Pentium, we expect the first dual-core desktop processor to be based on the NetBurst architecture and to ship in the 90nm process. Time-to-market pressure will also mean the part will likely be two complete Pentium 4 processors on one die, with separate L2 caches, connected only at the processor-bus interface.

Intel has not revealed the code-name for this part. Enough information leaks have reported "Smithfield" as the code-name for the dual-core desktop Pentium processor, however, that we feel reasonably confident it is the correct code-name. In a previous article, we took a quick

Code Name	Brand Name	Process Gen.	Die Size	Die per 300mm Wafer
Dothan	Pentium M	90nm	87mm ²	741*
Prescott	Pentium 4	90nm	112mm ²	568*
Prescott/2M	Pentium 4	90nm	143mm ² *	438*
Gallatin	Pentium 4 EE	130nm	211mm ² *	288*
Smithfield (dual core)	Pentium 4/5	90nm	224mm ² *	271*

Table 1. Die size and estimated die per 300mm wafer comparison for various Intel desktop and mobile processors. The Gallatin server die (normally used for the XeonMP processor) was used in 4Q03 to create the Pentium 4 Extreme Edition for PC gamers. The dual-core processor's code-name has been reported as "Smithfield" by various sources. Note: *MPR estimates

shortcut to estimating the die size of the dual-core Pentium by doubling Prescott's die size (112mm^2) to get 224mm^2 . (See *MPR 5/31/04-02*, "Intel's PC Roadmap Sees Double.") This estimate assumes the Smithfield die will have only 1MB of L2 cache per core. Later, when Intel shrinks dual-core parts to 65nm, it will give the company an opportunity to further increase the amount of cache memory, and replace the NetBurst core with an enhanced version of a dual-core Pentium M processor for the desktop market.

We estimated the die size of AMD's dual core would reach about 182mm^2 (see *MPR 7/06/04-01*, "AMD vs. Intel in Dual-Core Duel"), and AMD has said the die size is close to the current 130nm single-core Opteron (193mm^2). While AMD might have a die-size advantage, and it can be argued that AMD's dual-core processor is more elegant and integrated, AMD cannot match Intel's fab capacity and will have to carefully allocate the larger dual-core die. AMD will therefore introduce the dual-core processor in the Opteron server line first, whereas it appears Intel will launch its dual-core onslaught in the desktop market. More specifically, Intel will target media applications. The dual-core strategy should be an immediate hit with media-center PCs, where the two cores can better balance the demands of multiple streams of media data. One example of the usefulness of dual core would be in a Windows- or Linux-based media-center PC,

Price & Availability

The 4GHz Pentium 4 (1MB) is canceled by Intel (although at least one aggressive PC manufacturer has overclocked existing chips to 4GHz). Intel's Pentium 4 with 2MB L2 caches will ship in 1Q05. Dual-core Pentium 4 processors are scheduled to ship in mid-2005. Prices have not been announced at this time.

where the two cores could share responsibility for timed video-recording functions (personal video record, or PVR), along with handling the user GUI and running other concurrent application loads (for example, games).

While the cancellation of the 4.0GHz speed bump is another very public embarrassment for Intel (which also announced its discontinuance of the development of the LCOS video-projector chip for HDTV displays), the company's long-term strategy is sound and its fab capacity undiminished. The short-term challenge ahead for Intel will be in holding off AMD's advances in market share in desktop and servers while maintaining its own strong leadership position in mobile. ♦

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