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SPRING 03 IDF DETAILS PRESCOTT

Intel Gives a Peek Under the Hood

By Kevin Krewell {3/10/03-02}

With less than a year to the scheduled introduction of Intel's Prescott processor, the recent Intel Developer Forum gave the public a deeper look inside the next generation of the Net-Burst architecture, and, during a question and answer section, *MPR* convinced Intel designer Joe Shutz to reveal a few more clues. At a session entitled "IA 32 Processor Architecture Trends and Research," Intel's Shutz and Justin Rattner made the case that Net-Burst and Hyper-Threading are still key to Intel's IA-32 plans.

Prescott will have improvements to its architecture and design methodology that will allow it to reach clock speeds of 4–5GHz before Intel ships Tejas (the follow-on 90nm processor expected in 2H04). Our list of architectural goodies we would like added to the Northwood Pentium 4 processor includes more renaming registers, larger L1 caches and more L2 cache, lower power, deeper buffers and queues, and additional multimedia instructions. Prescott appears to deliver on most of our wish list. It will also be manufactured on Intel's advanced 90nm process, with strained silicon and seven layers of low-*k* dielectric for metal (copper) interconnects.

In his presentation, Shutz said that Prescott will increase the size of its L1 data cache from 8K to 16K and confirmed reports that the L2 cache will also double, from 512K to 1M. Prescott will also benefit from a front-side-bus speed increase to 800MHz (a quad-pumped 200MHz bus). Intel would not confirm launch frequencies for Prescott, but we expect it will be introduced at 3.4GHz.

Prescott will have a number of architectural refinements, including an improved branch predictor for the prefetch logic, better power management, improved latency for the imul (integer multiply) instruction, and additional write combining (WC) buffers. The additional buffers are particularly important for software tuned for single-threaded performance that is now running in a multi-threaded environment.

The processor design is obviously not a simple die shrink of Northwood. Intel also took care to improve clock distribution, and new design tools with greater automation improved the dataflow layout. The new tools separated logical design partitioning from the optimization of the actual circuit location on die. The clock scheme was recently presented at an ISSCC paper and reduced the clock skew across the die to less than one inverter delay.

In the question and answer section, Shutz also hinted that more improvements to the microarchitecture are yet to be revealed. Specifically, the L1 instruction trace cache was increased from Northwood's 12K instruction lines, and the domino-logic (often called double-pumped) ALUs of Willamette and Northwood underwent some unspecified improvements. The L1 instruction and data caches were small compared with almost every other single-threaded high-performance processor and hampered Hyper-Threading performance. The larger caches will significantly improve architectural performance.

Even with the larger caches, Prescott's die size is smaller than Northwood's. Although Intel would not be more specific, using our MDR cost model, we estimate the die size to be 112mm^2, with a manufacturing cost of $37.

Prescott New Instruction (PNI)

Another non-surprise is that Prescott will include new instructions, the long-rumored SSE3. Although Intel has not given the 13 new instructions an official marketing designation beyond "Prescott new instructions," we would be surprised if they were called anything else.

The new instructions, shown in Table 1, include two instructions to support Hyper-Threading applications.

Isn't Prescott LeGrande?

At IDF, spring 2003, Intel announced a security initiative for PCs that it dubbed "LeGrande technology." Prescott will incorporate this technology to protect PC data from hacking and other unauthorized access, but Intel did not reveal any new details on LeGrande. In fact, Intel was rather quiet on this initiative, leading us to believe that Intel is either working behind the scenes to promote this technology or it has been unable to gain any traction with key vendors. The problem with LeGrande is that it is an Intel-platform-only solution, and the market generally prefers industry-standard solutions that can be applied cross-platform.

IDF is Intel's key opportunity to reveal new platform initiatives. At this IDF, Intel revealed its plans for a new type of I/O expansion card for PCs that is based on PCI Express and USB 2.0. The new expansion card is simply called NewCard. The form factor is smaller than PCMCIA Type II cards but larger than memory cards such as Compact Flash and Memory Stick.

Prescott chip sets are code-named Canterwood and Springdale. Both chip sets support dual-channel DDR memory up to 400MHz. The chip sets provide a direct connection between the memory controller hub (MCH) and a Gigabit Ethernet chip (Kenia II CSA), using a new Communications Streaming Architecture (CSA) that, Intel says, is designed to optimize networking performance. The I/O controller hub ICH5 is used for both chip sets and supports dual Serial ATA channels for hard drives and two regular ATA-100 ports. The Serial ATA controller can support soft RAID features for greater performance and reliability. The chip set also supports surround-sound audio, AGP 8x, and six USB 2.0 ports.

The chief difference between the two chip sets is that the Springdale-G chip set has integrated graphics that Intel calls Extreme Graphics 2. The new graphics core will run at higher frequencies than previous integrated-graphics products. Springdale is also part of the two platforms Intel will support with a new driver image-longevity program for business IT customers called Granite Peak. Intel promises to support, for a period of six quarters, an unchanging driver model for both Springdale-G for the Pentium 4 processor and the Montara-GM chip set for Pentium M (Banias and Dothan). The goal is to provide corporate customers with a fixed platform-driver model (including graphics drivers) that is easier and less expensive to support. Intel and its OEMs must then support these chip sets, with the same die stepping, and sometimes even the same errata, for a year and a half after introduction.

Intel showed a concept PC called Powersville. It would use the Tejas processor at 5+GHz. The platform supports PCI-Express, PCI-Express Graphics (replacing AGP), DDR-II memory, and embedded security; it would fit into a smaller form factor than current Intel-based PCs. Intel continues to show new technology that will transform the physical form factor of the PC. The PC is still dependent on Microsoft for the evolution of the GUI and software.

IA-32 Forever?

In numerous venues, Intel executives have made it clear that they do not plan to adopt AMD's x86-64. The addressing

Instruction	Type	Description
FISTTP	FP to Integer Conversion	Converts Top of Stack (ST0) FP to integer with truncated rounding and pop the stack
ADDSUBPD	Complex Arithmetic	Converts Top of Stack (ST0) FP to integer with truncated rounding and pop the stack
ADDSUBPS	Complex Arithmetic	Performs packed single precision math: addition on the second and fourth set of source elements and subtraction on the first and third set of elements
MOVDDUP	Complex Arithmetic	Loads/moves 64-bits and duplicates in both halves in a 128-bit destination register
MOVSHDUP	Complex Arithmetic	Loads/moves 128-bits (four 32-bit data elements), duplicating the second and fourth elements
MOVSLDUP	Complex Arithmetic	Loads/moves 128-bits (four 32-bit data elements), duplicating the first and third elements
LDDQU	Video Encoding	Special 128-bit unaligned load designed to avoid cache line splits
HADDPD	SIMD FP Using AOS Format	Performs double-precision addition on contiguous data elements
HADDPS	SIMD FP Using AOS Format	Performs single-precision addition on contiguous data elements
HSUBPD	SIMD FP Using AOS Format	Performs double-precision subtraction on contiguous data elements
HSUBPS	SIMD FP Using AOS Format	Performs single-precision subtraction on contiguous data elements
MONITOR	Thread Synchronization	Sets up an address range used to monitor for write-back stores
MWAIT	Thread Synchronization	Enables a logical processor to enter into an optimized state while waiting for a write-back store to the range set up by the MONITOR instruction.

Table 1. The 13 new instructions included in Prescott, with a summary of their operation.

extension to Intel's IA-32, when it arrives (and we do believe it is when, not if), will probably be different from x86-64 (see *MPR 3/4/02-02*, "Is Yamhill Intel's True 64-Bit Future?"). Intel executives appear to believe that when the company does roll out an address-space extension to IA-32 (beyond the PAE36 paging scheme), Intel's market share domination will allow it to fairly quickly create a much larger user base for its instructions.

A good analogy for this situation would be AMD's floating-point SIMD instruction extensions, 3D-Now, and Intel's SSE SIMD extensions. AMD's extensions had a three-quarters head start on SSE, but within three quarters of the Pentium III launch (with the SSE instructions), Intel's extensions had caught up to 3D-Now's installed base—and then quickly surpassed it. Eventually, the original 3D-Now extensions became irrelevant and AMD was forced to adopt the SSE extensions (under the 3D-Now Professional brand).

The difference for AMD today is that it will launch x86-64 in 2003, and Intel is indicating that the PC market will not need 64-bit computing until late in the decade. Intel has yet to show any roadmap for its address extension plans. Intel's delay could give AMD time to build a substantial installed base, and the longer Intel waits, the larger the installed base of x86-64 will grow.

Price & Availability

The Prescott processor is scheduled to ship in 2H03. Pricing and frequencies have not been officially released by Intel.

The stage is now set for another interesting year in the PC-processor business. AMD will ship the first 64-bit PC processor with its Athlon 64, and Intel will ship the first 90nm volume processors: Prescott and an improved mobile-optimized Dothan (Pentium M) processor. Prescott's micro-architecture enhancements will improve instructions-per-cycle (IPC) performance, deliver more-effective Hyper-Threading performance, and have significantly higher clock frequencies.

This latest battle between these two archrivals will begin in 3Q03, but we don't foresee a clear victory by one side or the other. The dust is unlikely to clear until well into 2004.