CS60003: High Performance Computer Architecture
CLASS-TEST – ② [Spring 2023-2024]
Model Solution

1) (a) $T_{pipelined}\big|_{min} = T_{longest\_stage}\big|_{min} + d\big|_{register} = 2us + 0.1us = \underline{\underline{2.1us}}$

(b) In the steady state, in every 5 clocks, 4 instructions would ~~[illegible]~~ be comple

$\therefore CPI\big|_{pipelined} = \dfrac{5 \text{ cycles}}{4 \text{ instructions}} = \underline{\underline{1.25}}$

(c) Note that in a non-pipelined machine, there is no possibility of any stall
Suppose, a program consists of "I" instructions

$\therefore$ time taken to execute the program on the non-pipelined machine:

$\tau\big|_{non\text{-}pipelined} = I * CPI * T\big|_{non\text{-}pipelined} = I \cdot 1 \cdot 7 \ us$

Similarly, $\tau\big|_{pipelined} = I * 1.25 * T\big|_{pipelined} = I * 1.25 * 2.1 \underline{us}$.

$\therefore$ Speedup $= \dfrac{\tau_{non\text{-}pipelined}}{\tau_{pipelined}} = \dfrac{7I}{1.25 * 2.1 * I} = \underline{\underline{2.67}}$

(d) If the # of pipeline stages become infinite, then, the delay of the pipelined machine is only the delay of the registers, i.e.,

$\lim\limits_{\#\text{of stages} \to \infty} T\big|_{pipelined} = d\big|_{register} = \underline{\underline{0.1us}}$

$\therefore$ Speedup$\big|_{\text{ignoring extra \# cycles}} = \dfrac{7I}{1 * 0.1 I} = 70$.

Speedup$\big|_{\text{considering extra stall \# cycles}} = \dfrac{7I}{1.25 * 0.1} = 56$

Both answers could be accepted.

This answer also makes sense since the clock cycle time-period is now almost zero (because of infinite # of pipeline stages). Hence, the only pipeline delay now is because of the register delay.

(a) When there is no branch misprediction, the only stalls are because of RAW hazards, which cannot be resolved ($\because$ there is no forwarding), except those which can be resolved because of the nature of the register file, where WB $\rightarrow$ ID register file reading is possible.

```
Loop: ld, a1, 0(a2)
        ↘(1)
 addi, a1, a1, 1
     ↙(2)
  sd  a1, 0(a2)
 addi a2, a2, 4
           ↘(3)
 Sub a4, a3, a2
    (4)↓
bnez  a4, Loop
```

— : True Dependencies

(1): Cannot be resolved (even if there had been forwarding)

(2): Cannot be resolved ($\because$ there is no forwarding.) ~~However, by delaying instruction fetch for sd (see pipeline timing diagram below), they do not effectively affect the performance~~ (WB→ID "forwarding through register file" helps)

(3): Same as for #2.   (4): Same as for #2

Note that since branch outcomes are known in EX stage, there are 2 cycles penalty in case of branch mispredictions

~~1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16~~

S: Stall   → denotes "forwarding through register file"

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
ld	F	D	X	M	W ↓													
addi		F	S	S	D	X	M	W ↓										
sd					F	S	S	D	M	W								
addi								F	D	X	M	W ↓						
sub									F	S	S	D	X	M	W ↓			
bnez												F	S	S	D	X	M	W

(b) In the 1st ϕ cycle, assuming the 1-bit branch predictor is in Not Tak
state, there is a misprediction $\Rightarrow$ 2 ϕ cycles penalty because of pipeline flu

Again, in the last ϕ cycle, there is similarly a 2 ϕ cycle penalty.

The loop runs total $\frac{396}{4} = 99$ times ~~in the~~

The middle $99-1-1 = 97$ iterations take 18 ϕ cycles each

$\therefore$ total # of ϕ cycles $= 97*18+20+20 = \underline{\underline{1786}}$ ϕ cycles

Note: if the 2 cycle stall due to pipeline flushes in the last iteration is ignored, then # of ϕ cycles $= \underline{1784}$

Both answers are acceptable.

3) Note: only specific snapshots are shown.

Clock Cycle #4

Instr. Status		Issue	Read Op	Ex. Comp.	Write Res.
RAW Hazard	ld	1	2	3	4
	fsub.d	2			
	fdiv.d	3			
Structural hazard	fadd.d				

FU Status	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Int.	Yes	Load	f6		x5				
Mult1	No								
Mult2	No								
Add/Sub	Yes	Sub	f8	f6	f2	Int.		No	Yes
Divide	Yes	Div.	f10	f0	f6	Int.		Yes	No

Reg. Res. Status		f0	f2	f5	f6	f8	f10
Clock cycle # 4	FU				Int	Add/Sub	Div

Clock Cycle #7

	Issue	Read Op	Ex. Compl.	Write Res
ld	~~Yes~~ 1	2	3	4
fsub.d	2	5	7	
fdiv.d	3	5		
Structural hazard fadd.d				

FU Status	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Int	No								
M1	No								
M2	No								
Add/Sub	Yes	Sub	f8	f6	f2			Yes	Yes
Divide	Yes	Div	f10	f0	f6			Yes	Yes

Reg. Reg. Status		f0	f2	f5	f6	f8	f10
Clock Cycle # 4	FU				~~Int~~	Add/Sub	Div

Clock Cycle #10.

	Iss.	Read Op	Ex Comp.	Wr. Res
ld	1	2	3	4
fsub.d	2	5	7	8
fdiv.d	3	5		
fadd.d	9	10		

	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Integer	No								
M1	No								
M2	No								
Add/Sub	Yes	Add	f5	f8	f6			Yes	Yes
Div.	Yes	Div.	f10	f0	f6			Yes	Yes

Reg. Res. Status.		f0	f2	f5	f6	f8	f10
C Cycle# 10	FU			Add/Sub			Div.

Clock Cycle #13.

	Iss.	Read Op.	Ex. Comp.	Wr. Res.
ld	1	2	3	4
fsub.d	2	5	7	8
fdiv.d	3	5		
fadd.d	9	10	12	13

	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Int.	No								
M1	No								
M2	No								
Add/Sub	Yes		f5	f8	f6			Yes	Yes
Div.	Yes	Div.	f10	f0	f6			Yes	Yes

Reg. Status.		f0	f2	f5	f6	f8	f10
Clock Cycle# 13	FU			Add/Sub			Div.

~~Division ends execution on cycle #45~~.

Division ends execution ~~from~~ on Clock #45

" " Write Register on Clock #46.