States and their functions:

> **Fetch**:
Fetch instruction from memory (address given in PC) and load in register. Increment PC by 4.
PW=1, IW=1

>**RdAB:**
Load registers A and B
For MUL/MLA instruction, A= Ins[15-12] and B= Ins[3-0], hence **r1src = 01, r2src = 0.**
For other, A=Ins[19-16] and B=Ins[3-0]., hence **r1src=00, r2src=0**.
In both cases, **AW=1, BW=1**

>**RdBC:**
Load registers B and C (Needed for DP instructions where register amount is specified by register (Rs), and MUL/MLA instructions where Rd= Rm*Rs + Rn).
r1src=11, r2src=0

>**aluAB**:
Perform operation specified by opcode in ALU with A and B registers as operands (write ans into Res).
Asrc=000, Fset= Ins[20], ResW=1

>DTrw:
In case of store instruction, perform memory write of Rd stored in B into either address stored in A (pre-indexing) or Res (post-indexing). In case of load instruction, perform memory read from either address stored in A or Res and store it in DR.