طراحی دوم بخش اول:

گزارش زمانی:

:Timing Summary

Speed Grade: -3

Minimum period: No path found

Minimum input arrival time before clock: 86.269ns

Maximum output required time after clock: 3.597ns

Maximum combinational path delay: No path found

واحدها و تراشه ها:

:Primitive and Black Box Usage

BELS : 2802

LUT2 : 513

LUT3 : 57

LUT4 : 197

LUT5 : 94

LUT6 : 1939

MUXF7 : 2

FlipFlops/Latches : 4

FDC : 4

Clock Buffers : 1

BUFGP : 1

IO Buffers : 549

IBUF : 545

طراحی دوم بخش دوم:

گزارش زمانی:

:Timing Summary

Speed Grade: -3

Minimum period: 3.074ns (Maximum Frequency: 325.357MHz)

Minimum input arrival time before clock: 3.085ns

Maximum output required time after clock: 3.668ns

Maximum combinational path delay: No path found

واحدها و تراشه ها:

:Primitive and Black Box Usage

BELS : 49

LUT2 : 34

LUT3 : 1

LUT4 : 1

LUT5 : 1

LUT6 : 11

VCC : 1

FlipFlops/Latches : 42

FDC : 40

FDCE : 2

Clock Buffers : 1

BUFGP : 1

IO Buffers : 6

IBUF : 2

OBUF : 4

طراحی اول:

گزارش زمانی:

:Timing Summary

Speed Grade: -3

Minimum period: 3.502ns (Maximum Frequency: 285.523MHz)

Minimum input arrival time before clock: 6.374ns

Maximum output required time after clock: 3.732ns

Maximum combinational path delay: No path found

واحدها و تراشه ها:

:Primitive and Black Box Usage

BELS : 68

GND : 1

INV : 1

LUT1 : 8

LUT2 : 8

LUT3 : 1

LUT4 : 5

LUT5 : 3

LUT6 : 15

MUXCY : 12

XORCY : 14

FlipFlops/Latches : 20

FDC : 14

FDCE : 6

Clock Buffers : 1

BUFGP : 1

IO Buffers : 15

IBUF : 13

OBUF : 2